TPS737xx 1-A Low-Dropout Regulator With Reverse Current Protection

1 Features

- Stable With 1-μF or Larger Ceramic Output Capacitor
- Input Voltage Range: 2.2 V to 5.5 V
- Ultralow Dropout Voltage: 130 mV Typical at 1 A
- Excellent Load Transient Response—Even With Only 1-μF Output Capacitor
- NMOS Topology Delivers Low Reverse Leakage Current
- 1% Initial Accuracy
- 3% Overall Accuracy Over Line, Load, and Temperature
- Less Than 20 nA Typical I_Q in Shutdown Mode
- Thermal Shutdown and Current Limit for Fault Protection
- Available in Multiple Output Voltage Versions
  - Adjustable Output: 1.20 V to 5.5 V
  - Custom Outputs Available Using Factory Package-Level Programming

2 Applications

- Point-of-Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors
- Post-Regulation for Switching Supplies
- Portable and Battery-Powered Equipment

3 Description

The TPS737xx family of linear low-dropout (LDO) voltage regulators uses an NMOS pass element in a voltage-follower configuration. This topology is relatively insensitive to output capacitor value and ESR, allowing a wide variety of load configurations. Load transient response is excellent, even with a small 1-μF ceramic output capacitor. The NMOS topology also allows very low dropout.

The TPS737xx family uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is less than 20 nA and ideal for portable applications. These devices are protected by thermal shutdown and foldback current limit.

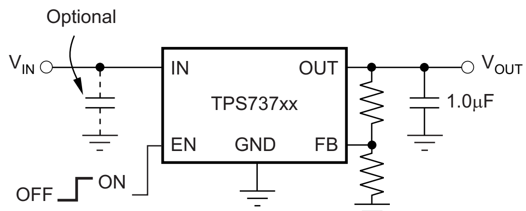
For applications that require higher output voltage accuracy, consider TI's TPS7A37xx family of 1% overall accuracy, 1-A low-dropout voltage regulators.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS737xx	VSON (8)	3.00 mm × 3.00 mm
	SOT-223 (6)	6.50 mm × 3.50 mm
	WSON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision P (July 2013) to Revision Q — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Changed "free-air temperature" to "junction temperature" in *Absolute Maximum Ratings* condition statement 5
- Changed "free-air temperature" to "junction temperature" in *Recommended Operating Conditions* condition statement 5
- Changed Internal Reference parameter (V_{FB}) typical values from 1.2 V to 1.204 V 7

Changes from Revision O (June 2012) to Revision P — **Page**

- Added last paragraph to *Description* section 1

Changes from Revision N (June 2011) to Revision O — **Page**

- Changed Thermal Information table data and footnote 2b 6
- Changed V_{FB} *Internal reference* parameter in *Electrical Characteristics* table 7
- Changed title of Figure 6 8

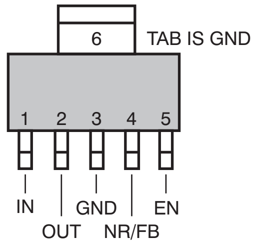
Changes from Revision M (October, 2010) to Revision N — **Page**

- Added footnote (3) to *Thermal Information* table 7
- Added footnote to Figure 39 21

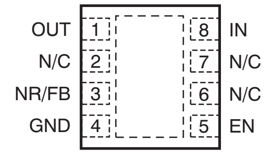
Changes from Revision L (August, 2010) to Revision M	Page
• Corrected typo in Figure 39	21

5 Pin Configuration and Functions

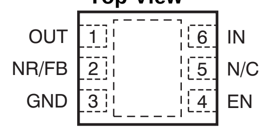
6-Pin SOT-223
DCQ Package
Top View



8-Pin VSON
DRB Package
Top View



6-Pin WSON
DRV Package[(1)]
Top View



(1)Power dissipation may limit operating range. Check *Thermal Information* table.

Pin Functions

PIN				I/O	DESCRIPTION
NAME	SOT-223	WSON	VSON		
IN	1	8	6	I	Unregulated input supply
GND	3, 6	4, Pad	3, Pad	—	Ground
EN	5	5	4	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to the *Enable Pin and Shutdown* section under *Application Information* for more details. EN must not be left floating and can be connected to IN if not used.
NR	4	3	2	—	Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.
FB	4	3	2	I	Adjustable voltage version only—this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	2	1	1	O	Regulator output. A 1.0-μF or larger capacitor of any type is required for stability.
NC	—	2, 6, 7	5	—	Not connected

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6	V
	V_{EN}	–0.3	6	
	V_{OUT}	–0.3	5.5	
	V_{NR}, V_{FB}	–0.3	6	
Peak output current	I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
Temperature	Junction range, T_J	–55	150	°C
	Storage range, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	2.2		5.5	V
I_{OUT}	Output current	0		1	A
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS737xx[2]			UNIT
		DRB [VSON]	DCQ [SOT-223]	DRV [WSON][3]	
		8 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[4]	49.5	53.1	67.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[5]	58.9	35.2	87.6	
$R_{\theta JB}$	Junction-to-board thermal resistance[6]	25.1	7.8	36.8	
ψ_{JT}	Junction-to-top characterization parameter[7]	1.7	2.9	1.8	
ψ_{JB}	Junction-to-board characterization parameter[8]	25.2	7.7	37.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance[9]	8.6	N/A	7.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
  (a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2 × 2 thermal via array.
  ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3 × 2 thermal via array.
  iii. DRV: The exposed pad is connected to the PCB ground layer through a 2 × 2 thermal via array. Due to size limitation of thermal pad, 0.8-mm pitch array is used which is off the JEDEC standard.
  (b) The top copper layer has a detailed copper trace pattern. The bottom copper layer is assumed to have a 20% thermal conductivity of copper, representing a 20% copper coverage.
  (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3-inch × 3-inch copper area. To understand the effects of the copper area on thermal performance, see the *Power Dissipation* and *Estimating Junction Temperature* sections of this data sheet.
(3) Power dissipation may limit operating range.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(7) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), $V_{IN} = V_{OUT(nom)}$ + 1 V[(1)], I_{OUT} = 10 mA, V_{EN} = 2.2 V, and C_{OUT} = 2.2 µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range[(1)(2)]		2.2		5.5	V
V_{FB}	Internal reference (DCQ package)	T_J = 25°C	1.198	1.204	1.21	V
V_{FB}	Internal reference (DRB and DRV packages)	T_J = 25°C	1.192	1.204	1.216	V
V_{OUT}	Output voltage range (TPS73701)[(3)]		V_{FB}		5.5 – V_{DO}	V
V_{OUT}	Accuracy[(1),(4)] — Nominal	T_J = 25°C	–1		1	V
V_{OUT}	Accuracy[(1),(4)]	5.36 V < V_{IN} < 5.5 V, V_{OUT} = 5.08 V, 10 mA < I_{OUT} < 800 mA, –40°C < T_J < 85°C, TPS73701 (DCQ)	–2		2	V
V_{OUT}	Accuracy[(1),(4)] — Over V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V; 10 mA ≤ I_{OUT} ≤ 1 A	–3	±0.5%	3	V
$\Delta V_{OUT(\Delta VIN)}$	Line regulation[(1)]	$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V		0.01		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	1 mA ≤ I_{OUT} ≤ 1 A		0.002		%/mA
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	10 mA ≤ I_{OUT} ≤ 1 A		0.0005		%/mA
V_{DO}	Dropout voltage[(5)] ($V_{IN} = V_{OUT(nom)}$ – 0.1 V)	I_{OUT} = 1 A		130	500	mV
$Z_{OUT(DO)}$	Output impedance in dropout	2.2 V ≤ V_{IN} ≤ V_{OUT} + V_{DO}		0.25		Ω
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$	1.05	1.6	2.2	A
I_{OS}	Short-circuit current	V_{OUT} = 0 V		450		mA
I_{REV}	Reverse leakage current[(6)] (–I_{IN})	V_{EN} ≤ 0.5 V, 0 V ≤ V_{IN} ≤ V_{OUT}		0.1		µA
I_{GND}	GND pin current	I_{OUT} = 10 mA		400		µA
I_{GND}	GND pin current	I_{OUT} = 1 A		1300		µA
I_{SHDN}	Shutdown current [I_{GND}]	V_{EN} ≤ 0.5 V, V_{OUT} ≤ V_{IN} ≤ 5.5		20		nA
I_{FB}	FB pin current (TPS73701)			0.1	0.6	µA
PSRR	Power-supply rejection ratio (ripple rejection)	f = 100 Hz, I_{OUT} = 1 A		58		dB
PSRR	Power-supply rejection ratio (ripple rejection)	f = 10 kHz, I_{OUT} = 1 A		37		dB
V_n	Output noise voltage BW = 10 Hz to 100 kHz	C_{OUT} = 10 µF		27 × V_{OUT}		$µV_{RMS}$
t_{STR}	Start-up time	V_{OUT} = 3 V, R_L = 30 Ω, C_{OUT} = 1 µF		600		µs
$V_{EN(HI)}$	EN pin high (enabled)		1.7		V_{IN}	V
$V_{EN(LO)}$	EN pin low (shutdown)		0		0.5	V
$I_{EN(HI)}$	EN pin current (enabled)	V_{EN} = 5.5 V		20		nA
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
T_{sd}	Thermal shutdown temperature	Reset, temperature decreasing		140		°C
T_J	Operating junction temperature		–40		125	°C

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.2 V, whichever is greater.
(2) For $V_{OUT(nom)}$ < 1.6 V, when V_{IN} ≤ 1.6V, the output locks to V_{IN} and may result in an over-voltage condition on the output. To avoid this situation, disable the device before powering down V_{IN}.
(3) TPS73701 is tested at V_{OUT} = 1.2 V.
(4) Tolerance of external resistors not included in this specification.
(5) V_{DO} is not measured for fixed output versions with $V_{OUT(nom)}$ < 2.3 V because minimum V_{IN} = 2.2 V.
(6) Fixed-voltage versions only; refer to the *Application Information* section for more information.

6.6 Typical Characteristics

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 10 mA, V_{EN} = 2.2 V, and C_{OUT} = 2.2 µF, unless otherwise noted.

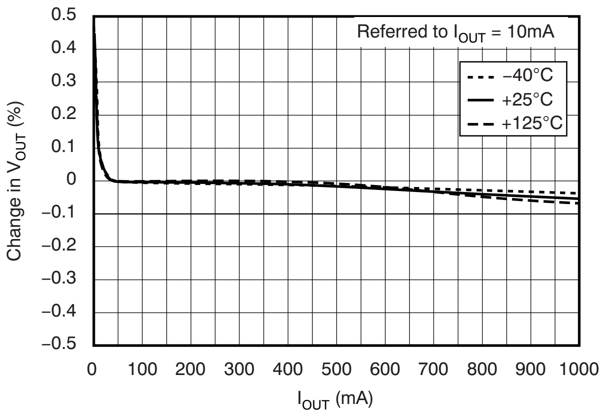


Figure 1. Load Regulation

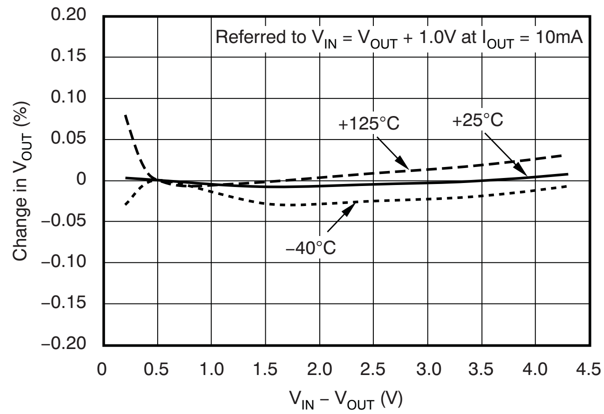


Figure 2. Line Regulation

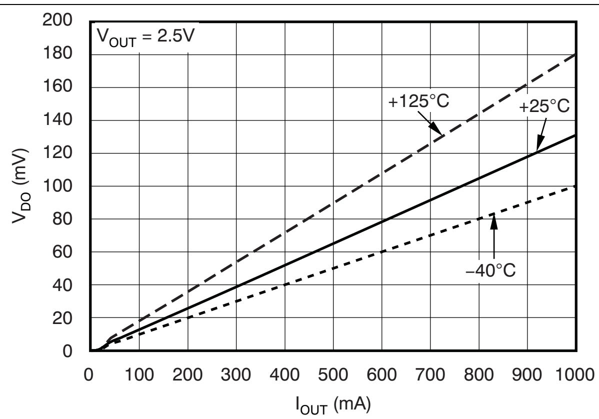


Figure 3. Dropout Voltage vs Output Current

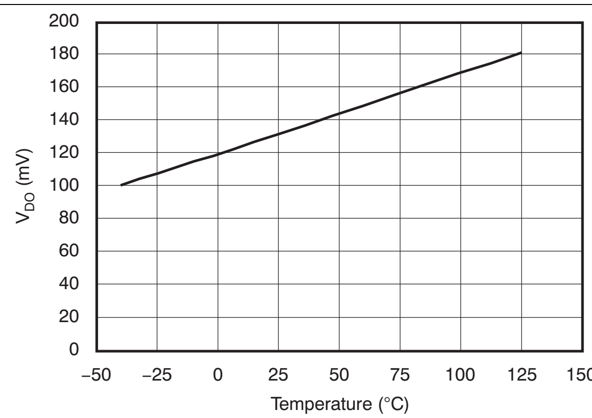


Figure 4. Dropout Voltage vs Temperature

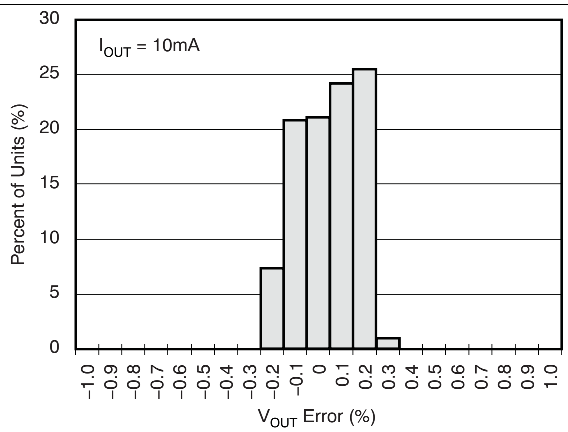


Figure 5. Output Voltage Histogram

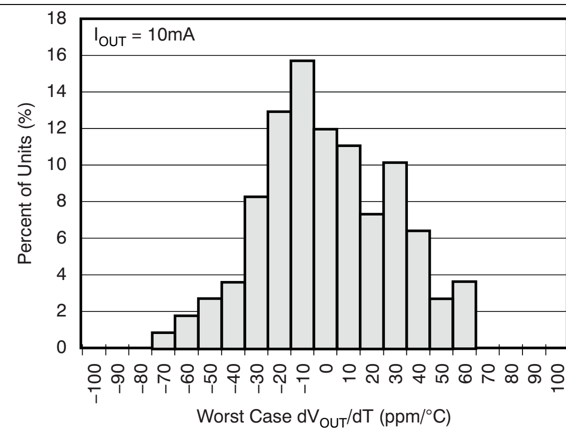


Figure 6. Output Voltage Drift Histogram

Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 10 mA, V_{EN} = 2.2 V, and C_{OUT} = 2.2 μF, unless otherwise noted.

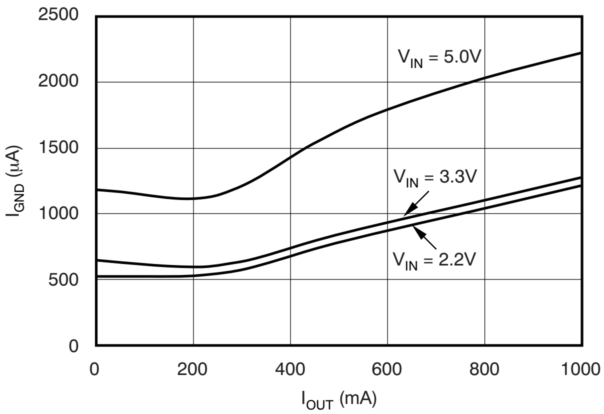


Figure 7. Ground Pin Current vs Output Current

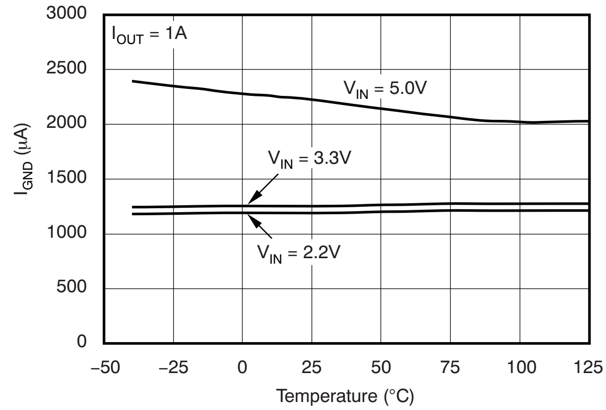


Figure 8. Ground Pin Current vs Temperature

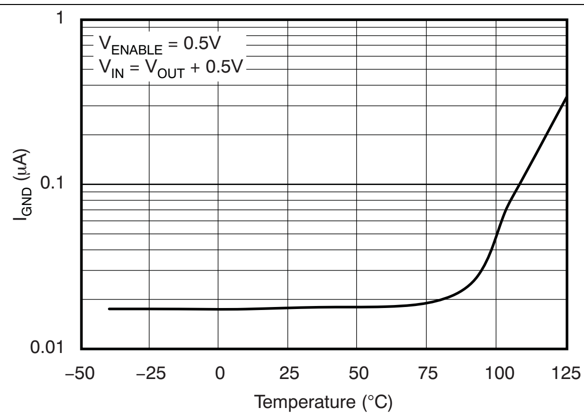


Figure 9. Ground Pin Current in Shutdown vs Temperature

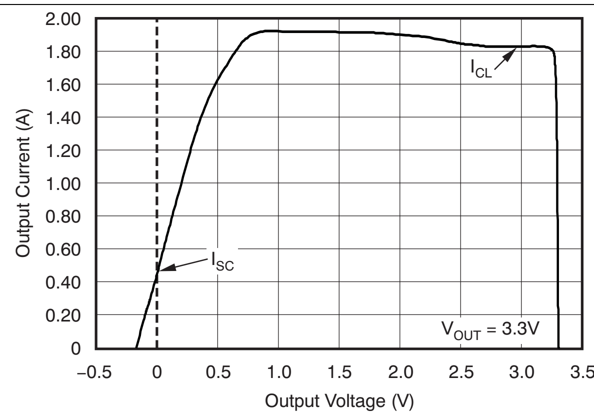


Figure 10. Current Limit vs V_{OUT} (Foldback)

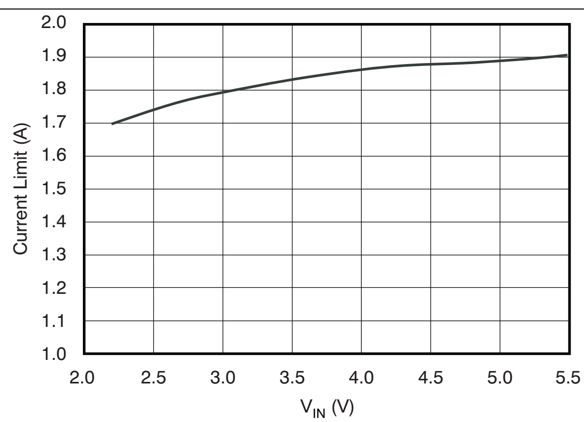


Figure 11. Current Limit vs V_{IN}

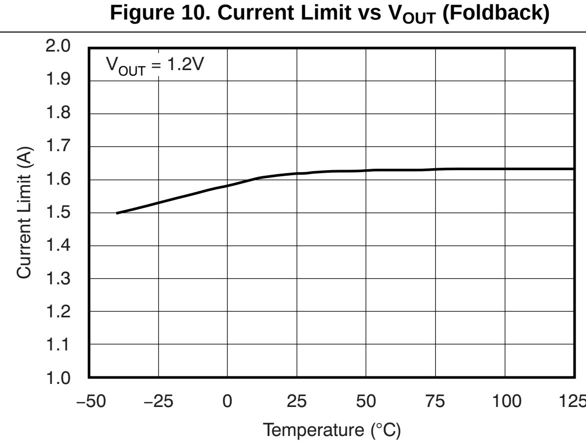


Figure 12. Current Limit vs Temperature

Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, $V_{IN} = V_{OUT(nom)}$ + 1 V, I_{OUT} = 10 mA, V_{EN} = 2.2 V, and C_{OUT} = 2.2 μF, unless otherwise noted.

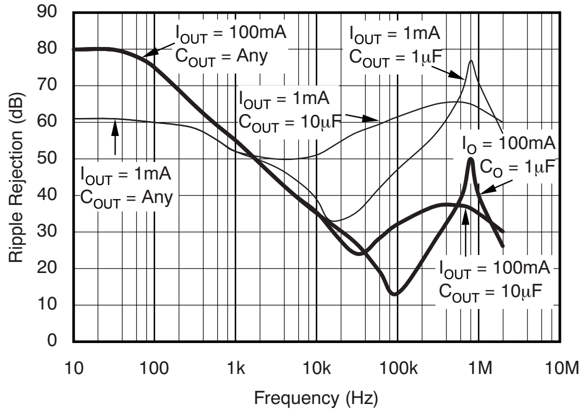


Figure 13. PSRR (Ripple Rejection) vs Frequency

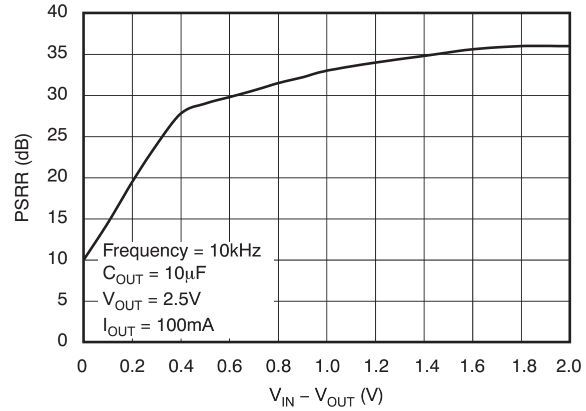


Figure 14. PSRR (Ripple Rejection) vs (V_{IN} – V_{OUT})

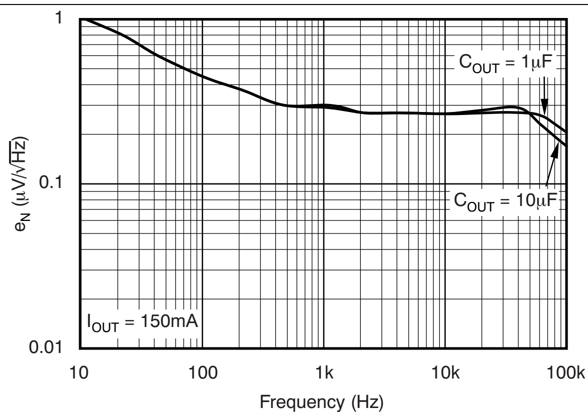


Figure 15. Noise Spectral Density

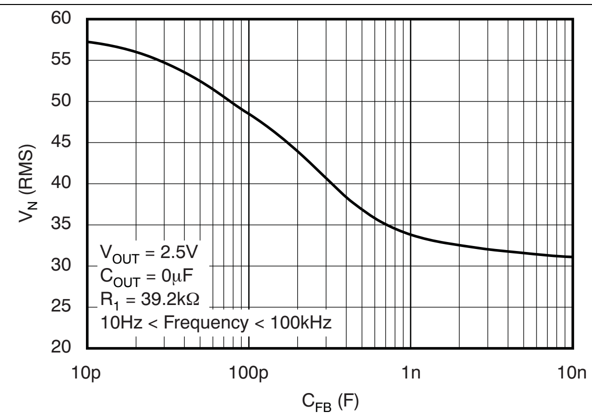


Figure 16. TPS73701 RMS Noise Voltage vs C_{FB}

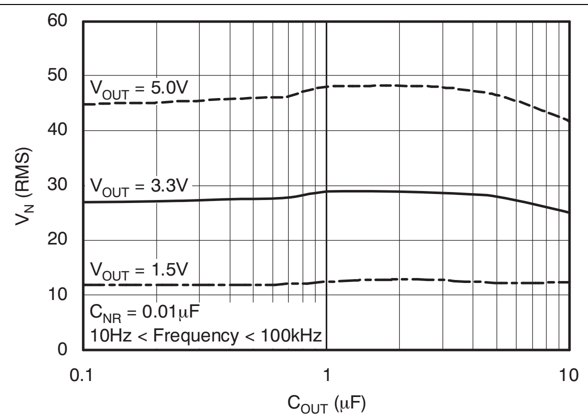


Figure 17. RMS Noise Voltage vs C_{OUT}

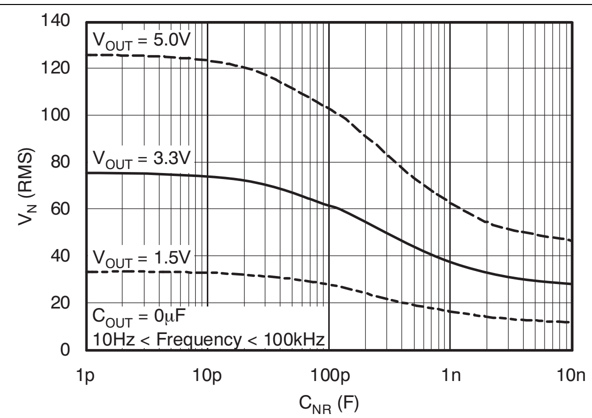


Figure 18. RMS Noise Voltage vs C_{NR}

Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, $V_{IN} = V_{OUT(nom)}$ + 1 V, I_{OUT} = 10 mA, V_{EN} = 2.2 V, and C_{OUT} = 2.2 µF, unless otherwise noted.

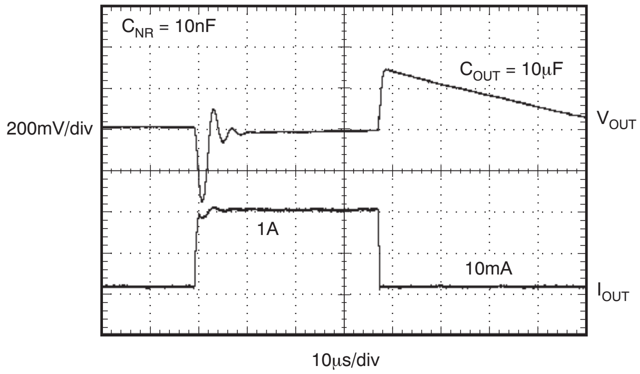


Figure 19. TPS73733 Load Transient Response

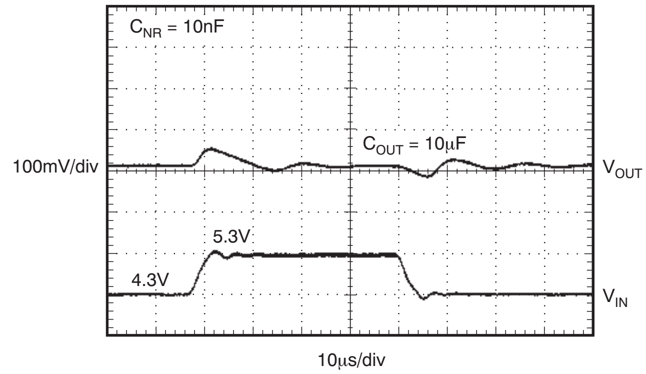


Figure 20. TPS73733 Line Transient Response

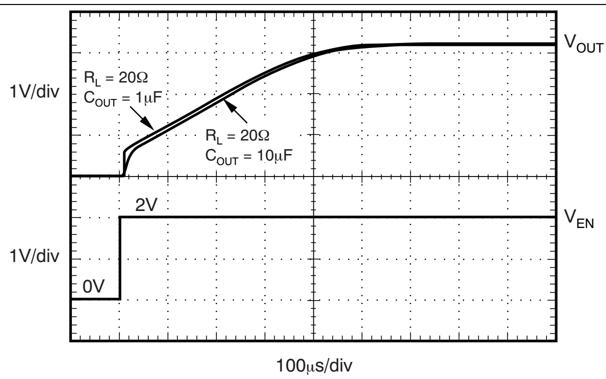


Figure 21. TPS73701 Turnon Response

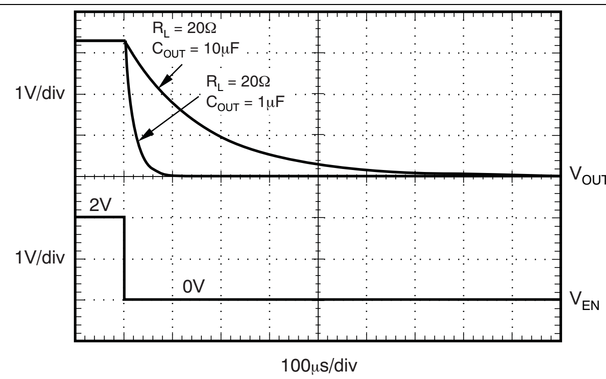


Figure 22. TPS73701 Turnoff Response

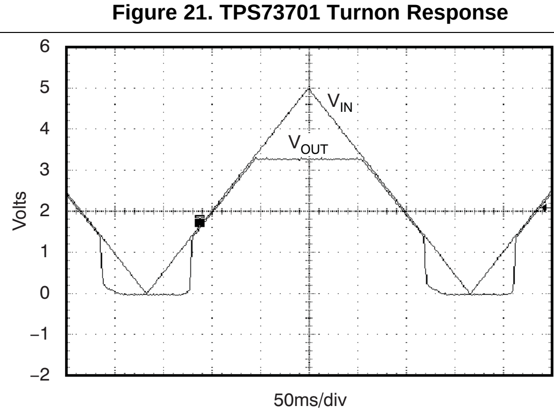


Figure 23. TPS73701, V_{OUT} = 3.3-V Power Up and Power Down

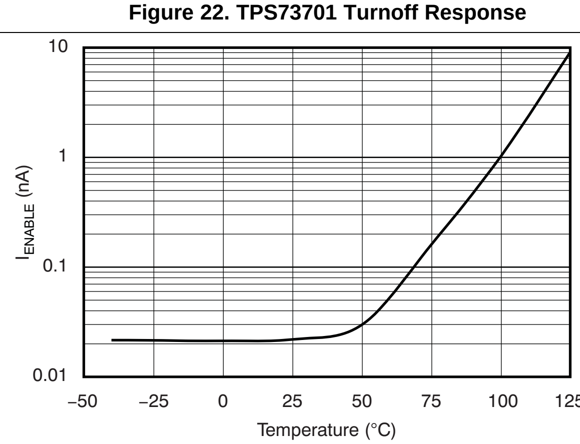


Figure 24. I_{EN} vs Temperature

Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, $V_{IN} = V_{OUT(nom)}$ + 1 V, I_{OUT} = 10 mA, V_{EN} = 2.2 V, and C_{OUT} = 2.2 μF, unless otherwise noted.

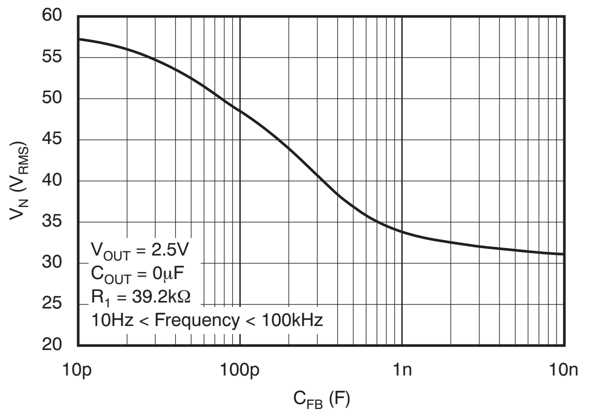


Figure 25. TPS73701 RMS Noise Voltage vs C_{FB}

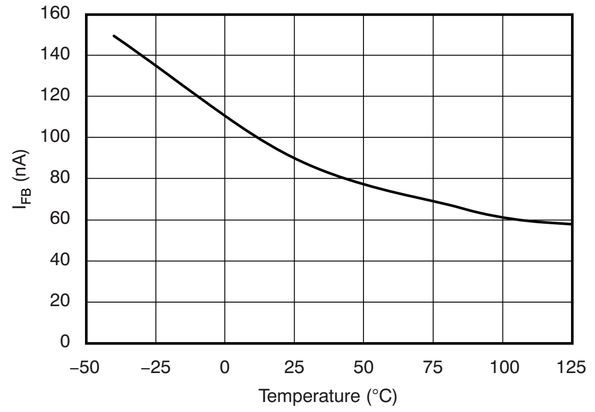


Figure 26. TPS73701 I_{FB} vs Temperature

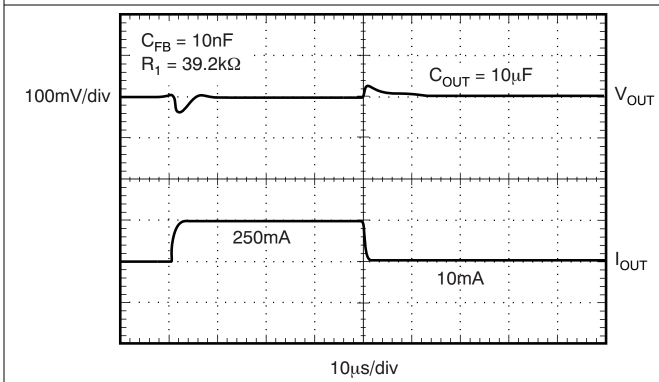


Figure 27. TPS73701 Load Transient, Adjustable Version

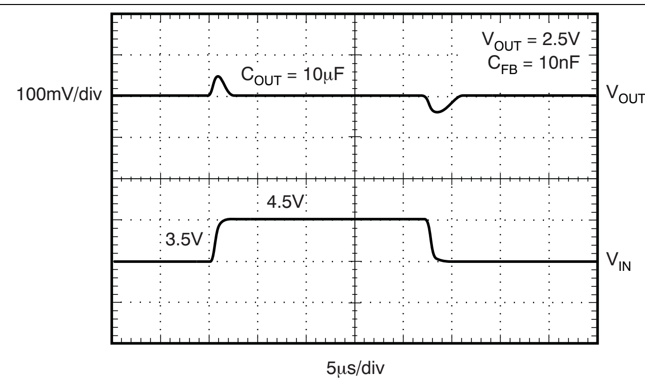


Figure 28. TPS73701 Line Transient, Adjustable Version

7 Detailed Description

7.1 Overview

The TPS737xx belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultralow dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features combined with an enable input make the TPS737xx ideal for portable applications. This regulator family offers a wide selection of fixed-output voltage versions and an adjustable-output version. All versions have thermal and overcurrent protection, including foldback current-limit.

7.2 Functional Block Diagrams

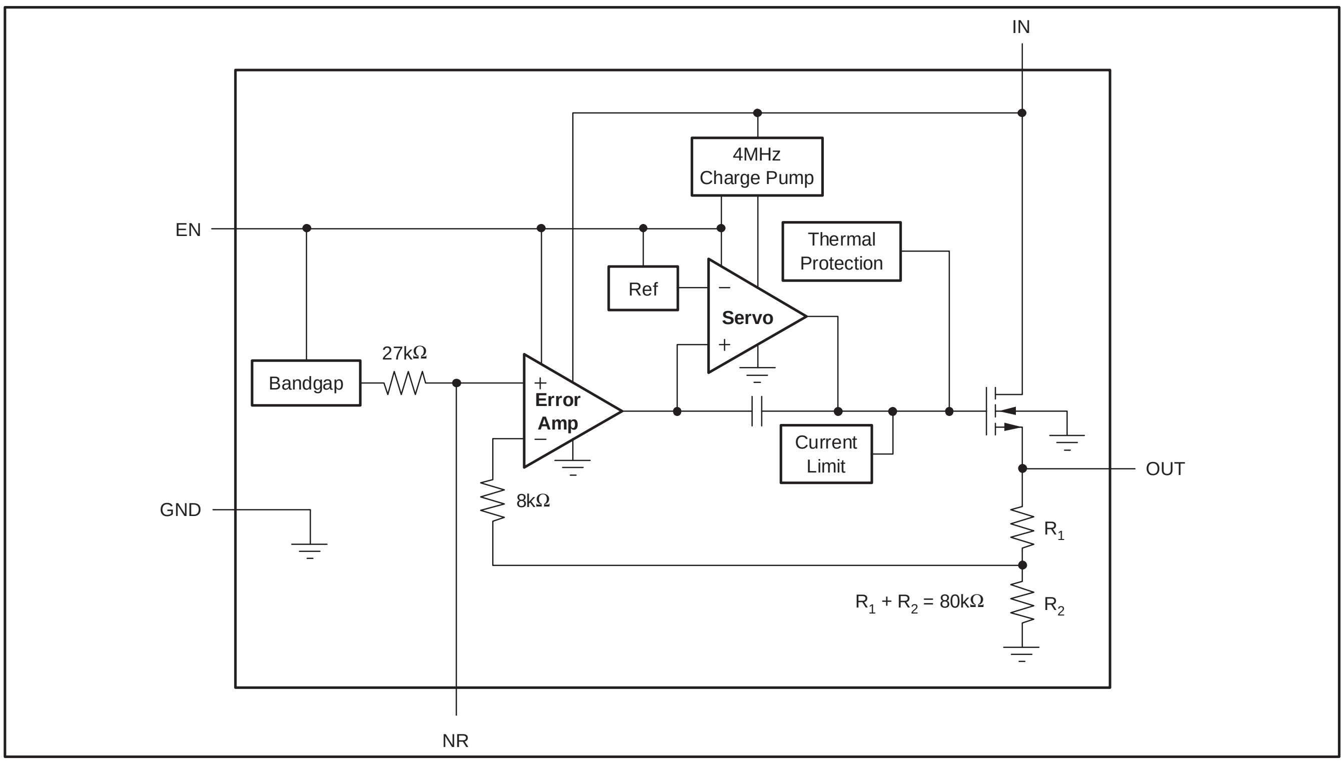
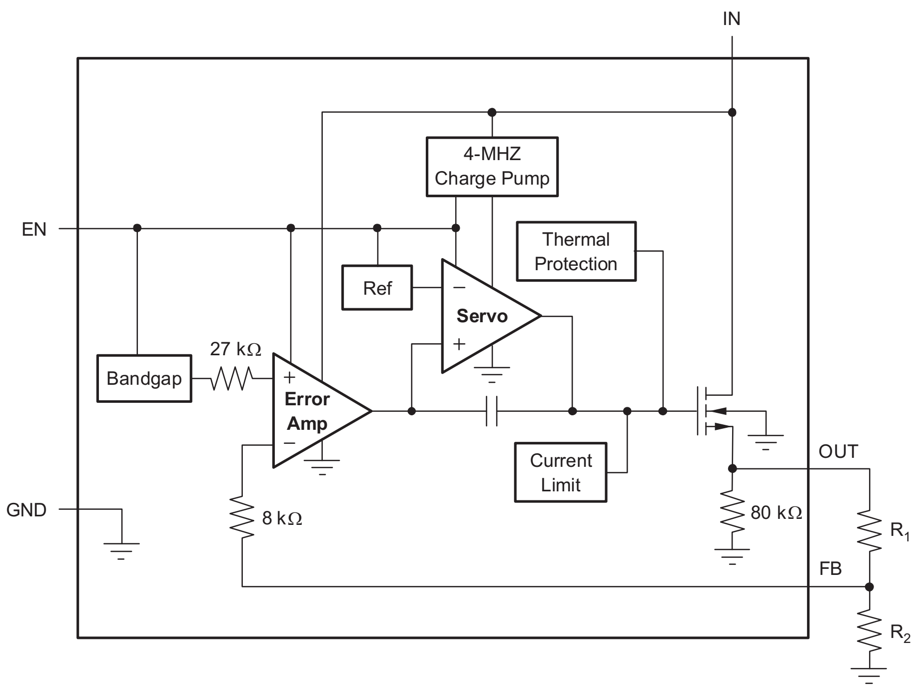


Figure 29. Fixed-Voltage Version

Functional Block Diagrams (continued)



Standard 1% Resistor Values for Common Output Voltages

V_{OUT}	R_1	R_2
1.2 V	Short	Open
1.5 V	23.2 kΩ	95.3 kΩ
1.8 V	28.0 kΩ	56.2 kΩ
2.5 V	39.2 kΩ	36.5 kΩ
2.8 V	44.2 kΩ	33.2 kΩ
3.0 V	46.4 kΩ	30.9 kΩ
3.3 V	52.3 kΩ	30.1 kΩ

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$; $R_1 \parallel R_2 \cong 19\ k\Omega$ for best accuracy.

Figure 30. Adjustable-Voltage Version

7.3 Feature Description

7.3.1 Output Noise

A precision bandgap reference is used to generate the internal reference voltage, V_{ref}. This reference is the dominant noise source within the TPS737xx and it generates approximately 32 μV_{RMS} (10 Hz to 100 kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Because the value of V_R is 1.2 V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (2)$$

for the case of no C_{NR}.

An internal 27-kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10 nF, the total noise in the 10-Hz to 100-kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \text{x } V_{OUT}(V) \quad (3)$$

for C_{NR} = 10 nF.

This noise reduction effect is shown as *RMS Noise Voltage vs C_{NR}* in the *Typical Characteristics* section.

Feature Description (continued)

The TPS73701 adjustable version does not have the NR pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the feedback pin (FB) reduces output noise and improve load transient performance. This capacitor should be limited to 0.1 µF.

The TPS737xx uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates approximately 250 µV of switching noise at approximately 4 MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

7.3.2 Internal Current Limit

The TPS737xx internal current limit helps protect the regulator during fault conditions. Foldback current-limit helps to protect the regulator from damage during output short-circuit conditions by reducing current-limit when V_{OUT} drops below 0.5 V. See Figure 10 in the *Typical Characteristics* section.

Note from Figure 10 that approximately –0.2 V of V_{OUT} results in a current-limit of 0 mA. Therefore, if OUT is forced below –0.2 V before EN goes high, the device may not start up. In applications that work with both a positive and negative voltage supply, the TPS737xx should be enabled first.

7.3.3 Enable Pin and Shutdown

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. V_{EN} below 0.5 V (maximum) turns the regulator off and drops the GND pin current to approximately 10 nA. When EN is used to shutdown the regulator, all charge is removed from the pass transistor gate, and the output ramps back up to a regulated V_{OUT} (see Figure 21).

When shutdown capability is not required, EN can be connected to V_{IN}. However, the pass gate may not be discharged using this configuration, and the pass transistor may be left on (enhanced) for a significant time after V_{IN} has been removed. This scenario can result in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output may overshoot upon power up.

Note that current limit foldback can prevent device start-up under some conditions. See the *Internal Current Limit* section for more information.

7.3.4 Reverse Current

The NMOS pass element of the TPS737xx provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the EN pin must be driven low before the input voltage is removed. If the EN pin is not driven low, the pass element may be left on because of stored charge on the gate.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Reverse current is specified as the current flowing out of the IN pin because of voltage applied on the OUT pin. There is additional current flowing into the OUT pin as a result of the 80-kΩ internal resistor divider to ground (see Figure 29 and Figure 30).

For the TPS73701, reverse current may flow when V_{FB} is more than 1.0 V above V_{IN}.

7.4 Device Functional Modes

Driving the EN pin over 1.7 V turns on the regulator. Driving the EN pin below 0.5 V causes the regulator to enter shutdown mode. In shutdown, the current consumption of the device is reduced to 20 nA, typically.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS737xx family of LDO regulators use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS737xx ideal for portable applications. This regulator family offers a wide selection of fixed-output voltage versions and an adjustable-output version. All versions have thermal and overcurrent protection, including foldback current-limit.

8.2 Typical Applications

Figure 31 shows the basic circuit connections for the fixed-voltage models. Figure 32 gives the connections for the adjustable output version (TPS73701).

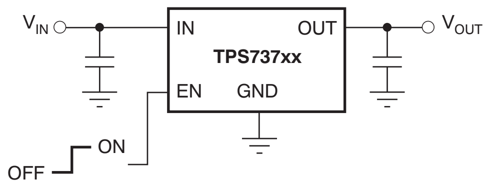


Figure 31. Typical Application Circuit for Fixed-Voltage Versions

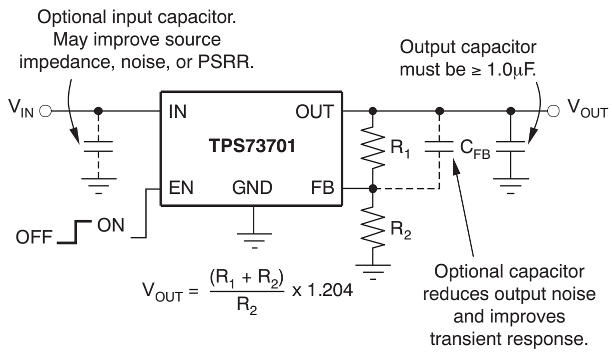


Figure 32. Typical Application Circuit for Adjustable-Voltage Version

8.2.1 Design Requirements

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 32. Sample resistor values for common output voltages are shown in Figure 30.

For best accuracy, make the parallel combination of R_1 and R_2 approximately equal to 19 kΩ. This 19 kΩ, in addition to the internal 8-kΩ resistor, presents the same impedance to the error amp as the 27-kΩ bandgap reference output. This impedance helps compensate for leakages into the error amp terminals.

8.2.2 Detailed Design Procedure

Provide an input supply with adequate headroom to account for dropout and output current to compensate for the GND terminal current and to power the load. Further, select adequate input and output capacitors as discussed in *Input and Output Capacitor Requirements*.

Typical Applications (continued)

8.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability if input impedance is very low, it is good analog design practice to connect a 0.1-μF to 1-μF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS737xx requires a 1-μF output capacitor for stability. It is designed to be stable for all available types and values of capacitors. In applications where multiple low-ESR capacitors are in parallel, ringing may occur when the product of C_{OUT} and total ESR drops below 50 nF. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

8.2.2.2 Dropout Voltage

The TPS737xx uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the NMOS pass element.

For large step changes in load current, the TPS737xx requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the DC dropout. Values of (V_{IN} – V_{OUT}) above this line ensure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN}-to-V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to DC dropout levels], the TPS737xx can take a couple of hundred microseconds to return to the specified regulation accuracy.

8.2.2.3 Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without a 1-μF output capacitor. As with any regulator, the addition of additional capacitance from the OUT pin to ground reduces undershoot magnitude but increases its duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the OUT pin to the FB pin will also improve the transient response.

The TPS737xx does not have active pulldown when the output is over-voltage. This architecture allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This architecture also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal/external load resistance. The rate of decay is given by:

(Fixed voltage version)

$$\frac{dV}{dT} = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel R_{LOAD}} \tag{4}$$

(Adjustable voltage version)

$$\frac{dV}{dT} = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \tag{5}$$

Typical Applications (continued)

8.2.3 Application Curves

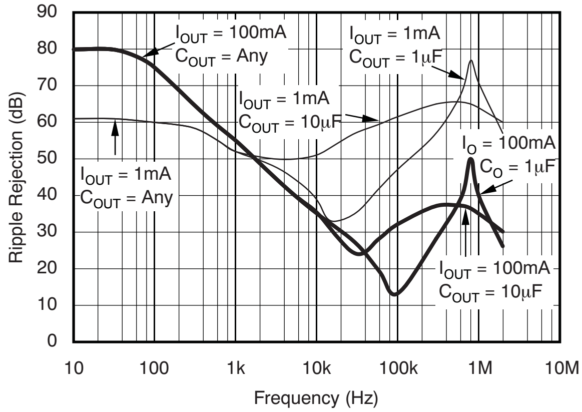


Figure 33. PSRR (Ripple Rejection) vs Frequency

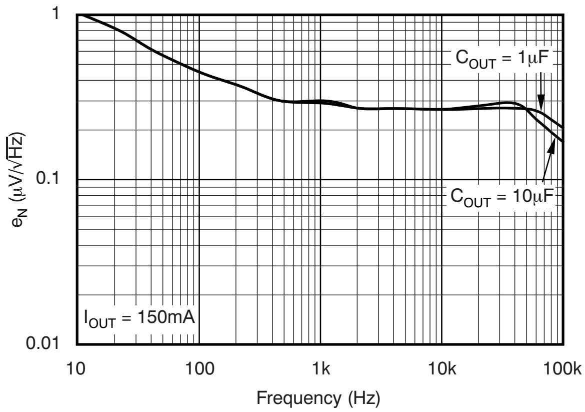


Figure 34. Noise Spectral Density

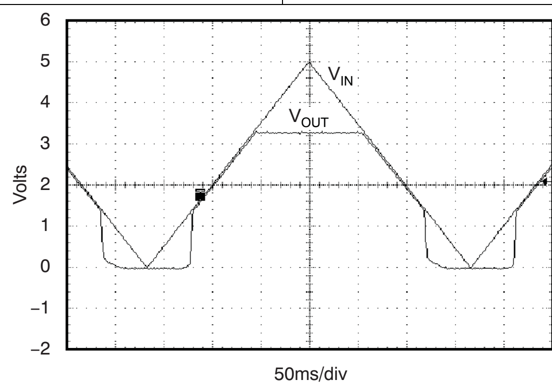


Figure 35. TPS73701, V_{OUT} = 3.3-V Power Up and Power Down

8.3 Do's and Don'ts

Place at least one 1-µF ceramic capacitor as close as possible to the OUT terminal of the regulator.

Do not place the output capacitor more than 10-mm away from the regulator.

Connect a 1-µF low equivalent series resistance (ESR) capacitor across the IN terminal and GND input of the regulator for improved transient performance.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.2 V and 5.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the printed-circuit-board (PCB) with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

10.2 Layout Example

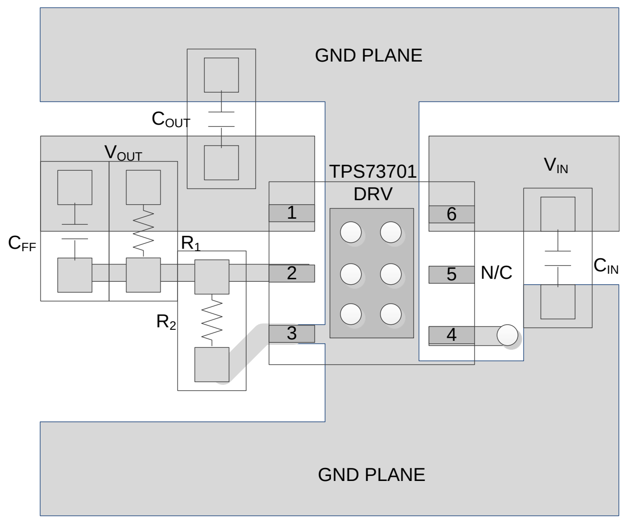


Figure 36. Layout Example

10.3 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 6:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{6}$$

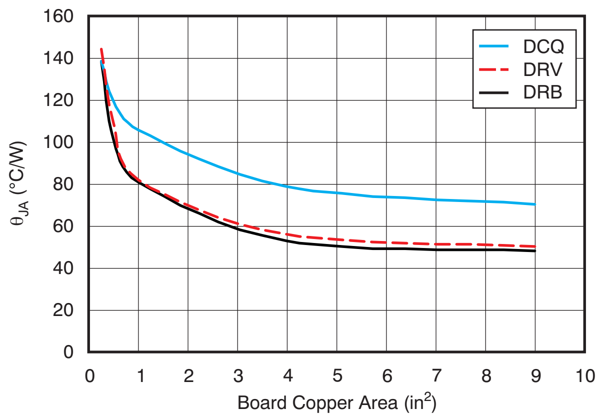
Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On both SON (DRB) and SON (DRV) packages, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. On the SOT-223 (DCQ) package, the primary conduction path for heat is through the tab to the PCB. That tab should be connected to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 7:

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \tag{7}$$

Power Dissipation (continued)

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 37.



Note: θ_{JA} value at board size of 9 in^2 (that is, 3 in × 3 in) is a JEDEC standard.

Figure 37. Θ_{JA} vs Board Size

Figure 37 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

NOTE

When the device is mounted on an application PCB, TI strongly recommends using Ψ_{JT} and Ψ_{JB}, as explained in the section.

10.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS737xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS737xx into thermal shutdown degrades device reliability.

10.5 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 8). For backward compatibility, an older $\theta_{JC,Top}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \qquad (8)$$

Estimating Junction Temperature (continued)

Where P_D is the power dissipation shown by Equation 6, T_T is the temperature at the center-top of the IC package, and T_B is the PCB temperature measured 1-mm away from the IC package *on the PCB surface* (as Figure 39 shows).

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note, *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

By looking at Figure 38, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 8 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

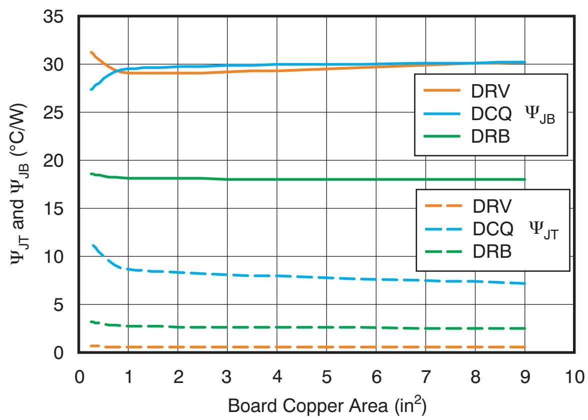
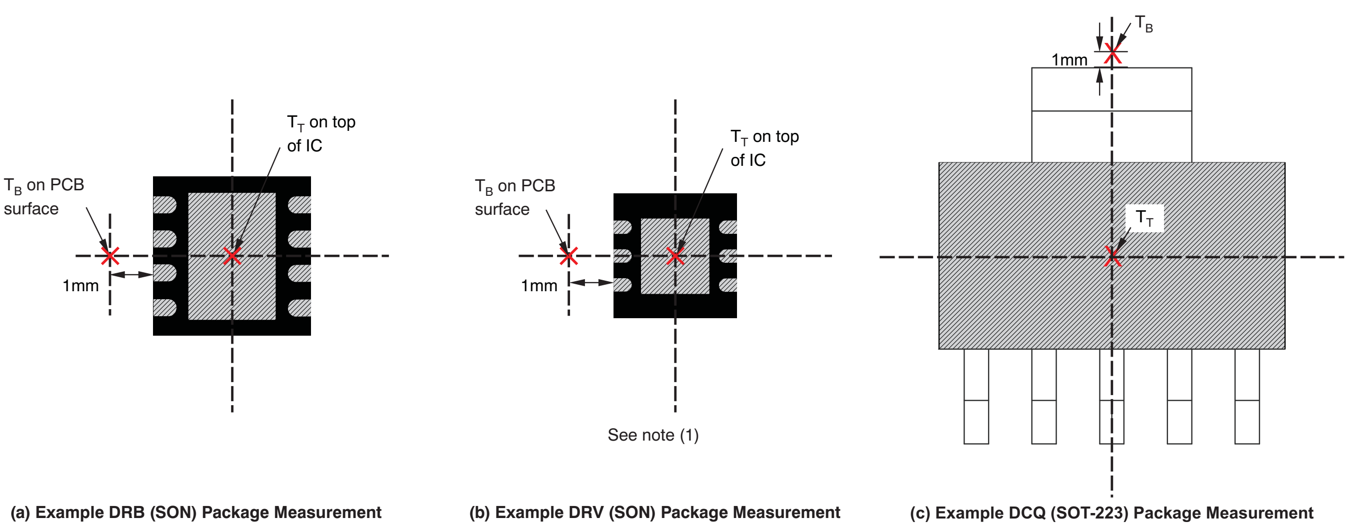


Figure 38. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, refer to application report, *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com. For further information, refer to application report, *IC Package Thermal Metrics* (SPRA953), also available on the TI website.



(1) Power dissipation may limit operating range. Check *Thermal Information* table.

Figure 39. Measuring Points for T_T and T_B

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS737xx. The TPS73701DRVEVM-529 evaluation module (and related user's guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS737 is available through the product folders under *Tools & Software*.

11.1.2 Device Nomenclature

Table 1. Ordering Information[1]

PRODUCT	V_{OUT}[1]
TPS737**xx yy yz**	**xx** is nominal output voltage (for example, 25 = 2.5 V, 01 = Adjustable [2]).
	yyy is the package designator.
	z is the package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.
(2) For fixed 1.20-V operation, tie FB to OUT.

11.2 Documentation Support

11.2.1 Related Documentation

- *Using New Thermal Metrics*, SBVA025
- *TPS73701DRVEVM-529 User's Guide*, SLVU880
- *TMS320DM644x Power Reference Design*, SLVA314
- *TPS73x01DRBEVM-518 User's Guide*, SBVU014

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73701DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS73701	Samples
TPS73701DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS73701	Samples
TPS73701DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS73701	Samples
TPS73701DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS73701	Samples
TPS73701DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BZN	Samples
TPS73701DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BZN	Samples
TPS73701DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BZN	Samples
TPS73701DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTN	Samples
TPS73701DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTN	Samples
TPS73718DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS73718	Samples
TPS73718DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS73718	Samples
TPS73718DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS73718	Samples
TPS73718DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS73718	Samples
TPS73718DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAL	Samples
TPS73718DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAL	Samples
TPS73725DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS73725	Samples
TPS73725DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS73725	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73725DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS73725	Samples
TPS73730DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVT	Samples
TPS73730DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVT	Samples
TPS73733DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS73733	Samples
TPS73733DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS73733	Samples
TPS73733DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS73733	Samples
TPS73733DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS73733	Samples
TPS73733DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIJ	Samples
TPS73733DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIJ	Samples
TPS73734DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCH	Samples
TPS73734DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS737 :

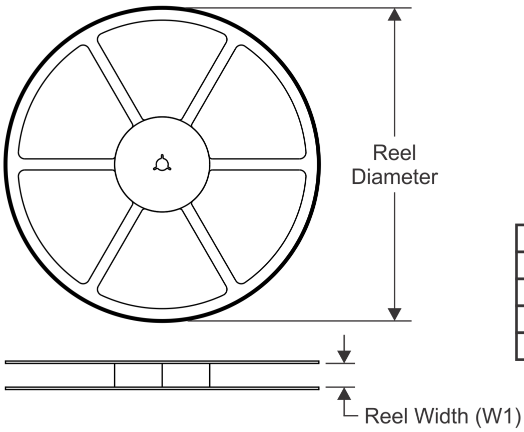
- Automotive: TPS737-Q1

NOTE: Qualified Version Definitions:

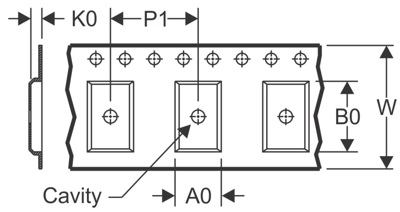
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

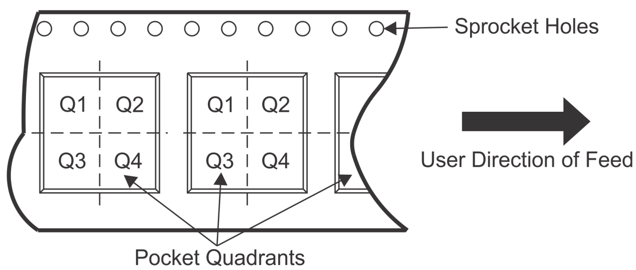


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

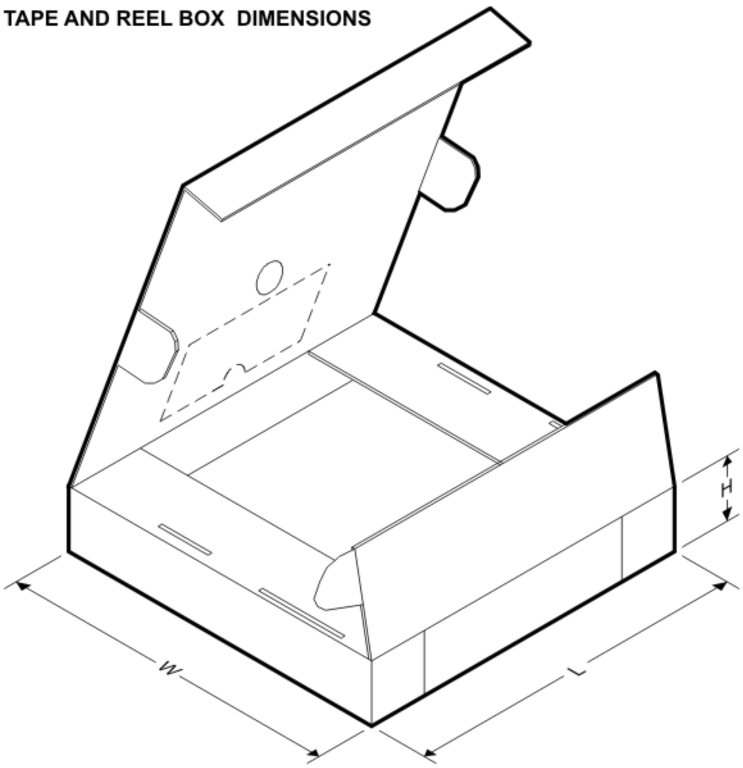


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73701DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73701DCQRG4	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73701DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73701DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73701DRBT	SON	DRB	8	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS73701DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73701DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73701DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73718DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73718DCQRG4	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73718DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73718DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73725DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73725DCQRG4	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73730DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73730DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73733DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73733DCQRG4	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73733DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73733DRVT	WSON	DRV	6	250	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73734DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS

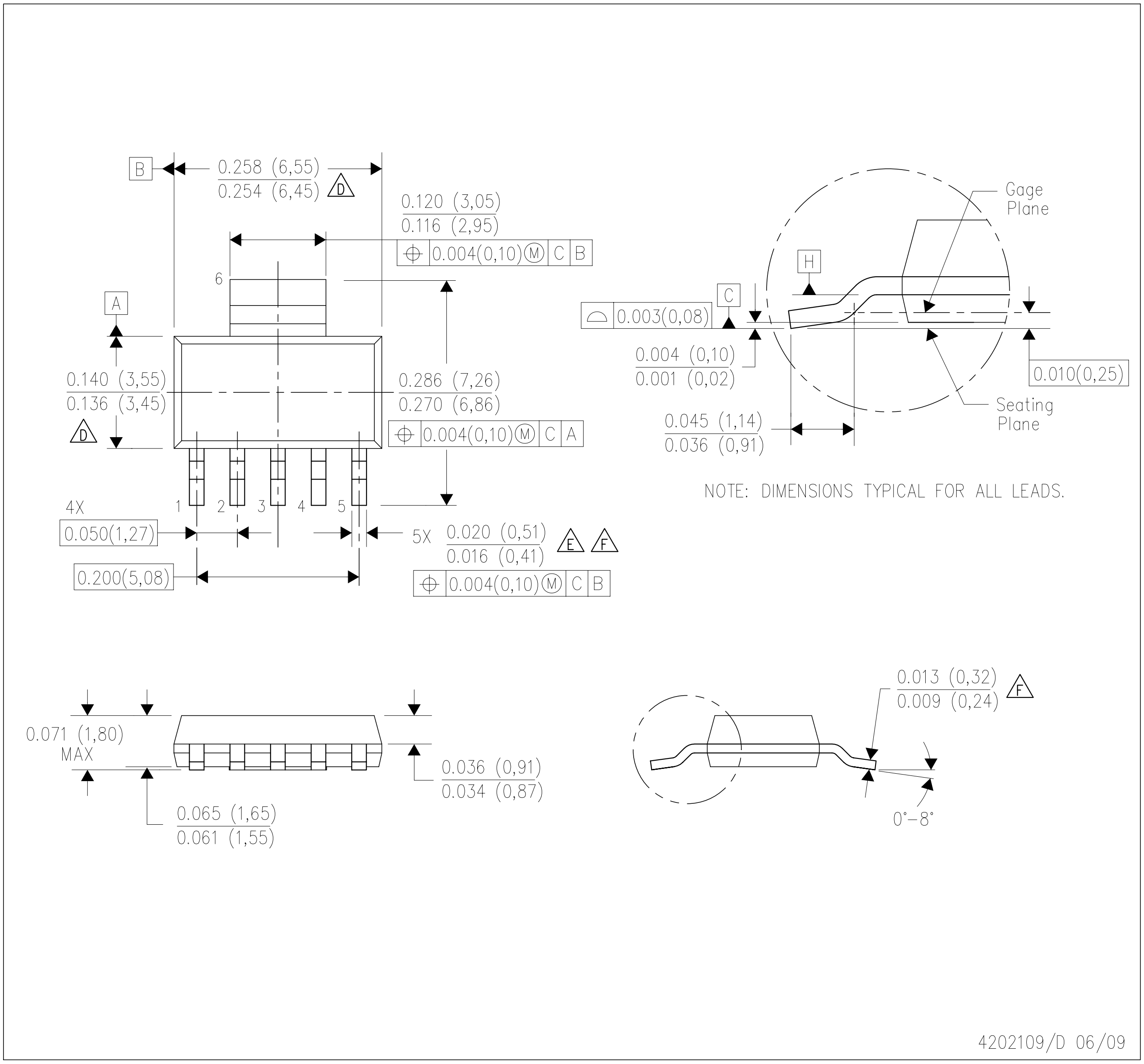


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73701DCQR	SOT-223	DCQ	6	2500	367.0	367.0	35.0
TPS73701DCQRG4	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS73701DRBR	SON	DRB	8	3000	338.0	355.0	50.0
TPS73701DRBR	SON	DRB	8	3000	552.0	367.0	36.0
TPS73701DRBT	SON	DRB	8	250	338.0	355.0	50.0
TPS73701DRBT	SON	DRB	8	250	552.0	185.0	36.0
TPS73701DRVR	WSON	DRV	6	3000	195.0	200.0	45.0
TPS73701DRVT	WSON	DRV	6	250	195.0	200.0	45.0
TPS73718DCQR	SOT-223	DCQ	6	2500	367.0	367.0	35.0
TPS73718DCQRG4	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS73718DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS73718DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS73725DCQR	SOT-223	DCQ	6	2500	367.0	367.0	35.0
TPS73725DCQRG4	SOT-223	DCQ	6	2500	346.0	346.0	41.0

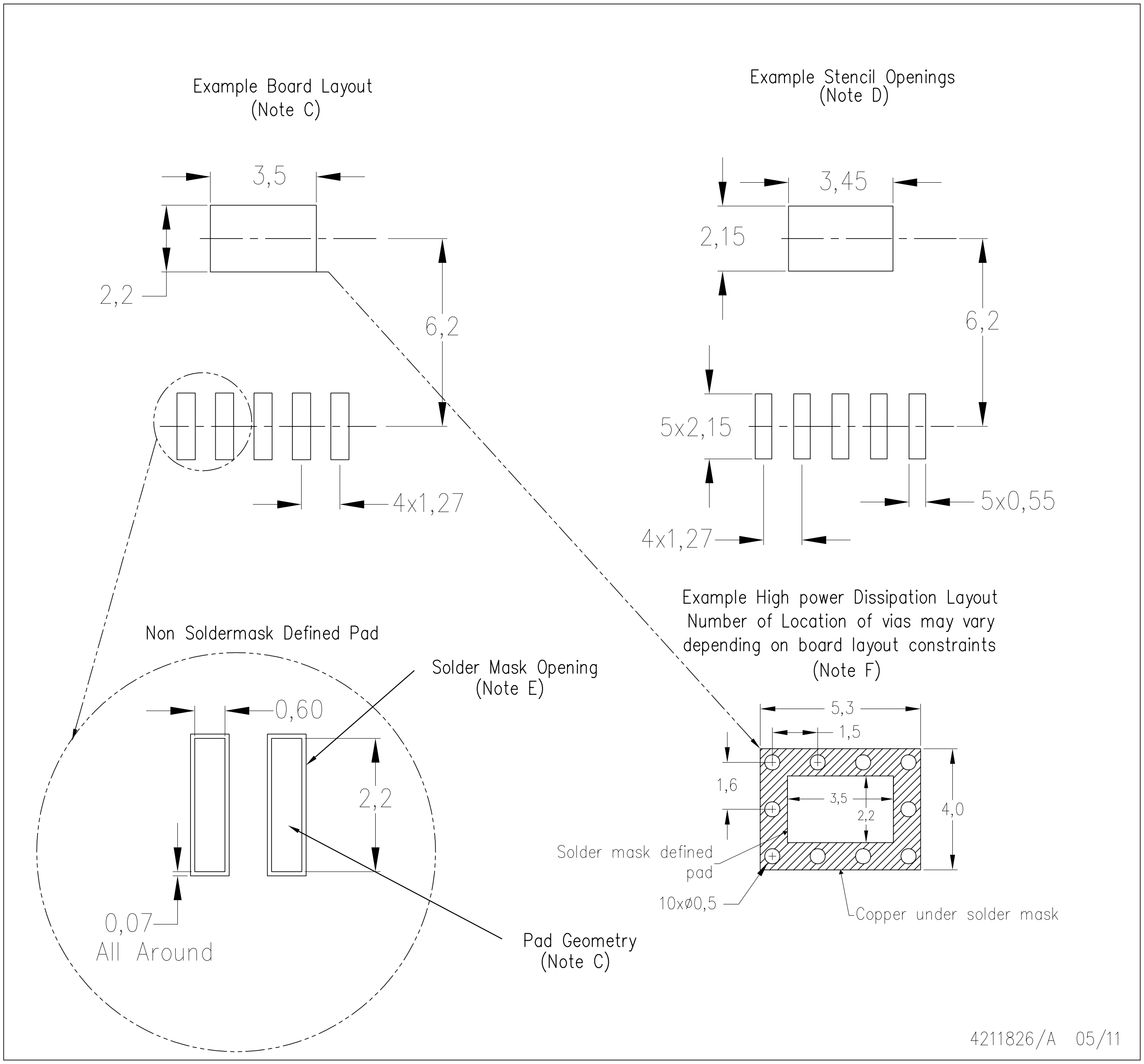
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73730DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS73730DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS73733DCQR	SOT-223	DCQ	6	2500	367.0	367.0	35.0
TPS73733DCQRG4	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS73733DRVR	WSON	DRV	6	3000	195.0	200.0	45.0
TPS73733DRVT	WSON	DRV	6	250	195.0	200.0	45.0
TPS73734DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0

DCQ (R–PDSO–G6) PLASTIC SMALL–OUTLINE



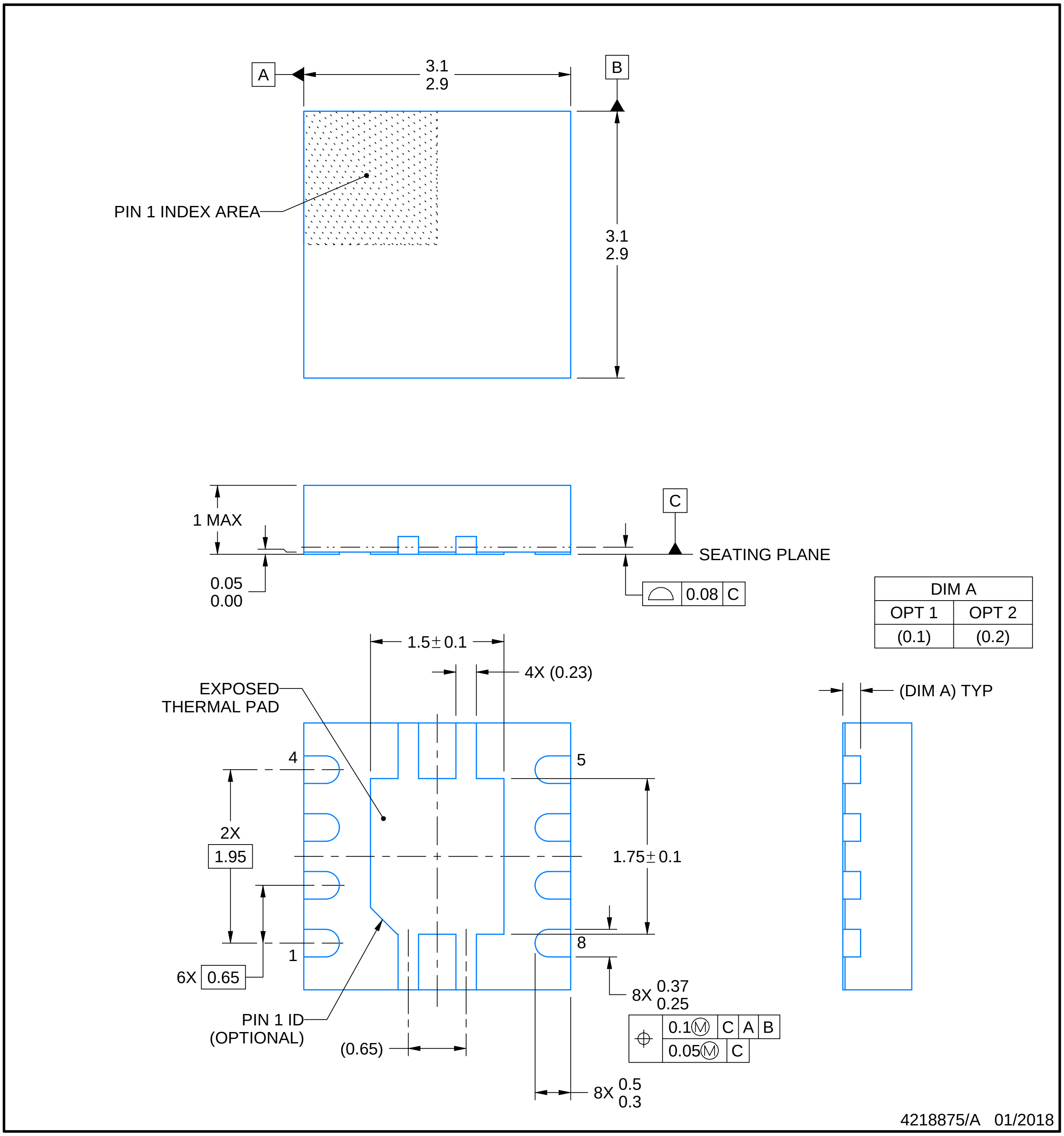
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Controlling dimension in inches.
- D. Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- E. Lead width dimension does not include dambar protrusion.
- F. Lead width and thickness dimensions apply to solder plated leads.
- G. Interlead flash allow 0.008 inch max.
- H. Gate burr/protrusion max. 0.006 inch.
- I. Datums A and B are to be determined at Datum H.

DCQ (R–PDSO–G6) PLASTIC SMALL OUTLINE



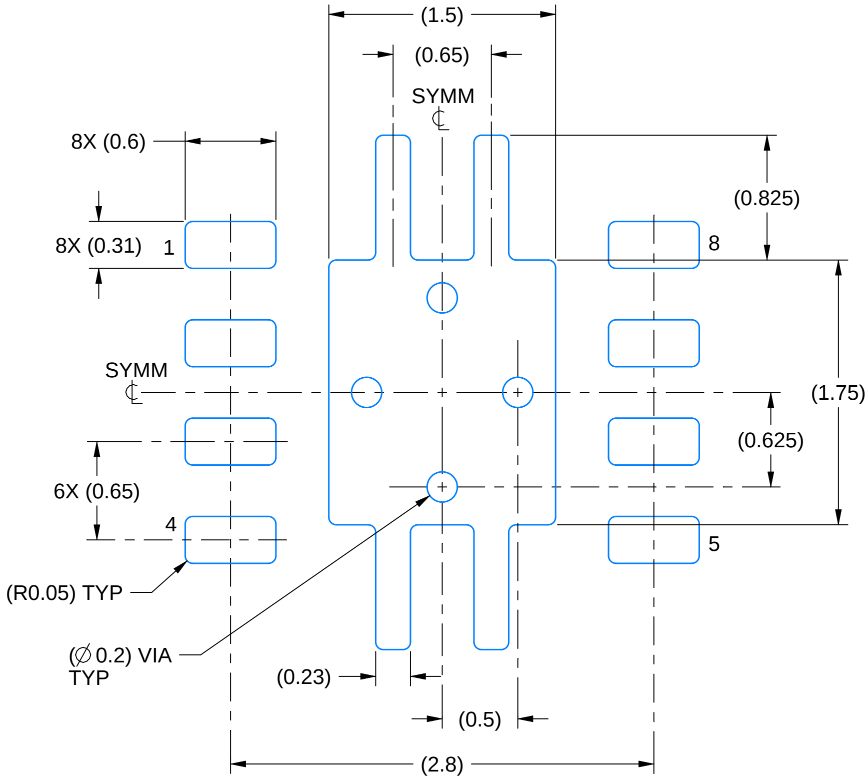
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. Please refer to the product data sheet for specific via and thermal dissipation requirements.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

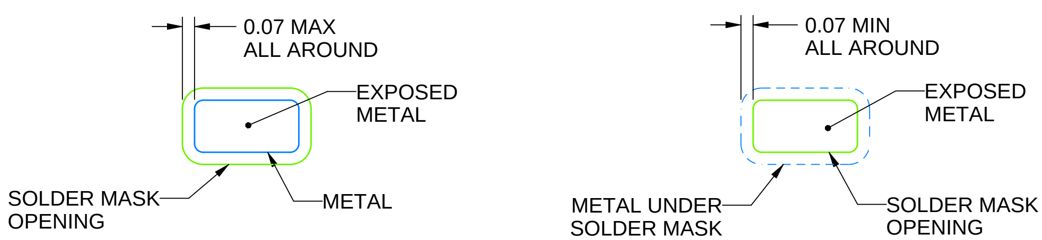


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK DEFINED (PREFERRED)

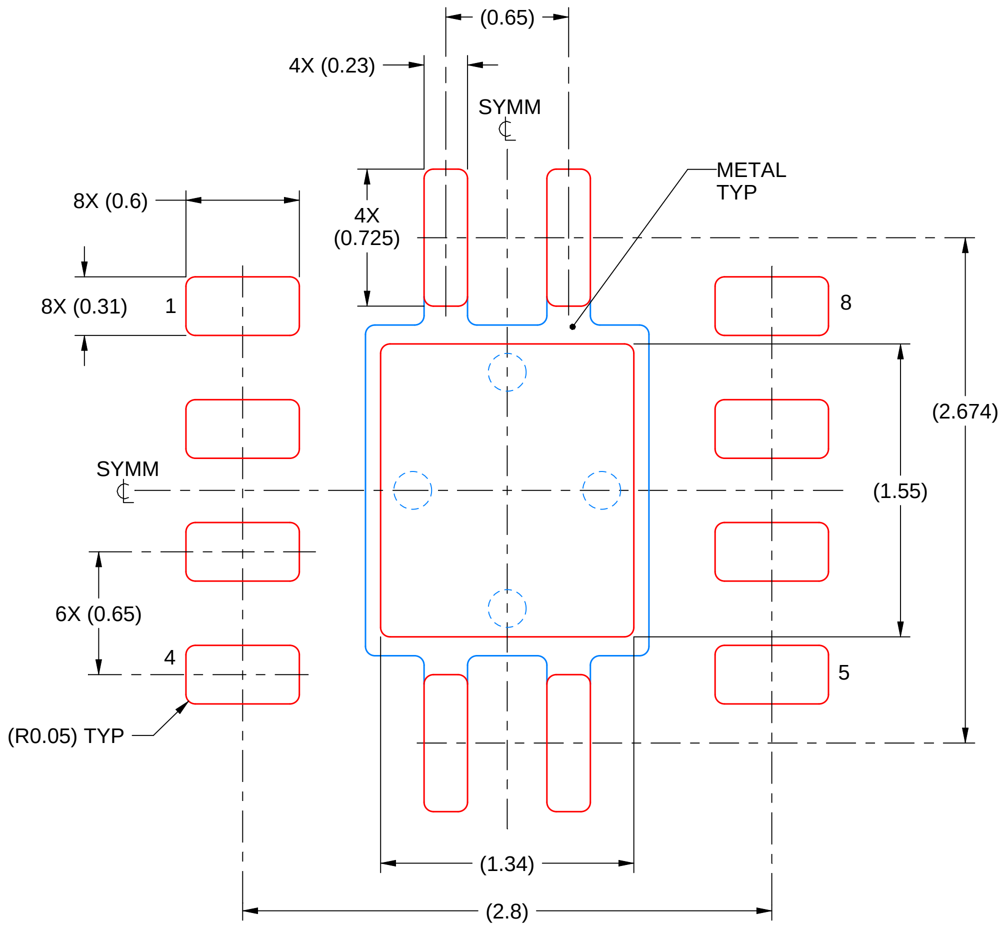
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



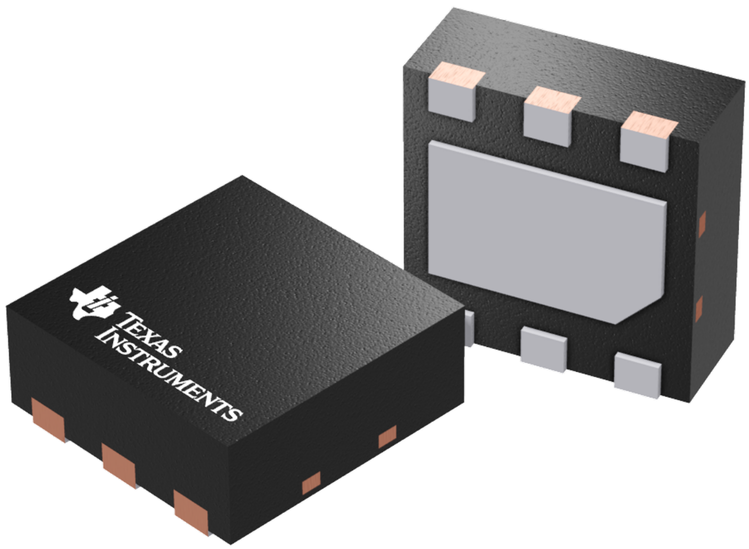
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

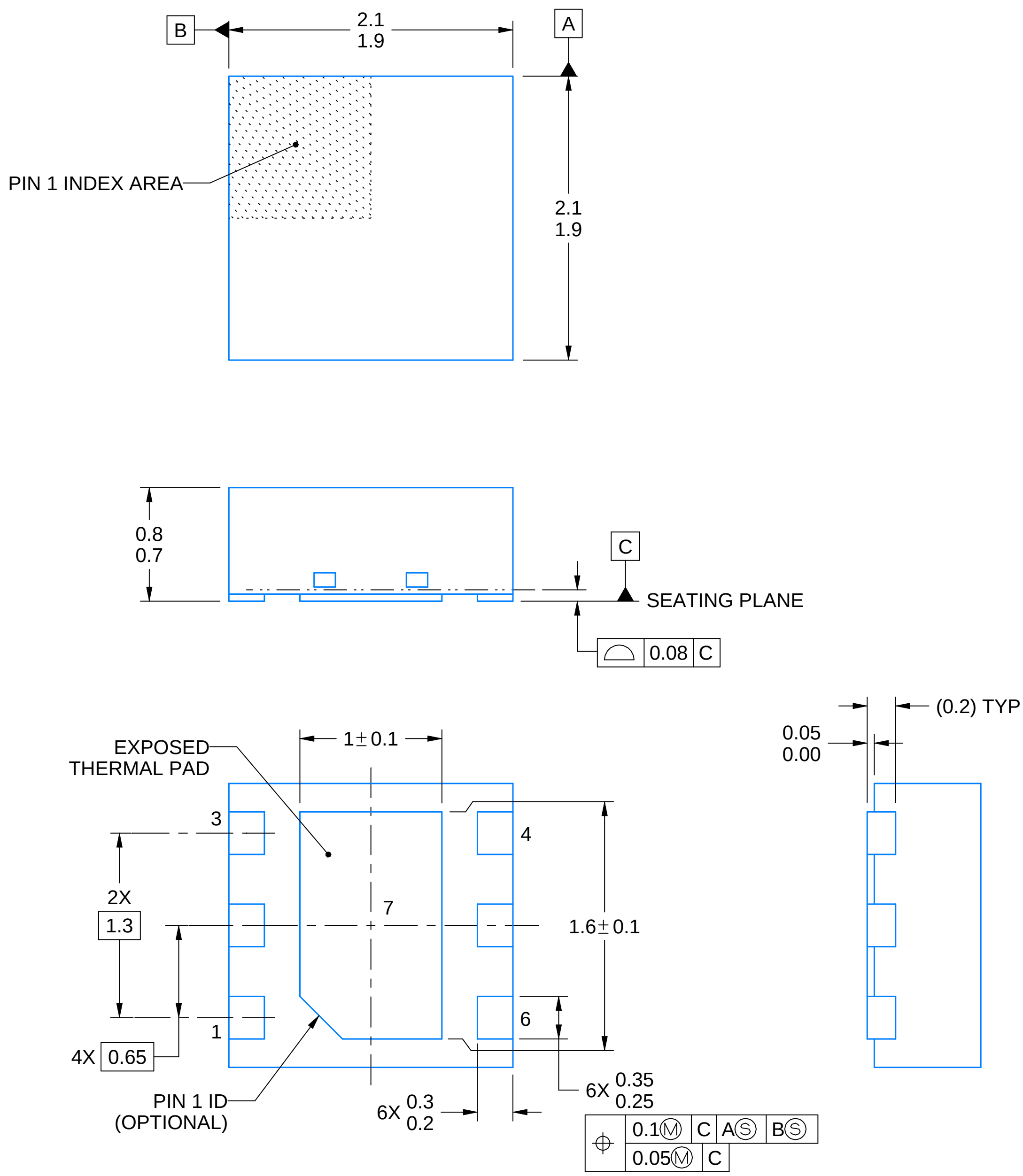
4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



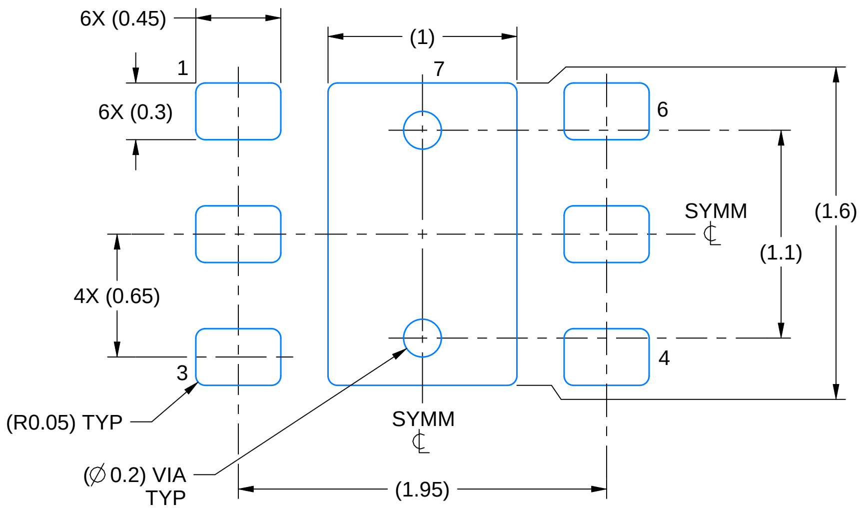
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



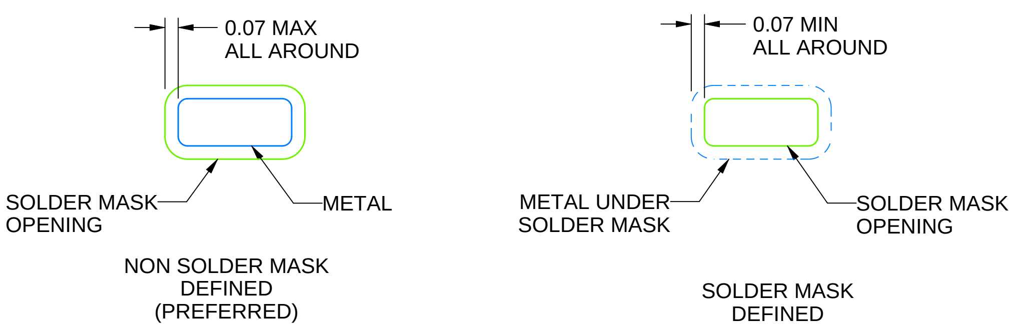
4222173/B 04/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X

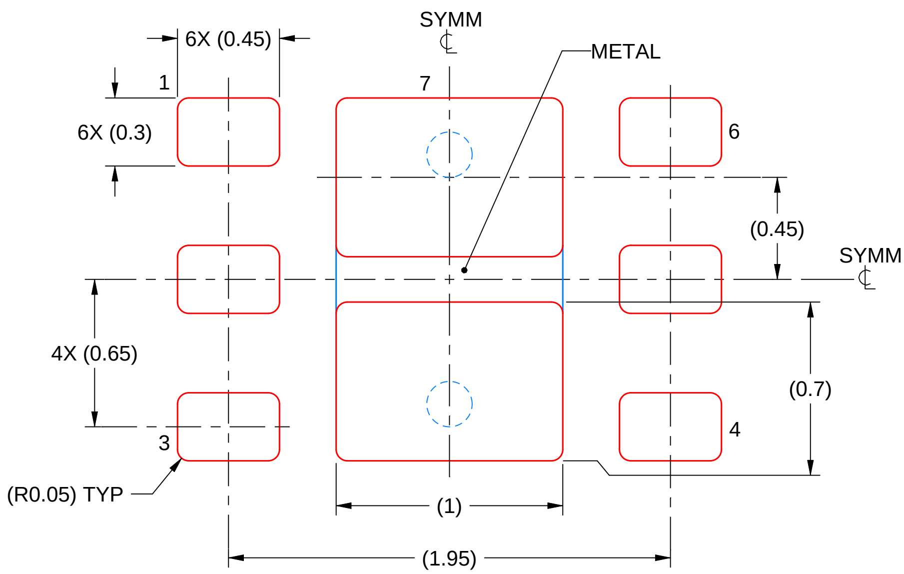


SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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