CDB8422

Evaluation Board for CS8422

Features

- IEC-60958, AES3/EBU, S/PDIF Inputs
  - Single-Ended Inputs via Optical and RCA Input Jacks
  - Differential Inputs via XLR Input Jack
- S/PDIF Outputs
  - Optical and RCA Output Jacks
  - CS8406 Digital Audio Transmitter
- I/O Stake Headers
  - External Control Port Accessibility
  - External Serial Audio I/O Accessibility
- 3.3 V Logic Interface
- Powered by Single External Power Supply or PC USB Port Connection
- H/W Control via DIP Switches
- FlexGUI S/W Control - Windows® Compatible
  - Pre-Defined & User-Configurable Scripts

Description

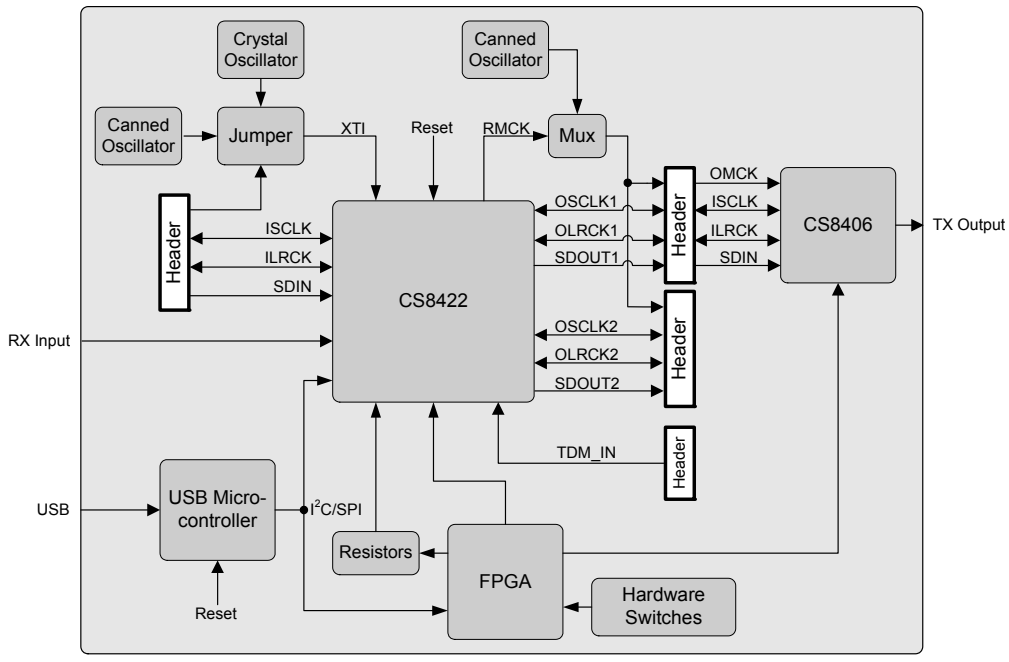
Using the CDB8422 evaluation board is an ideal way to evaluate the CS8422. Use of the board requires a digital signal source, an analyzer, and a power supply. A Windows PC-compatible computer is also required if using software mode to configure the CDB8422.

S/PDIF and AES3/EBU input connections are made via RCA phono, optical, or XLR connectors to the CS8422. S/PDIF output connections are made via RCA phono or optical connectors from the CS8406 (S/PDIF Tx). System timing can be provided by a S/PDIF or AES3/EBU input signal, by the CS8422 with supplied master clock, or by an I/O stake header with a DSP connected.

The provided Windows-based software GUI makes configuring the CDB8422 easy. The software communicates through the PC's USB port to configure the board so that all features of the CS8422 can be evaluated. The board may also be configured without a PC connection by using hardware switches; however, not all configurations of the CDB8422 are possible in hardware mode.

ORDERING INFORMATION

CDB8422	Evaluation Board



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1. SYSTEM OVERVIEW

The CDB8422 platform provides S/PDIF and AES3/EBU digital interfaces to the CS8422 and allows for external DSP and I²C® or SPI™ control port interconnects. On-board voltage regulators are provided so that a single external power supply of +5 V can be used to provide power for the CDB8422. Optionally, the evaluation board may be powered from a USB connection, which also serves as an interface to a PC. The CDB8422 is configured in software mode using Cirrus Logic's Windows-compatible FlexGUI software to read/write to device registers. In hardware mode, the evaluation board is configured using several DIP switches.

This section describes the various components on the CDB8422 and how they are used. The two following sections (Section 2 and Section 3) provide details on operating the CDB8422 in software and hardware mode, respectively. Both sections begin with a simplified quick connect guide provided for user convenience which can be used to set up the board quickly with the CS8422 in its startup default configuration. Next, descriptions are given for several useful configuration options in which the board can be used. Then, complete configuration details for each mode are described. Section 4, Section 5, and Section 6 provide a description of all stake headers, connectors, and LEDs on the board, including the default factory settings for all jumpers. The CDB8422 schematic and layout set is shown in Figures 15 through 29.

1.1 Power

Power and ground is supplied to the evaluation board via binding posts J2 and J3 (respectively) or the USB connection J37. Jumper J20 allows the user to select the power source (see Section 5 for details). The voltage connected to the binding posts should be +5 V. An on-board voltage regulator provides +3.3 V for the CS8422's VA, VL, and V_REG supplies. All voltage inputs are referenced to ground using the black binding post J3.

1.2 Grounding and Power Supply Decoupling

The CDB8422 demonstrates the optimal power supply and grounding arrangements for the CS8422. Figure 14 provides an overview of the connections to the CS8422. Figure 27 shows the component placement, Figure 28 shows the top layout, and Figure 29 shows the bottom layout. Power supply decoupling capacitors are located as close as possible to the CS8422. Extensive use of ground plane fill helps reduce radiated noise.

1.3 FPGA

The FPGA controls digital signal routing between the CS8422, the CS8406, and the I/O stake headers. It also provides routing control of the system master clock from an on-board canned oscillator, an on-board crystal oscillator, and the CS8422. The FPGA configures the CDB8422 in hardware mode and routes serial control signals from the micro controller to the CS8422 in software mode. The Cirrus FlexGUI software provides full control of the FPGA's routing and configuration options, see Section 2.3, Section 2.4, and Section 2.5 for details. A subset of the FPGA's options are accessible in hardware mode using DIP switches, see Section 3.3 for details.

1.4 CS8422

A complete description of the CS8422 can be found in the CS8422 product data sheet.

When the evaluation board is connected to a PC via the USB connector, the CS8422 is placed in software mode and is configured using the Cirrus FlexGUI. The device configuration registers are accessible via the "Register Maps" tab of the Cirrus FlexGUI software. This tab provides low-level control of each bit. For easier configuration, additional tabs provide high-level control. Section 2.3 provides configuration details.

When the evaluation board is not connected to a PC, the CS8422 is placed in hardware mode and is configured using DIP switches. Certain switch settings require a board reset to take affect, see Section 3.3 for more information.

1.5 CS8406 Digital Audio Transmitter

A complete description of the CS8406 transmitter and a discussion of the digital audio interface can be found in the CS8406 data sheet.

The CS8406 converts the output PCM data stream from the CS8422 into S/PDIF data that is output to the optical (J28) and RCA (J27) connectors. In software mode, device configuration pins are controlled by using the “FPGA Controls” tab of the Cirrus FlexGUI software, see Section 2.3 for details.

1.6 CS8422 XTI Sources

The CS8422 XTI clock source is selected by jumper J23. The clock signal may be provided by the socketed on-board canned oscillator (Y1), socketed on-board parallel resonant crystal (Y2), or input serial header J22. The oscillator and crystal are mounted in pin sockets, allowing for easy removal and replacement. The device footprint on the board for Y1 will only accommodate half-can-sized oscillators. Section 5 describes which jumper position selects each clock source.

1.7 I/O Stake Headers

The evaluation board has been designed to allow interfacing with external systems via several serial port headers and a control port header (J26). The input serial port header (J22) provides access to the input serial audio port of the CS8422. The output serial port headers provide access to both output serial audio port 1 (J24) and output serial audio port 2 (J25) of the CS8422. All three serial port headers can be placed in master or slave mode with respect to the CS8422. The TDM input header (J30) allows TDM data to be input from another system into the CS8422.

The control port header provides bidirectional access to the I²C or SPI control port signals by simply removing all the shunts from the “PC Control” position. The user may then connect a ribbon cable connector to the “External Connection” pins for external control of board functions. A single row of “GND” pins is provided to maintain signal ground integrity. Two unpopulated pull-up resistors are also available should the user choose to use the CDB8422 logic supply (VL) externally.

1.8 S/PDIF and AES3/EBU Inputs

The CDB8422 allows for both S/PDIF and AES3/EBU input signals to be connected to the CS8422. Four pairs of optical and RCA connectors are provided to connect single-ended S/PDIF signals to the four receiver ports on the CS8422. A single XLR connector is provided to connect a differential AES3/EBU signal to either of the two differential receiver ports on the CS8422.

Figure 16 illustrates how the S/PDIF and AES3/EBU inputs are connected and routed. Table 7 details the associated jumper selections. The CS8422 data sheet specifies the maximum allowed input voltage levels.

Note that, as a result of signal attenuation resulting from PCB parasitics, the input S/PDIF signal amplitude at the receiver input pins of the CS8422 may be lower than at the input connectors. See the CS8422 data sheet for the minimum signal amplitude required at the receiver input pins of the CS8422.

2. SOFTWARE MODE

Connecting a USB port cable from a PC to the USB connector (J37) on the CDB8422 and launching the provided graphical user interface (Cirrus Logic FlexGUI) software enables one to use the board in software mode. The GUI for the CDB8422 allows the user to configure the CS8422 and FPGA registers via the on-board I²C or SPI control bus.

2.1 Quick Start Guide

Figure 1 below is a simplified quick start up guide made for user convenience. The user may choose from steps 8 through 13 depending on the desired measurement. Refer to Section 2.2 for details on how the various components on the board interface with each other in different board configurations. Refer to Section 2.3 for descriptions on control settings in the Cirrus FlexGUI software.

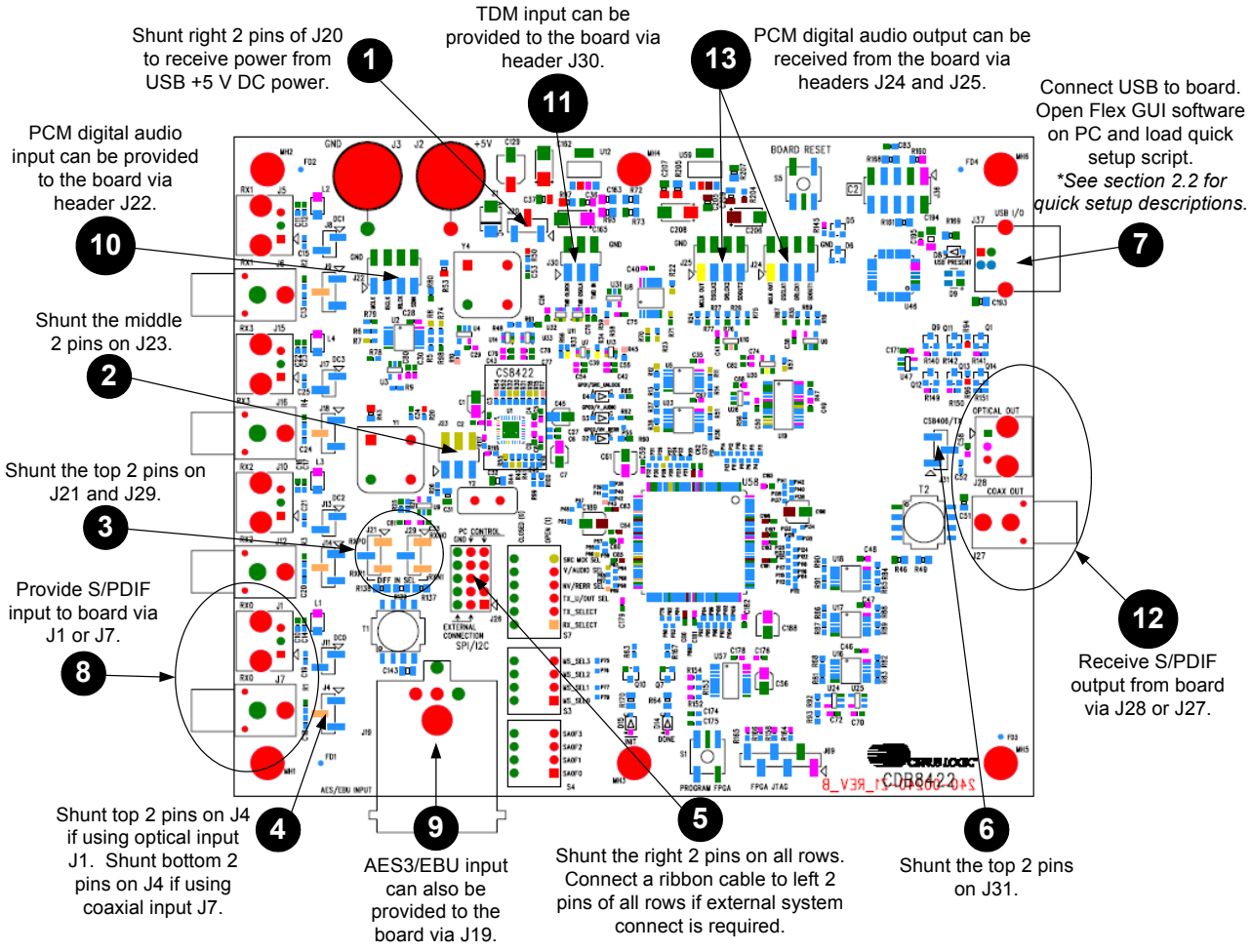


Figure 1. Software Mode Quick Start Guide

2.2 Configuration Options

In software mode, to configure the CDB8422 for making performance measurements, one needs to use Cirrus Logic's Windows compatible FlexGUI software to program the various components on the board. This section serves to give a deeper understanding of the on-board circuitry and the digital clock and data signal routing involved in several common software mode configurations of the CDB8422. These scripts only serve as a starting point; after loading a script, the GUI can be further configured as needed (clock ratios, serial formats, etc).

2.2.1 S/PDIF In to S/PDIF and PCM Out

The CS8422's S/PDIF receiver and SRC output performance can be tested by loading the **"SPDIF In to SPDIF and PCM Out"** quick setup file provided with the software package. The script configures the digital clock and data signal routing on the board as shown in Figure 2.

Digital S/PDIF input can be provided on the optical (J1) or RCA (J7) jacks. Jumper J4 selects which input signal is connected to the RX0 pin of the CS8422. The script configures the CS8422's internal circuitry to send the input audio data through its SRC to serial output port 1. This data is presented as PCM audio at header J24 and S/PDIF audio at J27 (coaxial) and J28 (optical). The input data is also passed through (SRC is bypassed) to serial output port 2. This data is presented as PCM audio at header J25. Refer to Section 2.3 for details on software configuration.

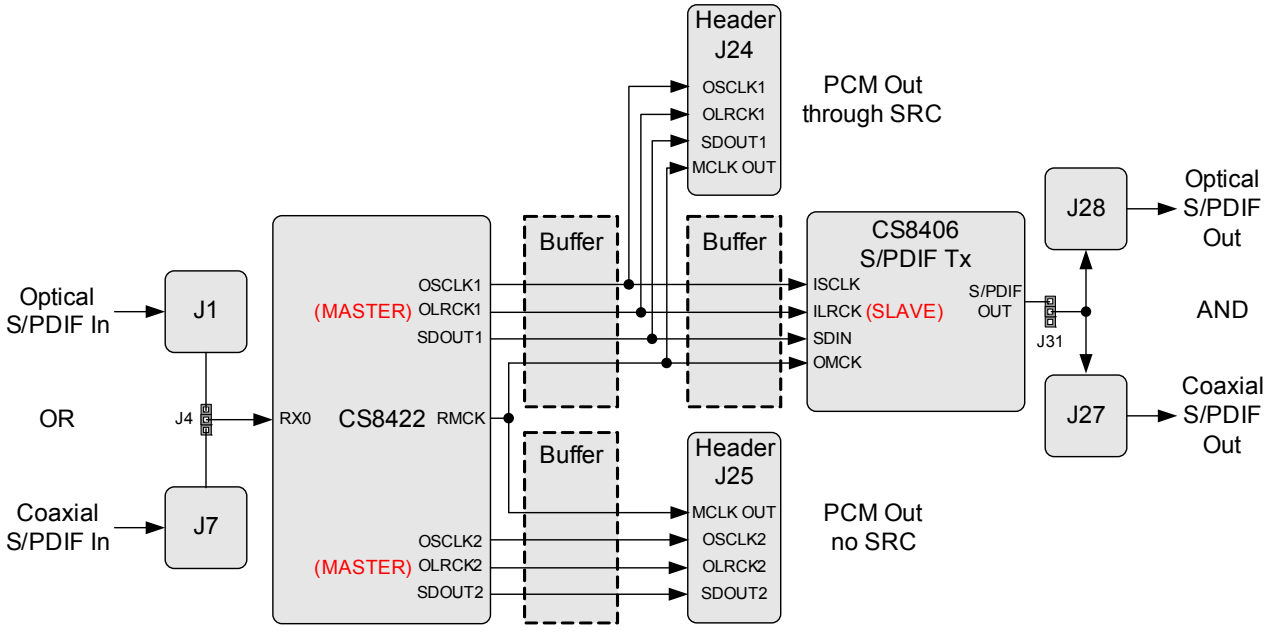


Figure 2. S/PDIF In to S/PDIF and PCM Out

2.2.2 AES3/EBU In to S/PDIF and PCM Out

The CS8422's AES3/EBU receiver and SRC output performance can be tested by loading the **"AES3 In to SPDIF and PCM Out"** quick setup file provided with the software package. The script configures the digital clock and data signal routing on the board as shown in Figure 3.

Digital AES3/EBU input is provided by the XLR jack J19 to the RXP0 and RXN0 pins of the CS8422. The script configures the CS8422's internal circuitry to send the input audio data through its SRC to serial output port 1. This data is presented as PCM audio at header J24 and S/PDIF audio at J27 (coaxial) and J28 (optical). The input data is also passed through (SRC is bypassed) to serial output port 2. This data is presented as PCM audio at header J25. Refer to Section 2.3 for details on software configuration.

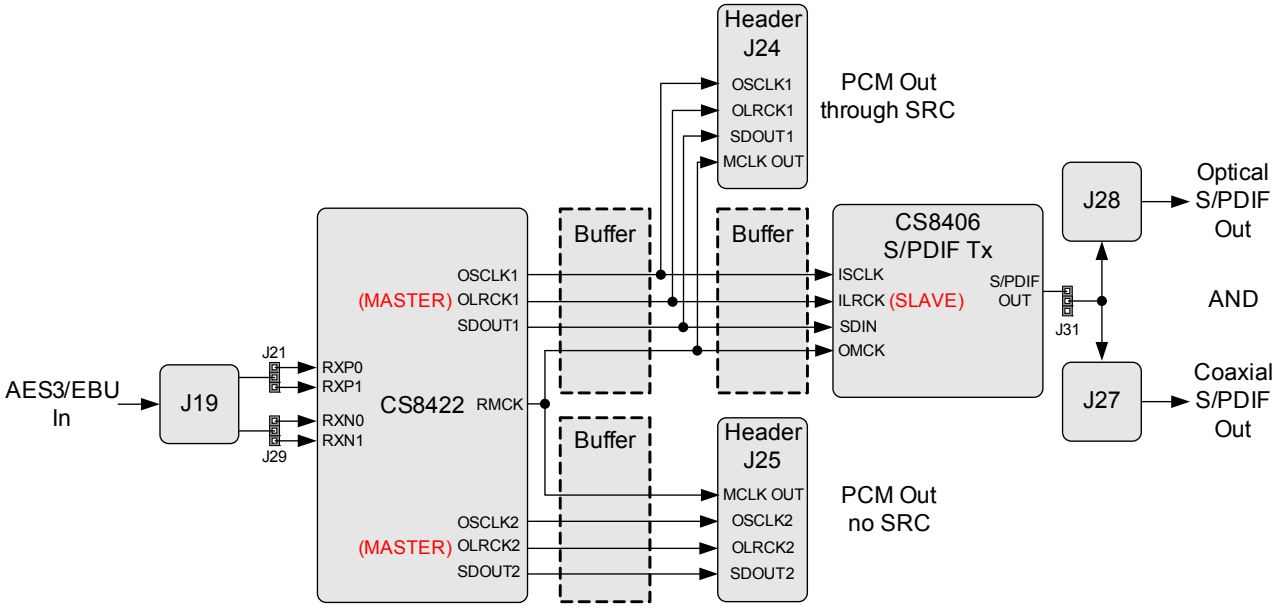


Figure 3. AES3/EBU In to S/PDIF and PCM Out

2.2.3 PCM In to S/PDIF and PCM Out

The CS8422's serial input port and SRC output performance can be tested by loading the **"PCM In to SPDIF and PCM Out"** quick setup file provided with the software package. The script configures the digital clock and data signal routing on the board as shown in Figure 4.

PCM audio input is provided by the PCM input header J22. The jumper position on J23 may be changed to use the MCLK signal from J22 for the CS8422's XTI signal. The script configures the CS8422's internal circuitry to send the input audio data through its SRC to serial output port 1. This data is presented as PCM audio at header J24 and S/PDIF audio at J27 (coaxial) and J28 (optical). The input data is also passed through (SRC is bypassed) to serial output port 2. This data is presented as PCM audio at header J25. Refer to Section 2.3 for details on software configuration.

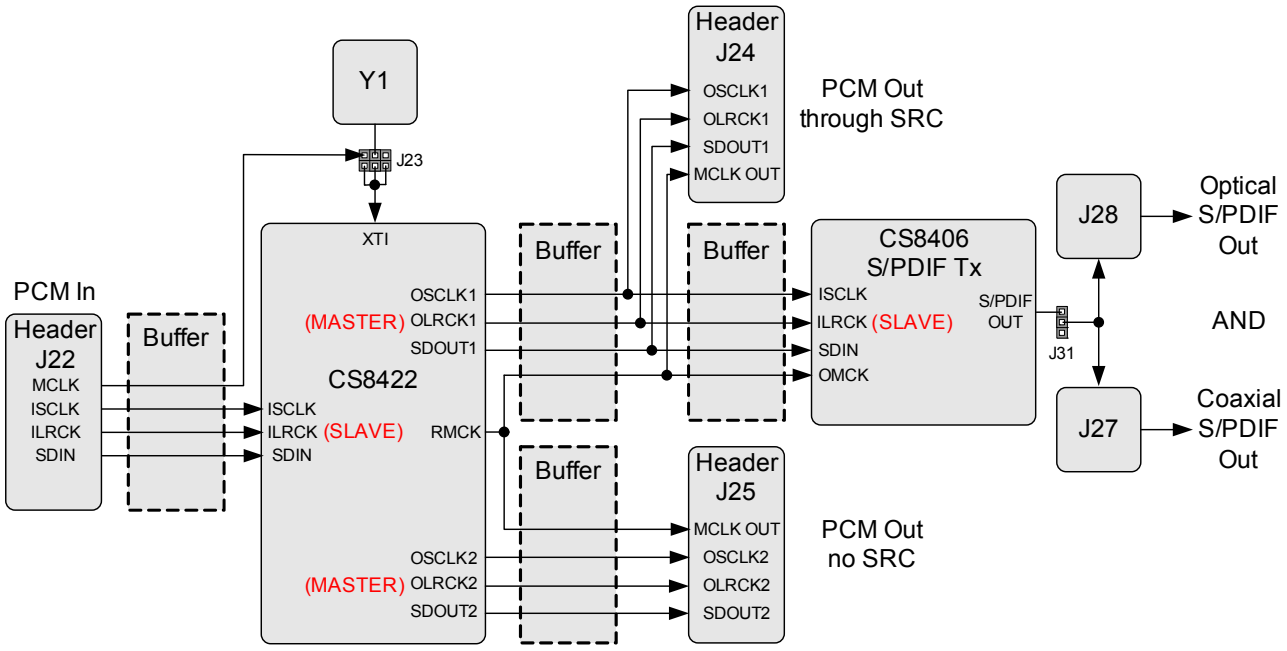


Figure 4. PCM In to S/PDIF and PCM Out

2.2.4 TDM In to TDM Out

The CS8422's TDM output performance can be tested by loading the **"TDM In to TDM Out"** quick setup file provided with the software package. The script configures the digital clock and data signal routing on the board as shown in Figure 5.

TDM audio input data is provided by the TDM input header J30. The LRCK and SCLK signals located at header J30 should be used to clock in the input TDM data. Optionally, digital S/PDIF input can be provided on the optical (J1) or RCA (J7) jacks. Jumper J4 selects which input signal is connected to the RX0 pin of the CS8422. The script configures the CS8422's internal circuitry to multiplex the TDM input and S/PDIF input data together and send the output data to serial output port 1. This data is presented as TDM audio at header J24. The S/PDIF input data is also passed through (not multiplexed) to serial output port 2. This data is presented as PCM audio at header J25. Refer to Section 2.3 for details on software configuration.

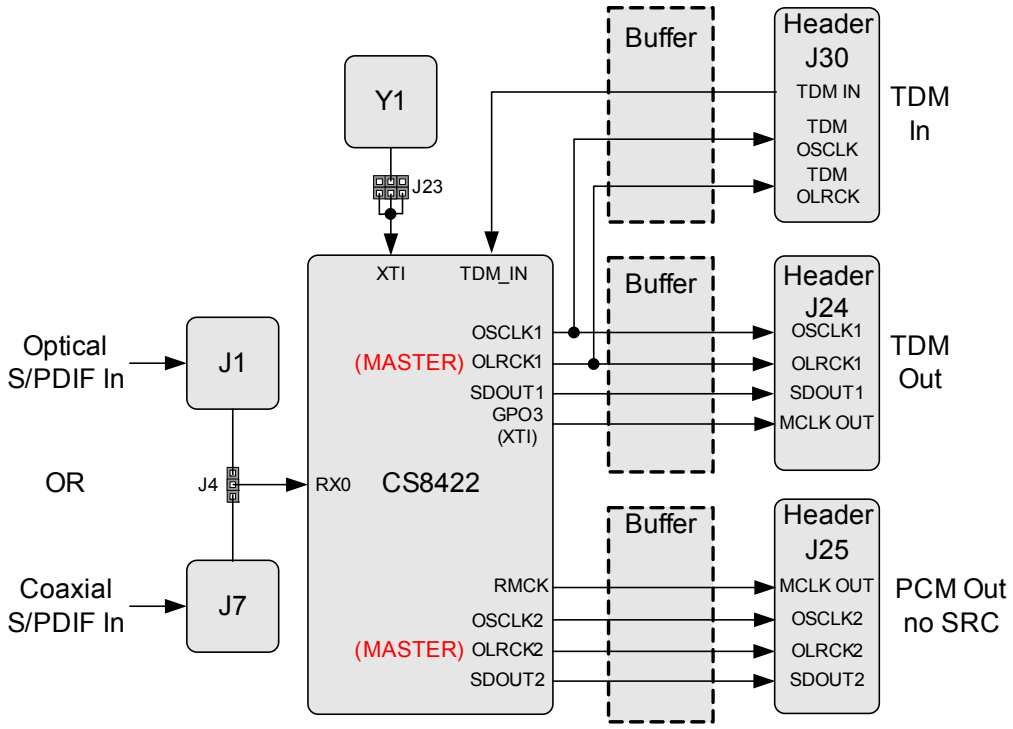


Figure 5. TDM In to TDM Out

2.3 Software Mode Control

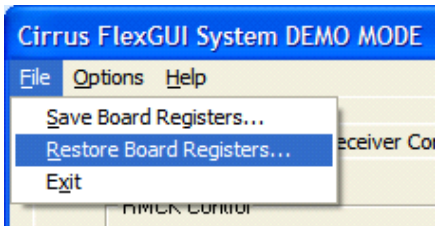
The CDB8422 may be used with the Microsoft® Windows®-based FlexGUI graphical user interface, allowing software control of the CS8422 and FPGA registers. The latest control software may be downloaded from www.cirrus.com/msasoftware. Step-by-step instructions for setting up the FlexGUI are provided as follows:

1. Download and install the FlexGUI software as instructed on the Website.
2. Connect the CDB to the host PC using a USB cable (make sure pin 1 and pin 2 of J20 are shunted).
3. Launch the Cirrus FlexGUI. *Once the GUI is launched successfully, all registers are set to their default reset state.*
4. Refresh the GUI by clicking on the “Update All Devices” button. *The default state of all registers are now visible.*

For standard set-up:

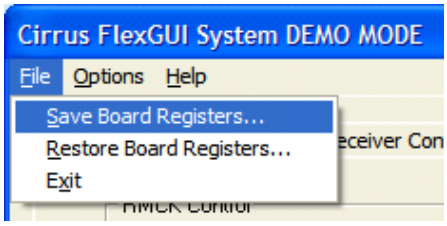
5. Set up the CS8422 in the “CS8422 Main Setup”, “CS8422 Receiver Controls and Status”, and “CS8422 Interrupt Controls and Status” tabs as desired.
6. Set up the FPGA and CS8406 in the “FPGA Controls” tab as desired.
7. Begin evaluating the CS8422.

For quick set-up, the CDB8422 may, alternatively, be configured by loading a predefined sample script file:



8. On the File menu, click "Restore Board Registers..."
9. Browse to Boards\CDB8422\Scripts\.
10. Choose any one of the provided scripts to begin evaluation.

To create personal scripts files:



11. On the File menu, click "Save Board Registers..."
12. Enter any name that sufficiently describes the created setup.
13. Choose the desired location and save the script.
14. To load this script, follow the instructions from step 8 above.

2.3.1 CS8422 Main Setup Tab

The “CS8422 Main Setup” tab provides high-level control of the serial port related registers within the CS8422. A description of each control group is outlined below. See the CS8422 data sheet for complete register descriptions.

RMCK Control - Configures the CS8422’s RMCK source and behavior.

SAI Control - Configures the serial audio input port of the CS8422.

SAO1 and SAO2 Control - Configures the two serial audio output ports of the CS8422.

SRC Control - Configures the CS8422’s sample rate converter (SRC).

GPO Control - Specifies the signals located on each of the four GPO pins of the CS8422.

TDM Control - Enables TDM Mode on either serial audio output port of the CS8422.

Quick Setup - Loads register settings for preset configurations of the CDB8422, see Section 2.2.

Miscellaneous Controls - Controls the power-down bit of CS8422, resets to return either the CS8422 or CDB8422 to default setup, and an update button to read all registers and reflect the current values in the GUI.

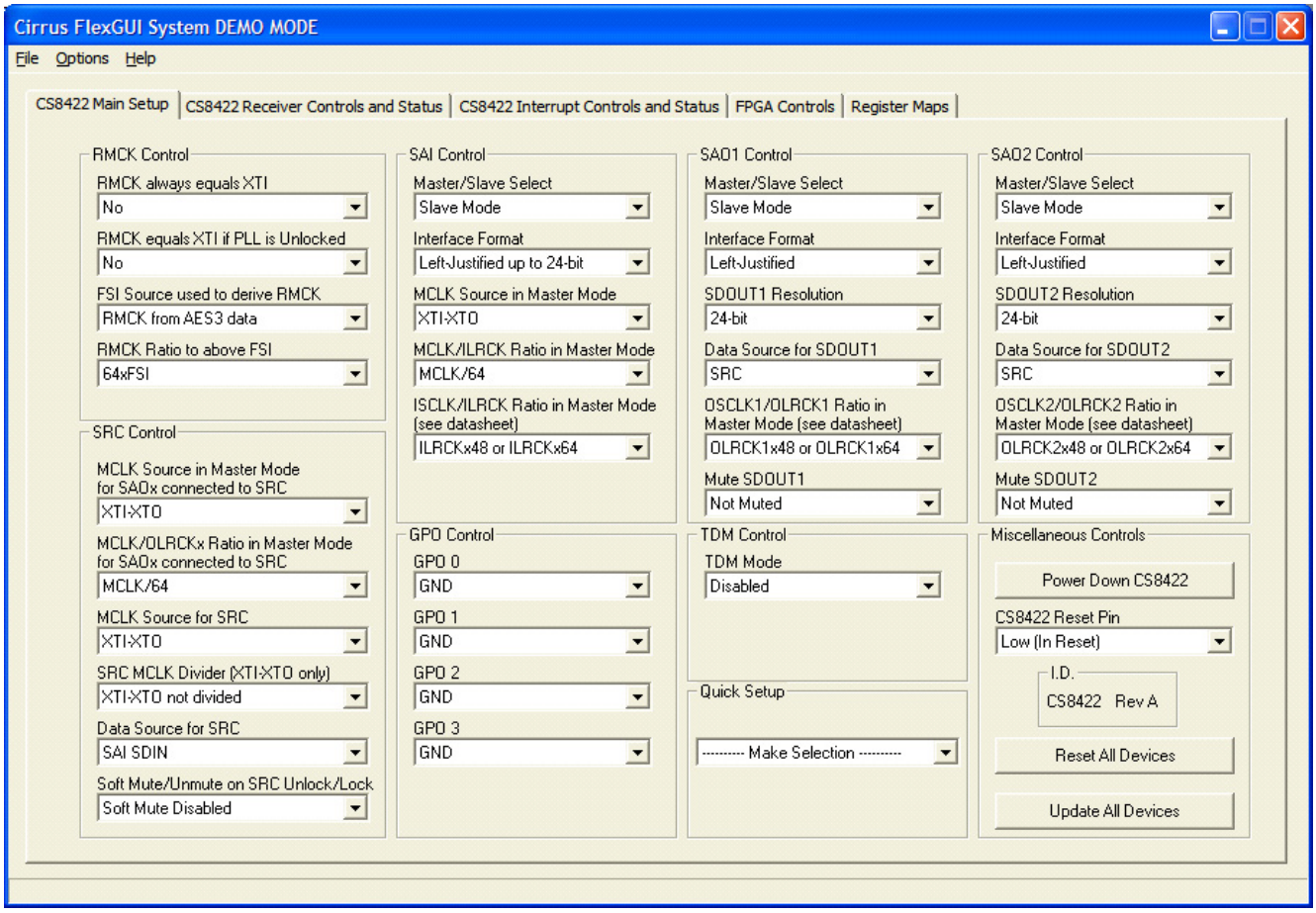


Figure 6. CS8422 Main Setup Tab

2.3.2 CS8422 Receiver Controls and Status Tab

The “CS8422 Receiver Controls and Status” tab provides high-level control of the CS8422’s S/PDIF receiver register settings. A description of each group is outlined below. See the CS8422 data sheet for complete register descriptions.

Receiver Input Control - Configures the CS8422’s receiver input pins and mux.

Receiver Data Control - Configures the CS8422’s receiver data processing.

Receiver Error Unmasking - Configures the CS8422’s receiver error unmasking.

Receiver Error - Shows the status for the CS8422’s unmasked receiver errors.

Receiver Channel Status - Shows the status bits for the CS8422’s selected receiver channel.

Receiver Status - Shows CS8422’s receiver errors occurring within last input data block.

Receiver Format Detect Status - Shows the data format detected on the CS8422’s receiver.

Update CS8422 - Reads all registers in the CS8422 and reflects the current values in the GUI.

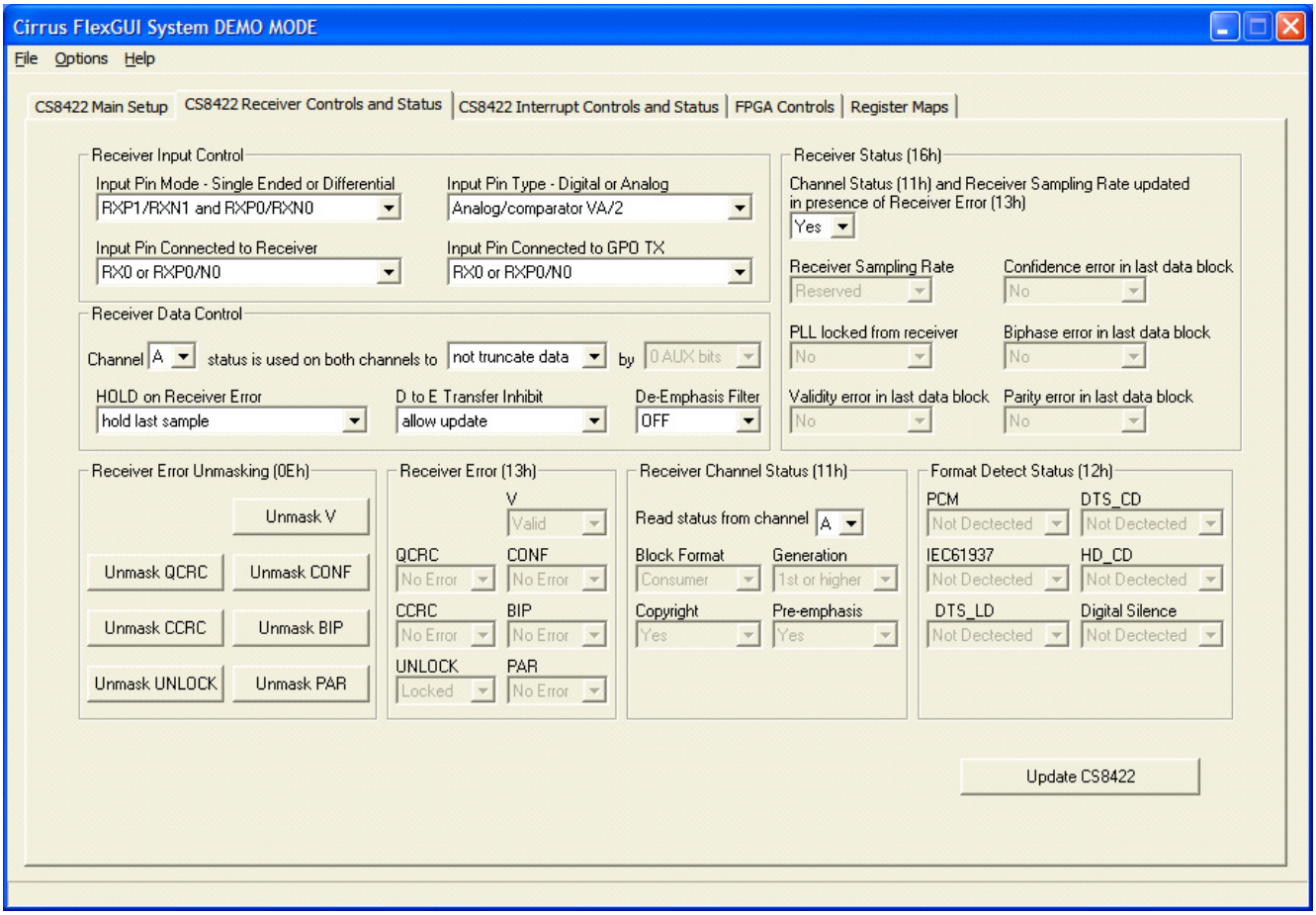


Figure 7. CS8422 Receiver Controls and Status Tab

2.3.3 CS8422 Interrupt Controls and Status Tab

The “CS8422 Interrupt Controls and Status” tab provides high-level control of the CS8422’s interrupt pin register settings. A description of each control group is outlined below. See the CS8422 data sheet for complete register descriptions.

INT Pin Control - Controls the CS8422’s INT pin polarity and modes.

Interrupt Error Unmasking - Controls the CS8422’s interrupt error unmasking to affect the INT pin.

Interrupt Status - Shows the status of CS8422’s unmasked interrupt errors.

Update CS8422 - Reads all registers in the CS8422 and reflects the current values in the GUI.

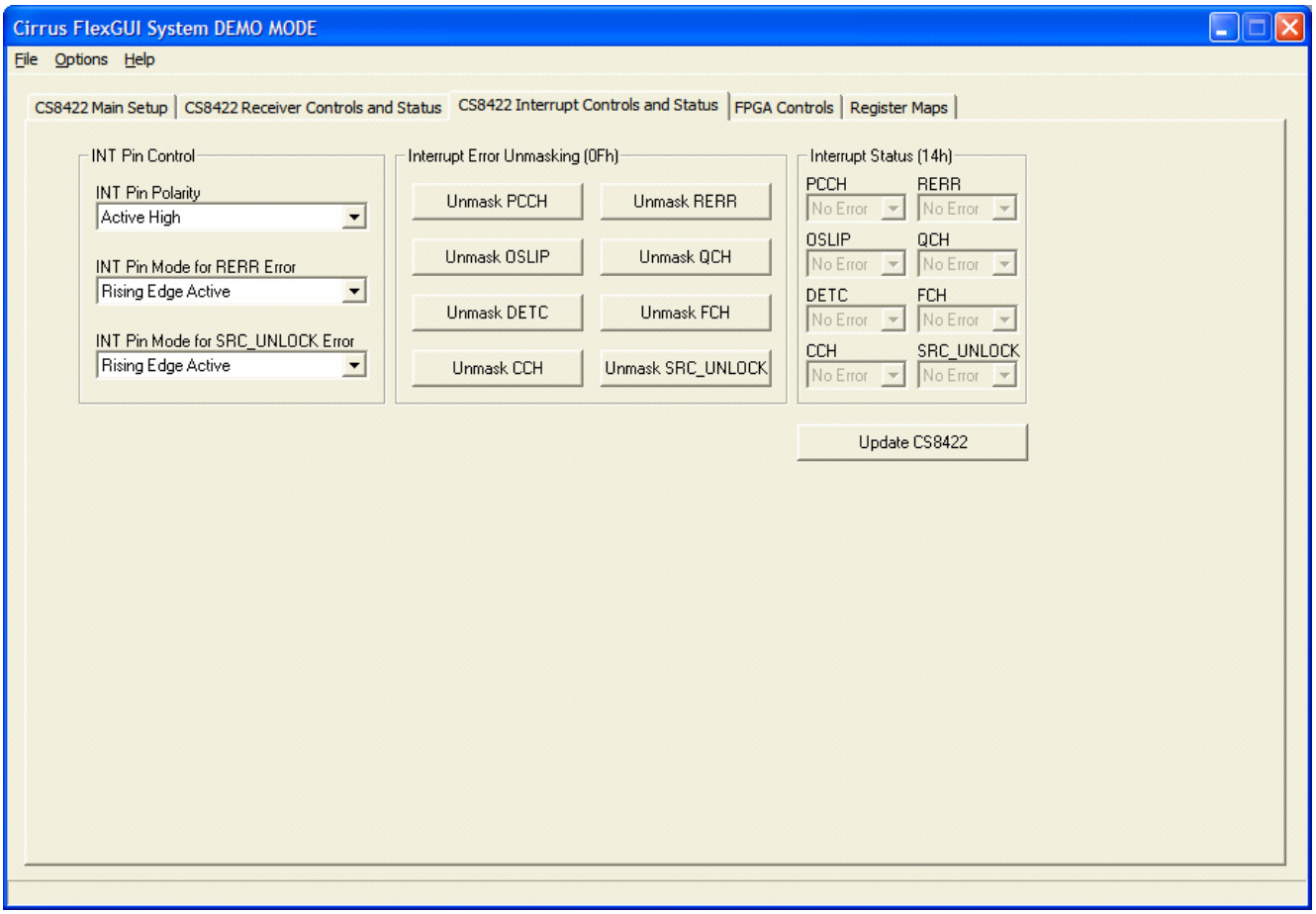


Figure 8. CS8422 Interrupt Controls and Status Tab

2.3.4 FPGA Controls Tab

The “FPGA Controls” tab provides high-level control of the on-board FPGA’s register settings. This tab provides controls for MCLK and subclock routing between devices on the CDB8422. Controls for the CS8406 S/PDIF transmitter are also provided. A description of each control group is outlined below.

MCLK Routing - Specifies MCLK source for both serial audio output port headers on the board.

Subclock Routing - Controls bidirectional buffers to determine subclock signal direction between the CS8422 and serial I/O interface headers. Make sure the CS8422 is also configured to properly output sub-clocks in master mode or receiver subclocks in slave mode for each serial port.

CS8422 Controls - The state of the CS8422 reset pin may be set.

CS8406 Controls - Controls CS8406 settings and reset pin state.

Reset FPGA - Returns the FPGA and CS8422 to their default setup.

Update FPGA - Reads all registers in the FPGA and reflects the current values in the GUI.

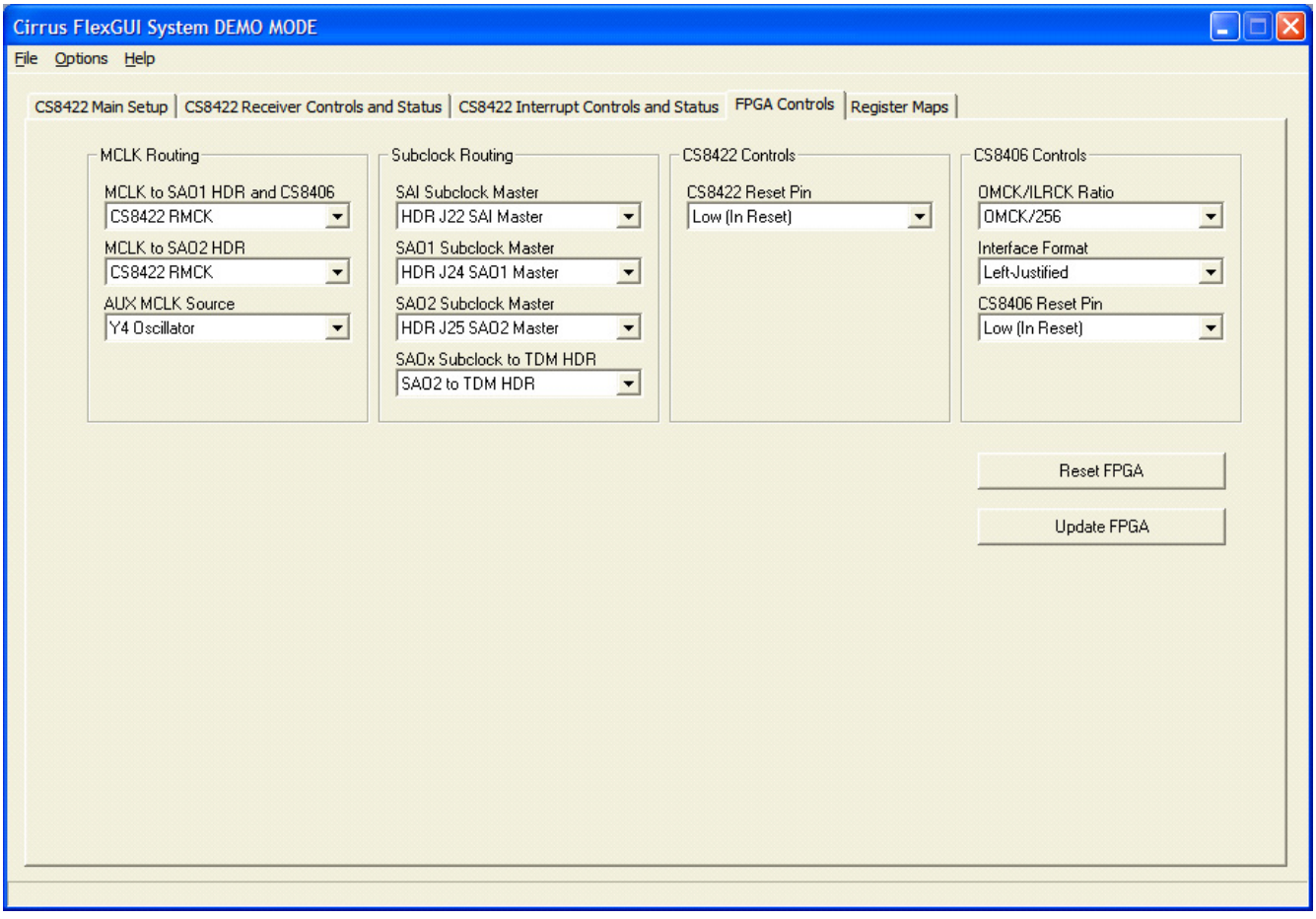


Figure 9. FPGA Controls Tab

2.3.5 Register Maps Tab

The Register Maps tabs provide low-level control of the CS8422, FPGA, and GPIO register settings. Register values can be modified bit-wise or byte-wise. “Left-clicking” on a particular register accesses that register and shows its contents at the bottom. The user can change the register contents by using the push-buttons, by selecting a particular bit and typing in the new bit value, or by selecting the register in the map and typing in a new hex value. The communication mode of the CS8422 (I²C or SPI) may be selected as well. See Section 2.5 for details on each register setting of the FPGA. If the CS8422’s configurable I²C address bits (AD1 or AD0) are modified in the GPIO tab, the FPGA and CS8422 will be reset. The CS8422’s AD2 bit is always set to zero (GPO2 has no pull-up resistor).

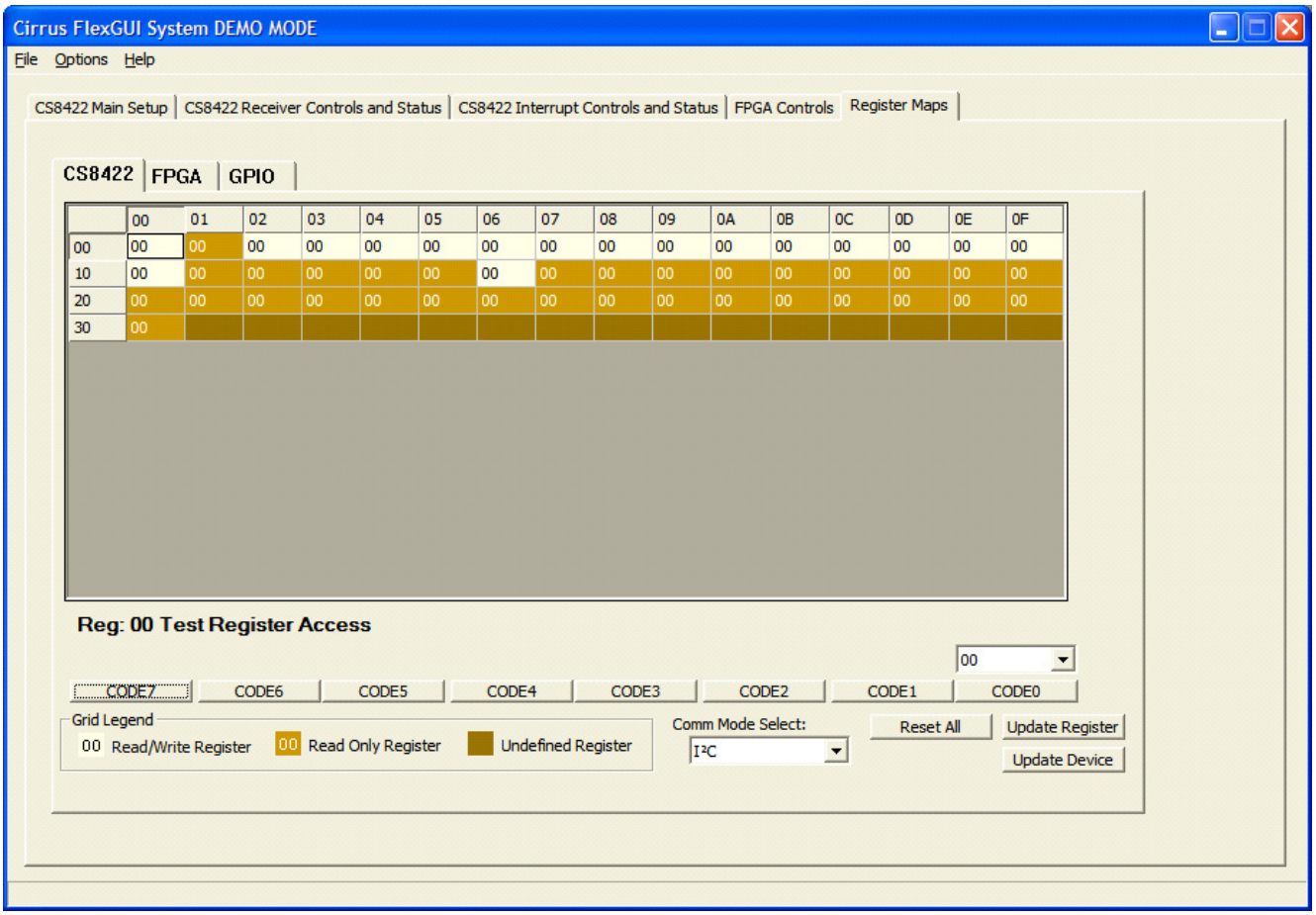


Figure 10. Register Maps Tab - CS8422

2.4 FPGA Register Quick Reference

This table shows the register names and their associated default values.

Adr	Name	7	6	5	4	3	2	1	0
01h	Rev_ID	RevID7	RevID6	RevID5	RevID4	RevID3	RevID2	RevID1	RevID0
	page 17	x	x	x	x	x	x	x	x
02h	Mclk_Ctl	Reserved	SAO2_Mclk	SAO1_Mclk	AUX_Mclk	Reserved	Reserved	Reserved	DUT_RST
	page 17	0	0	0	0	0	0	0	1
03h	Subclk_Ctl	TDM_SEL	Reserved	SAI_MS1	SAI_MS0	SAO2_MS1	SAO2_MS0	SAO1_MS1	SAO1_MS0
	page 18	0	0	0	0	0	0	0	0
04h	CS8406 Ctl 1	HWCK1	HWCK0	VBIT_IN	UBIT_IN	TCBL	CBIT_INT	SFMT1	SFMT0
	page 19	0	0	0	0	0	0	0	0
05h	CS8406 Ctl 2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	8406_RST	AUDIOb
	page 21	0	0	0	0	0	0	1	1

2.5 FPGA Register Descriptions

All registers are read/write unless otherwise stated. All “Reserved” bits must maintain their default state.

2.5.1 Code Revision ID (Address 01h) - Read Only

7	6	5	4	3	2	1	0
RevID7	RevID6	RevID5	RevID4	RevID3	RevID2	RevID1	RevID0

Function:
This register identifies the revision of the FPGA code. This register is read-only.

2.5.2 MCLK Control (Address 02h)

7	6	5	4	3	2	1	0
Reserved	SAO2_Mclk	SAO1_Mclk	AUX_Mclk	Reserved	HDR_AD1	HDR_AD0	DUT_RST

2.5.2.1 SAO2 HDR MCLK Source (SAO2_Mclk)

Default = 0

Function:
This bit controls the source of the MCLK signal sent to the SAO2 header J25. If the auxiliary source is used, see Section 2.5.2.3 for options.

SAO2_Mclk Setting	SAO2 HDR MCLK Source
0	CS8422 RMCK.
1	AUX MCLK.

2.5.2.2 SAO1 HDR and CS8406 MCLK Source (SAO1_Mclk)

Default = 0

Function:
This bit controls the source of the MCLK signal sent to the SAO1 header J24 and the CS8406’s OMCK pin. If the auxiliary source is used, see Section 2.5.2.3 for options.

SAO1_Mclk Setting	SAO1 HDR and CS8406 MCLK Source
0	CS8422 RMCK.
1	AUX MCLK.

2.5.2.3 AUX MCLK Source (AUX_Mclk)

Default = 0

Function:
This bit controls the source of the auxiliary MCLK signal. If the CS8422's GPO3 pin is selected, the GPO3 pin should be configured to output XTI_OUT (CS8422 register 06h = XFh).

AUX_Mclk Setting	AUX MCLK Source
0	Y4 Canned Oscillator.
1	CS8422 pin 30 (GPO3).

2.5.2.4 CS8422 Reset Pin (DUT_RST)

Default = 1

Function:
This bit controls the state of the CS8422's $\overline{\text{RST}}$ pin.

DUT_RST Setting	CS8422 Reset State
0	CS8422 in reset.
1	CS8422 out of reset.

2.5.3 Subclock Control (Address 03h)

7	6	5	4	3	2	1	0
TDM_SEL	Reserved	SAI_MS1	SAI_MS0	SAO2_MS1	SAO2_MS0	SAO1_MS1	SAO1_MS0

2.5.3.1 TDM Header Subclock Source (TDM_SEL)

Default = 0

Function:
This bit controls the source of the LRCK and SCLK signals sent to the TDM header J30.

TDM_SEL Setting	TDM HDR Subclock Source
0	CS8422 OLRCK2/OSCLK2.
1	CS8422 OLRCK1/OSCLK1.

2.5.3.2 SAI Subclock Source (SAI_MS)

Default = 00

Function:
These bits control the direction of the LRCK and SCLK signals between the SAI header J22 and the CS8422. The CS8422' SAI port should be configured in the appropriate master/slave mode.

SAI_MS Setting	SAI Subclock Source
00	HDR J22 drives CS8422's ILRCK and ISCLK inputs.
01	CS8422's ILRCK and ISCLK outputs drive HDR J22.
10	Reserved.
11	Reserved.

2.5.3.3 SAO2 Subclock Source (SAO2_MS)

Default = 00

Function:
These bits control the direction of the LRCK and SCLK signals between the SAO2 header J25 and the CS8422. The CS8422' SAO2 port should be configured in the appropriate master/slave mode.

SAO2_MS Setting	SAO2 Subclock Source
00	HDR J25 drives CS8422's OLRCK2 and OSCLK2 inputs.
01	CS8422's OLRCK2 and OSCLK2 outputs drive HDR J25.
10	Reserved.
11	Reserved.

2.5.3.4 SAO1 Subclock Source (SAO1_MS)

Default = 00

Function:
These bits control the direction of the LRCK and SCLK signals between the SAO1 header J24, the CS8422, and the CS8406. The CS8406 will automatically switch between master and slave modes. The CS8422's SAO1 port should be configured in the appropriate master/slave mode.

SAO1_MS Setting	SAO1 Subclock Source
00	HDR J24 drives CS8422's OLRCK1 and OSCLK1 inputs and CS8406's ILRCK and ISCLK inputs.
01	CS8406's ILRCK and ISCLK outputs drive HDR J24 and CS8422's OLRCK1 and OSCLK1 inputs.
10	CS8422's OLRCK1 and OSCLK1 outputs drive HDR J24 and CS8406's ILRCK and ISCLK inputs.
11	Reserved.

2.5.4 CS8406 Control 1 (Address 04h)

7	6	5	4	3	2	1	0
HWCK1	HWCK0	VBIT_IN	UBIT_IN	TCBL	CBIT_INT	SFMT1	SFMT0

2.5.4.1 OMCK/ILRCK Ratio (HWCK)

Default = 00

Function:
These bits control the ratio between the CS8406's OMCK and ILRCK signals.

HWCK Setting	OMCK/ILRCK Ratio
00	ILRCK = OMCK/256.
01	ILRCK = OMCK/128.
10	ILRCK = OMCK/512.
11	Reserved.

2.5.4.2 Validity Bit (VBIT_IN)

Default = 0

Function:
This bit controls the state of the validity bit for the CS8406's output S/PDIF data.

VBIT_IN Setting	Validity Polarity
0	Low.
1	High.

2.5.4.3 User Data (UBIT_IN)

Default = 0

Function:
This bit controls the state of the user data bit for the CS8406's output S/PDIF data.

UBIT_IN Setting	User Data Polarity
0	Low.
1	High.

2.5.4.4 TCBL (TCBL)

Default = 0

Function:
This bit controls the state of the CS8406's TCBL pin.

TCBL Setting	TCBL Polarity
0	Low.
1	High.

2.5.4.5 C BIT (CBIT_INT)

Default = 0

Function:
This bit controls the state of the C data bit for the CS8406's output S/PDIF data.

CBIT_INT Setting	C Bit Polarity
0	Low.
1	High.

2.5.4.6 Interface Format (SFMT)

Default = 00

Function:
These bits control the CS8406's input data interface format.

SFMT Setting	Interface Format
00	Left-Justified.
01	I^2S.
10	Right-Justified 24-bit.
11	Right-Justified 16-bit.

2.5.5 CS8406 Control 2 (Address 05h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	8406_RST	AUDIOb

2.5.5.1 CS8406 Reset Pin (8406_RST)

Default = 1

Function:
This bit controls the state of the CS8406's $\overline{\text{RST}}$ pin.

8406_RST Setting	CS8406 Reset State
0	CS8406 in reset.
1	CS8406 out of reset.

2.5.5.2 $\overline{\text{AUDIO}}$ Bit (AUDIOb)

Default = 1

Function:
This bit controls the state of the audio bit for the CS8406's output S/PDIF data.

AUDIOb Setting	$\overline{\text{AUDIO}}$ Polarity
0	Low.
1	High.

3. HARDWARE MODE

Powering up the CDB8422 without a USB connection to a PC operates the evaluation board in hardware mode. In this mode, on-board DIP switches allow the user to configure the CDB8422 without the use of a PC and GUI. However, only a subset of configuration options are available in hardware mode.

3.1 Quick Start Guide

Figure 11 below is a simplified quick start up guide made for user convenience. The user may choose from steps 7 through 10 depending on the desired measurement. Refer to Section 3.2 for details on how the various components on the board interface with each other in different board configurations. Refer to Section 3.3 for descriptions on hardware switches S3, S4, and S7 control settings.

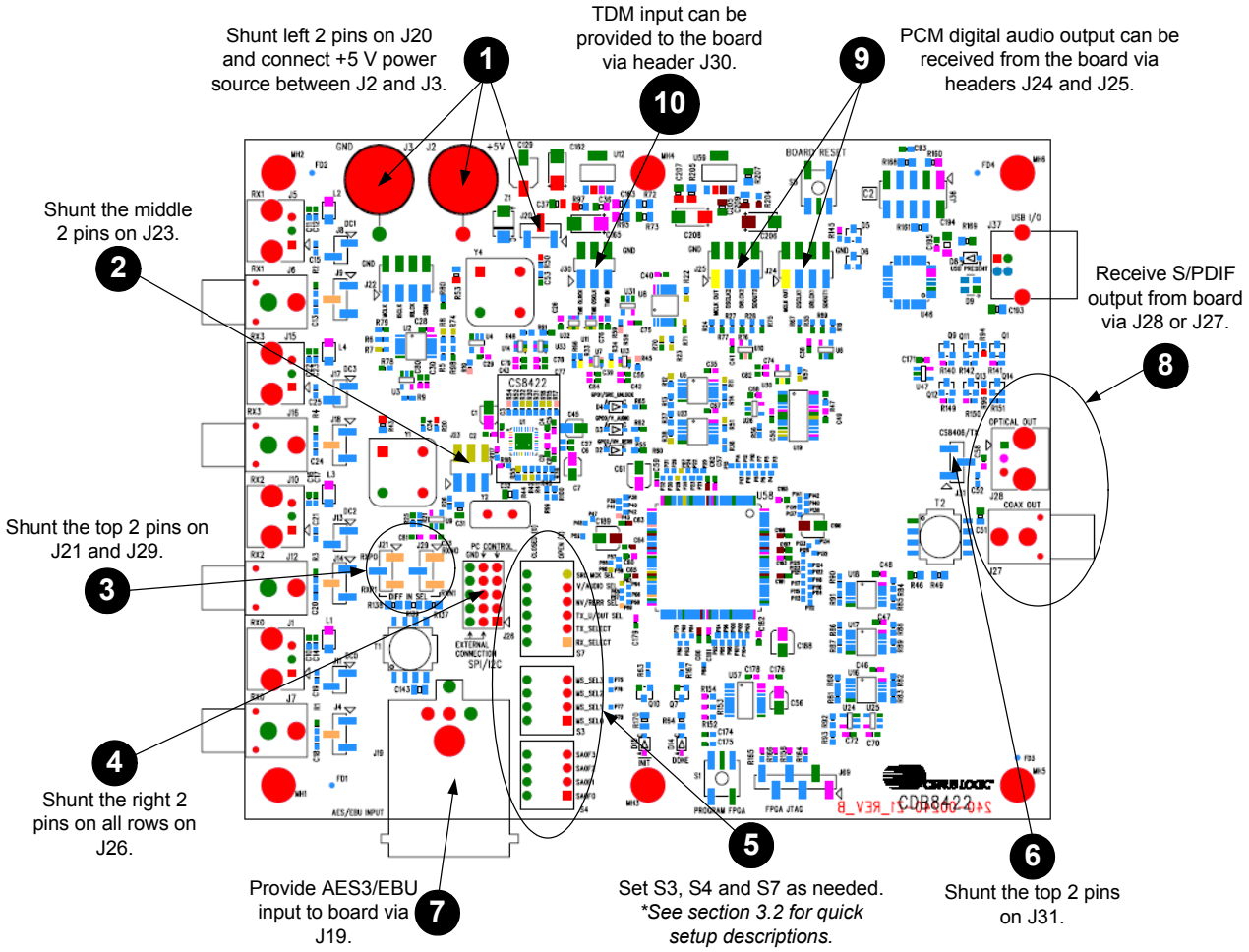


Figure 11. Hardware Mode Quick Start Guide

3.2 Configuration Options

In hardware mode, to configure the CDB8422 for making performance measurements, one needs to use the on-board control switches to set up the various components on the board. This section serves to give a deeper understanding of the on-board circuitry and the digital clock and data signal routing involved in two different hardware mode configurations of the CDB8422. These setups only serve as a starting point; the switches can be further configured as needed (clock ratios, serial formats, etc).

3.2.1 AES3/EBU In to S/PDIF and PCM Out

The CS8422's AES3/EBU receiver and SRC output performance can be tested by setting the hardware switches as shown in Table 1. This configures the digital clock and data signal routing on the board as shown in Figure 12.

Digital AES3/EBU input is provided by the XLR jack J19 to the RXP0 and RXN0 pins of the CS8422. The CS8422's internal circuitry is configured to send the input audio data through its SRC to serial output port 1. This data is presented as PCM audio at header J24 and S/PDIF audio at J27 (coaxial) and J28 (optical). The input data is also passed through (SRC is bypassed) to serial output port 2. This data is presented as PCM audio at header J25. Refer to Section 3.3 for full details on hardware configuration.

Switch	Position	Setting
S3	MS_SEL[3:0]	1010
S4	SAOF[3:0]	0011
S7	RX_SELECT	0
	TX_SELECT	0
	TX_U/OUT SEL	0
	NV/RERR SEL	0
	V/AUDIO SEL	0
	SRC MCK SEL	1

Table 1. Switch Settings - AES3/EBU In to S/PDIF and PCM Out

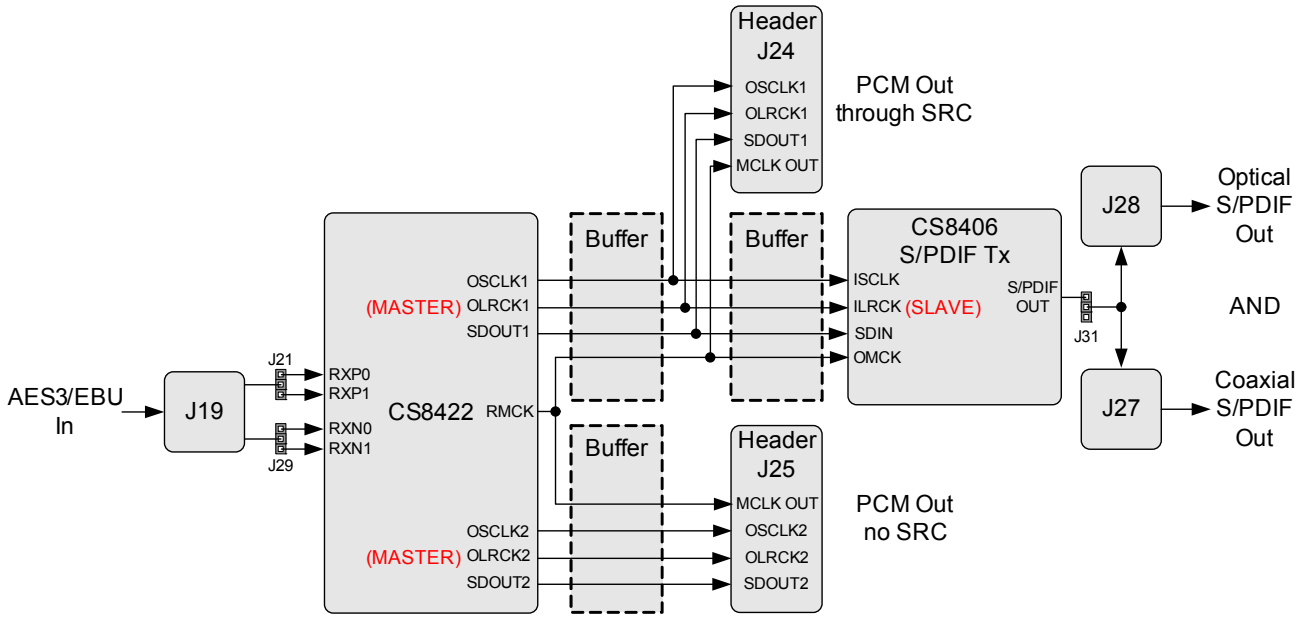


Figure 12. AES3/EBU In to S/PDIF and PCM Out

3.2.2 TDM In to TDM Out

The CS8422's TDM output performance can be tested by setting the hardware switches as shown in Table 2. This configures the digital clock and data signal routing on the board as shown in Figure 13.

TDM audio input data is provided by the TDM input header J30. The LRCK and SCLK signals located at header J30 should be used to clock in the input TDM data. Optionally, digital AES3/EBU input can be provided by the XLR jack J19 to the RXP0 and RXN0 pins of the CS8422. The CS8422's internal circuitry is configured to multiplex the TDM input and AES3/EBU input data together and send the output data to serial output port 1. This data is presented as TDM audio at header J24. The AES3/EBU input data is also passed through (not multiplexed) to serial output port 2. This data is presented as PCM audio at header J25. Refer to Section 3.3 for full details on hardware configuration.

Switch	Position	Setting
S3	MS_SEL[3:0]	1010
S4	SAOF[3:0]	1001
S7	RX_SELECT	0
	TX_SELECT	0
	TX_U/OUT SEL	0
	NV/RERR SEL	0
	V/AUDIO SEL	0
	SRC MCK SEL	0

Table 2. Switch Settings - TDM In to TDM Out

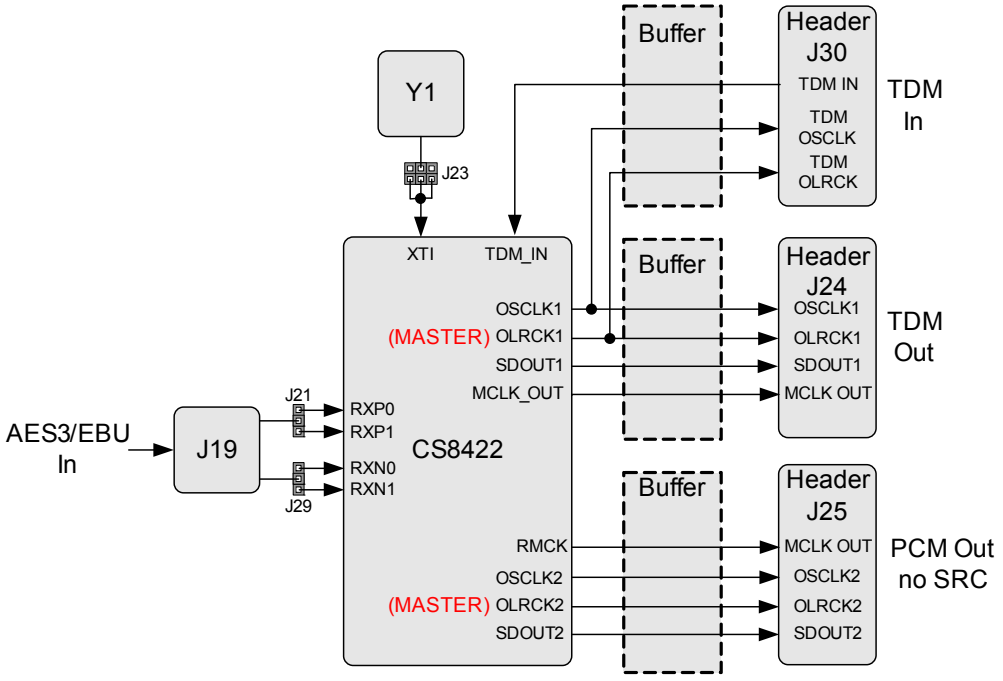


Figure 13. TDM In to TDM Out

3.3 Hardware Mode Control

This section provides a full description for the hardware mode control switches S3, S4, and S7, see the tables below. Switches S3 and S4 control the pull-up or pull-down resistor value attached to the MS_SEL and SAOF pins of the CS8422, respectively. Each resistor value is sensed during the power-up sequence to configure the device correctly. Consequently, for a modification to S3 or S4 to take affect, the CDB8422 should be reset by pressing push-button S5. For all switch positions, 0 = OPEN and 1 = CLOSED. See the CS8422 data sheet for complete details of hardware mode behavior.

Due to a limited number of switches, the following CS8422 hardware mode configuration settings are not changeable on the CDB8422: de-emphasis auto-detect is always enabled and the SRC MCLK is always the PLL clock.

Also, some FPGA register settings are fixed in hardware mode. The MCLK sent to the SAO2 header J25 is always the CS8422's RMCK, the TDM subclocks at header J30 are always from SAO1, and the CS8406's V, U, C, TCBL, and AUDIO pins are always low.

Switch S3 controls the master/slave and clock ratio options for both serial output ports, see Table 3 for switch configurations. For SDOUT1, when the serial port is set to master mode, the master clock ratio determines what the output sample rate will be based on the MCLK selected for SDOUT1 (chosen by position 6 on S7). For SDOUT2, the output sample rate is equal to the sample rate of the incoming receiver data, and the master mode clock ratio determines the frequency of RMCK relative to the incoming receiver sample rate.

MS_SEL[3:0]	SDOUT1	SDOUT2
0000	Slave Mode	Slave Mode, RMCK = 256*Fsi
0001	Master Mode, Fso = MCLK/128	
0010	Master Mode, Fso = MCLK/256	
0011	Master Mode, Fso = MCLK/512	
0100	Slave Mode	Master Mode, RMCK = 128*Fsi
0101	Master Mode, Fso = MCLK/128	
0110	Master Mode, Fso = MCLK/256	
0111	Master Mode, Fso = MCLK/512	
1000	Slave Mode	Master Mode, RMCK = 256*Fsi
1001	Master Mode, Fso = MCLK/128	
1010	Master Mode, Fso = MCLK/256	
1011	Master Mode, Fso = MCLK/512	
1100	Slave Mode	Master Mode, RMCK = 512*Fsi
1101	Master Mode, Fso = MCLK/128	
1110	Master Mode, Fso = MCLK/256	
1111	Master Mode, Fso = MCLK/512	

Table 3. S3 Settings

Note: If SDOUT1 is set to slave mode, the SAO1 header J24 will be the master (not the CS8406) and the CS8406's OMCK/ILRCK ratio will be set to 256xFs.

Note: If TDM Mode is selected for SDOUT1 by switch S4, then SDOUT1 cannot be set to "Master Mode, Fso = MCLK/128"

Switch S4 controls the data format options for both serial output ports, see Table 4 for switch configurations. For SDOUT2, the output resolution will be equal to the resolution of the incoming receiver data. The exception is the case where right-justified mode is selected and the receiver input word-length is an odd number of bits. In this case, the SDOUT2 word-length will be zero-stuffed to be 1 bit longer than the receiver input word-length (example: a 19-bit receiver input word will result in an 20-bit right-justified serial format).

SAOF[3:0]	SDOUT1	SDOUT2
0000	I²S 24-bit	I²S
0001	I²S 20-bit	
0010	I²S 16-bit	
0011	Left-Justified 24-bit	Left-Justified
0100	Left-Justified 20-bit	
0101	Left-Justified 16-bit	
0110	Right-Justified 24-bit (Master Mode only)	Right-Justified (Master Mode only)
0111	Right-Justified 20-bit (Master Mode only)	
1000	Right-Justified 16-bit (Master Mode only)	
1001	TDM Mode 24-bit	I²S
1010	TDM Mode 20-bit	
1011	TDM Mode 16-bit	
1100	Reserved	Reserved
1101		
1110		
1111		

Table 4. S4 Settings

Note: The CS8406 does not support Right-Justified 20-bit resolution in hardware mode.

Switch S7 controls the remaining options for the CS8422 in hardware mode, see Table 5 for switch configurations. The NV/RERR (CS8422 pin 9) and V/AUDIO (CS8422 pin 10) signals are provided at header J26 pins 5 and 2, respectively, and their states are indicated by LEDs D2 and D3. The TX/U (CS8422 pin 18) signal is provided at pin 1 of J31. If the transmitter pass-through option is selected for this signal, the data can be sent to the optical and coaxial output S/PDIF connectors by shunting the bottom two pins of J31.

POSITION	LABEL	PURPOSE	SETTING	FUNCTION SELECTED
1	RX_SELECT	Selects Active Receiver Input Pins	0	RXP0/RXN0 Selected
			1	RXP1/RXN1 Selected
2	TX_SELECT	Selects Receiver Input to be Output to Transmitter Pass-through	0	RXP0/RXN0 Selected
			1	RXP1/RXN1 Selected
3	TX_U/OUT SEL	Selects Transmitter Pass-through or U Data Output on Pin 18	0	Transmitter Pass-through Output
			1	Incoming U Data Output
4	NV/RERR SEL	Selects NV or RERR Output on Pin 9	0	NVERR Output
			1	RERR Output
5	V/AUDIO SEL	Selects Validity Data Output or AUDIO Indicator Output on Pin 10	0	Validity Data Output
			1	AUDIO Indicator Output
6	SRC MCK SEL	Selects MCLK Source for Serial Output Port 1	0	XTI - XTO Selected
			1	RMCK Selected

Table 5. S7 Settings

Note: Position 6 also selects either the CS8422's RMCK or MCLK_OUT signal to send to the SAO1 header J24 and the CS8406's OMCK pin.

4. SYSTEM CONNECTIONS

CONNECTOR	REF	INPUT/OUTPUT	SIGNAL PRESENT
+5V	J2	Input	+5 V Power Supply
GND	J3	Input	Ground Reference
USB I/O	J37	Input/Output	USB connection to PC for I²C or SPI control port signals
RX0 RX1 RX2 RX3	J1 J5 J10 J15	Input Input Input Input	CS8422 digital audio input via optical cable
RX0 RX1 RX2 RX3	J7 J6 J12 J16	Input Input Input Input	CS8422 digital audio input via coaxial cable
AES/EBU INPUT	J19	Input	CS8422 digital audio input via XLR cable
OPTICAL OUT	J28	Output	CS8406 digital audio output via optical cable
COAX OUT	J27	Output	CS8406 digital audio output via coaxial cable
Input Serial Port Header	J22	Input/Output	I/O for Clocks & Data to/from the CS8422's input serial port
Output Serial Port 1 Header	J24	Input/Output	I/O for Clocks & Data to/from the CS8422's output serial port 1
Output Serial Port 2 Header	J25	Input/Output	I/O for Clocks & Data to/from the CS8422's output serial port 2
TDM Input Header	J30	Input/Output	I/O for Clocks & Data to/from the CS8422's TDM input
SPI/I2C	J26	Input/Output	I/O for external I²C or SPI control port signals
C2	J36	Input/Output	I/O for programming the micro controller (U46)
FPGA JTAG	J69	Input/Output	I/O for programming the FPGA (U58)
BOARD RESET	S5	Input	Reset for the CDB8422
FPGA PROGRAM	S1	Input	Reload Xilinx program into the FPGA from Flash (U57)
MS SEL	S3	Input	Selects master/slave mode and clock ratio settings for the serial output ports of the CS8422 in hardware mode (see Section 3.3)
SAOF	S4	Input	Selects data format for the serial output ports of the CS8422 in hardware mode (see Section 3.3)
HW CONFIG	S7	Input	Misc. control of the CS8422 in hardware mode (see Section 3.3)

Table 6. System Connections

5. JUMPER SETTINGS

JMP	LABEL	PURPOSE	POSITION	FUNCTION SELECTED
J20	[No Label]	Selects voltage source for the CDB8422	1 - 2	Voltage source is USB connection (J37).
			*2 - 3	Voltage source is +5 V binding post (J2).
J11 J8 J13 J17	DC0 DC1 DC2 DC3	Bypasses optical S/PDIF input DC coupling capacitor	SHUNTED	0.01 µF series capacitor is shorted.
			*OPEN	0.01 µF series capacitor in optical input path.
J4 J9 J14 J18	[No Label]	Selects S/PDIF input source to receiver input pins of CS8422	*1 - 2	Optical S/PDIF input selected.
			2 - 3	Coaxial S/PDIF input selected.
J23	[No Label]	Selects XTI clock source for CS8422	1 - 2	Crystal Y2 selected.
			*3 - 4	Oscillator Y1 selected.
			5 - 6	MCLK from header J22 selected.
J31	CS8406/TX	Selects S/PDIF signal source for J27 and J28	1 - 2	GPO2 S/PDIF pass through from CS8422 selected.
			*2 - 3	CS8406 S/PDIF output selected.
J21 J29	DIFF IN SEL	Connects AES3/EBU signal from J19 to receiver input pins of CS8422	*RXP0/RXN0	RXP0/RXN0 input pair selected.
			RXP1/RXN1	RXP1/RXN1 input pair selected.

Table 7. Jumper Settings

Note: All settings denoted by an asterisk (*) are the Default Factory Settings.

Note: If a S/PDIF source is connected to the board, the AES3/EBU jumpers (J21 and J29) should be unpopulated to ensure proper operation. If an AES3/EBU source is connected to the board, the S/PDIF jumpers (J4, J9, J14, and J18) should be unpopulated to ensure proper operation.

6. LEDS

LED	LABEL	Hardware Mode	Software Mode
D2	GPO2/NV_RERR	NV/RERR (CS8422 pin 9)	GPO2 (CS8422 pin 18)
D3	GPO0/V_AUDIO	V/AUDIO (CS8422 pin 10)	GPO0 (CS8422 pin 16)
D4	GPO1/SRC_UNLOCK	SRC_UNLOCK (CS8422 pin 30)	GPO1 (CS8422 pin 17)
D8	USB PRESENT	USB power indicator	USB power indicator
D14	DONE	FPGA programming finished	FPGA programming finished
D15	INIT	FPGA programming initialized	FPGA programming initialized

Table 8. LEDs

7. CDB8422 BLOCK DIAGRAM

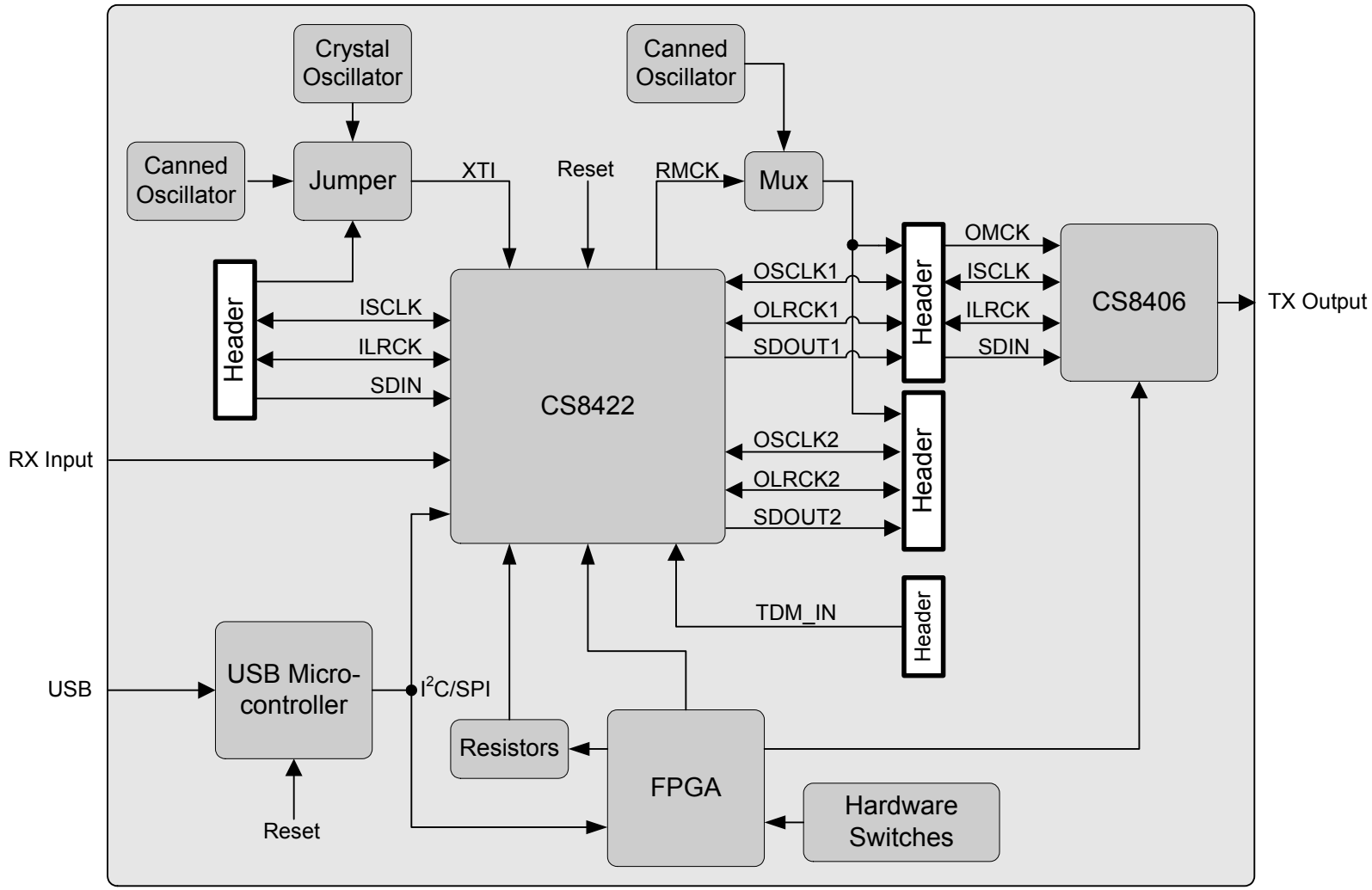
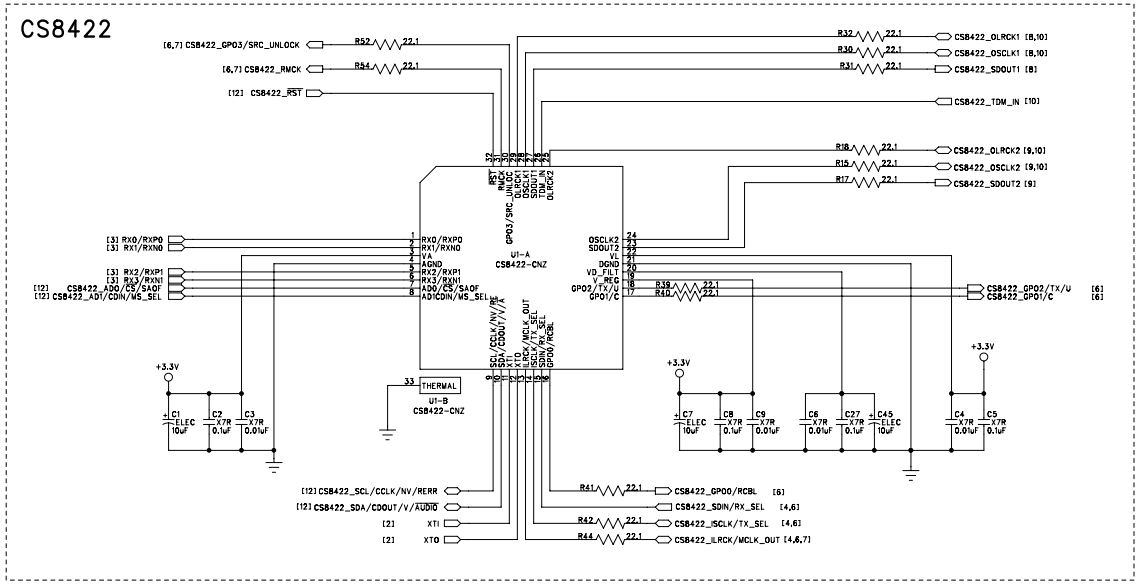


Figure 14. Block Diagram

8. CDB8422 SCHEMATICS



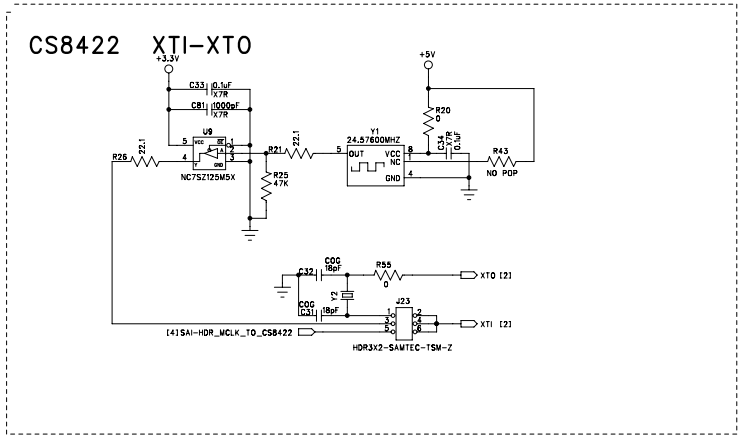


Figure 15. CS8422 & XTI (Schematic Sheet 1)

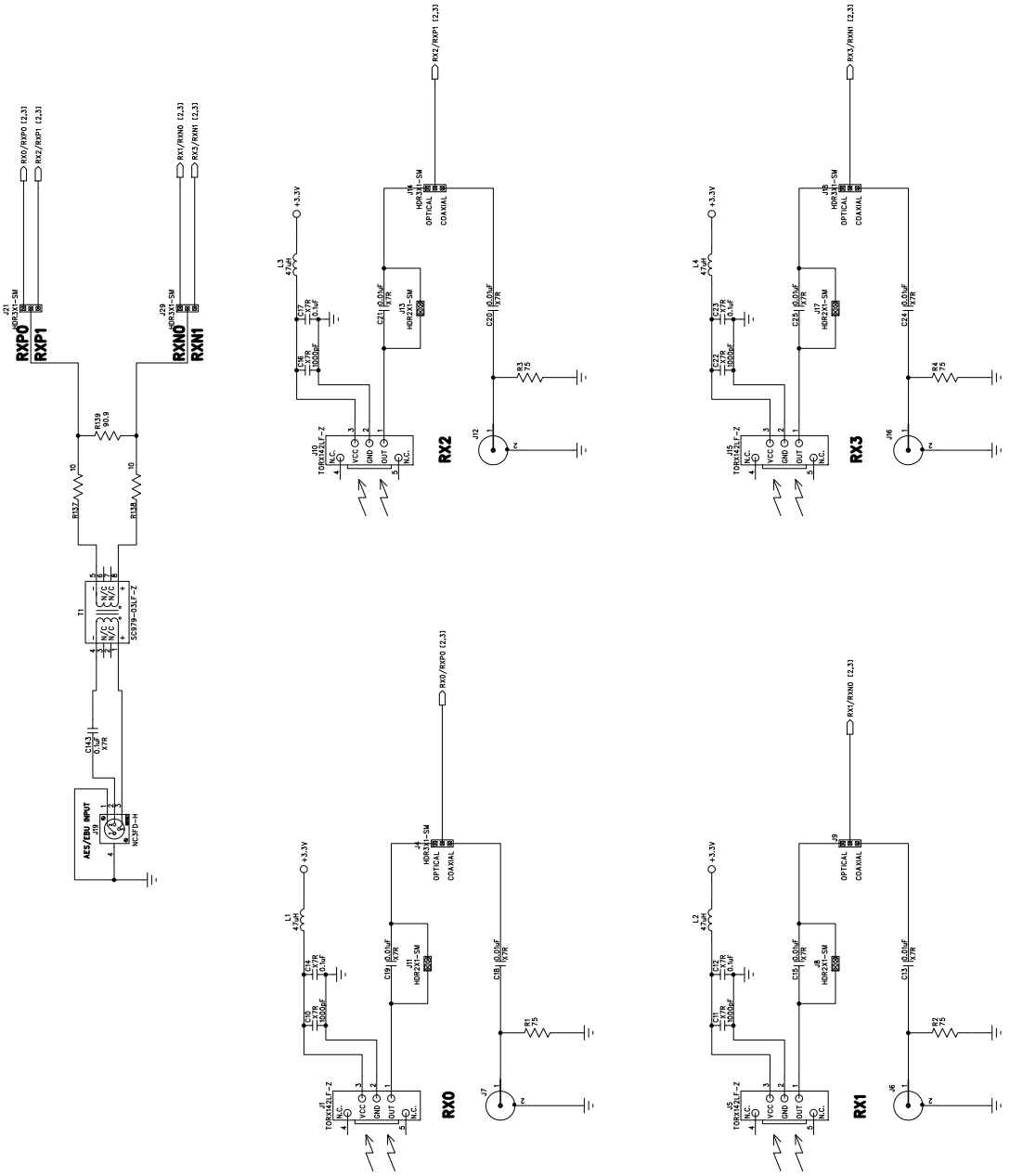


Figure 16. RX Inputs (Schematic Sheet 2)

*SERIAL AUDIO INPUT ONLY AVAILABLE IN SOFTWARE MODE

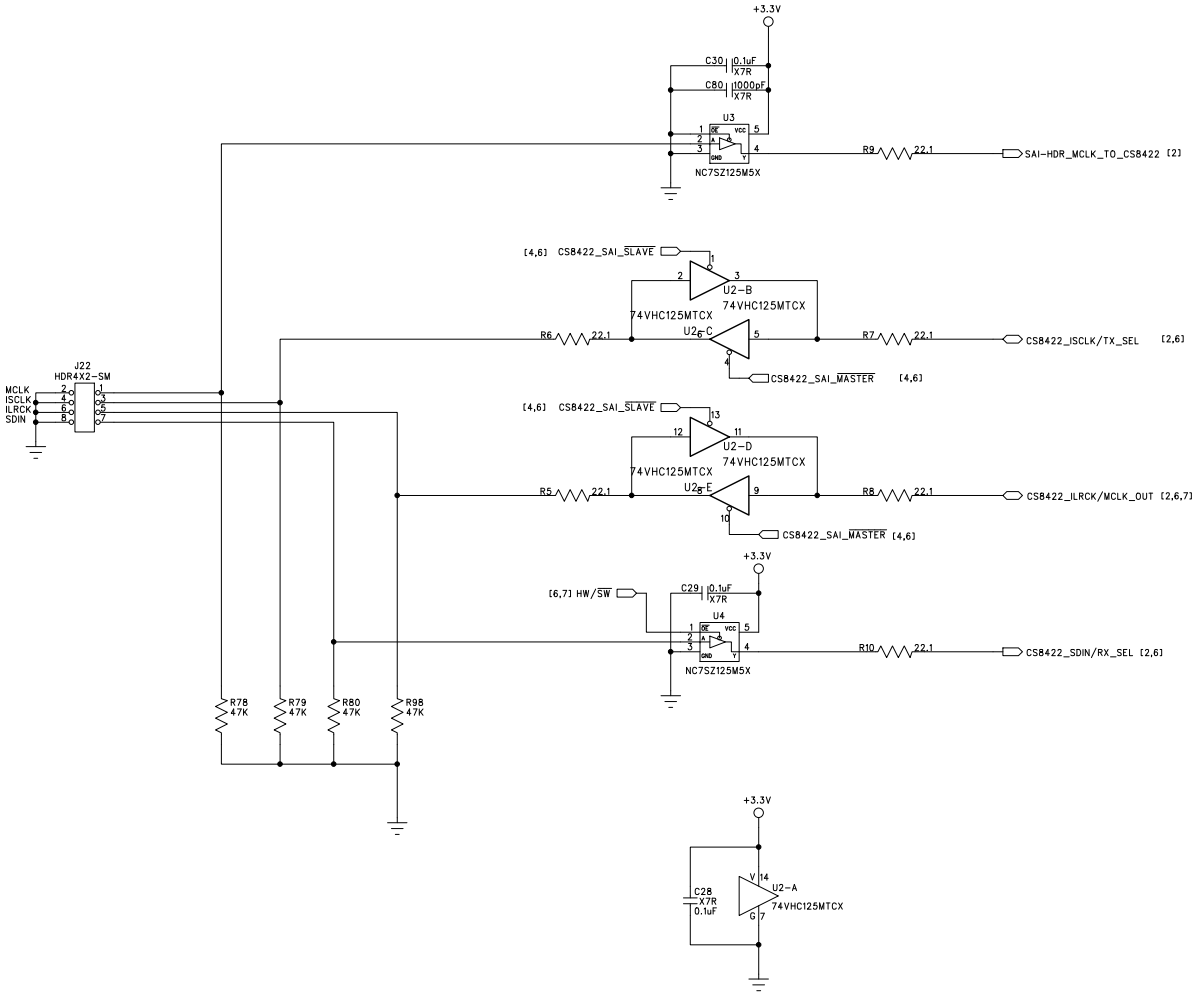
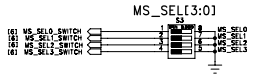
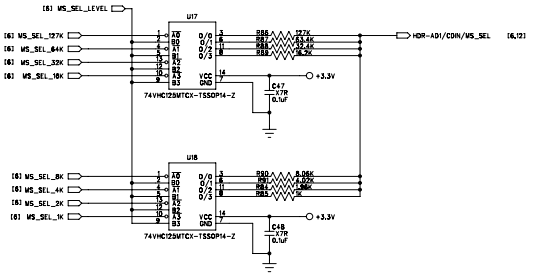


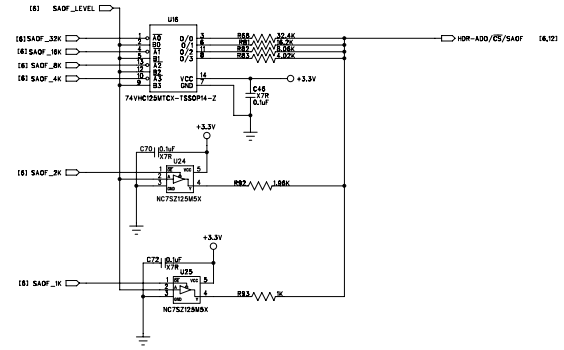
Figure 17. PCM Input Header (Schematic Sheet 3)

CS8422 Hardware Mode Master/Slave and Clock Ratio Selection (S3)

MS_SEL[3:0]	CS8422 SDOUT1	CS8422 SDOUT2
0000	Slave	Slave/RMCK=256xFsi
0001	Master (128*Fs)	
0010	Master (256*Fs)	
0011	Master (512*Fs)	
0100	Slave	Master/RMCK=128xFsi
0101	Master (128*Fs)	
0110	Master (256*Fs)	
0111	Master (512*Fs)	
1000	Slave	Master/RMCK=256xFsi
1001	Master (128*Fs)	
1010	Master (256*Fs)	
1011	Master (512*Fs)	
1100	Slave	Master/RMCK=512xFsi
1101	Master (128*Fs)	
1110	Master (256*Fs)	
1111	Master (512*Fs)	

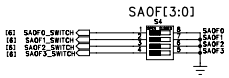






CS8422 Hardware Mode Serial Audio Output Format Select (S4)

SAOF[3:0]	SDOUT 1 Data Format	SDOUT 2 Data Format
0000	I2S 24-bit Data	I2S
0001	I2S 20-bit Data	
0010	I2S 16-bit Data	
0011	Left Justified 24-bit Data	Left Justified
0100	Left Justified 20-bit Data	
0101	Left Justified 16-bit Data	
0110	Right Justified 24-bit Data	Right Justified
0111	Right Justified 20-bit Data	
1000	Right Justified 16-bit Data	
1001	TDM Mode 24-bit Data	I2S
1010	TDM Mode 20-bit Data	
1011	TDM Mode 16-bit Data	
ALL OTHER POSITIONS RESERVED		



CS8422 Hardware Mode Misc. Control (S7)

SW	Description	Open	Closed
1	RX Select	RXP/N1	RXP/N0
2	TX Select	RXP/N1	RXP/N0
3	TX/U Output Select	U OUT	TX OUT
4	NV/RERR Select	RERR	NVERR
5	V/$\overline{\text{AUDIO}}$ Select	$\overline{\text{AUDIO}}$	V
6	SRC MCLK Select	RMCK	XTI-XTO

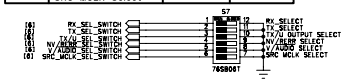


Figure 18. HW Mode Control (Schematic Sheet 4)

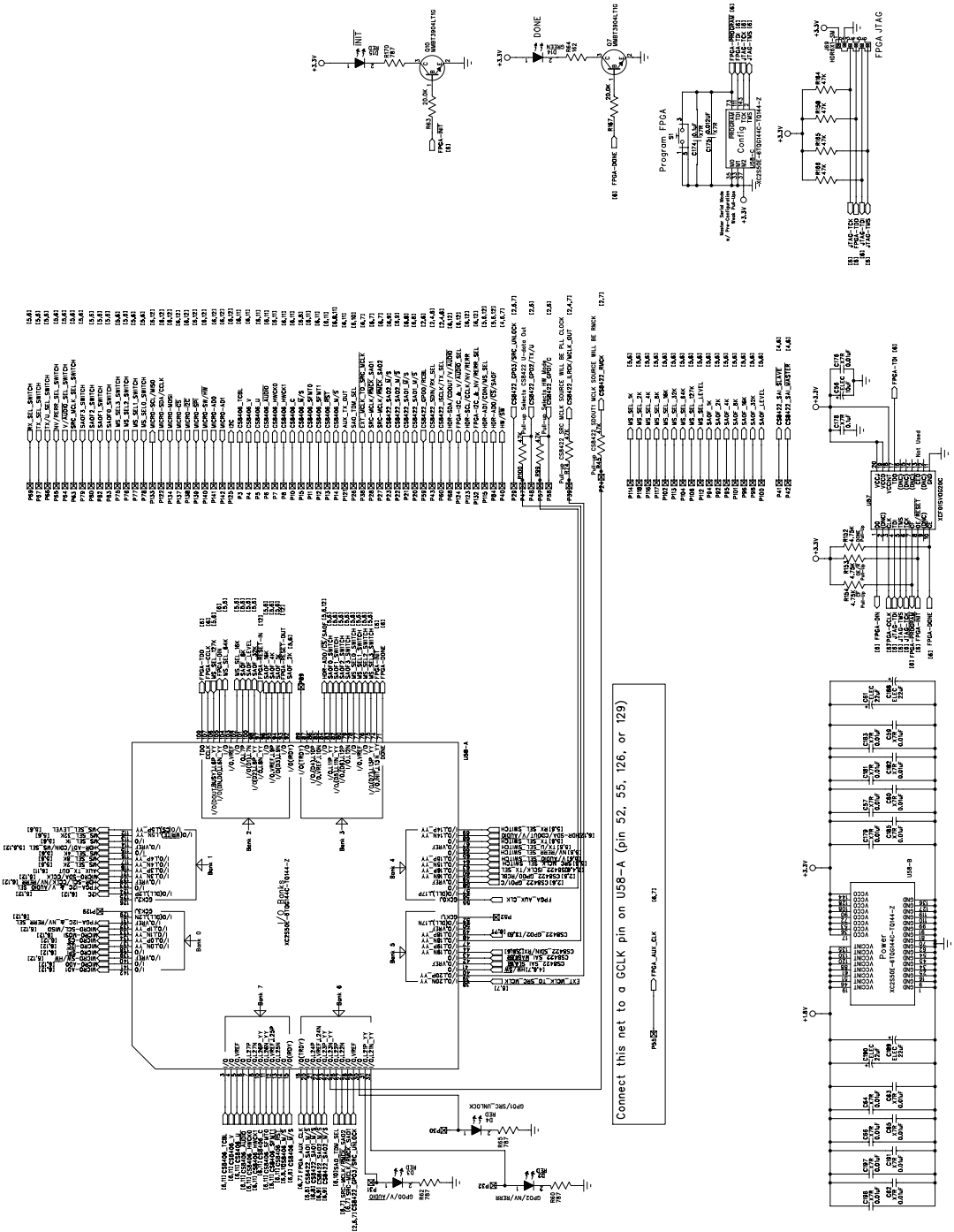
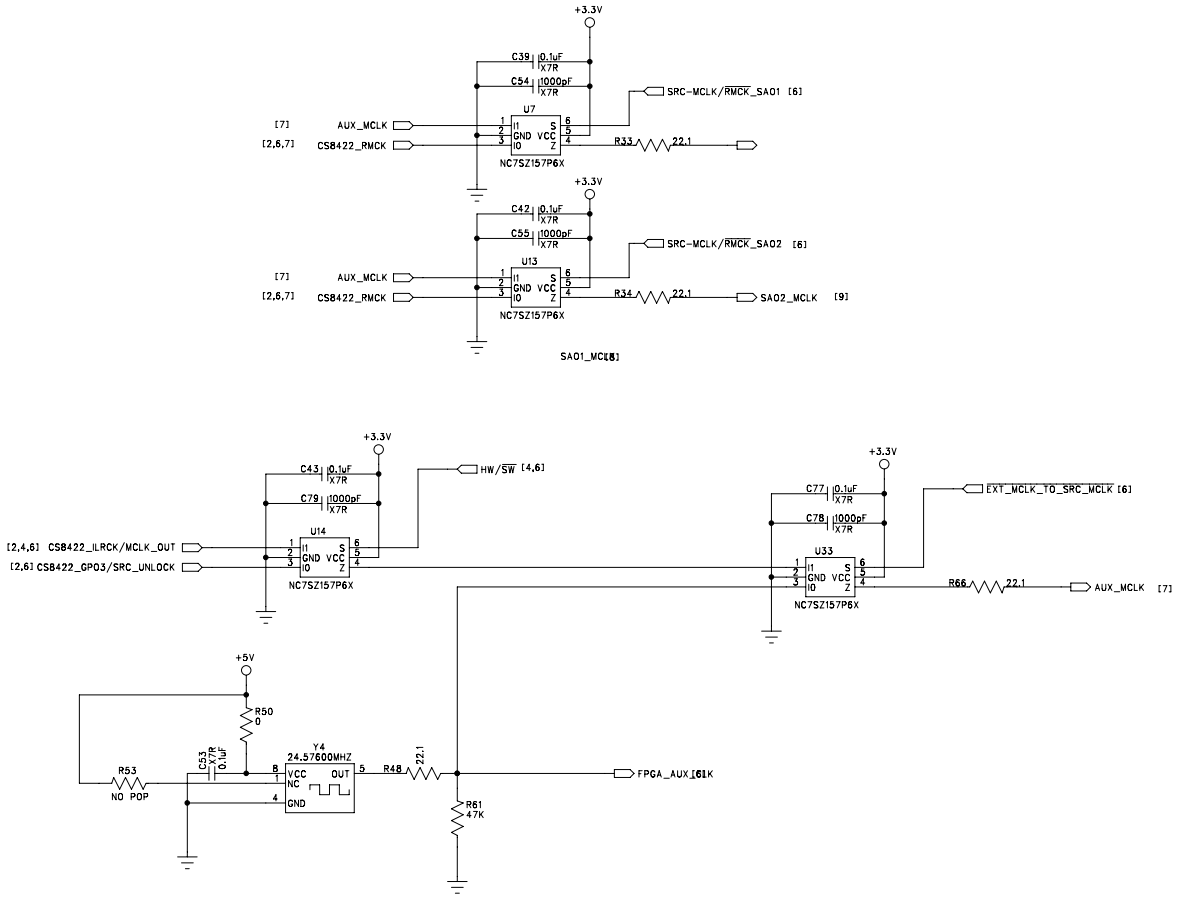


Figure 19. FPGA (Schematic Sheet 5)



GPO3 function should be set to "XTI – XTO" for use as MCLK source

Figure 20. MCLK Routing (Schematic Sheet 6)

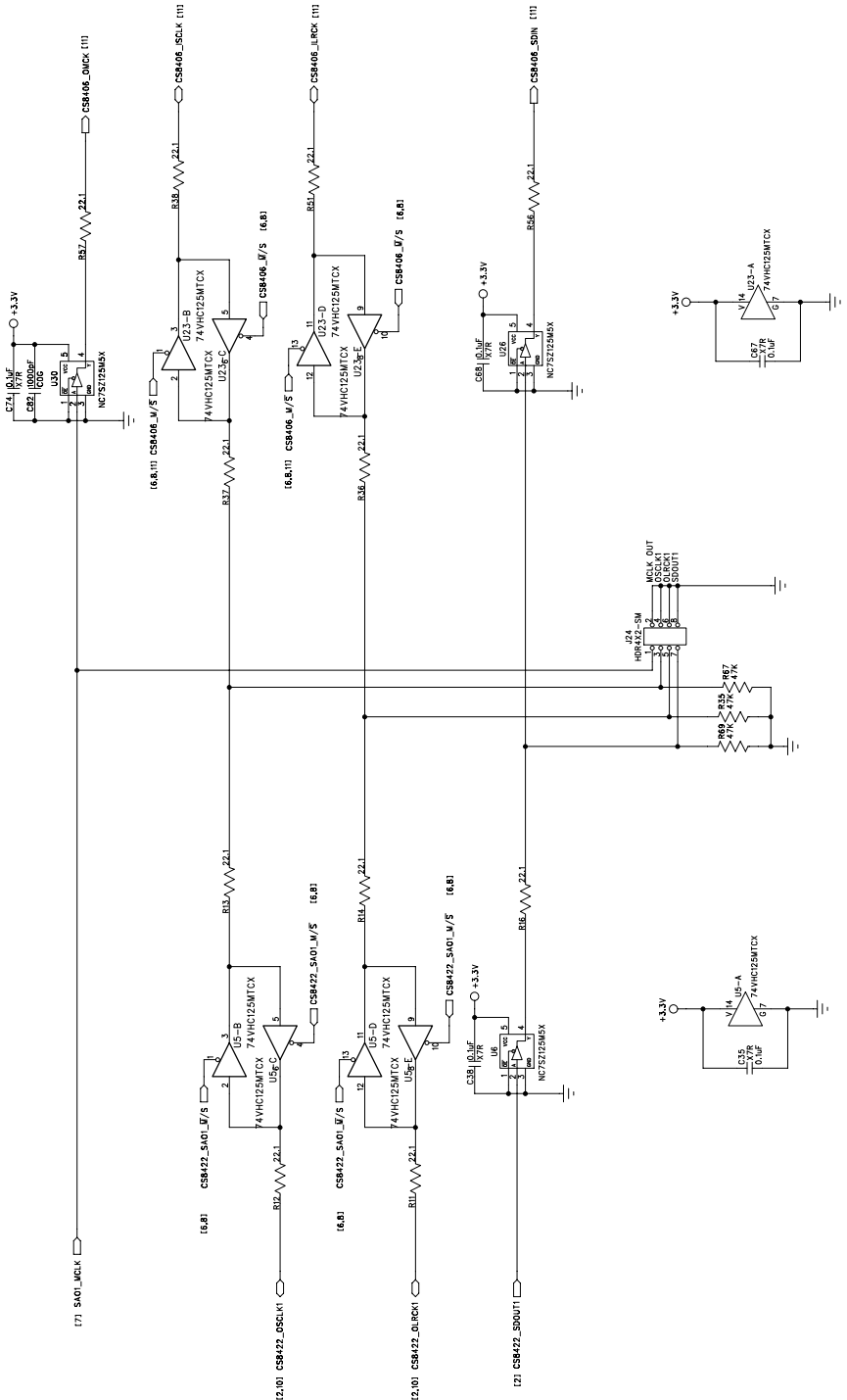


Figure 21. Serial Audio 1 Output Header (Schematic Sheet 7)

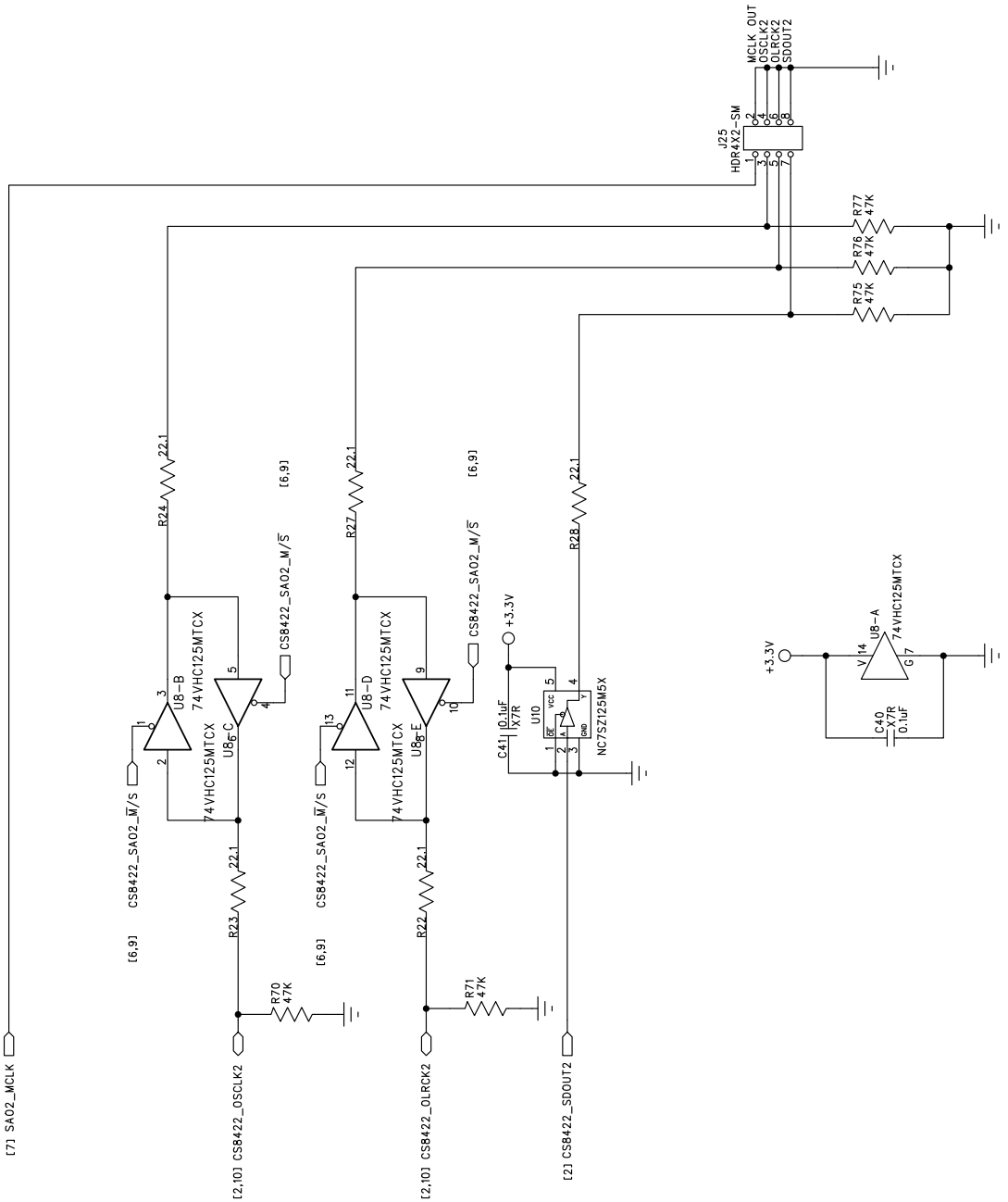


Figure 22. Serial Audio 2 Output Header (Schematic Sheet 8)

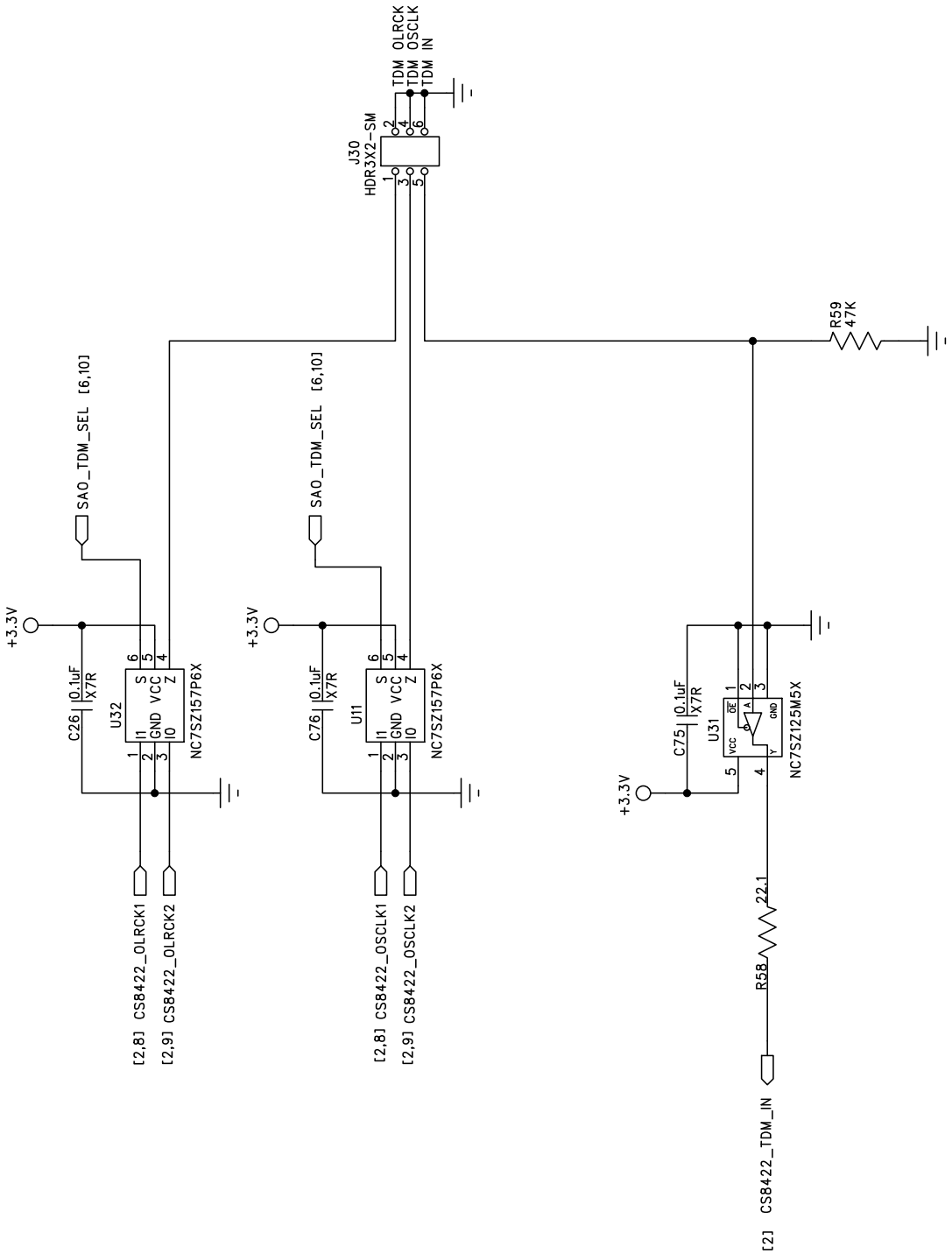


Figure 23. TDM Header (Schematic Sheet 9)

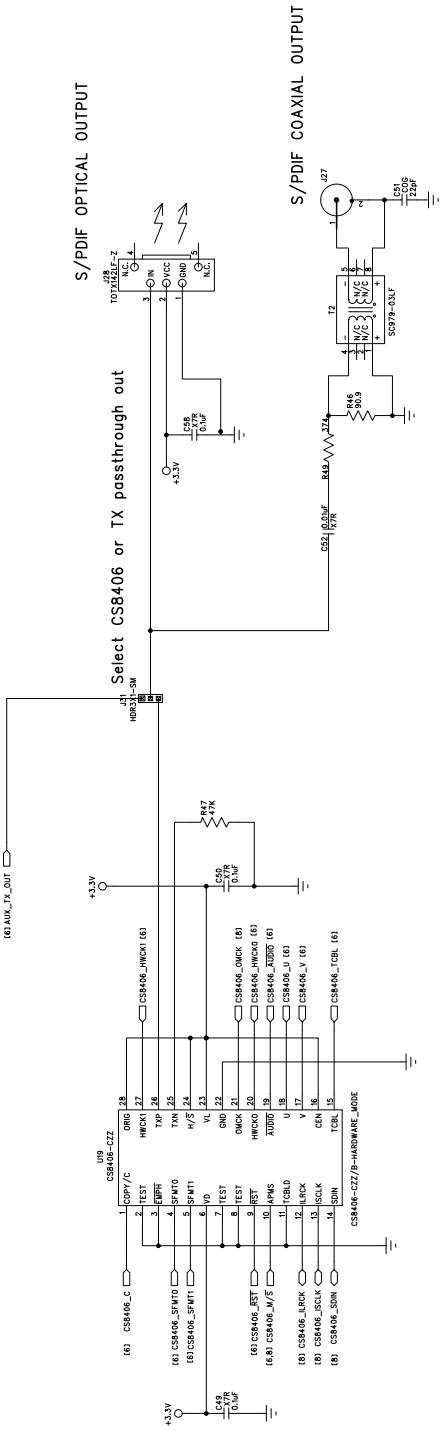


Figure 24. CS8406 and Auxiliary TX (Schematic Sheet 10)

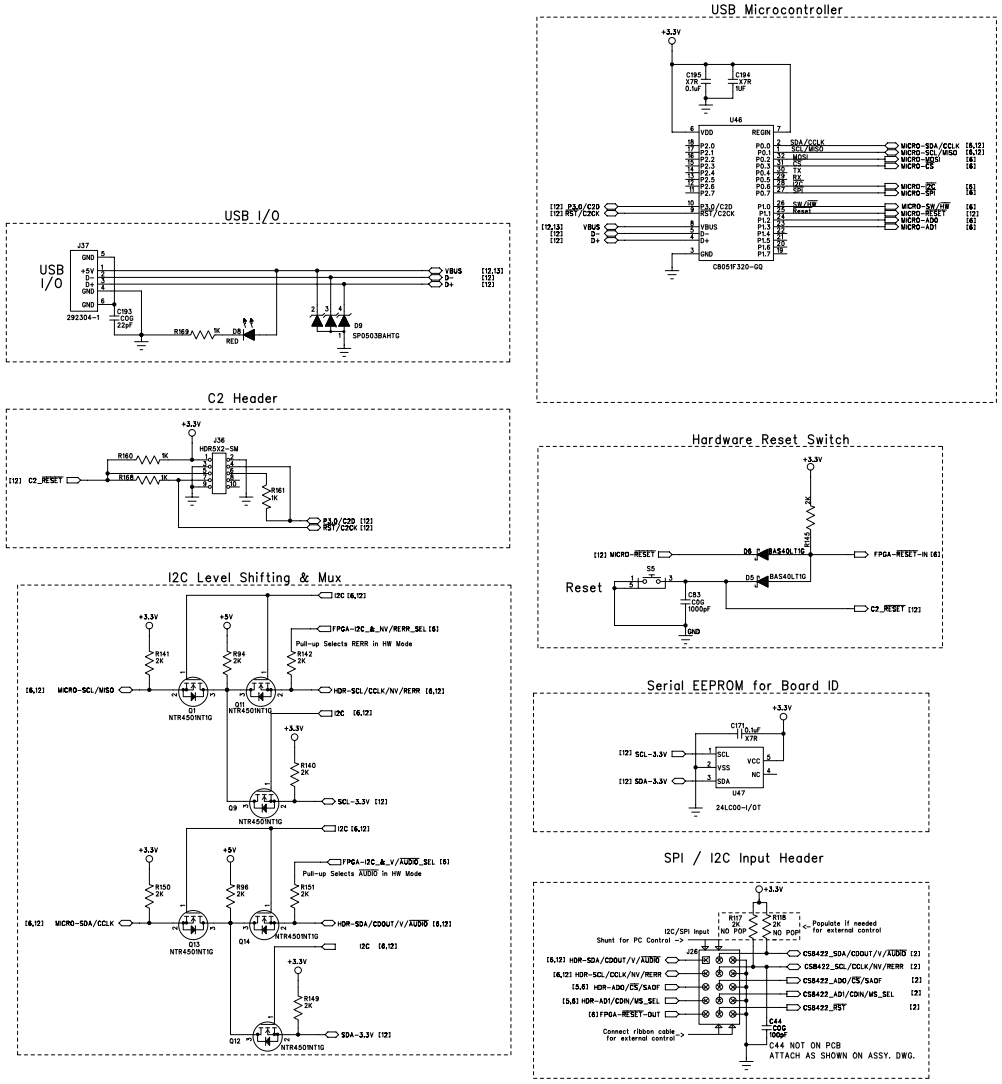


Figure 25. USB and MCU (Schematic Sheet 11)

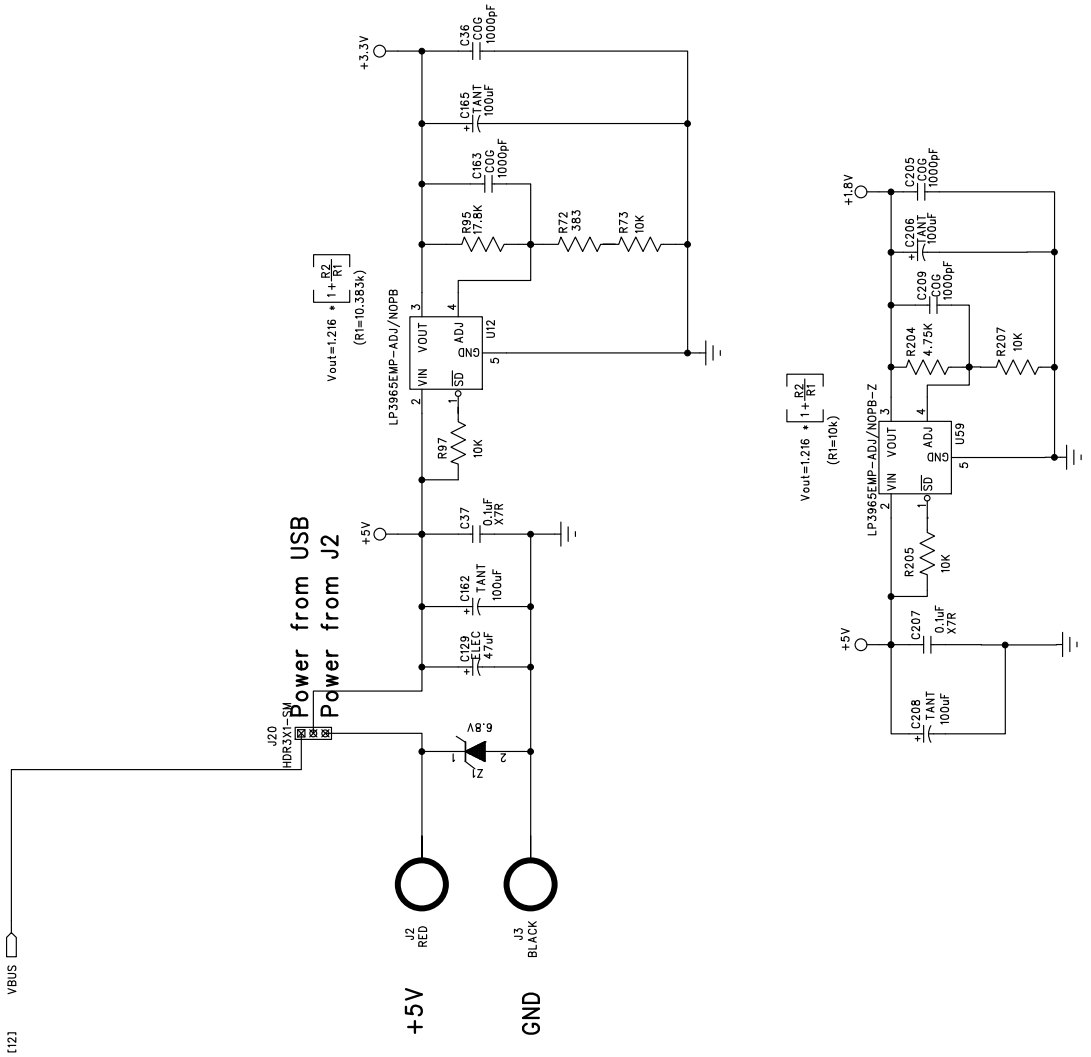


Figure 26. Power (Schematic Sheet 12)

9. CDB8422 LAYOUT

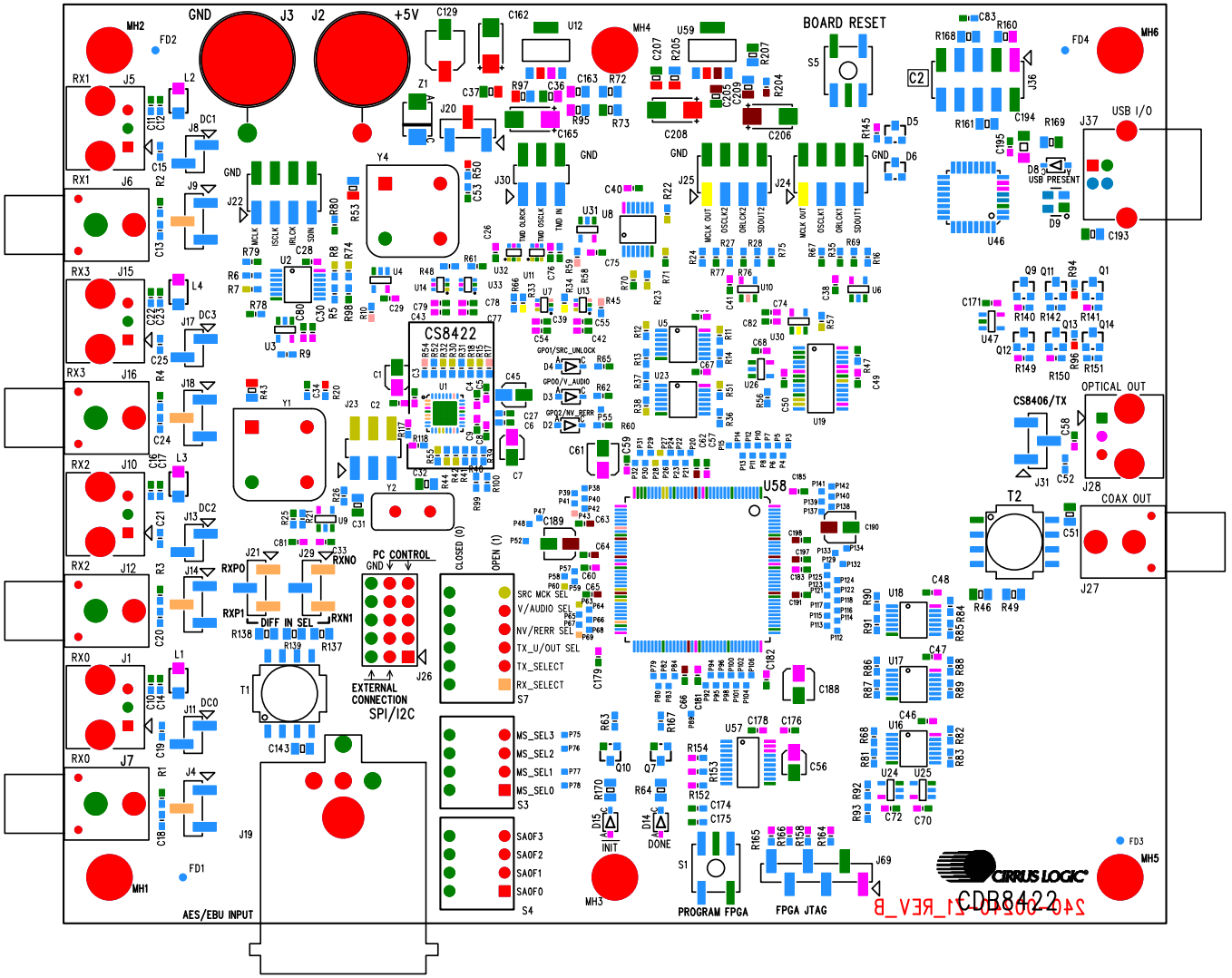


Figure 27. Silk Screen

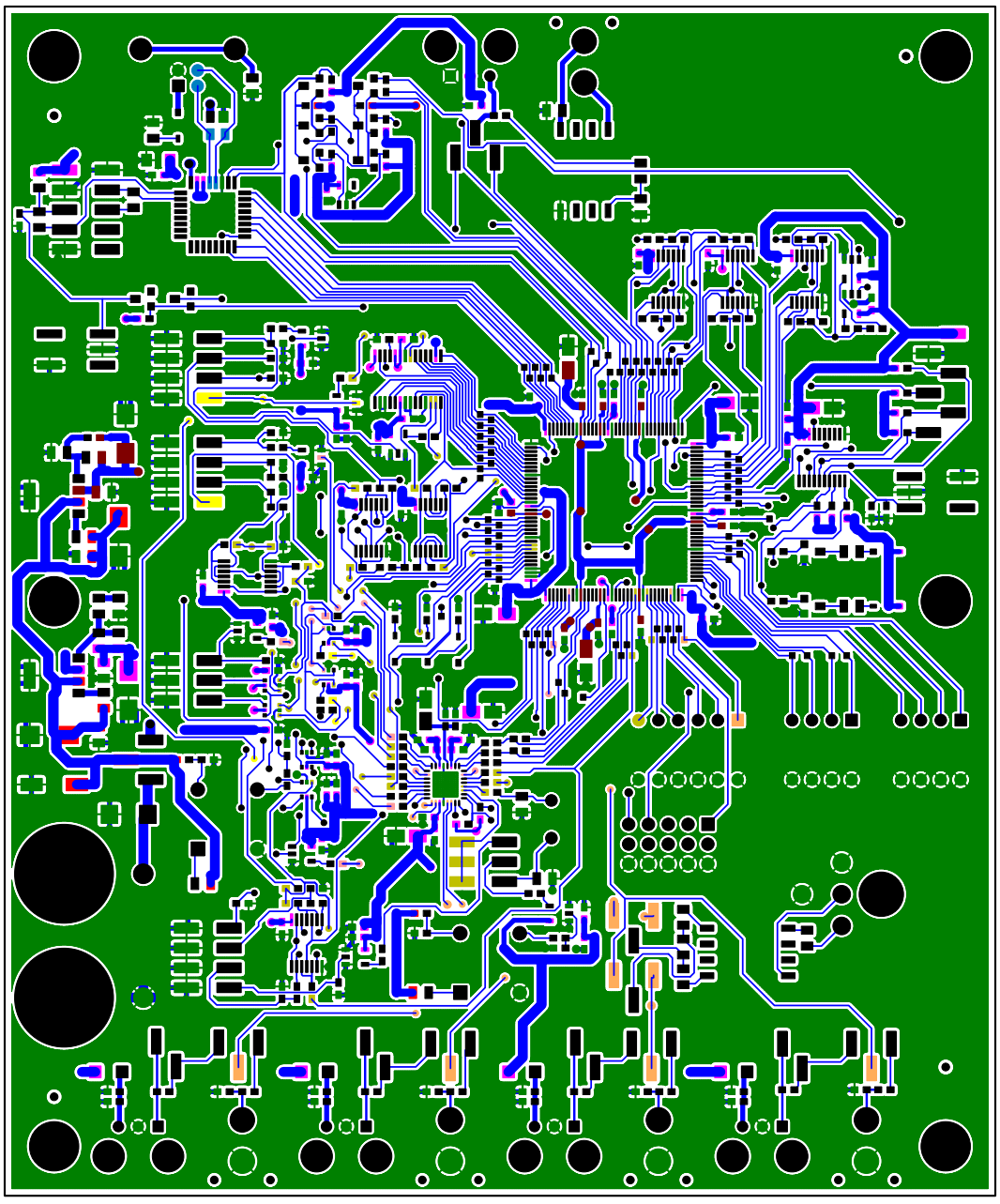


Figure 28. Top-Side Layer

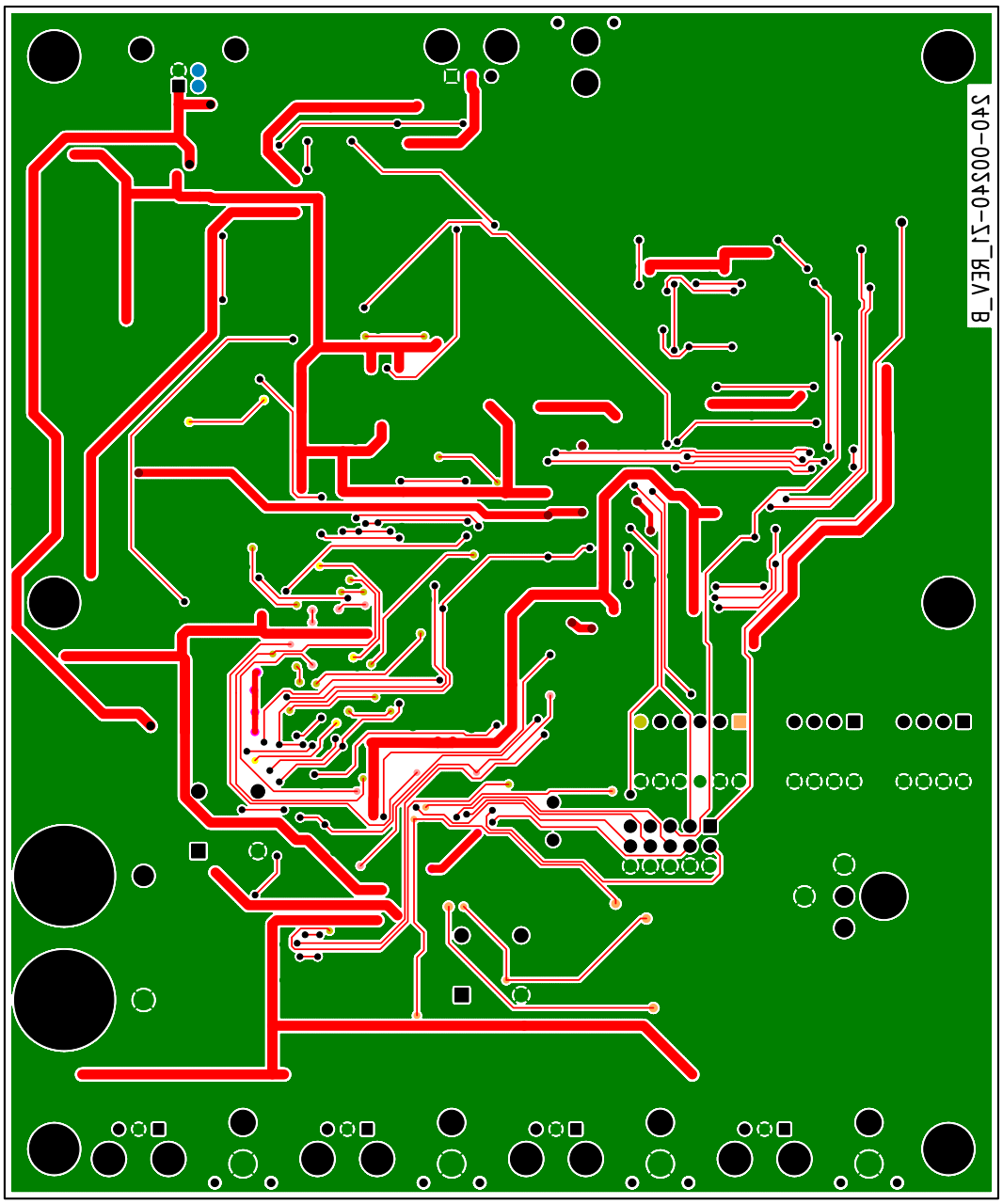


Figure 29. Bottom-Side Layer

10.REVISION HISTORY

Revision	Changes
DB1	Initial Release
DB2	Added S/PDIF receiver sensitivity note to Section 1.8 on page 5. Changed 0.01 pF to 0.01 µF in Table 7 on page 29.

Contacting Cirrus Logic Support

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