

## 1. General description

The CBT3253 is a dual 1-of-4 high-speed TTL-compatible FET multiplexer/demultiplexer. The low ON-resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The select control inputs (S0, S1) can select the data path, when both output enable inputs ( $1\bar{OE}$ ,  $2\bar{OE}$ ) are LOW. When  $n\bar{OE}$  is HIGH, the switch terminals are in the high impedance OFF-state, independent of S0 and S1.

The CBT3253 is characterized for operation from -40 °C to +85 °C.

## 2. Features and benefits

- 5 Ω switch connection between two ports
- TTL-compatible input levels
- Minimal propagation delay through the switch
- Latch-up protection exceeds 100 mA per JEDEC standard JESD78 class II level A
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package			Version
		Name	Description		
CBT3253D	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm		SOT109-1
CBT3253DB	-40 °C to +85 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm		SOT338-1
CBT3253PW	-40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm		SOT403-1

## 4. Functional diagram

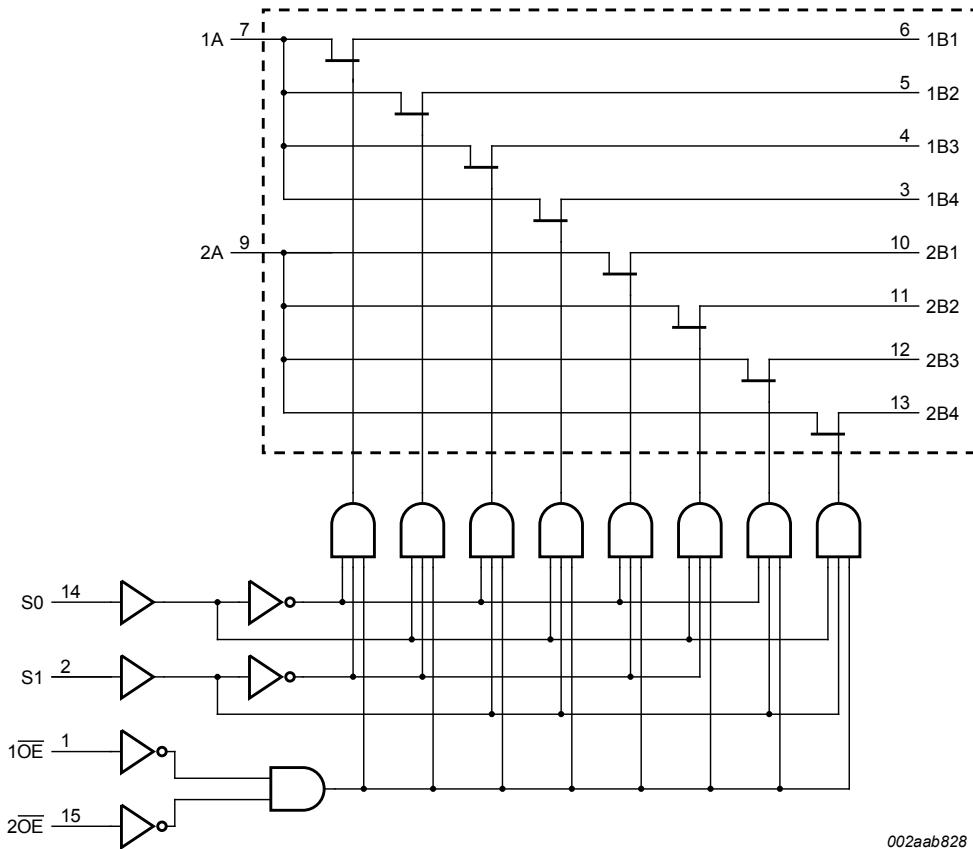


Fig. 1. Logic diagram

## 5. Pinning information

### 5.1. Pinning

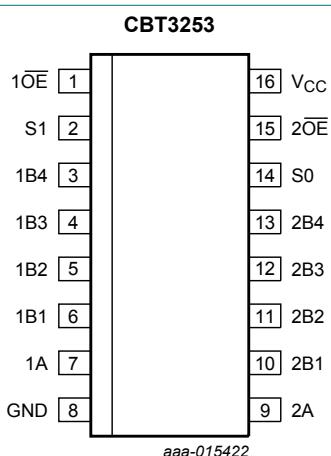


Fig. 2. Pin configuration SOT109-1 (SO16)

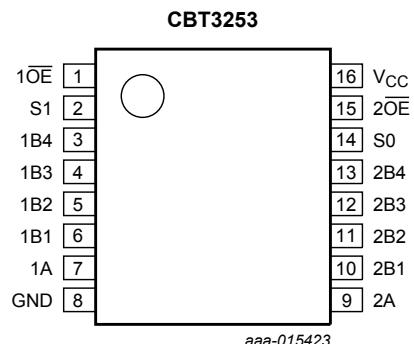


Fig. 3. Pin configuration SOT338-1 (SSOP16) and SOT403-1 (TSSOP16)

## 5.2. Pin description

**Table 2. Pin description**

Symbol	Pin	Description
1OE, 2OE	1, 15	output enable (active LOW)
S1, S0	2, 14	select control input
1B4, 1B3, 1B2, 1B1	3, 4, 5, 6	1B outputs/inputs
1A	7	1A input/output
GND	8	ground (0 V)
2A	9	2A input/output
2B1, 2B2, 2B3, 2B4	10, 11, 12, 13	2B outputs/inputs
V <sub>CC</sub>	16	positive supply voltage

## 6. Functional description

**Table 3. Function selection**

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

Inputs				Switch
1OE	2OE	S1	S0	
X	H	X	X	disconnect 1A to 1Bn and 2A to 2Bn
H	X	X	X	disconnect 1A to 1Bn and 2A to 2Bn
L	L	L	L	1A to 1B1 and 2A to 2B1
L	L	L	H	1A to 1B2 and 2A to 2B2
L	L	H	L	1A to 1B3 and 2A to 2B3
L	L	H	H	1A to 1B4 and 2A to 2B4

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V	
V <sub>I</sub>	input voltage		[1]	-0.5	+7.0	V
I <sub>sw</sub>	switch current	continuous current through each switch	-	128	mA	
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA	
T <sub>stg</sub>	storage temperature		-65	+150	°C	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C				
		SO16 package	[2]	-	500	mW
		(T)SSOP16 package	[3]	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] For SO16 package: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.

[3] For SSOP16 and TSSOP16 package: P<sub>tot</sub> derates linearly with 5.5 mW/K above 70 °C.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		4.5	5.5	V
$V_{IH}$	HIGH-level input voltage		2.0	-	V
$V_{IL}$	LOW-level input voltage		-	0.8	V
$T_{amb}$	ambient temperature	operating in free-air	-40	+85	°C

## 9. Static characteristics

**Table 6. Static characteristics**

$T_{amb}$  = -40 °C to +85 °C.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5$ V; $I_I = -18$ mA	-	-	-1.2	V
$V_{pass}$	pass voltage	$V_I = V_{CC} = 5.0$ V; $I_O = -100$ $\mu$ A	3.6	3.9	4.2	V
$I_I$	input leakage current	$V_{CC} = 5.5$ V; $V_I = GND$ or 5.5 V	-	-	$\pm 1$	$\mu$ A
$I_{CC}$	supply current	$V_{CC} = 5.5$ V; $I_O = 0$ mA; $V_I = V_{CC}$ or GND	-	-	3	$\mu$ A
$\Delta I_{CC}$	additional supply current	per input; $V_{CC} = 5.5$ V; one input at 3.4 V, other inputs at $V_{CC}$ or GND	[2]	-	-	mA
$C_I$	input capacitance	control pins; $V_I = 3$ V or 0 V	-	4.5	-	pF
$C_{IO(off)}$	off-state input/output capacitance	A port; $V_O = 3$ V or 0 V; $nOE = V_{CC}$	-	11.4	-	pF
		B port; $V_O = 3$ V or 0 V; $n\overline{OE} = V_{CC}$	-	3.8	-	pF
$C_{IO(on)}$	on-state input/output capacitance	A port and B port	-	18.6	-	pF
$R_{ON}$	ON resistance	$V_{CC} = 4.5$ V	[3]			
		$V_I = 0$ V; $I_I = 64$ mA	-	5	7	$\Omega$
		$V_I = 0$ V; $I_I = 30$ mA	-	5	7	$\Omega$
		$V_I = 2.4$ V; $I_I = -15$ mA	-	10	15	$\Omega$

[1] All typical values are measured at  $V_{CC} = 5$  V;  $T_{amb} = 25$  °C.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

[3] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. The lowest voltage of the two (A or B) terminals determines the ON resistance.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

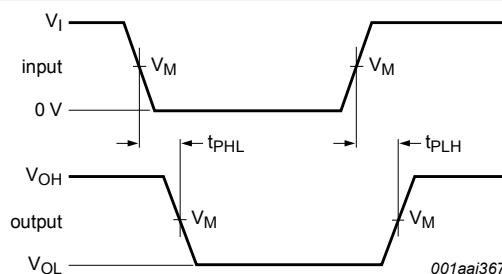
$T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;  $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ ; for test circuit, see [Fig. 6](#).

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{pd}$	propagation delay	nA to nBn or nBn to nA; see <a href="#">Fig. 4</a>	[1][2]	-	0.25 ns
		Sn to nA; see <a href="#">Fig. 4</a>	[1][2]	1.2	6.2 ns
$t_{en}$	enable time	Sn to nBn; see <a href="#">Fig. 5</a>	[2]	1.3	6.3 ns
		nOE to nA or nBn; see <a href="#">Fig. 5</a>	[2]	1.4	6.4 ns
$t_{dis}$	disable time	Sn to nBn; see <a href="#">Fig. 5</a>	[2]	1.1	7.2 ns
		nOE to nA or nBn; see <a href="#">Fig. 5</a>	[2]	1.0	7 ns

[1] This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance).

[2]  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ ;  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ ;  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

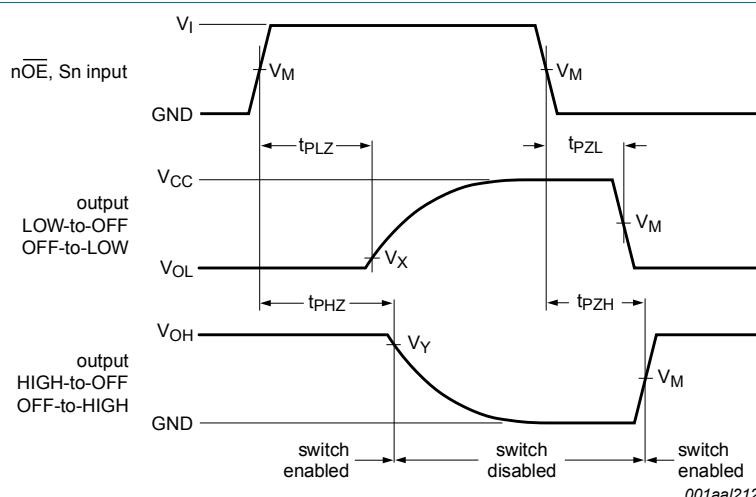
### 10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 4. The input (nA, nBn) to output (nBn, nA) or input (Sn) to output (nA) propagation delay times**



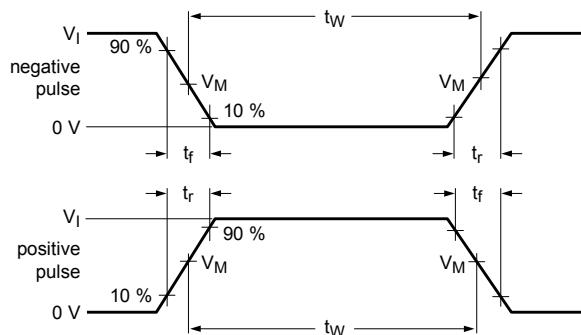
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 5. Enable and disable times**

Table 8. Measurement points

Supply voltage	Input		Output		
$V_{CC}$	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
4.5 V to 5.5 V	GND to 3.0 V	1.5 V	1.5 V	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V



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Test data is given in [Table 9](#).

Definitions for test circuit:

 $R_L$  = Load resistance. $C_L$  = Load capacitance including jig and probe capacitance. $R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator. $V_{EXT}$  = External voltage for measuring switching times.

Fig. 6. Test circuit for measuring switching times

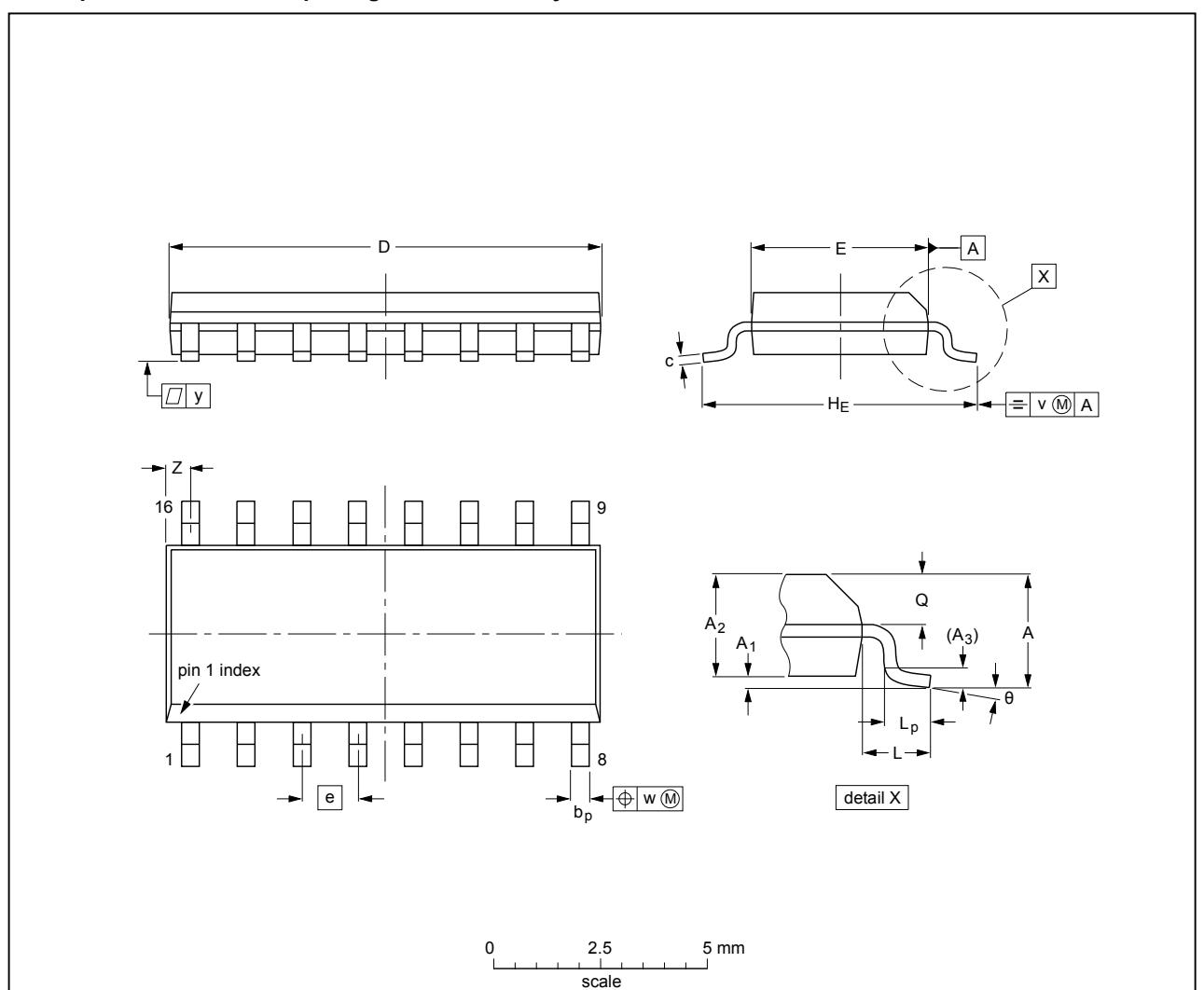
Table 9. Test data

Supply voltage	Input		Load		$V_{EXT}$			
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$	
4.5 V to 5.5 V	GND to 3.0 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	7.0 V	open	

## 11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.75 0.10	0.25 1.25	1.45 0.36	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

**Note**

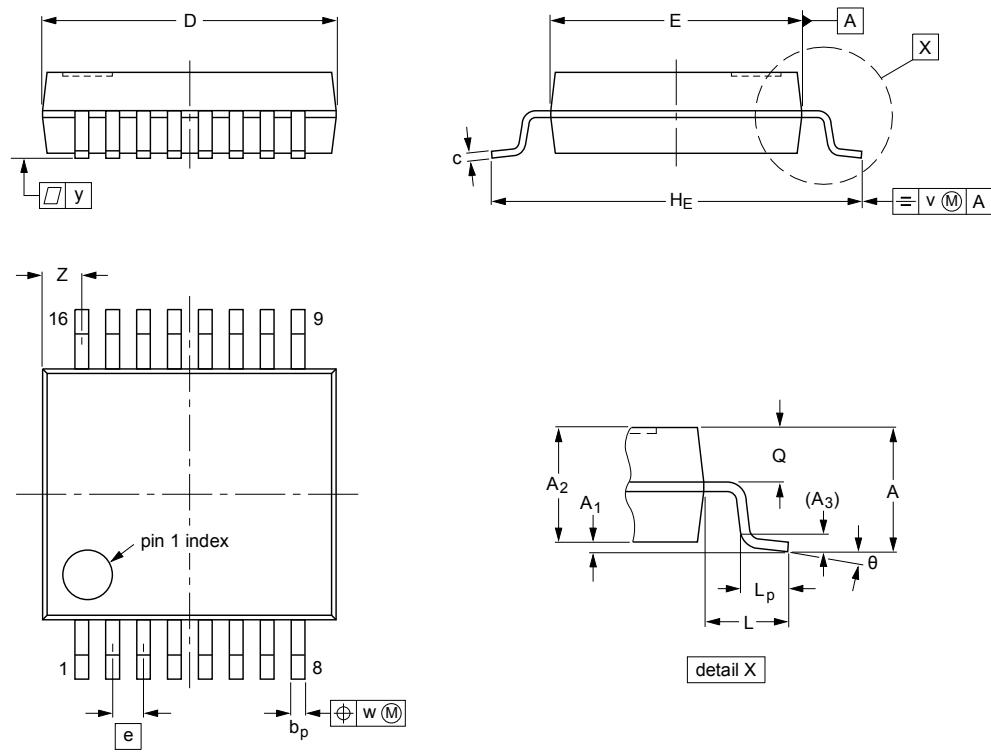
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig. 7. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



## DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2 0.05	0.21 1.65	1.80	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

## Note

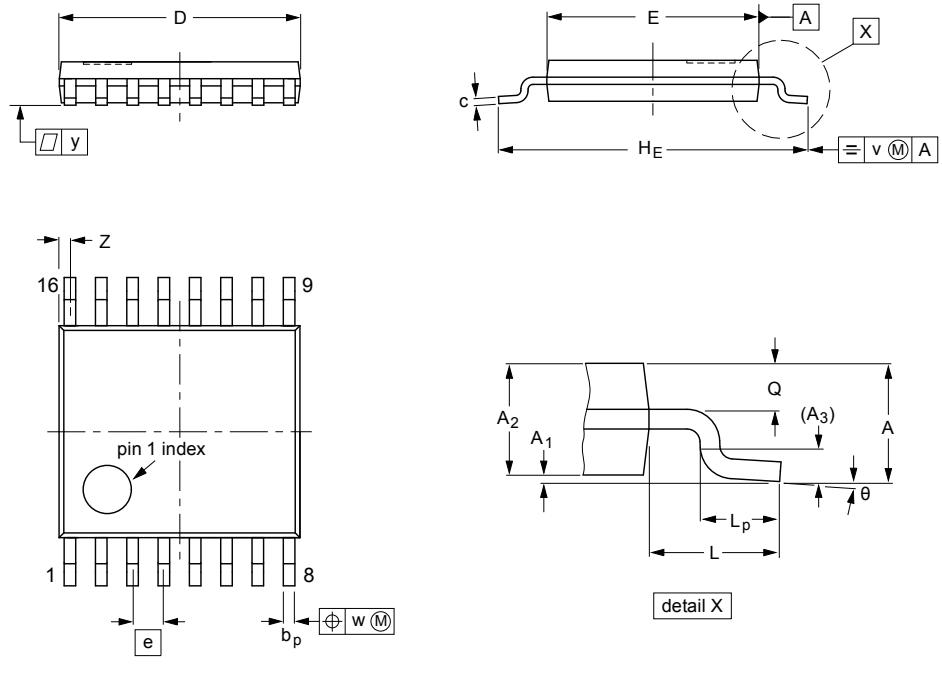
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				99-12-27 03-02-19

Fig. 8. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



0 2.5 5 mm  
scale

## DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.1 0.05	0.15 0.80	0.95 0.25	0.25 0.19	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

## Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				-99-12-27 03-02-18

Fig. 9. Package outline SOT403-1 (TSSOP16)

## 12. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3253 v.3	20181122	Product data sheet	-	CBT3253 v.2
Modifications:		<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number CBT3253DS (SOT519-1/SSOP16) removed.</li> </ul>		
CBT3253 v.2	20141203	Product data sheet	-	CBT3253 v.1
Modifications:		<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 1</a>: text changed to align with the function of the device.</li> <li><a href="#">Fig. 1</a>: schematic changed.</li> <li><a href="#">Table 3</a>: switch description changed to align with the function of the device.</li> <li><a href="#">Table 6</a>: <ul style="list-style-type: none"> <li><math>C_{io(off)}</math>, A port: changed typical value from 23.5 pF to 11.4 pF</li> <li><math>C_{io(off)}</math>, B port: changed typical value from 6.5 pF to 3.8 pF</li> <li>added <math>C_{io(on)}</math> specification</li> <li>values for pass voltage modified.</li> </ul> </li> </ul>		
CBT3253 v.1	20021104	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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