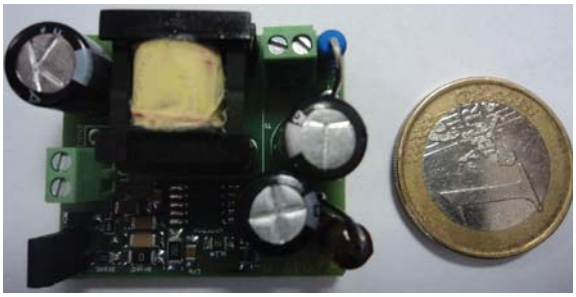
# STEVAL-ISA113V1

## Wide range single-output demonstration board based on the VIPER06HS

**Data brief**

## Features

- Universal input mains range:
  - input voltage 90 - 265 $V_{AC}$
  - frequency 45 - 65 Hz
- Single-output voltage: 12 V at 0.35 A continuous operation
- Standby mains consumption: < 30 mW at 230 $V_{AC}$
- Average efficiency: > 74%
- Fully protected against faults (overload, feedback disconnection and overheating)
- EMI: according to EN55022-Class-B
- RoHS compliant



STEVAL-ISA113V1

## Description

The STEVAL-ISA113V1 demonstration board is a 12 V-0.35 A power supply set in non-isolated flyback topology using the new VIPER06HS offline high-voltage converter by STMicroelectronics.

The features of the device include an 800 V avalanche rugged power section, PWM operation at 115 kHz with frequency jittering for lower EMI, current limiting with adjustable set point, onboard soft-start, a safe auto-restart after a fault condition and a low standby power.

The protection features available include a thermal shutdown with hysteresis, delayed overload protection, and open loop failure protection.

# 1 Adapter features

The electrical specifications are given in *Table 1*, the schematic in *Figure 1*, and the bill of material in *Table 2*.

**Table 1. Electrical specifications**

| Parameter | Symbol | Value |
|---|---|---|
| Input voltage range | $V_{IN}$ | [90 $V_{AC}$; 265 $V_{AC}$] |
| Output voltage | $V_{OUT}$ | 12 V |
| Max. output current | $I_{OUT}$ | 0.35 A |
| Precision of output regulation | $\Delta V_{OUT\_LF}$ | ±5% |
| High frequency output voltage ripple | $\Delta V_{OUT\_HF}$ | 50 mV |
| Max. ambient operating temperature | $T_{AMB}$ | 60 °C |

**Table 2. Bill of material**

| Ref. | Part | Description | Package | Manufacturer |
|---|---|---|---|---|
| Cin1 | | 2.2 µF, 400 V NHG series electrolytic capacitor | | |
| Cin2 | | 4.7 µF, 400 V AX series electrolytic capacitor | | Saxon |
| CVDD | | 1 µF, 50 V electrolytic capacitor | 1206 | Murata |
| Cfilt1 | | 100 nF, 50 V ceramic capacitor | 0805 | |
| Cfilt2 | Not mounted | | | |
| Cc | | 10 nF, 50 V ceramic capacitor | 1206 | |
| Cp | | 1 nF, 50 V ceramic capacitor | 1206 | |
| Cfb | | 1 nF, 50 V ceramic capacitor | 0805 | |
| Cout | | 330 µF, 16 V ZL series ultra-low ESR electrolytic cap. | | Rubycon |
| D0 | MB6S | 600 V, 1 A diode bridge | TO-269AA | Vishay |
| D2 | STPS2H100 | 100 V, 2 A power Schottky rectifier | SMA | ST |
| Daux | 1N4148W | Surface mount fast switching diode | SOD-123 | Zetex |
| R0 | | 4.7 Ω 3/4 W resistor | | |
| RLIM | | 15 kΩ 5% 1/4 W resistor | 0805 | |
| Rc | | 47 kΩ 5% 1/4 W resistor | 0805 | |
| RfbH1 | | 33 kΩ 1% 1/4 W resistor | 0805 | |
| RfbH2 | | 0 Ω | 1206 | |
| RfbL1 | | 12 kΩ 1% 1/4 W resistor | 1206 | |
| RfbL2 | | 0.47 kΩ 1% 1/4 W resistor | 0805 | |

**Table 2. Bill of material (continued)**

| Ref. | Part | Description | Package | Manufacturer |
|---|---|---|---|---|
| IC1 | VIPer06HS | Offline high-voltage PWM controller | SSO-10 | ST |
| T1 | 1921.0040 | Transformer | | Magnetica |
| Lin | B82144A2105J | 1 mH inductor LBC series | | Epcos |

The transformer core is a standard E13. The output voltage value is set in a simple way through the RfbH-RfbL voltage divider between the output terminal and the FB pin, according to the following formula:

**Equation 1**

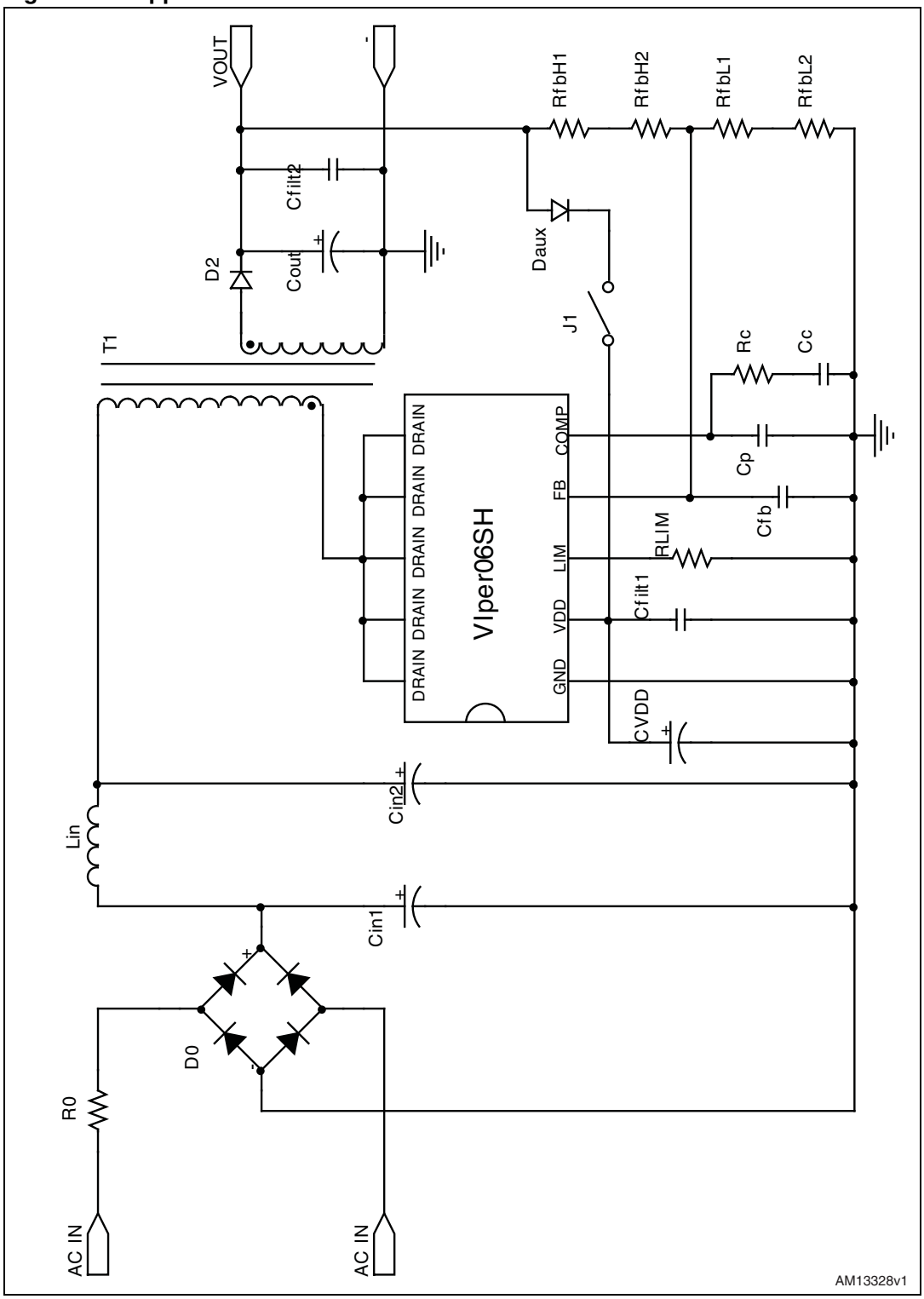
$$V_{OUT} = 3.3V \cdot \left(1 + \frac{RfbH}{RfbL}\right)$$

In the schematic, RfbH has been split into RfbH1 and RfbH2; and RfbL into RfbL1 and RfbL2 in order to allow a better tuning of the output voltage value.

If the jumper J1 is not selected, the IC is biased through the internal HV-startup current generator (“self-biasing”).

If low standby consumption and good efficiency performance are required, the HV-startup current generator must be excluded. This can be done selecting the jumper J1, which connects the output terminal to the $V_{DD}$ pin through a small signal diode. The IC biasing through the output is referred to as “external biasing”.

**Figure 1. Application schematic**



# 2 Measurements

**Figure 2. Line regulation at different loads: IC externally biased (J1 selected)**

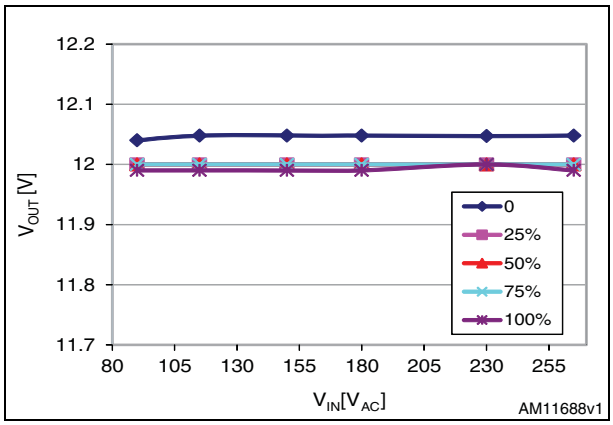



**Figure 3. Line regulation at different loads: IC self-biased (J1 not selected)**

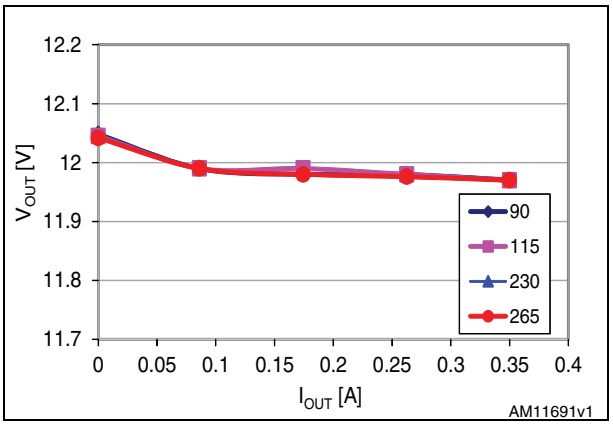



**Figure 4. Efficiency vs. $V_{IN}$ IC externally biased (J1 selected)**

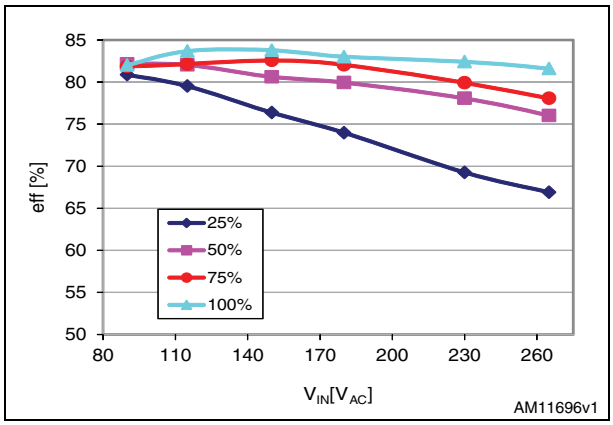



**Figure 5. Efficiency vs. $V_{IN}$ IC self-biased (J1 not selected)**

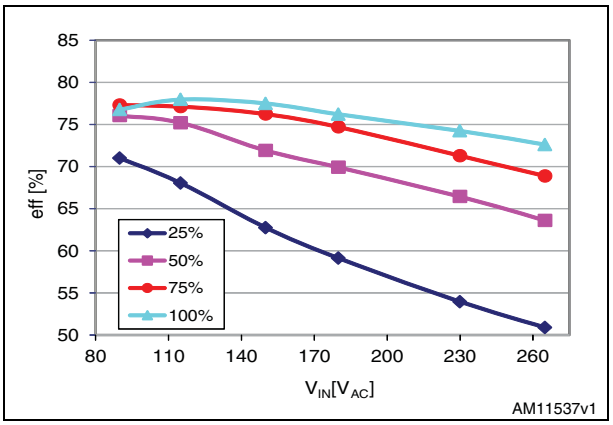



**Figure 6. Efficiency at different input voltages: IC externally biased (J1 selected)**

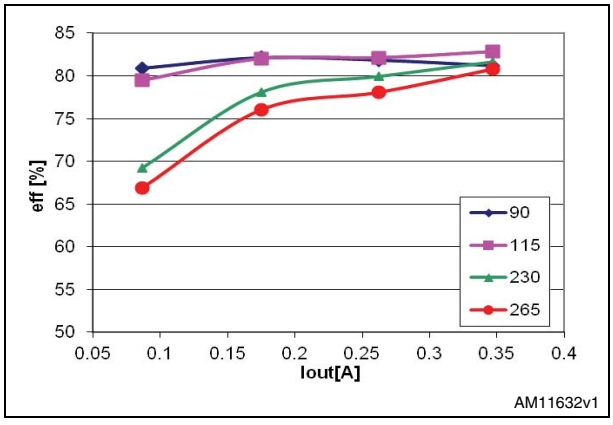



**Figure 7. Efficiency at different input voltages: IC self-biased (J1 not selected)**

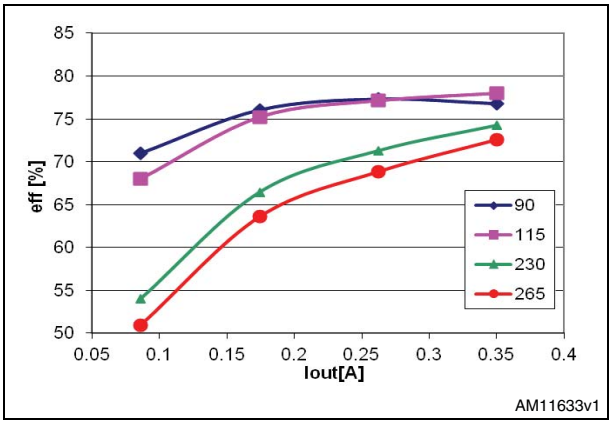


**Figure 8. Active mode efficiency vs. $V_{IN}$ IC externally biased (J1selected)**

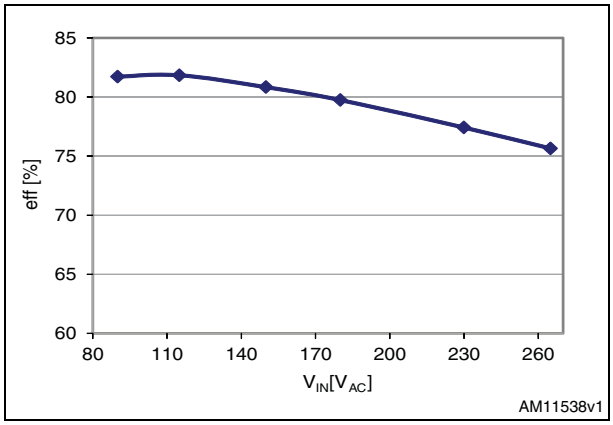



**Figure 9. Active mode efficiency vs. $V_{IN}$ IC self-biased (J1 not selected)**

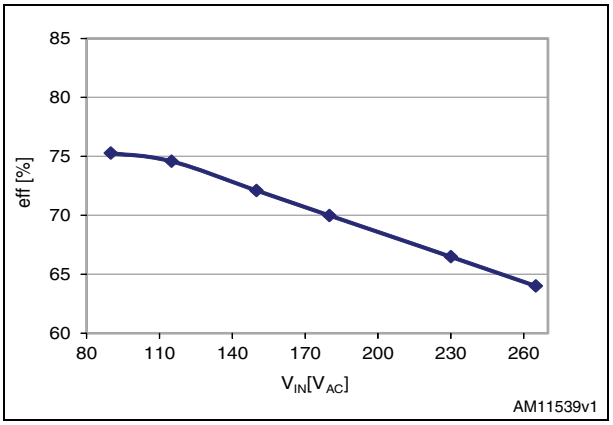



**Figure 10. Input voltage averaged efficiency vs. load IC externally biased (J1 selected)**

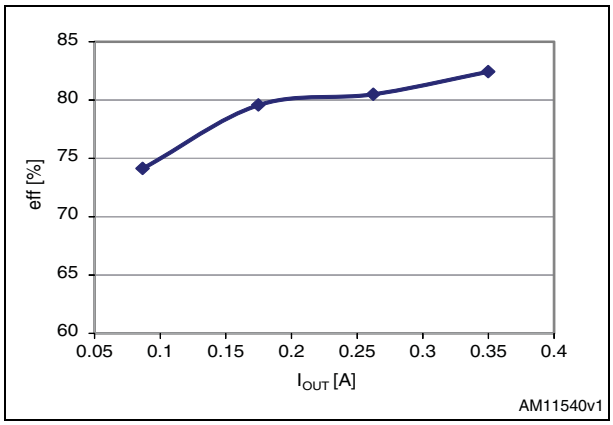



**Figure 11. Input voltage averaged efficiency vs. load IC self-biased (J1 not selected)**

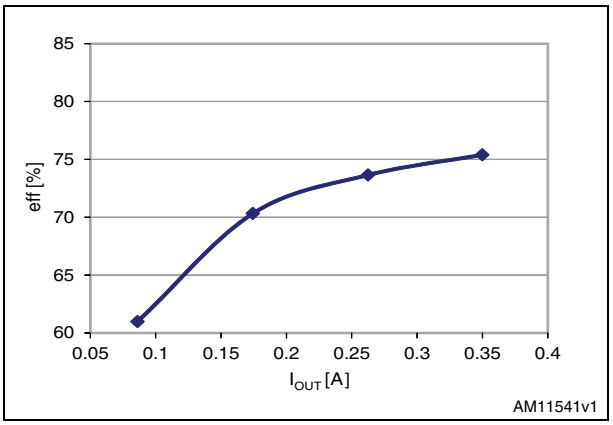



**Figure 12. $P_{IN}$ vs. $V_{IN}$ at no load and light load: IC externally biased (J1 selected)**

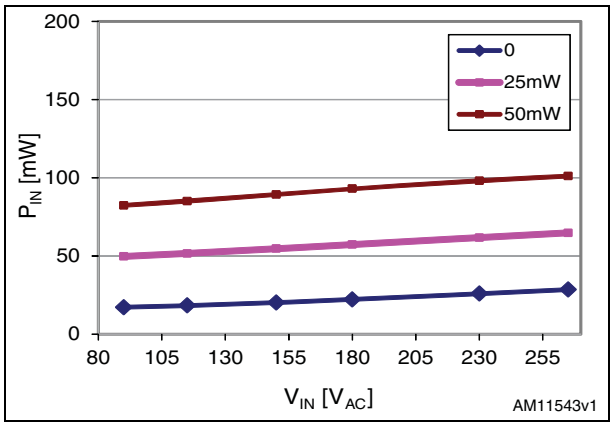



**Figure 13. $P_{IN}$ vs. $V_{IN}$ at no load and light load: IC self-biased (J1 not selected)**

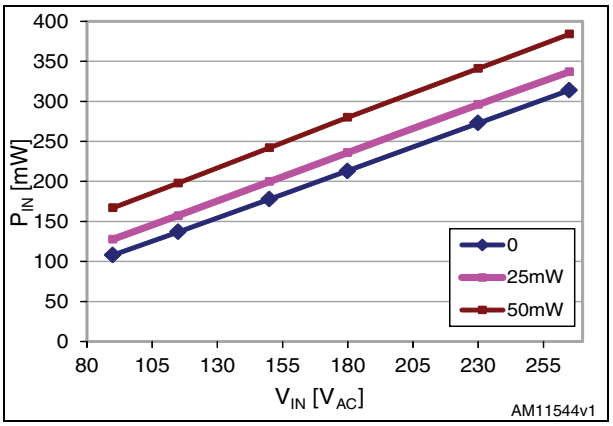


**Figure 14. Efficiency at $P_{IN}$ = 1 W: IC externally biased (J1 selected)**

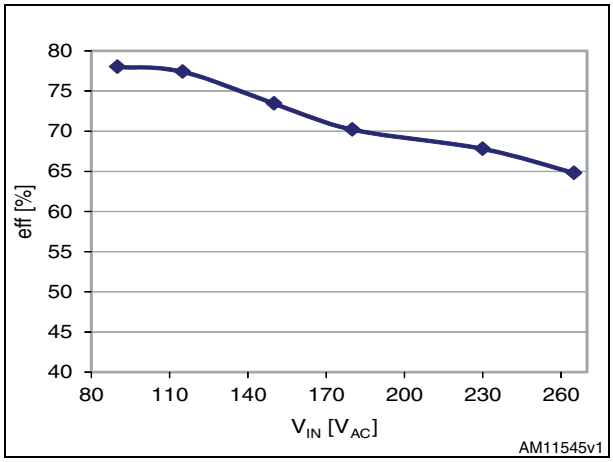



**Figure 15. Efficiency at $P_{IN}$ = 1 W: IC self-biased (J1 not selected)**

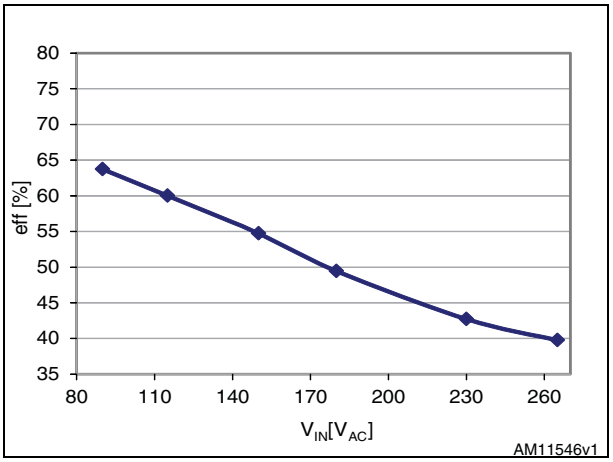



**Figure 16. $P_{IN}$ at $P_{OUT}$ = 250 mW: IC externally biased (J1 selected)**

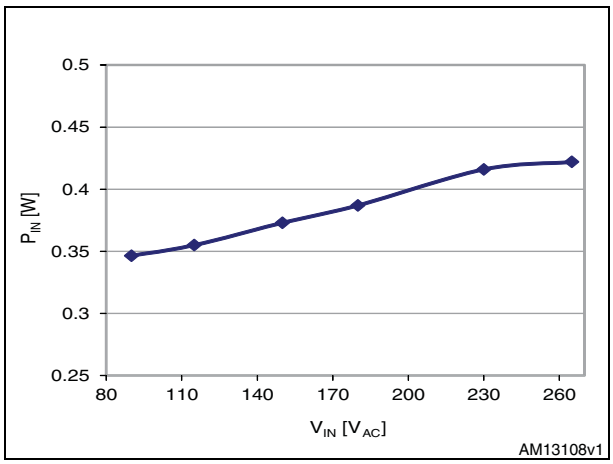
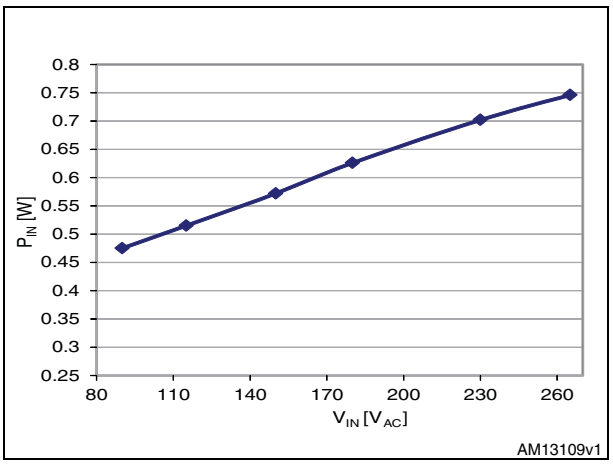



**Figure 17. $P_{IN}$ at $P_{OUT}$ = 250 mW: IC self-biased (J1 not selected)**



# 3 Board layout

**Figure 18. Board layout - complete**

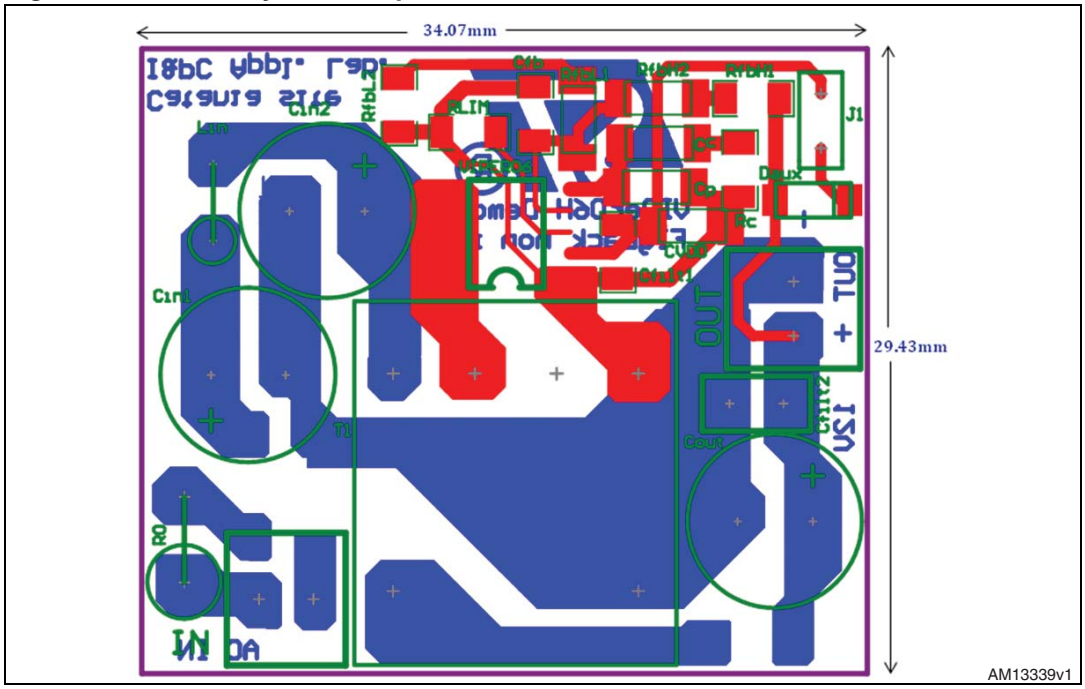



**Figure 19. Board layout - top layer + top overlay**

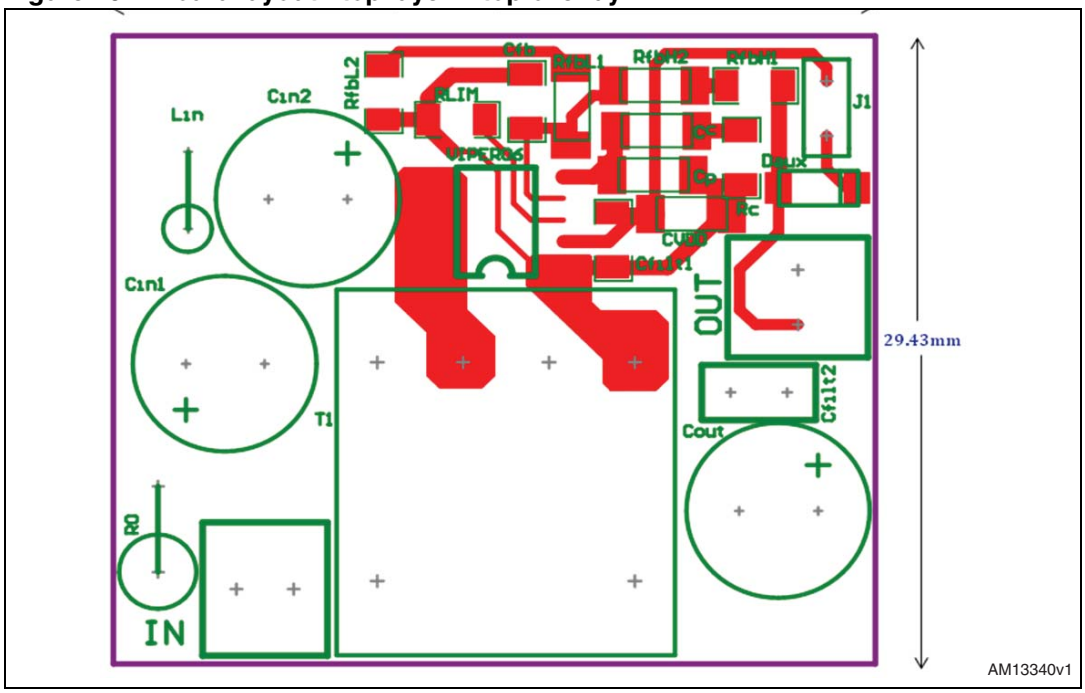
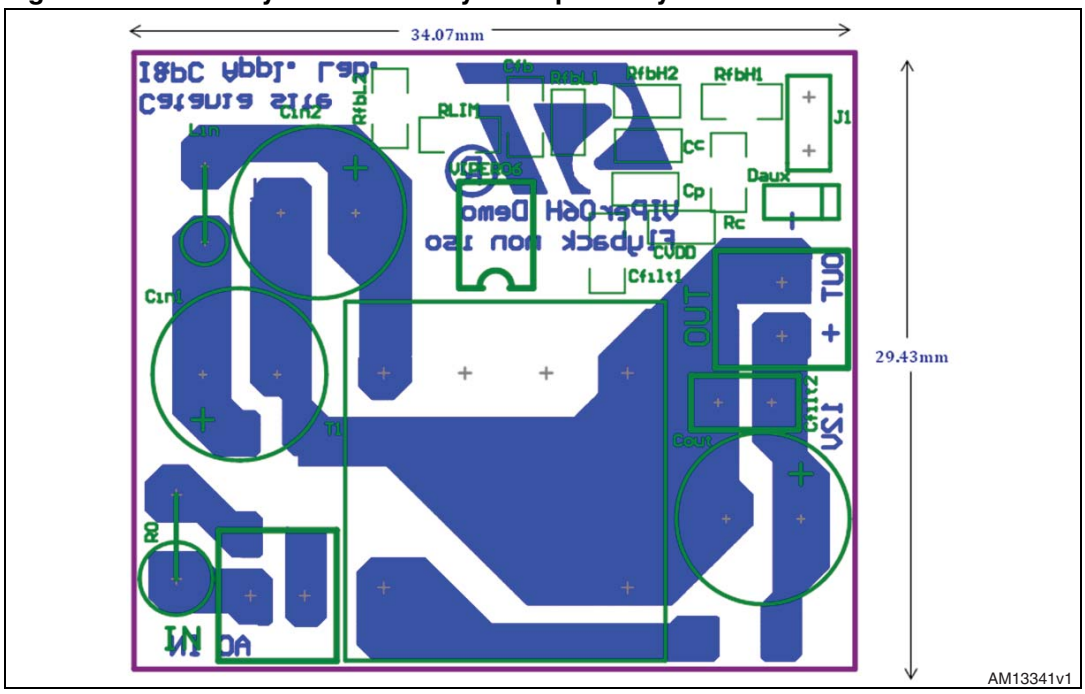


**Figure 20. Board layout - bottom layer + top overlay**



# 4 Revision history

Table 3. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 10-Jan-2013 | 1 | Initial release. |

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