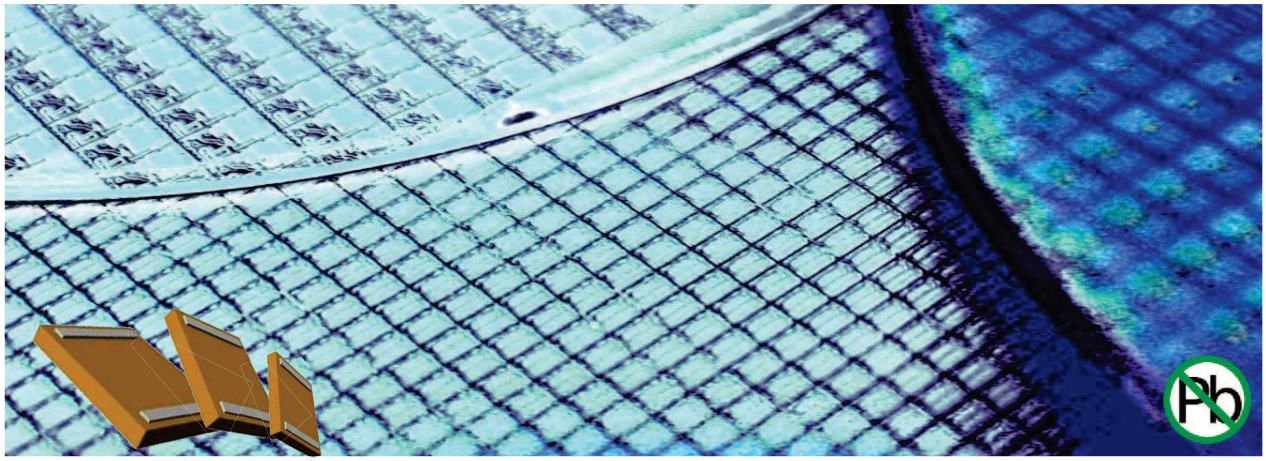
LPSC427.xxx - 1206 Low Profile Silicon Capacitor

Rev 3.1



Key features

- **Ultra low profile (100µm)**
- **High stability of capacitance value:**
  - **Temperature <±0.5% (-55°C to +150°C)**
  - **Voltage <0.1%/Volts**
  - **Negligible capacitance loss through ageing**
- **Unique high capacitance in 1206 package size, up to 1 µF**
- **High reliability (FIT <0.017 parts / billion hours)**
- **Low leakage current down to 100 pA**
- **Low ESL and Low ESR**
- **Suitable for lead free reflow-soldering** *Please refer to our assembly Application Note for further recommendations

Key applications

- **All demanding applications, such as medical, telecom, computer industries**
- **Decoupling / Filtering / Charge pump (i.e.: Pacemakers / mobile phones)**
- **High reliability applications**
- **Devices with battery operations**
- **Extreme miniaturization**
- **Suitable for Embedded technologies**

Thanks to the unique IPDiA Silicon capacitor technology, most of the problems encountered in demanding applications can be solved.

Low **P**rofile **S**ilicon **C**apacitors are available with **thicknesses down to 80µm** and are the most appropriate solution in applications with height constraints.

LPSC is the perfect choice for embedded technologies, modules, systems in package, when designers are looking at **utmost decoupling behaviours.**

The Silicon capacitor technology offers a capacitor integration capability (up to 250nF/mm^2) which allows **downsizing** compared to Tantalum and MLCC.

The IPDiA technology features **high reliability**, up to 10 times better than alternative capacitor technologies, such as Tantalum or MLCC, and eliminates cracking phenomena.

Silicon Capacitor technology also offers a very stable capacitor value over the full operating voltage & temperature range, with a high and stable insulation resistance.

This Silicon based technology is RoHS compliant and compatible with lead free reflow soldering process.

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Electrical specification

Unit	Capacitance value	10	15	22	33	47	68
	1 nF	10nF 935.121.427.510	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*
	10 nF	100nF 935.121.427.610	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*	*Contact IPDIA Sales*
	0,1 µF	1µF 935.121.427.710					
	1 µF						

(*) 80 µm thickness on request

(**) Extended temperature range (up to +250 °C) available, see Xtreme Temperature Silicon Capacitor product: XTSC

(***) Other values on request.

Parameters	Value
Capacitance range	*10 nF to 1µF(***)*
Capacitance tolerances	*±15 %(***)*
Operating temperature range	*-55 °C to 150 °C (**)*
Storage temperatures	*- 70 °C to 165 °C*
Temperature coefficient	*<±0.5 %, from -55 °C to +150 °C*
Breakdown voltage (BV)	*11 VDC(***)*
Capacitance variation versus RVDC	*0.1 % /V (from 0 V to RVDC)*
Equivalent Serial Inductor (ESL)	*Max 1nH*
Equivalent Serial Resistor (ESR)	*Max 500mΩ(***)*
Insulation resistance	*100GΩ min @ 3V, 25°C*
Ageing	*Negligible, < 0.001 % / 1000 h*
Reliability	*FIT<0.017 parts / billion hours,*
Capacitor height	*Max 100 µm (*)*

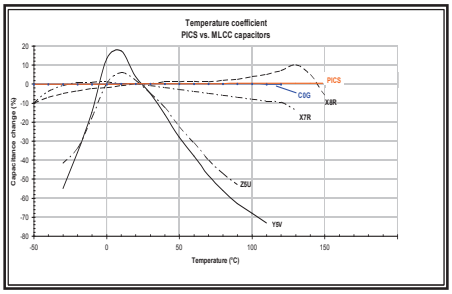


Fig.1 Capacitance change versus temperature variation compared with alternative dielectrics

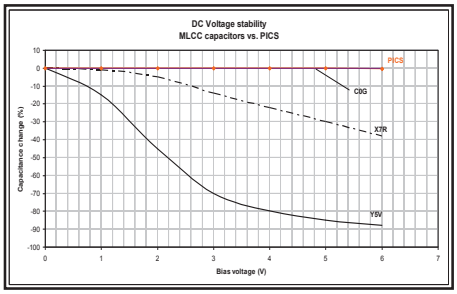


Fig.2 Capacitance change versus voltage variation compared with alternative dielectrics

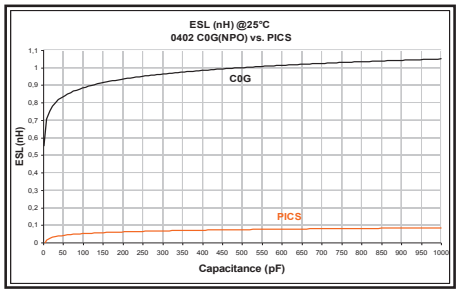


Fig.3 ESL versus capacitance value compared with alternative dielectrics

Part Number

935.121. **B.2** **S.** **U** **xx** → Value (E6)

B.2 → Breakdown Voltage
4 = 11V

S. → Size
7 = 1206

U → Unit

0 = 10 f	5 = 1 n
1 = 0.1 p	6 = 10 n
2 = 1 p	7 = 0.1 µ
3 = 10 p	8 = 1 µ
4 = 0.1 n	9 = 10 µ

xx → Value (E6)
10
15
22
33
47
68

i.e.: 1 µF/1206 case (LPSC type)
→ 935.121.427.710

Termination and Outline

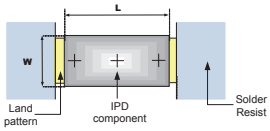
Termination

Lead-free nickel/solder coating compatible with automatic soldering technologies: reflow and manual.

Typical dimensions, all dimensions in mm.

Package outline

Typ.		1206
Comp. size	L	3.40±0.05
	W	1.80±0.05



(1206 PCB footprint)

Packaging

Tape and reel, tray, waffle pack or wafer delivery.

For more information, please visit: http://www.ipdia.com
To contact us, email to: sales@ipdia.com

Date of release: 28th February 2014
Document identifier: CL431 111 615 124

IPD Capacitor Assembly Set Up

Rev 1.0

Application Note

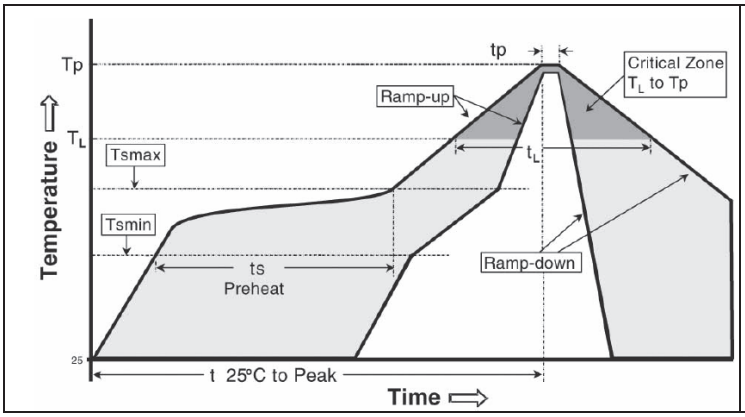
Outline

Silicon Capacitor for surface mounting device (SMD) assembly is a Wafer Level Chip Scale Packaging with the following features:

- Package dedicated to solve tombstoning effect of small SMD package;
- Package compatible with SMD assembly;
- Package without underfilling step;
- Interconnect available with various optional finishing for specific assembly.

Assembly consideration

- Standard pick & place equipment dedicated to WLCSP down to 400µm pitch.
- Solder paste type 3 in most cases of EIA size.
- Reflow has to be done with standard lead-free profile (for SAC alloys) or according to JEDEC recommendations J-STD 020D-01.



	Lead	Leadfree
	Tp: 235 °C	Tp: 260 °C
	TL: 183 °C	TL: 217 °C
	Ts min: 100 °C	Ts min: 150 °C
	Ts max: 150 °C	Ts max: 200 °C
	tL: 60-150 s	tL: 60-150 s

Process recommendation

After soldering, no solder paste should touch the side of the capacitor die as that might results in leakage currents due to remaining flux.

In order to use IPDiA standard capacitors within the JEDEC format and recommendation, the solder flux must be cleaned after reflow soldering step.
Notes: for a proper flux cleaning process, “rosin” flux type (R) or “water soluble” flux type (WS) is recommended for the solder printing material. “No clean” flux (NC) solder paste is not recommended.

In case the flux is not cleaned after the reflow soldering, the standard JEDEC would probably not be appropriate and the solder volume must be controlled:

- using smallest aperture design for the stencil, and using finer solder paste type 4 or 5 for a proper printing process.
- Mirroring pads would be the best recommendation

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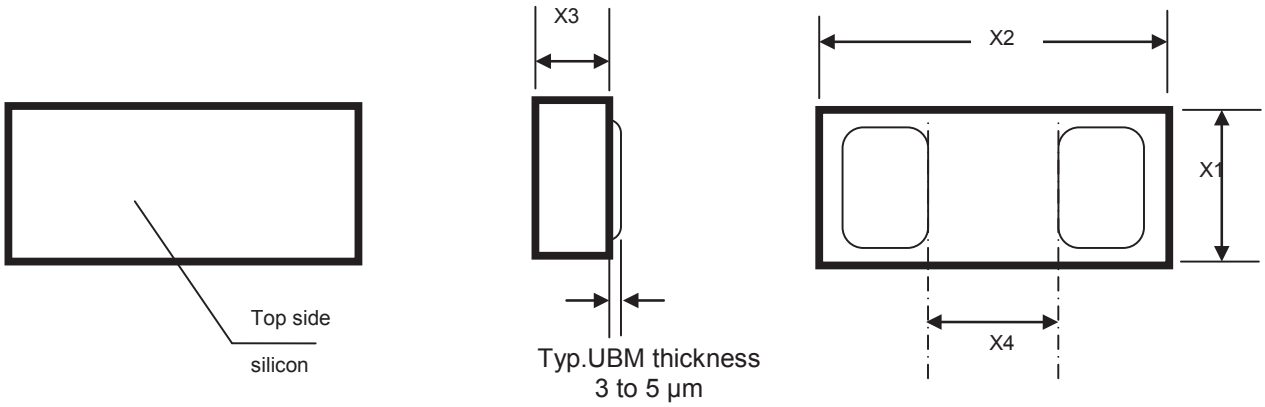
Pad recommendation

The capacitor is compatible with generic requirements for flip chip design (IPC7094).
Standard IPDiA 3D package can be compliant with established EIA size (0201, 0402, 0603, …).

Die size and land pattern dimensions is set up according to following range :

EIA size	0201	0402	0603	0805	1206	1812
Dimension max(X1 x X2) mm	0.86x0.66	1.26x0.76	1.86x1.16	2.26x1.46	3.46x1.86	4.76x3.66
Typical . die thickness X3 (mm)	0.1 or 0.4					
Typical pad size* (mm)	0.15x0.40	0.30x0.50	0.40x0.90	0.50x1.20	0.60x1.60	0.90x3.40
Typical pad separation (X4 mm)	0.3	0.4	0.8	1	2	2.7



After soldering, no solder paste should touch the side of the capacitor die as that might result in leakage currents due to remaining flux.

Manual Handling Considerations

These capacitors are designed to be mounted with a standard SMT line, using solder printing step, pick and place machine and a final reflow soldering step. In case of manual handling and mounting conditions, please follow below recommendations:

- Minimize mechanical pressure on the capacitors (use of a vacuum nozzle is recommended).
- Use of organic tip instead of metal tip for the nozzle.
- Minimize temperature shocks (Substrate pre-heating is recommended).
- No wire bonding on 0402 47nF, 0402 100nF, 1206 1µF and 1812 3,3µF

Process steps:

- On substrate, form the solder meniscus on each land pattern targeting 100 µm height after reflow (screen printing, dispensing solder paste or by wire soldering).
- Pick the capacitor from the tape & reel or the Gel Pack keeping backside visible using a vacuum nozzle and organic tip.
- Temporary place the capacitor on land pattern assuming the solder paste (Flux) will stick and maintain the capacitor.
- Reflow the assembly module with a dedicated thermal profile (see reflow recommendation profile).

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