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Evaluation Board for Single, High Speed Op Amps Offered in 8-Lead SOIC Packages

FEATURES

Enables quick breadboarding/prototyping
User-defined circuit configuration
Edge-mounted SMA connector provisions
Easy connection to test equipment and other circuits
RoHS compliant

GENERAL DESCRIPTION

The Analog Devices, Inc., 8-lead SOIC evaluation board is designed to help users evaluate single, high speed op amps offered in 8-lead SOIC packages. The evaluation board is a bare board (that is, there are no components or amplifier soldered to the board, these must be ordered separately) that enables users to quickly prototype a variety of single op amp circuits, which minimizes risk and reduces time to market.

The evaluation board is a 2-layer printed circuit board (PCB) that accepts SMA edge-mounted connectors on the inputs and outputs for efficient connection to test equipment or other circuitry. The evaluation board is designed to work with almost any of the Analog Devices op amps offered in an 8-lead SOIC package. The evaluation board can accommodate amplifiers that feature a power-down or disable pin. The board can also be used with op amps that feature external frequency compensation capacitors, such as the AD8021AR.

Figure 1 shows the component side of the bare evaluation board, and Figure 2 shows the circuit side of the bare evaluation board.

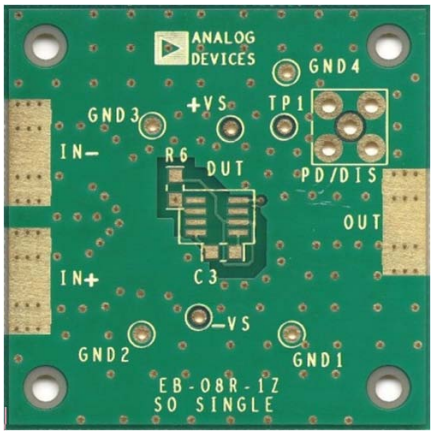
The ground plane, component placement, and supply bypassing have been designed to provide maximum flexibility while minimizing parasitic inductances and capacitances. The components of the evaluation board are primarily SMT 1206 case size, with the exception of the electrolytic bypass capacitors (C1, C4), which are 3528 case size.

Figure 3 shows the evaluation board schematic. The assembly drawings are shown in Figure 4 and Figure 6. The recommended layout patterns for making connections to the op amp and supporting circuitry are shown in Figure 5 and Figure 7.

Two options for supply bypassing include the following:

1. Connect additional shunt capacitors (C2, C5) in parallel with the electrolytic capacitors (C1, C4) from each supply to ground. This technique of power supply bypassing provides wideband rejection of unwanted noise on the supply lines. It is implemented by placing a 0 Ω resistor in the C6 position and shunt capacitors in the C1, C2, C4, and C5 positions.
2. Connect a capacitor between the supply rails. This method uses fewer components and can improve the PSRR at higher frequencies but does not provide shunt bypassing to the negative supply rail. It is implemented by inserting a 0 Ω resistor in the C2 position, then inserting the bypass capacitor in the C5 position, and omitting C6. Optimal bypassing is circuit dependent and, therefore, must be evaluated by the designer for each application.

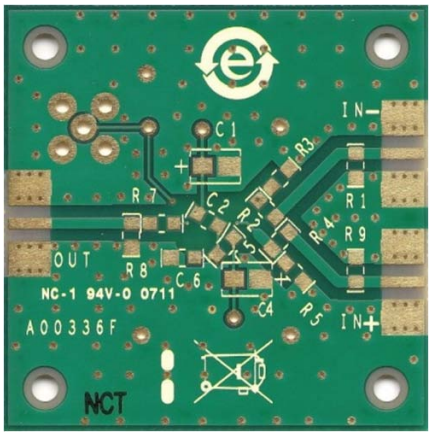
EVALUATION BOARD COMPONENT AND CIRCUIT SIDES



NOTES
1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELING ON THE BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

08885-001

Figure 1. Component Side of Evaluation Board



NOTES
1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELING ON THE BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

08885-002

Figure 2. Circuit Side of Evaluation Board

TABLE OF CONTENTS

REVISION HISTORY

4/11—Rev. 0 to Rev. A

Changes to Product Title, General Description Section, Figure 1, and Figure 2 1
Changed Evaluation Board Schematic, Assembly Drawings, and Layout Patterns Section to Evaluation Board Schematic Section 3
Added Evaluation Board Assembly Drawings and Layout Patterns Section 4
Changes to Figure 4 through Figure 7 4

3/10—Revision 0: Initial Version

EVALUATION BOARD SCHEMATIC

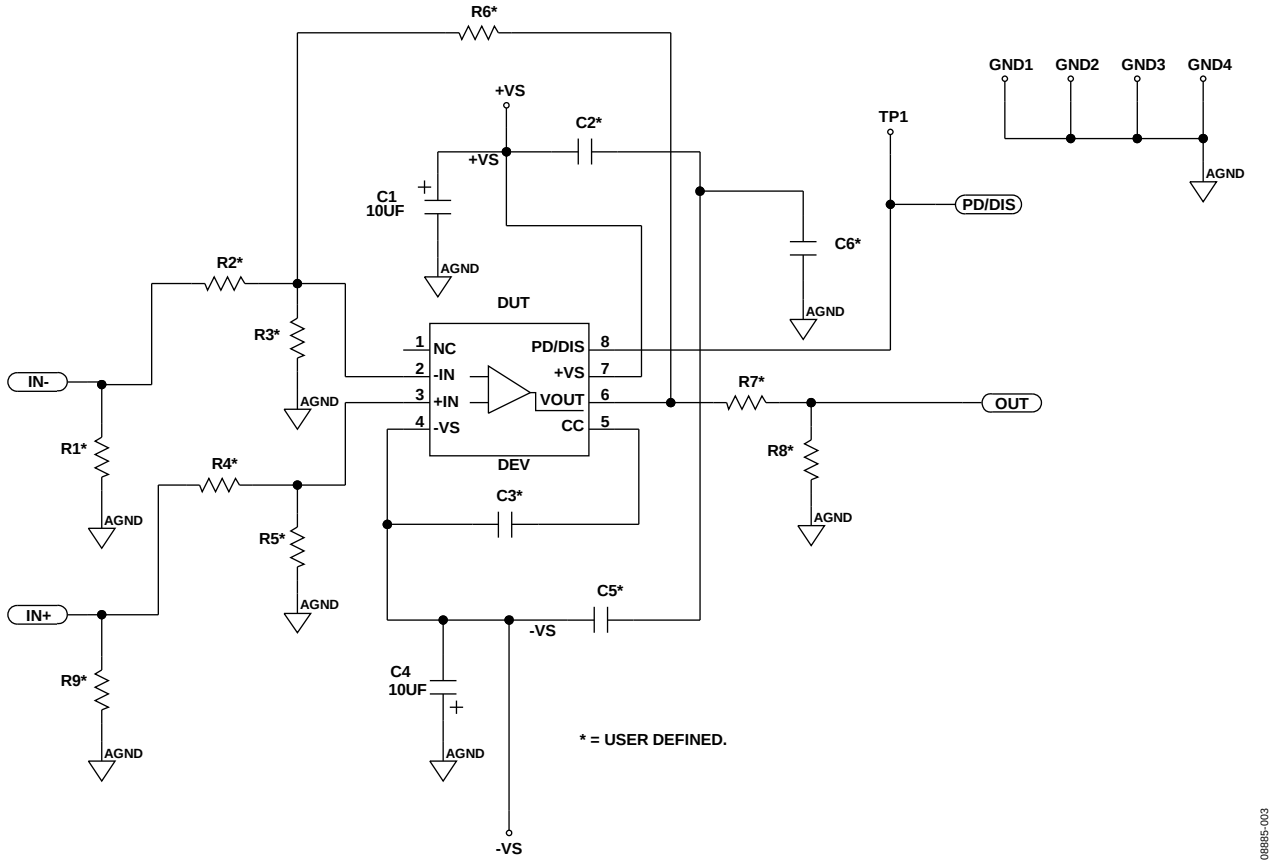


Figure 3. 8-Lead SOIC Evaluation Board Schematic

EVALUATION BOARD ASSEMBLY DRAWINGS AND LAYOUT PATTERNS

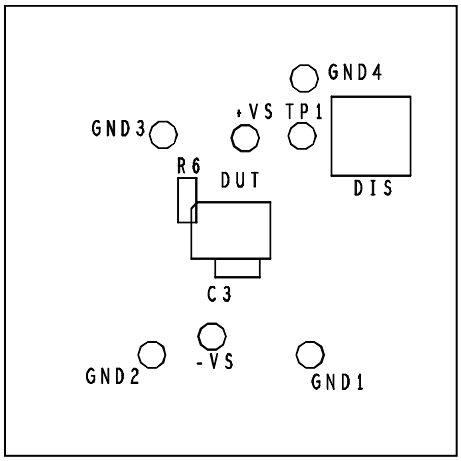


Figure 4. Component Side Assembly Drawing

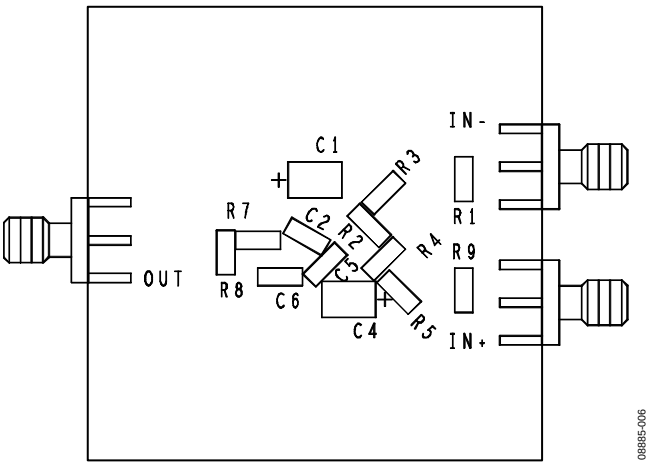


Figure 6. Circuit Side Assembly Drawing

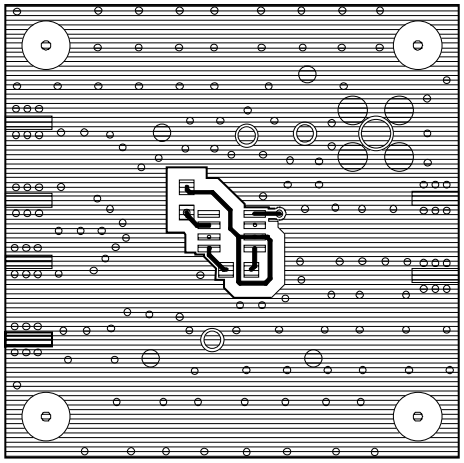


Figure 5. Component Side Layout Pattern

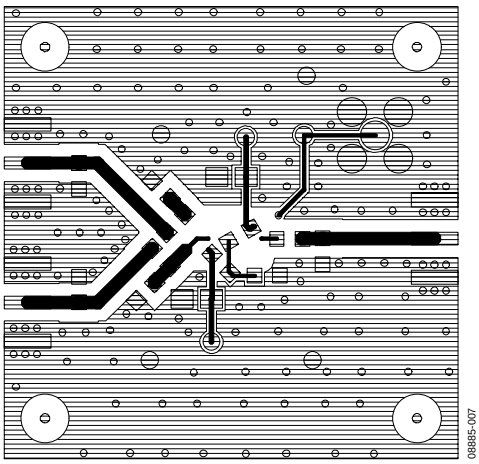


Figure 7. Circuit Side Layout Pattern

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Quantity	Reference Designator	Description	Package
7	+VS, −VS, GND1, GND2, GND3, GND4, TP1	Test point	TP
2	C1, C4	10 µF capacitor	3528
4	C2, C3, C5, C6	Capacitor, user defined	C1206
1	DUT	DEV, SO8_SPEC	8-lead SOIC
4	PD/DIS, IN+, IN−, OUT	SMA/SMT	SMA/SMT
9	R1, R2, R3, R4, R5, R6, R7, R8, R9	Resistor, user defined	R1206

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ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG08885-0-4/11(A)

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