5 kV RMS Quad-Channel Digital Isolators

Automotive Products

ADuM4400W/ADuM4401W/ADuM4402W

FEATURES

Enhanced system-level ESD performance per IEC 61000-4-x
Safety and regulatory approvals
- UL recognition: 5000 V rms for 1 minute per UL 1577
- CSA Component Acceptance Notice #5A
  - IEC 60950-1: 380 V rms (reinforced)
- VDE Certificate of Conformity
- DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - V_{IORM} = 849 V peak

Low power operation
- 5 V operation
  - 1.4 mA per channel maximum @ 0 Mbps to 1 Mbps
  - 4.3 mA per channel maximum @ 10 Mbps
- 3.3 V operation
  - 0.9 mA per channel maximum @ 0 Mbps to 1 Mbps
  - 2.4 mA per channel maximum @ 10 Mbps

Bidirectional communication
3.3 V/5 V level translation
High temperature operation: 125°C
High data rate: dc to 10 Mbps (NRZ)
Precise timing characteristics
- 3.5 ns maximum pulse width distortion
- 3.5 ns maximum channel-to-CHANNEL matching

High common-mode transient immunity: >25 kV/μs
Output enable function
16-lead SOIC wide body package (RW-16)
Qualified for automotive applications

APPLICATIONS

Hybrid electric vehicles
Battery monitor
Motor drive

GENERAL DESCRIPTION

The ADuM4400W/ADuM4401W/ADuM4402W[1] are 4-channel digital isolators based on the Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics that are superior to the alternatives, such as optocoupler devices and other integrated couplers.

The ADuM4400W/ADuM4401W/ADuM4402W isolators provide four independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). All models operate with the supply voltage on either side ranging from 3.135 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. The ADuM4400W/ADuM4401W/ADuM4402W isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

This family of isolators, like many Analog Devices isolators, offers very low power consumption, consuming one-tenth to one-sixth the power of comparable isolators at comparable data rates up to 10 Mbps. All models of the ADuM4400W/ADuM4401W/ADuM4402W provide low pulse width distortion (<3.5 ns for WB grade). In addition, every model has an input glitch filter to protect against extraneous noise disturbances.

The ADuM4400W/ADuM4401W/ADuM4402W contain circuit and layout enhancements to help achieve system-level IEC 61000-4-x compliance (ESD/burst/ surge). The precise capability in these tests for the ADuM4400W/ADuM4401W/ADuM4402W are strongly determined by the design and layout of the user's board or module. For more information, see the AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products*.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329.

FUNCTIONAL BLOCK DIAGRAMS

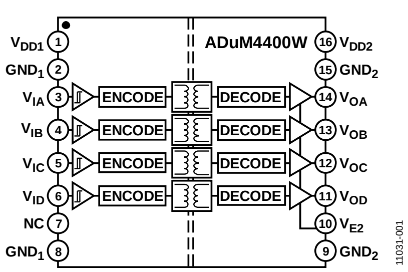

Figure 1. ADuM4400W

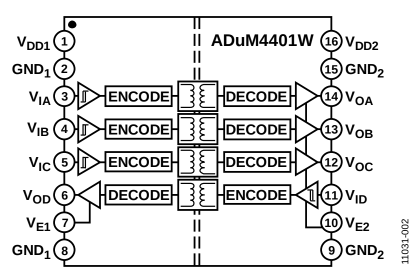

Figure 2. ADuM4401W

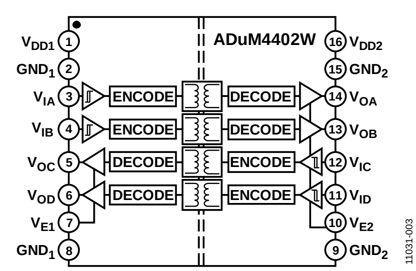

Figure 3. ADuM4402W

Rev. A

Document Feedback

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REVISION HISTORY

3/15—Rev.0 to Rev. A

Change to Minimum Supply Voltage Parameter (Throughout) .. 1

11/12—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at $T_A = 25°C$, $V_{DD1} = V_{DD2} = 5$ V. Minimum/maximum specifications apply over the entire recommended operation range of $4.5\ V \leq V_{DD1} \leq 5.5\ V$, $4.5\ V \leq V_{DD2} \leq 5.5\ V$, and $-40°C \leq T_A \leq 125°C$, unless otherwise noted. Switching specifications are tested with $C_L = 15$ pF and CMOS signal levels, unless otherwise noted.

Table 1.

Parameter	Symbol	WA Grade Min	WA Grade Typ	WA Grade Max	WB Grade Min	WB Grade Typ	WB Grade Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	50	65	100	18	32	36	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			3.5	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			11			5		ps/°C	
Pulse Width	PW	1000			100			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			50			15	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			50			3.5	ns	
Opposing-Direction	t_{PSKOD}			50			6	ns	

Table 2.

Parameter	Symbol	1 Mbps—WA, WB Grades Min	1 Mbps—WA, WB Grades Typ	1 Mbps—WA, WB Grades Max	10 Mbps—WB Grade Min	10 Mbps—WB Grade Typ	10 Mbps—WB Grade Max	Unit	Test Conditions/Comments
SUPPLY CURRENT									
ADuM4400W	I_{DD1}		2.9	3.5		9.0	11.6	mA	
	I_{DD2}		1.2	2.0		3.0	5.5	mA	
ADuM4401W	I_{DD1}		2.5	3.2		7.4	10.6	mA	
	I_{DD2}		1.6	2.4		4.4	6.5	mA	
ADuM4402W	I_{DD1}		2.0	2.8		6.0	7.5	mA	
	I_{DD2}		2.0	2.8		6.0	7.5	mA	

Table 3. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	2.0			V	
Logic Low Input Threshold	V_{IL}			0.8	V	
Logic High Output Voltage	V_{OH}	$V_{DDx} - 0.1$	5.0		V	$I_{Ox} = -20\ \mu A$, $V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.4$	4.8		V	$I_{Ox} = -4$ mA, $V_{Ix} = V_{IxH}$
Logic Low Output Voltage	V_{OL}		0.0	0.1	V	$I_{Ox} = 20\ \mu A$, $V_{Ix} = V_{IxL}$
			0.04	0.1	V	$I_{Ox} = 400\ \mu A$, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	$I_{Ox} = 4$ mA, $V_{Ix} = V_{IxL}$
Input Current per Channel	I_I	−10	+0.01	+10	μA	$0\ V \leq V_{Ix} \leq V_{DDx}$
VE_x Input Pull-up Current	I_{PU}	−10	−3		μA	$VE_x = 0$ V
Tristate Leakage Current per Channel	I_{OZ}	−10	+0.01	+10	μA	
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.57	0.83	mA	All data inputs at logic low
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.23	0.35	mA	All data inputs at logic low
Dynamic Input Supply Current	$I_{DDI(D)}$		0.20		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	$V_{Ix} = V_{DDx}$, $V_{CM} = 1000$ V, transient magnitude = 800 V
Output Disable Propagation Delay	t_{PHZ}, t_{PLH}		6	8	ns	High/low-to-high impedance
Output Enable Propagation Delay	t_{PZH}, t_{PZL}		6	8	ns	High impedance-to-high/low
Refresh Rate	f_r		1.0		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{Ox} > 0.8\ V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at $T_A = 25°C$, $V_{DD1} = V_{DD2} = 3.3$ V. Minimum/maximum specifications apply over the entire recommended operation range: $3.135 \text{ V} \leq V_{DD1} \leq 3.6$ V, $3.135 \text{ V} \leq V_{DD2} \leq 3.6$ V, and $-40°C \leq T_A \leq 125°C$, unless otherwise noted. Switching specifications are tested with $C_L = 15$ pF and CMOS signal levels, unless otherwise noted.

Table 4.

Parameter	Symbol	WA Grade Min	WA Grade Typ	WA Grade Max	WB Grade Min	WB Grade Typ	WB Grade Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	50	75	100	20	38	45	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			3.5	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			11			5		ps/°C	
Pulse Width	PW	1000			100			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			50			22	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			50			3.5	ns	
Opposing-Direction	t_{PSKOD}			50			6	ns	

Table 5.

Parameter	Symbol	1 Mbps—WA, WB Grades Min	1 Mbps—WA, WB Grades Typ	1 Mbps—WA, WB Grades Max	10 Mbps—WB Grade Min	10 Mbps—WB Grade Typ	10 Mbps—WB Grade Max	Unit	Test Conditions/Comments
SUPPLY CURRENT									
ADuM4400W	I_{DD1}		1.6	2.2		4.8	7.1	mA	
	I_{DD2}		0.7	1.4		1.8	2.6	mA	
ADuM4401W	I_{DD1}		1.4	2.0		0.1	5.6	mA	
	I_{DD2}		0.9	1.6		2.5	3.3	mA	
ADuM4402W	I_{DD1}		1.2	1.8		3.3	4.4	mA	
	I_{DD2}		1.2	1.8		3.3	4.4	mA	

Table 6. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	1.6			V	
Logic Low Input Threshold	V_{IL}			0.4	V	
Logic High Output Voltage	V_{OH}	$V_{DDx} - 0.1$	3.0		V	$I_{Ox} = -20$ µA, $V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.4$	2.8		V	$I_{Ox} = -4$ mA, $V_{Ix} = V_{IxH}$
Logic Low Output Voltage	V_{OL}		0.0	0.1	V	$I_{Ox} = 20$ µA, $V_{Ix} = V_{IxL}$
			0.04	0.1	V	$I_{Ox} = 400$ µA, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	$I_{Ox} = 4$ mA, $V_{Ix} = V_{IxL}$
Input Current per Channel	I_I	−10	+0.01	+10	µA	$0 \text{ V} \leq V_{Ix} \leq V_{DDx}$
VE_x Input Pull-up Current	I_{PU}	−10	−3		µA	$VE_x = 0$ V
Tristate Leakage Current per Channel	I_{OZ}	−10	+0.01	+10	µA	
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.31	0.49	mA	All data inputs at logic low
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.19	0.27	mA	All data inputs at logic low
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		3		ns	10% to 90%
Common-Mode Transient Immunity[1]	$\lvert CM \rvert$	25	35		kV/µs	$V_{Ix} = V_{DDx}$, $V_{CM} = 1000$ V, transient magnitude = 800 V
Output Disable Propagation Delay	t_{PHZ}, t_{PLH}		6	8	ns	High/low-to-high impedance
Output Enable Propagation Delay	t_{PZH}, t_{PZL}		6	8	ns	High impedance-to-high/low
Refresh Rate	f_r		1.0		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{Ox} > 0.8 V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.135 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ 125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 7.

Parameter	Symbol	WA Grade Min	WA Grade Typ	WA Grade Max	WB Grade Min	WB Grade Typ	WB Grade Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	50	70	100	20	30	42	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			3.5	ns	$\|t_{PLH} − t_{PHL}\|$
Change vs. Temperature			11			5		ps/°C	
Pulse Width	PW	1000			100			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			50			22	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			50			3.5	ns	
Opposing-Direction	t_{PSKOD}			50			6	ns	

Table 8.

Parameter	Symbol	1 Mbps—WA, WB Grades Min	1 Mbps—WA, WB Grades Typ	1 Mbps—WA, WB Grades Max	10 Mbps—WB Grade Min	10 Mbps—WB Grade Typ	10 Mbps—WB Grade Max	Unit	Test Conditions/Comments
SUPPLY CURRENT									
ADuM4400W	I_{DD1}		2.9	3.5		9.0	11.6	mA	
	I_{DD2}		0.7	1.4		1.8	2.6	mA	
ADuM4401W	I_{DD1}		2.5	3.2		7.4	10.6	mA	
	I_{DD2}		0.9	1.6		2.5	3.3	mA	
ADuM4402W	I_{DD1}		2.0	2.8		6.0	7.5	mA	
	I_{DD2}		1.2	1.8		3.3	4.4	mA	

Table 9. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
5 V Logic High Input Threshold	V_{IH}	2.0			V	
3.3 V Logic High Input Threshold	V_{IH}	1.6			V	
5 V Logic Low Input Threshold	V_{IL}			0.8	V	
3.3 V Logic Low Input Threshold	V_{IL}			0.4	V	
Logic High Output Voltage	V_{OH}	V_{DDx} − 0.1	3.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.4	2.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltage	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
VE_x Input Pull-up Current	I_{PU}	−10	−3		µA	VE_x = 0 V
Tristate Leakage Current per Channel	I_{OZ}	−10	+0.01	+10	µA	
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.57	0.83	mA	All data inputs at logic low
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.29	0.27	mA	All data inputs at logic low
Dynamic Input Supply Current	$I_{DDI(D)}$		0.20		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		3		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Output Disable Propagation Delay	t_{PHZ}, t_{PLH}		6	8	ns	High/low-to-high impedance
Output Enable Propagation Delay	t_{PZH}, t_{PZL}		6	8	ns	High impedance-to-high/low
Refresh Rate	f_r		1.0		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{Ox} > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V, V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.135 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 10.

		WA Grade			WB Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS									
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	50	70	100	20	30	42	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			3.5	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			11			5		ps/°C	
Pulse Width	PW	1000			100			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			50			22	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			50			3.5	ns	
Opposing-Direction	t_{PSKOD}			50			6	ns	

Table 11.

		1 Mbps—WA,W B Grades			10 Mbps—WB Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SUPPLY CURRENT									
ADuM4400W	I_{DD1}		1.6	2.2		4.8	7.1	mA	
	I_{DD2}		1.2	2.0		3.0	5.5	mA	
ADuM4401W	I_{DD1}		1.4	2.0		4.1	5.6	mA	
	I_{DD2}		1.6	2.4		4.4	6.5	mA	
ADuM4402W	I_{DD1}		1.2	1.8		3.3	4.4	mA	
	I_{DD2}		2.0	2.8		6.0	7.5	mA	

Table 12. For All Models

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DC SPECIFICATIONS						
5 V Logic High Input Threshold	V_{IH}	2.0			V	
3.3 V Logic High Input Threshold		1.6			V	
5 V Logic Low Input Threshold	V_{IL}			0.8	V	
3.3 V Logic Low Input Threshold				0.4		
Logic High Output Voltage	V_{OH}	$V_{DDx} - 0.1$	5.0		V	I_{Ox} = −20 µA, $V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.4$	4.8		V	I_{Ox} = −4 mA, $V_{Ix} = V_{IxH}$
Logic Low Output Voltage	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, $V_{Ix} = V_{IxL}$
			0.04	0.1	V	I_{Ox} = 400 µA, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	I_{Ox} = 4 mA, $V_{Ix} = V_{IxL}$
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
VE_x Input Pull-up Current	I_{PU}	−10	−3		µA	VE_x = 0 V
Tristate Leakage Current per Channel	I_{OZ}	−10	+0.01	+10	µA	
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.31	0.49	mA	All data inputs at logic low
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.19	0.35	mA	All data inputs at logic low
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
Output Disable Propagation Delay	t_{PHZ}, t_{PLH}		6	8	ns	High/low-to-high impedance
Output Enable Propagation Delay	t_{PZH}, t_{PZL}		6	8	ns	High impedance-to-high/low
Refresh Rate	f_r		1.0		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{Ox} > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 13.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to- Ambient Thermal Resistance	$θ_{JA}$		45		°C/W	

[1] Device considered a 2-terminal device: Pin 1 to Pin 8 shorted together and Pin 9 to Pin 16 shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM4400W/ADuM4401W/ADuM4402W are approved by the organizations listed in Table 14. Refer to Table 19 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 14.

UL	CSA	VDE
Recognized under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12[2]
Single Protection 5000 V rms Isolation Voltage	Basic insulation per CSA 60950-1-07 and IEC 60950-1, 600 V rms (848 V peak) maximum working voltage Reinforced insulation per CSA 60950-1-07 and IEC 60950-1, 380 V rms (537 V peak) maximum working voltage; reinforced insulation per IEC 60601-1 125 V rms (176 V peak) maximum working voltage	Reinforced insulation, 849 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL1577, each ADuM4400W/ADuM4401W/ADuM4402W is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM4400W/ADuM4401W/ADuM4402W is proof tested by applying an insulation test voltage ≥1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 15.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.0 min	mm	Distance measured from input terminals to output terminals, shortest distance through air along the PCB mounting plane, as an aid to PC board layout
Minimum External Tracking (Creepage)	L(I02)	7.7 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits.

Note that the * marking on packages denotes DIN V VDE V 0884-10 approval for 846 V peak working voltage.

Table 16.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V peak
Input-to-Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, $t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V peak
Input-to-Output Test Voltage, Method a		$V_{pd(m)}$		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC		1273	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC		1018	V peak
Highest Allowable Overvoltage	Transient overvoltage, $t_{TR} = 10$ seconds	V_{IOTM}	6000	V peak
Surge Isolation Voltage	$V_{PEAK} = 10$ kV, 1.2 μs rise time, 50 μs, 50% fall time	V_{IOSM}	6000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure; see Figure 4			
Maximum Junction Temperature		T_S	150	°C
Safety Total Dissipated Power		P_S	0.56	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

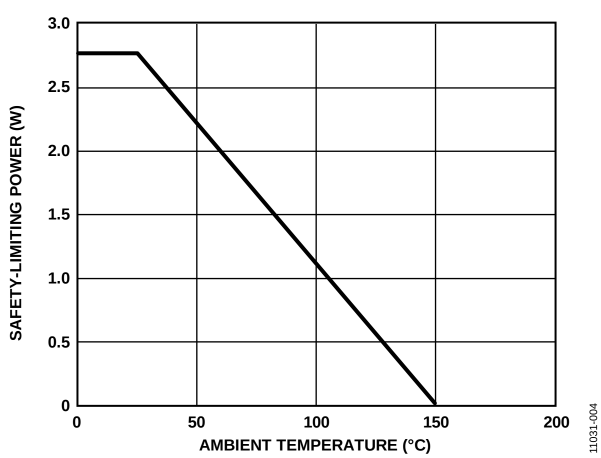


Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 17.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+125	°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	3.135	5.5	V
Input Signal Rise and Fall Times			1.0	ms

[1] All voltages are relative to their respective ground.

ABSOLUTE MAXIMUM RATINGS

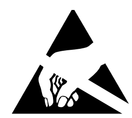
Table 18.

Parameter	Rating
Storage Temperature (T_{ST})	−65°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})[1]	−0.5 V to +7.0 V
Input Voltage (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{E1}, V_{E2})[1, 2]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB}, V_{OC}, V_{OD})[1, 2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current Per Pin[3]	
Side 1 (I_{O1})	−18 mA to +18 mA
Side 2 (I_{O2})	−22 mA to +22 mA
Common-Mode Transients[4]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the PC Board Layout section.
[3] See Figure 4 for maximum rated current values for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 19. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50 year minimum lifetime
AC Voltage, Unipolar Waveform			
Reinforced Insulation	846	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10
DC Voltage			
Reinforced Insulation	846	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10

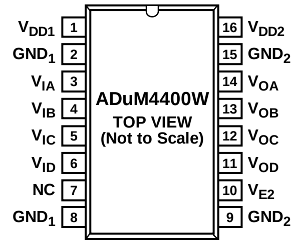
[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Table 20. Truth Table (Positive Logic)

V_{Ix} Input[1]	V_{Ex} Input	V_{DDI} State[1]	V_{DDO} State[1]	V_{Ox} Output[1]	Notes
H	H or NC	Powered	Powered	H	
L	H or NC	Powered	Powered	L	
X	L	Powered	Powered	Z	
X	H or NC	Unpowered	Powered	H	Outputs return to input state within 1 µs of V_{DDI} power restoration.
X	L	Unpowered	Powered	Z	
X	X	Powered	Unpowered	Indeterminate	Outputs return to input state within 1 µs of V_{DDO} power restoration if V_{Ex} state is H or NC. Outputs return to high impedance state within 8 ns of V_{DDO} power restoration if V_{Ex} state is L.

[1] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, or D). V_{Ex} refers to the output enable signal on the same side as the V_{Ox} outputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



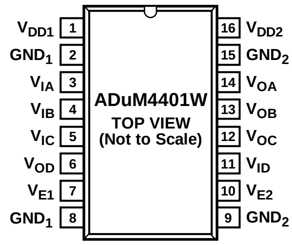
NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.
2. PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND_1 IS RECOMMENDED.
3. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND_2 IS RECOMMENDED.

11031-005

Figure 5. ADuM4400W Pin Configuration

Table 21. ADuM4400W Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 3.135 V to 5.5 V.
2	GND_1	Ground 1. Ground reference for isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{ID}	Logic Input D.
7	NC	This pin is not Connected Internally (see Figure 5).
8	GND_1	Ground 1. Ground reference for isolator Side 1.
9	GND_2	Ground 2. Ground reference for isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. V_{Ox} outputs on Side 2 are enabled when V_{E2} is high or disconnected. V_{Ox} Side 2 outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
11	V_{OD}	Logic Output D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for isolator Side 2.
16	V_{DD2}	Supply Voltage for Isolator Side 2, 3.135 V to 5.5 V.



NOTES
1. PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED, AND CONNECTING BOTHTO GND_1 IS RECOMMENDED.
2. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND_2 IS RECOMMENDED.

11031-006

Figure 6. ADuM4401W Pin Configuration

Table 22. ADuM4401W Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 3.135 V to 5.5 V.
2	GND_1	Ground 1. Ground reference for isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{OD}	Logic Output D.
7	V_{E1}	Output Enable. Active high logic input. V_{Ox} Side 1 outputs are enabled when V_{E1} is high or disconnected. V_{OX} Side 1 outputs are disabled when V_{E1} is low. In noisy environments, connecting V_{E1} to an external logic high or low is recommended.
8	GND_1	Ground 1. Ground reference for isolator Side 1.
9	GND_2	Ground 2. Ground reference for isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. V_{Ox} outputs on Side 2 are enabled when V_{E2} is high or disconnected. V_{Ox} Side 2 outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
11	V_{ID}	Logic Input D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for isolator Side 2.
16	V_{DD2}	Supply Voltage for Isolator Side 2, 3.135 V to 5.5 V.

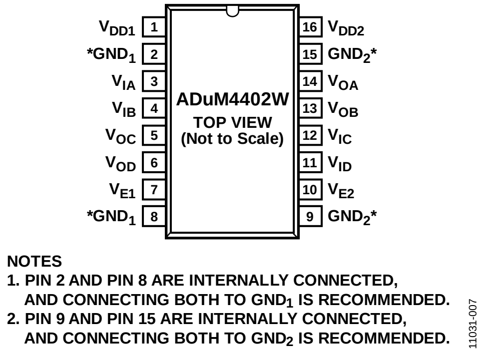


Figure 7. ADuM4402W Pin Configuration

Table 23. ADuM4402W Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 3.135 V to 5.5 V.
2	GND_1	Ground 1. Ground reference for isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{OC}	Logic Output C.
6	V_{OD}	Logic Output D.
7	V_{E1}	Output Enable 1. Active high logic input. V_{Ox} Side 1 outputs are enabled when V_{E1} is high or disconnected. V_{OX} Side 1 outputs are disabled when V_{E1} is low. In noisy environments, connecting V_{E1} to an external logic high or low is recommended.
8	GND_1	Ground 1. Ground reference for isolator Side 1.
9	GND_2	Ground 2. Ground reference for isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. V_{Ox} outputs on Side 2 are enabled when V_{E2} is high or disconnected. V_{Ox} Side 2 outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
11	V_{ID}	Logic Input D.
12	V_{IC}	Logic Input C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for isolator Side 2.
16	V_{DD2}	Supply Voltage for Isolator Side 2, 3.135 V to 5.5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

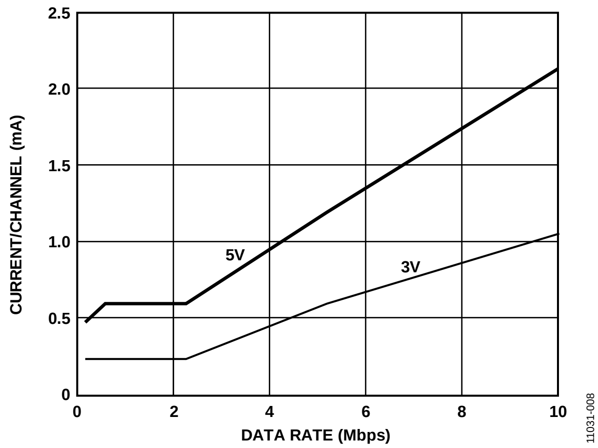


Figure 8. Typical Input Supply Current per Channel vs. Data Rate (No Load)

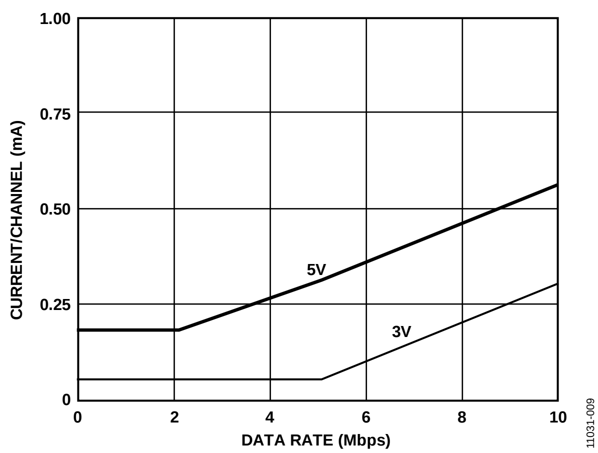


Figure 9. Typical Output Supply Current per Channel vs. Data Rate (No Load)

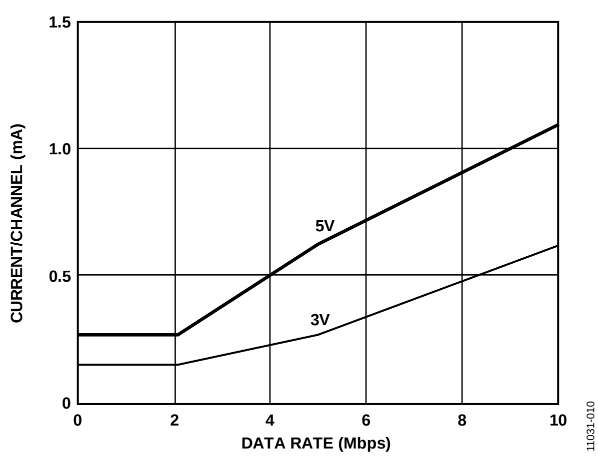


Figure 10. Typical Output Supply Current per Channel vs. Data Rate (15 pF Output Load)

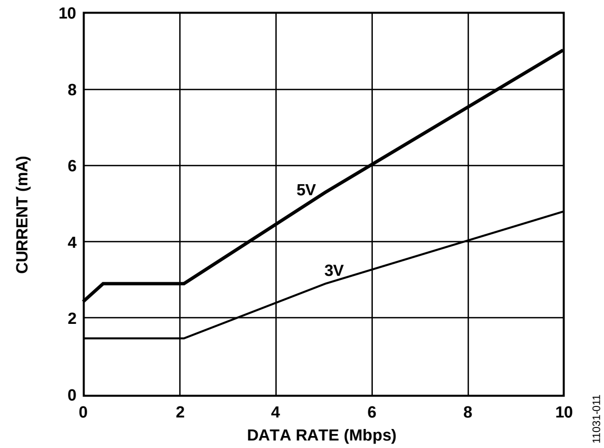


Figure 11. Typical ADuM4400W V_{DD1} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

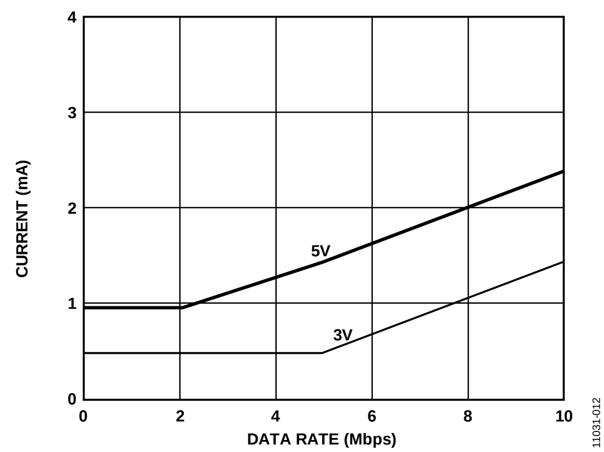


Figure 12. Typical ADuM4400W V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

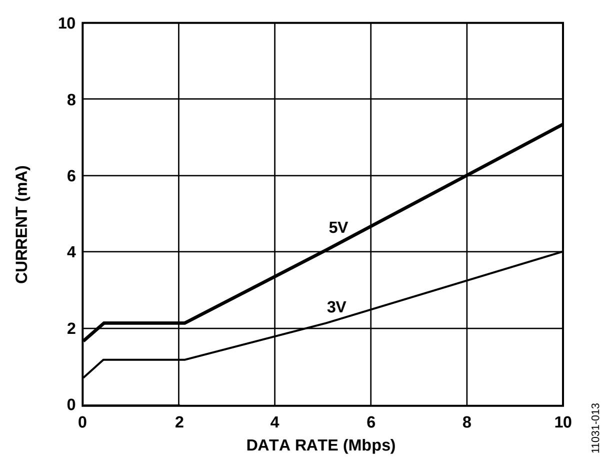


Figure 13. Typical ADuM4401W V_{DD1} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

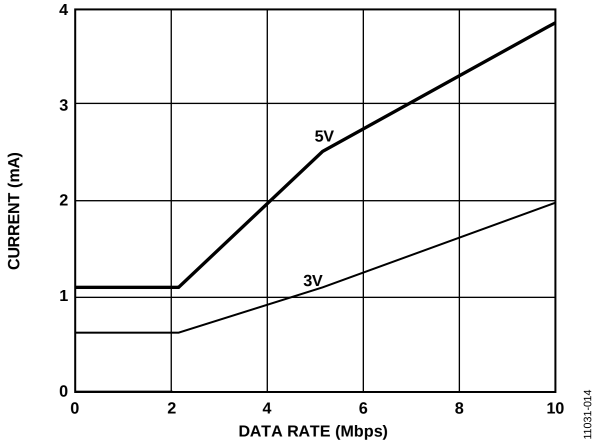


Figure 14. Typical ADuM4401W V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

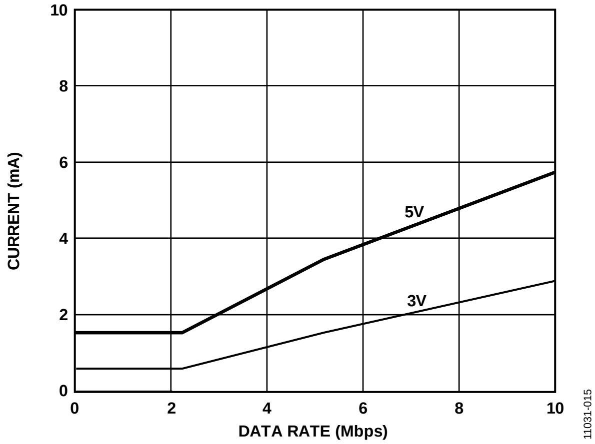


Figure 15. Typical ADuM4402W V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

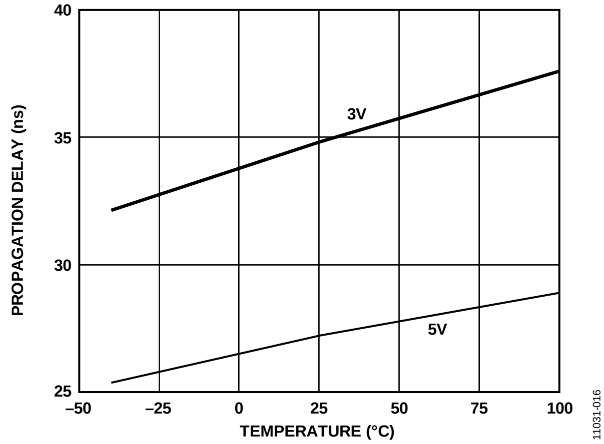


Figure 16. Propagation Delay vs. Temperature, WB Grade

APPLICATIONS INFORMATION

PC BOARD LAYOUT

The ADuM4400W/ADuM4401W/ADuM4402W digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 17). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. The capacitor value should be between 0.01 μF and 0.1 μF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered unless the ground pair on each package side is connected close to the package.

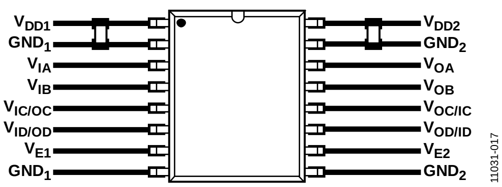


Figure 17. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the Absolute Maximum Ratings of the device, thereby leading to latch-up or permanent damage.

See the AN-1109 Application Note for board layout guidelines.

SYSTEM-LEVEL ESD CONSIDERATIONS AND ENHANCEMENTS

System-level ESD reliability (for example, per IEC 61000-4-x) is highly dependent on system design, which varies widely by application. The ADuM4400W/ADuM4401W/ADuM4402W incorporate many enhancements to make ESD reliability less dependent on system design. The enhancements include:

- ESD protection cells added to all input/output interfaces.
- Key metal trace resistances reduced using wider geometry and paralleling of lines with vias.
- The SCR effect, inherent in CMOS devices, minimized by using guarding and isolation techniques between PMOS and NMOS devices.
- Areas of high electric field concentration eliminated using 45° corners on metal traces.
- Supply pin overvoltage prevented with larger ESD clamps between each supply pin and its respective ground.

While the ADuM4400W/ADuM4401W/ADuM4402W improve system-level ESD reliability, they are no substitute for a robust system-level design. See the AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products*, for detailed recommendations on board layout and system-level design.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the length of time for a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to logic high.

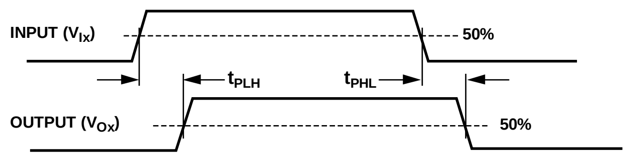


Figure 18. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal's timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs among channels within a single ADuM4400W/ADuM4401W/ADuM4402W component.

Propagation delay skew refers to the maximum amount the propagation delay differs among multiple ADuM4400W/ ADuM4401W/ADuM4402W components operated under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent via the transformer to the decoder. The decoder is bistable and is therefore either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 μs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than approximately 5 μs, the input side is assumed to be without power or nonfunctional; in which case, the isolator output is forced to a default state (see Table 20) by the watchdog timer circuit.

The limitation on the ADuM4400W/ADuM4401W/ ADuM4402W magnetic field immunity is set by the condition in which induced voltage in the trans-former's receiving coil is large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3.3 V operating condition of the ADuM4400W/ ADuM4401W/ADuM4402W is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thereby establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\prod r_n^2;\ n = 1, 2,\ldots, N$$

where:
β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM4400W/ADuM4401W/ADuM4402W and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 19.

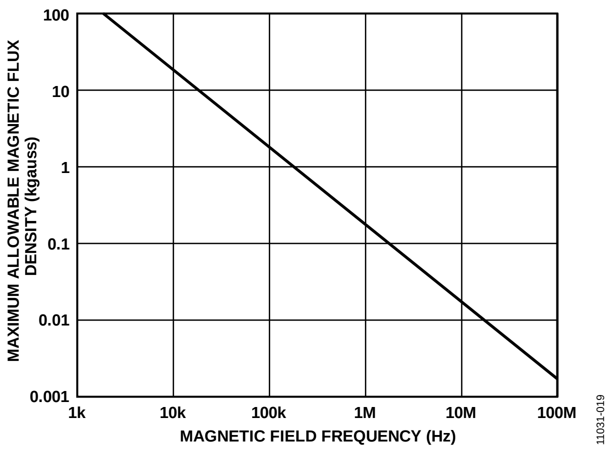


Figure 19. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and was of the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM4400W/ADuM4401W/ADuM4402W transformers. Figure 20 expresses these allowable current magnitudes as a function of frequency for selected distances. As can be seen, the ADuM4400W/ADuM4401W/ADuM4402W are immune and can be affected only by extremely large currents operated at high frequency and very close to the component. For the 1 MHz example noted, one would have to place a 0.5 kA current 5 mm away from the ADuM4400W/ADuM4401W/ADuM4402W to affect the component's operation.

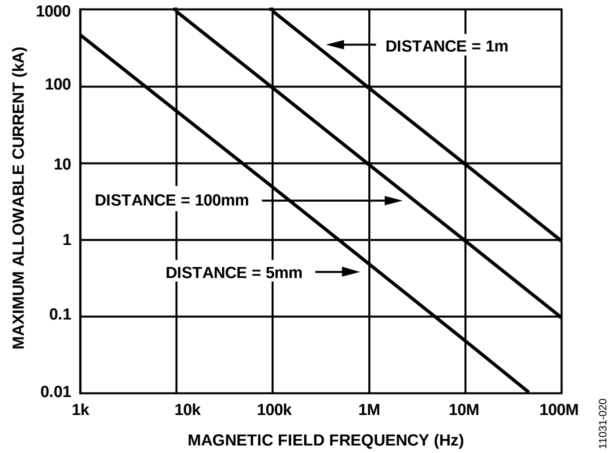


Figure 20. Maximum Allowable Current for Various Current-to-ADuM4400W/ADuM4401W/ADuM4402W Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces may induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM4400W/ADuM4401W/ADuM4402W isolator is a function of the supply voltage, the channel's data rate, and the channel's output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \leq 0.5f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5f_r$$

For each output channel, the supply current is given by:

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \leq 0.5f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f > 0.5f_r$$

where:
$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
C_L is the output load capacitance (pF).
V_{DDO} is the output supply voltage (V).
f is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).
f_r is the input stage refresh rate (Mbps).
$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total I_{DD1} and I_{DD2}, the supply currents for each input and output channel corresponding to I_{DD1} and I_{DD2} are calculated and totaled. Figure 8 and Figure 9 provide per channel supply currents as a function of data rate for an unloaded output condition. Figure 10 provides per channel supply current as a function of data rate for a 15 pF output condition. Figure 11 through Figure 15 provide total I_{DD1} and I_{DD2} as a function of data rate for ADuM4400W/ADuM4401W/ADuM4402W channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM4400W/ADuM4401W/ADuM4402W.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 19 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM4400W/ADuM4401W/ADuM4402W depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates, depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 21, Figure 22, and Figure 23 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 19 can be applied while maintaining the 50-year minimum lifetime, provided the voltage conforms to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 22 or Figure 23 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 19.

Note that the voltage presented in Figure 22 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

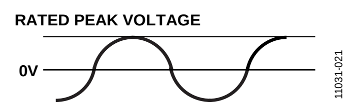


Figure 21. Bipolar AC Waveform

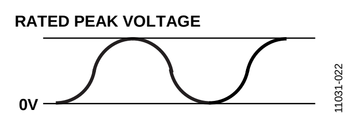


Figure 22. Unipolar AC Waveform

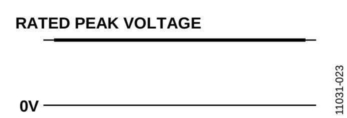


Figure 23. DC Waveform

OUTLINE DIMENSIONS

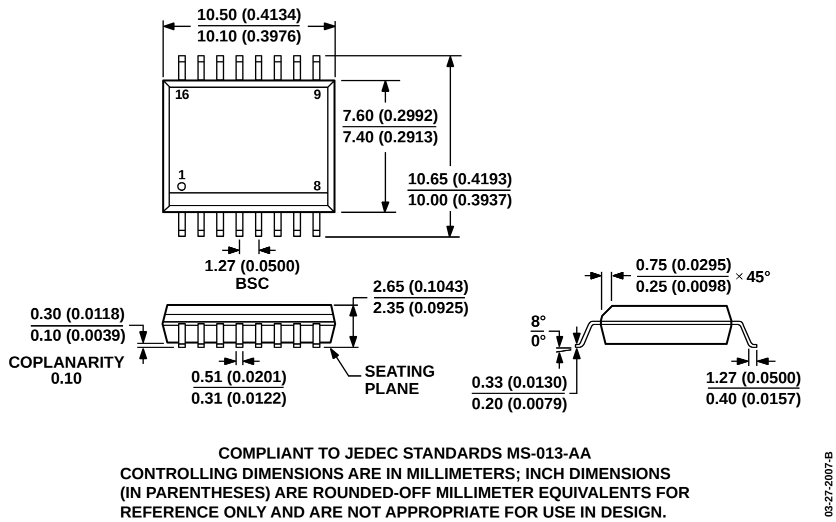


Figure 24. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1, 2, 3]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range	Package Description	Package Option
ADuM4400WARWZ	4	0	1	100	40	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM4400WBRWZ	4	0	10	36	3.5	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM4401WARWZ	3	1	1	100	40	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM4401WBRWZ	3	1	10	36	3.5	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM4402WARWZ	2	2	1	100	40	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM4402WBRWZ	2	2	10	36	3.5	−40°C to +125°C	16-Lead SOIC_W	RW-16

[1] Tape and reel is available. The addition of an -RL suffix designates a 13" (1,000 units) tape and reel option.
[2] Z = RoHS Compliant Part.
[3] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADuM4400W/ADuM4401W/ADuM4402W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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