



# MCP6271/1R/2/3/4/5

## 170 $\mu$ A, 2 MHz Rail-to-Rail Op Amp

### Features

- Gain Bandwidth Product: 2 MHz (typ.)
- Supply Current:  $I_Q = 170 \mu\text{A}$  (typ.)
- Supply Voltage: 2.0V to 5.5V
- Rail-to-Rail Input/Output
- Extended Temperature Range:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$
- Available in Single, Dual and Quad Packages
- Parts with Chip Select ( $\overline{\text{CS}}$ )
  - Single (**MCP6273**)
  - Dual (**MCP6275**)

### Applications

- Automotive
- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery Powered Systems

### Available Tools

- SPICE Macro Model (at [www.microchip.com](http://www.microchip.com))
- FilterLab<sup>®</sup> Software (at [www.microchip.com](http://www.microchip.com))

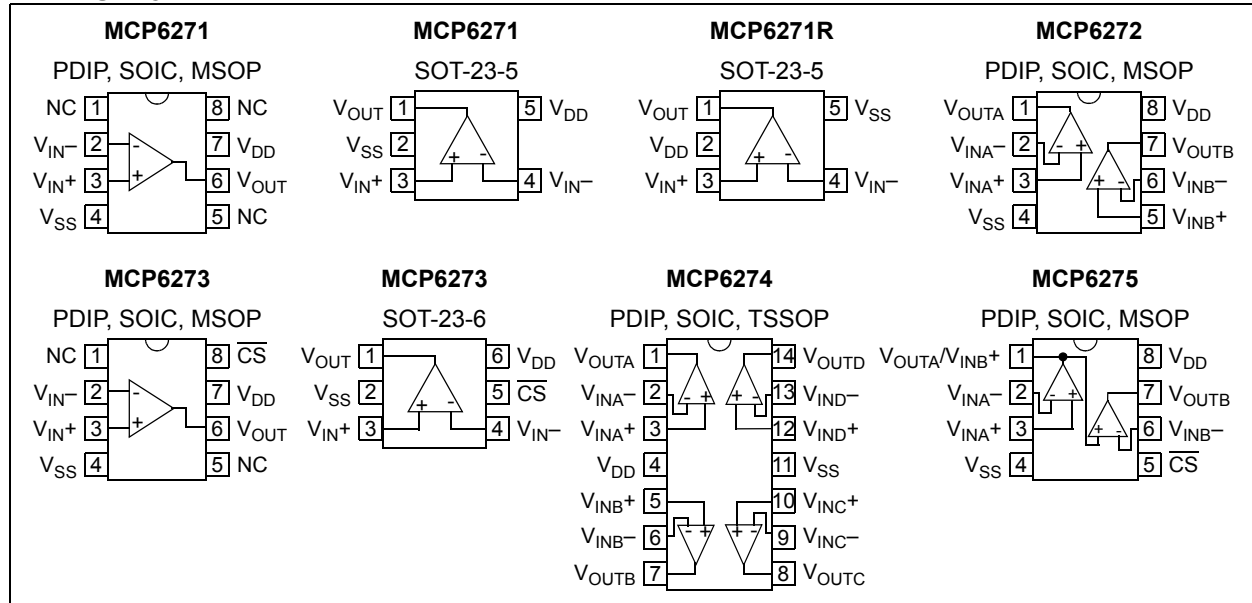
### Description

The Microchip Technology Inc. MCP6271/1R/2/3/4/5 family of operational amplifiers (op amps) provide wide bandwidth for the current. This family has a 2 MHz Gain Bandwidth Product (GBWP) and a  $65^\circ$  Phase Margin. This family also operates from a single supply voltage as low as 2.0V, while drawing 170  $\mu\text{A}$  (typ.) quiescent current. The MCP6271/1R/2/3/4/5 supports rail-to-rail input and output swing, with a common mode input voltage range of  $V_{DD} + 300 \text{ mV}$  to  $V_{SS} - 300 \text{ mV}$ . This family of op amps is designed with Microchip's advanced CMOS process.

The MCP6275 has a Chip Select input ( $\overline{\text{CS}}$ ) for dual op amps in an 8-pin package and is manufactured by cascading two op amps (the output of op amp A connected to the non-inverting input of op amp B). The  $\overline{\text{CS}}$  input puts the device in low power mode.

The MCP6271/1R/2/3/4/5 family operates over the Extended Temperature Range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ , with a power supply range of 2.0V to 5.5V.

### Package Types



# MCP6271/1R/2/3/4/5

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ .....	7.0V
Current at Analog Input Pins ( $V_{IN+}$ and $V_{IN-}$ ) .....	$\pm 2$ mA
Analog Inputs ( $V_{IN+}$ and $V_{IN-}$ ) †† ..	$V_{SS} - 1.0V$ to $V_{DD} + 1.0V$
All other Inputs and Outputs .....	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input Voltage .....	$ V_{DD} - V_{SS} $
Output Short Circuit Current .....	Continuous
Current at Output and Supply Pins .....	$\pm 30$ mA
Storage Temperature .....	$-65^{\circ}C$ to $+150^{\circ}C$
Junction Temperature ( $T_J$ ) .....	$+150^{\circ}C$
ESD Protection On All Pins (HBM/MM) .....	$\geq 4$ kV/400V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See Section 4.1.2 “Input Voltage and Current Limits”.

### DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, $T_A = +25^{\circ}C$ , $V_{DD} = +2.0V$ to $+5.5V$ , $V_{SS} = GND$ , $V_{CM} = V_{DD}/2$ , $V_{OUT} \approx V_{DD}/2$ , $R_L = 10$ k $\Omega$ to $V_{DD}/2$ and $\overline{CS}$ is tied low.						
Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Input Offset (Note 1)</b>						
Input Offset Voltage	$V_{OS}$	-3.0	—	+3.0	mV	$V_{CM} = V_{SS}$
Input Offset Voltage (Extended Temperature)	$V_{OS}$	-5.0	—	+5.0	mV	$T_A = -40^{\circ}C$ to $+125^{\circ}C$ , $V_{CM} = V_{SS}$
Input Offset Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	$\pm 1.7$	—	$\mu V/^{\circ}C$	$T_A = -40^{\circ}C$ to $+125^{\circ}C$ , $V_{CM} = V_{SS}$
Power Supply Rejection Ratio	PSRR	70	90	—	dB	$V_{CM} = V_{SS}$
<b>Input Bias Current and Impedance</b>						
Input Bias Current	$I_B$	—	$\pm 1.0$	—	pA	<b>Note 2</b>
At Temperature	$I_B$	—	50	200	pA	$T_A = +85^{\circ}C$ ( <b>Note 2</b> )
At Temperature	$I_B$	—	2	5	nA	$T_A = +125^{\circ}C$ ( <b>Note 2</b> )
Input Offset Current	$I_{OS}$	—	$\pm 1.0$	—	pA	<b>Note 3</b>
Common Mode Input Impedance	$Z_{CM}$	—	$10^{13}  6$	—	$\Omega  pF$	<b>Note 3</b>
Differential Input Impedance	$Z_{DIFF}$	—	$10^{13}  3$	—	$\Omega  pF$	<b>Note 3</b>
<b>Common Mode (Note 4)</b>						
Common Mode Input Voltage Range	$V_{CMR}$	$V_{SS} - 0.15$	—	$V_{DD} + 0.15$	V	$V_{DD} = 2.0V$ ( <b>Note 5</b> )
	$V_{CMR}$	$V_{SS} - 0.30$	—	$V_{DD} + 0.30$	V	$V_{DD} = 5.5V$ ( <b>Note 5</b> )
Common Mode Rejection Ratio	CMRR	70	85	—	dB	$V_{CM} = -0.3V$ to $2.5V$ , $V_{DD} = 5V$ ( <b>Note 6</b> )
Common Mode Rejection Ratio	CMRR	65	80	—	dB	$V_{CM} = -0.3V$ to $5.3V$ , $V_{DD} = 5V$ ( <b>Note 6</b> )
<b>Open-Loop Gain</b>						
DC Open-Loop Gain (Large Signal)	$A_{OL}$	90	110	—	dB	$V_{OUT} = 0.2V$ to $V_{DD} - 0.2V$ , $V_{CM} = V_{SS}$ ( <b>Note 1</b> )

- Note 1:** The MCP6275's  $V_{CM}$  for op amp B (pins  $V_{OUTA}/V_{INB+}$  and  $V_{INB-}$ ) is  $V_{SS} + 100$  mV.
- Note 2:** The current at the MCP6275's  $V_{INB-}$  pin is specified by  $I_B$  only.
- Note 3:** This specification does not apply to the MCP6275's  $V_{OUTA}/V_{INB+}$  pin.
- Note 4:** The MCP6275's  $V_{INB-}$  pin (op amp B) has a common mode input voltage range ( $V_{CMR}$ ) of  $V_{SS} + 100$  mV to  $V_{DD} - 100$  mV. CMRR is not measured for op amp B of the MCP6275. The MCP6275's  $V_{OUTA}/V_{INB+}$  pin (op amp B) has a voltage range specified by  $V_{OH}$  and  $V_{OL}$ .
- Note 5:** Set by design and characterization.
- Note 6:** Does not apply to op amp B of the MCP6275.

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## DC ELECTRICAL SPECIFICATIONS (CONTINUED)

**Electrical Characteristics:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +2.0\text{V}$  to  $+5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_{DD}/2$  and  $\overline{\text{CS}}$  is tied low.

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Output</b>						
Maximum Output Voltage Swing	$V_{OL}, V_{OH}$	$V_{SS} + 15$	—	$V_{DD} - 15$	mV	0.5V output overdrive ( <b>Note 4</b> )
Output Short Circuit Current	$I_{SC}$	—	$\pm 25$	—	mA	
<b>Power Supply</b>						
Supply Voltage	$V_{DD}$	2.0	—	5.5	V	
Quiescent Current per Amplifier	$I_Q$	100	170	240	$\mu\text{A}$	$I_O = 0$

- Note 1:** The MCP6275's  $V_{CM}$  for op amp B (pins  $V_{OUTA}/V_{INB+}$  and  $V_{INB-}$ ) is  $V_{SS} + 100\text{ mV}$ .
- Note 2:** The current at the MCP6275's  $V_{INB-}$  pin is specified by  $I_B$  only.
- Note 3:** This specification does not apply to the MCP6275's  $V_{OUTA}/V_{INB+}$  pin.
- Note 4:** The MCP6275's  $V_{INB-}$  pin (op amp B) has a common mode input voltage range ( $V_{CMR}$ ) of  $V_{SS} + 100\text{ mV}$  to  $V_{DD} - 100\text{ mV}$ . CMRR is not measured for op amp B of the MCP6275. The MCP6275's  $V_{OUTA}/V_{INB+}$  pin (op amp B) has a voltage range specified by  $V_{OH}$  and  $V_{OL}$ .
- Note 5:** Set by design and characterization.
- Note 6:** Does not apply to op amp B of the MCP6275.

## AC ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +2.0\text{V}$  to  $+5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$  and  $\overline{\text{CS}}$  is tied low.

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>AC Response</b>						
Gain Bandwidth Product	GBWP	—	2.0	—	MHz	
Phase Margin	PM	—	65	—	$^\circ$	$G = +1$
Slew Rate	SR	—	0.9	—	$\text{V}/\mu\text{s}$	
<b>Noise</b>						
Input Noise Voltage	$E_{ni}$	—	4.6	—	$\mu\text{V}_{P-P}$	$f = 0.1\text{ Hz to }10\text{ Hz}$
Input Noise Voltage Density	$e_{ni}$	—	20	—	$\text{nV}/\sqrt{\text{Hz}}$	$f = 1\text{ kHz}$
Input Noise Current Density	$i_{ni}$	—	3	—	$\text{fA}/\sqrt{\text{Hz}}$	$f = 1\text{ kHz}$

## TEMPERATURE SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated,  $V_{DD} = +2.0\text{V}$  to  $+5.5\text{V}$  and  $V_{SS} = \text{GND}$ .

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Temperature Ranges</b>						
Specified Temperature Range	$T_A$	-40	—	+125	$^\circ\text{C}$	
Operating Temperature Range	$T_A$	-40	—	+125	$^\circ\text{C}$	<b>Note</b>
Storage Temperature Range	$T_A$	-65	—	+150	$^\circ\text{C}$	
<b>Thermal Package Resistances</b>						
Thermal Resistance, 5L-SOT-23	$\theta_{JA}$	—	256	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 6L-SOT-23	$\theta_{JA}$	—	230	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 8L-PDIP	$\theta_{JA}$	—	85	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 8L-SOIC	$\theta_{JA}$	—	163	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 8L-MSOP	$\theta_{JA}$	—	206	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 14L-PDIP	$\theta_{JA}$	—	70	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 14L-SOIC	$\theta_{JA}$	—	120	—	$^\circ\text{C}/\text{W}$	
Thermal Resistance, 14L-TSSOP	$\theta_{JA}$	—	100	—	$^\circ\text{C}/\text{W}$	

**Note:** The Junction Temperature ( $T_J$ ) must not exceed the Absolute Maximum specification of  $+150^\circ\text{C}$ .

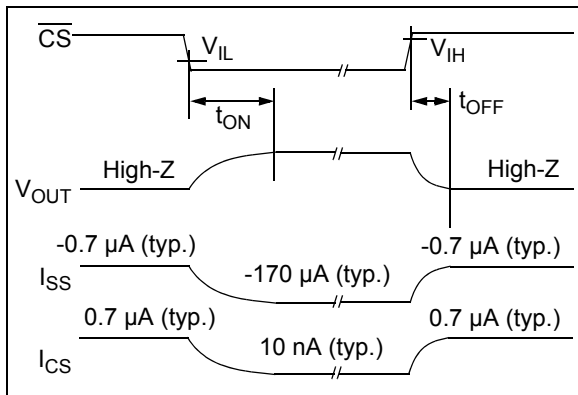
# MCP6271/1R/2/3/4/5

## MCP6273/MCP6275 CHIP SELECT ( $\overline{CS}$ ) SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +2.0\text{V}$  to  $+5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$  and  $\overline{CS}$  is tied low.

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b><math>\overline{CS}</math> Low Specifications</b>						
$\overline{CS}$ Logic Threshold, Low	$V_{IL}$	$V_{SS}$	—	$0.2V_{DD}$	V	
$\overline{CS}$ Input Current, Low	$I_{CSL}$	—	0.01	—	$\mu\text{A}$	$\overline{CS} = V_{SS}$
<b><math>\overline{CS}</math> High Specifications</b>						
$\overline{CS}$ Logic Threshold, High	$V_{IH}$	$0.8V_{DD}$	—	$V_{DD}$	V	
$\overline{CS}$ Input Current, High	$I_{CSH}$	—	0.7	2	$\mu\text{A}$	$\overline{CS} = V_{DD}$
GND Current per Amplifier	$I_{SS}$	—	-0.7	—	$\mu\text{A}$	$\overline{CS} = V_{DD}$
Amplifier Output Leakage	—	—	0.01	—	$\mu\text{A}$	$\overline{CS} = V_{DD}$
<b>Dynamic Specifications (Note 1)</b>						
$\overline{CS}$ Low to Valid Amplifier Output, Turn on Time	$t_{ON}$	—	4	10	$\mu\text{s}$	$\overline{CS}$ Low $\leq 0.2 V_{DD}$ , $G = +1\text{ V/V}$ , $V_{IN} = V_{DD}/2$ , $V_{OUT} = 0.9 V_{DD}/2$ , $V_{DD} = 5.0\text{V}$
$\overline{CS}$ High to Amplifier Output High-Z	$t_{OFF}$	—	0.01	—	$\mu\text{s}$	$\overline{CS}$ High $\geq 0.8 V_{DD}$ , $G = +1\text{ V/V}$ , $V_{IN} = V_{DD}/2$ , $V_{OUT} = 0.1 V_{DD}/2$
Hysteresis	$V_{HYST}$	—	0.6	—	V	$V_{DD} = 5\text{V}$

**Note 1:** The input condition ( $V_{IN}$ ) specified applies to both op amp A and B of the MCP6275. The dynamic specification is tested at the output of op amp B ( $V_{OUTB}$ ).

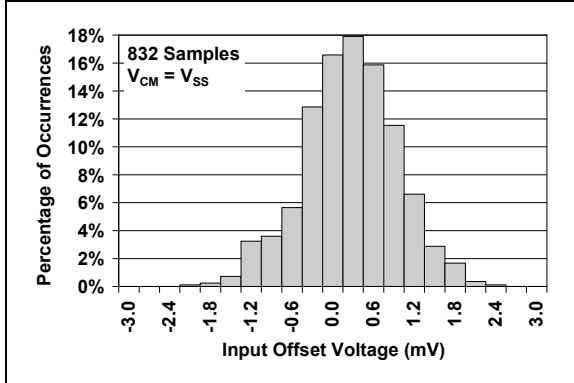


**FIGURE 1-1:** Timing Diagram for the Chip Select ( $\overline{CS}$ ) pin on the MCP6273 and MCP6275.

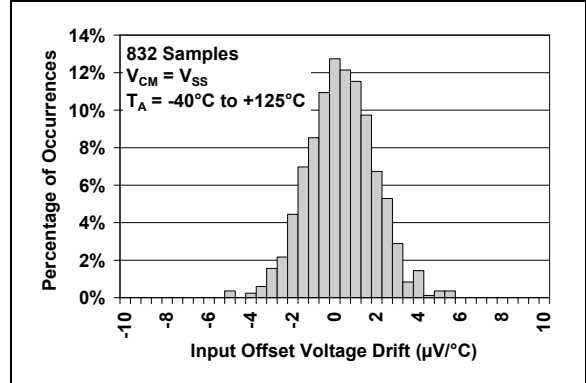
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

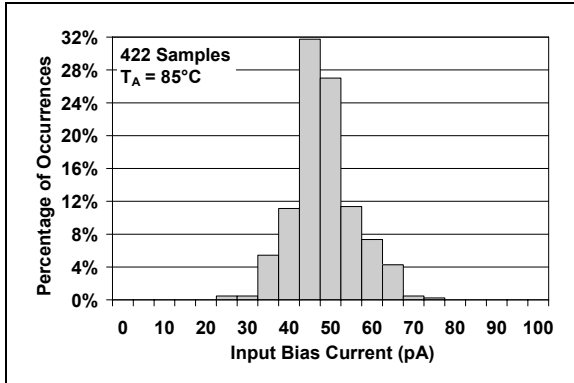
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +2.0\text{V to } +5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$  and  $\overline{\text{CS}}$  is tied low.



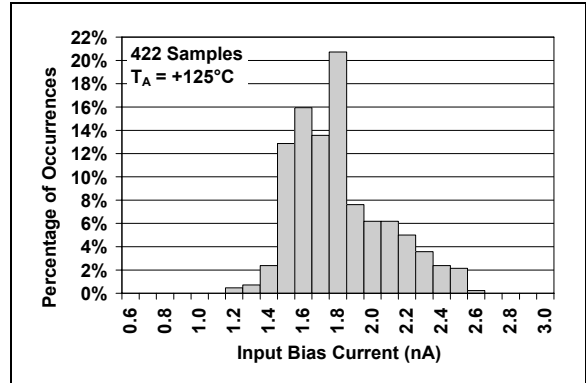
**FIGURE 2-1:** Input Offset Voltage.



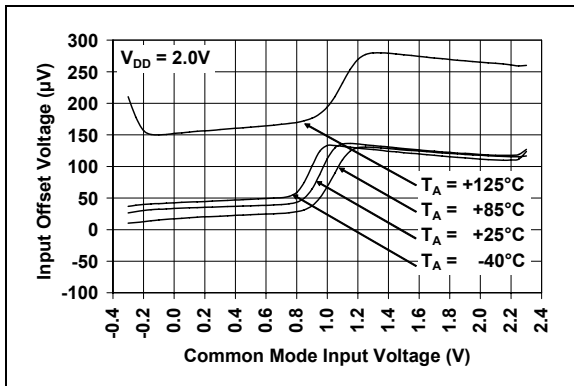
**FIGURE 2-4:** Input Offset Voltage Drift.



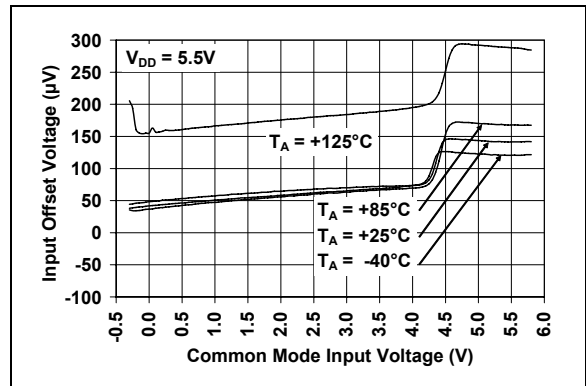
**FIGURE 2-2:** Input Bias Current at  $T_A = +85^\circ\text{C}$ .



**FIGURE 2-5:** Input Bias Current at  $T_A = +125^\circ\text{C}$ .



**FIGURE 2-3:** Input Offset Voltage vs. Common Mode Input Voltage, with  $V_{DD} = 2.0\text{V}$ .

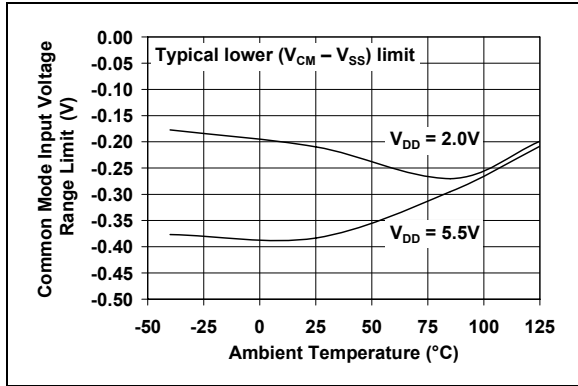


**FIGURE 2-6:** Input Offset Voltage vs. Common Mode Input Voltage, with  $V_{DD} = 5.5\text{V}$ .

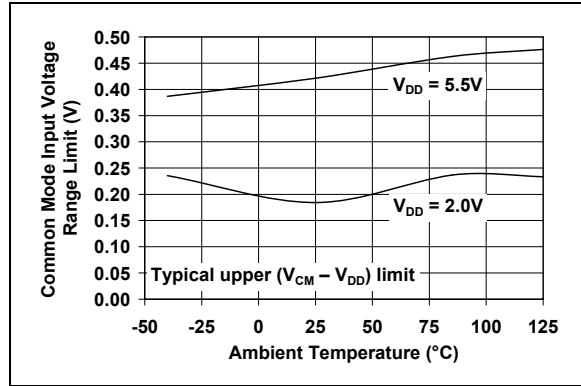
# MCP6271/1R/2/3/4/5

## TYPICAL PERFORMANCE CURVES (Continued)

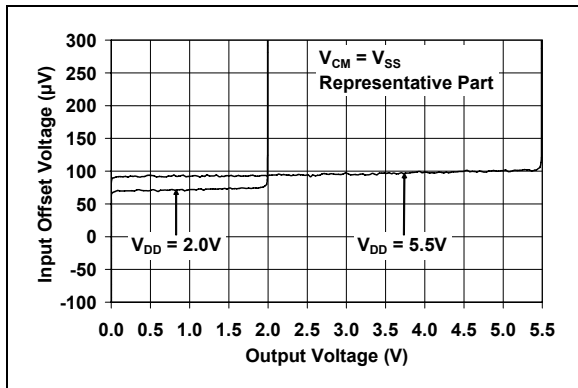
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{CM} = +2.0\text{V}$  to  $+5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$ , and  $\overline{\text{CS}}$  is tied low.



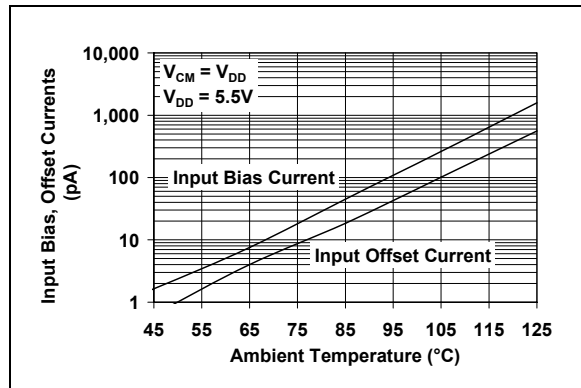
**FIGURE 2-7:** Common Mode Input Voltage Range Lower Limit vs. Temperature.



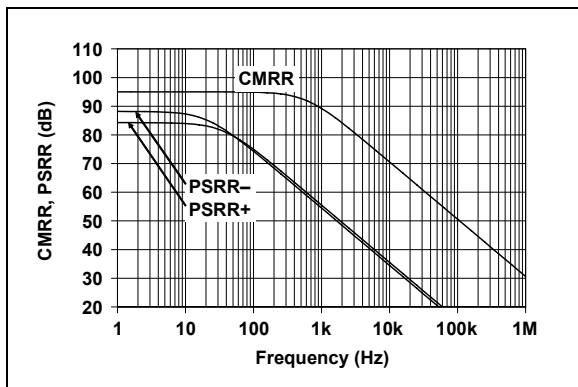
**FIGURE 2-10:** Common Mode Input Voltage Range Upper Limit vs. Temperature.



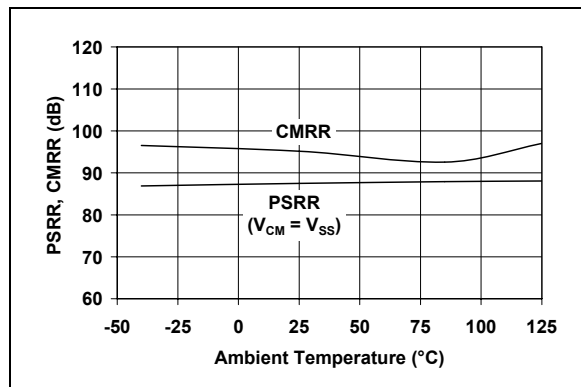
**FIGURE 2-8:** Input Offset Voltage vs. Output Voltage.



**FIGURE 2-11:** Input Bias, Input Offset Currents vs. Temperature.



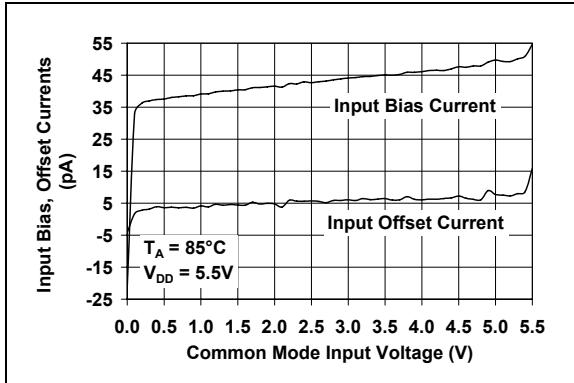
**FIGURE 2-9:** CMRR, PSRR vs. Frequency.



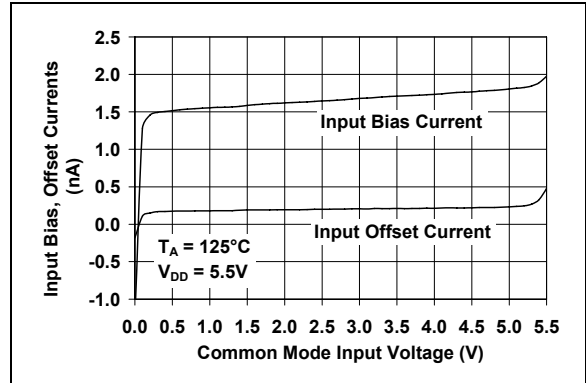
**FIGURE 2-12:** CMRR, PSRR vs. Temperature.

## TYPICAL PERFORMANCE CURVES (Continued)

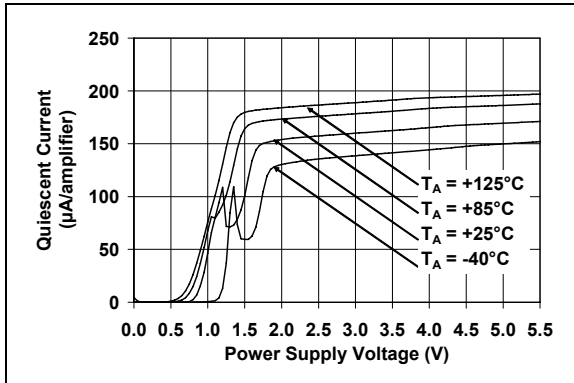
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{\text{CM}} = +2.0\text{V}$  to  $+5.5\text{V}$ ,  $V_{\text{SS}} = \text{GND}$ ,  $V_{\text{CM}} = V_{\text{DD}}/2$ ,  $V_{\text{OUT}} \approx V_{\text{DD}}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_{\text{DD}}/2$ ,  $C_L = 60\text{ pF}$ , and  $\overline{\text{CS}}$  is tied low.



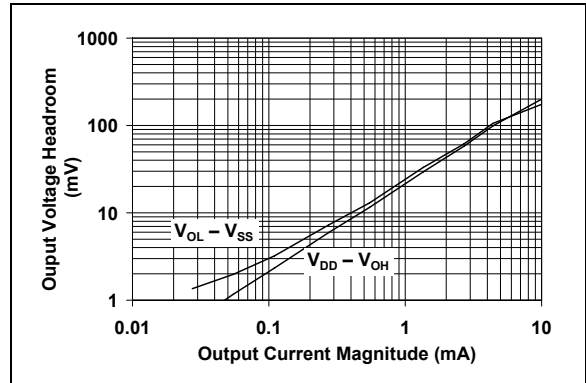
**FIGURE 2-13:** Input Bias, Offset Currents vs. Common Mode Input Voltage, with  $T_A = +85^\circ\text{C}$ .



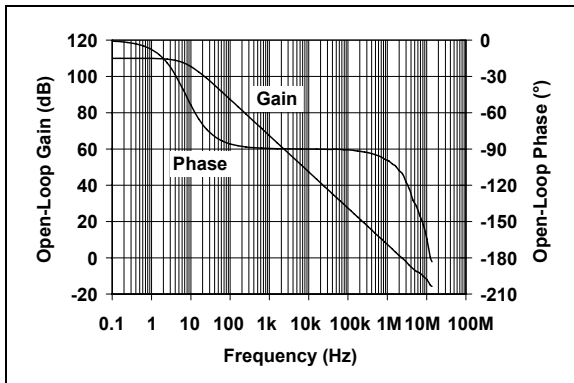
**FIGURE 2-16:** Input Bias, Offset Currents vs. Common Mode Input Voltage, with  $T_A = +125^\circ\text{C}$ .



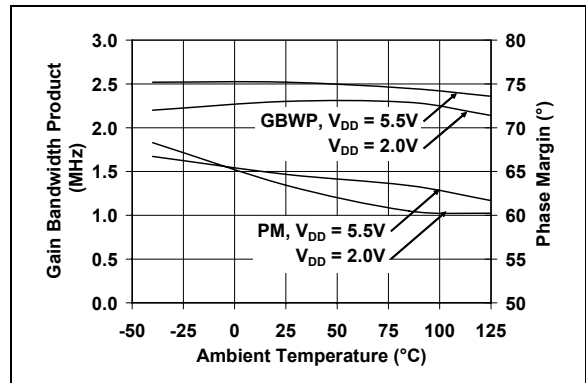
**FIGURE 2-14:** Quiescent Current vs. Supply Voltage.



**FIGURE 2-17:** Output Voltage Headroom vs. Output Current Magnitude.



**FIGURE 2-15:** Open-Loop Gain, Phase vs. Frequency.

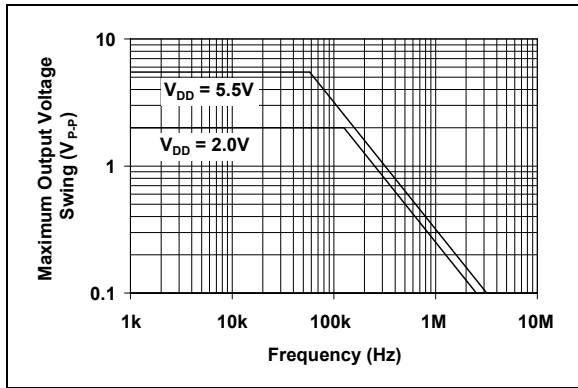


**FIGURE 2-18:** Gain Bandwidth Product, Phase Margin vs. Temperature.

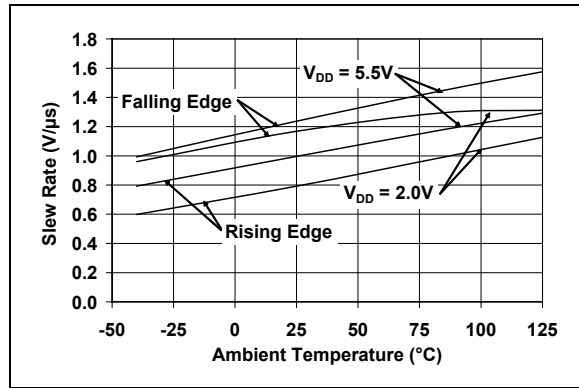
# MCP6271/1R/2/3/4/5

## TYPICAL PERFORMANCE CURVES (Continued)

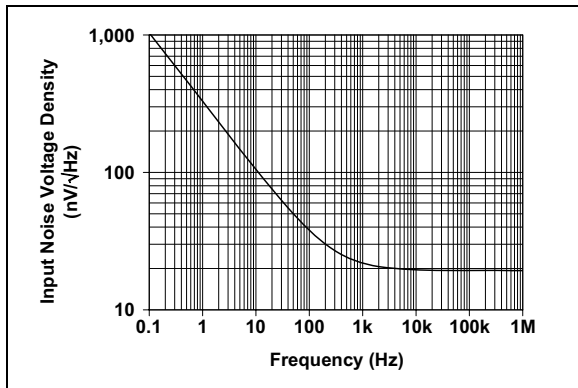
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{CM} = +2.0\text{V}$  to  $+5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$ , and  $\overline{\text{CS}}$  is tied low.



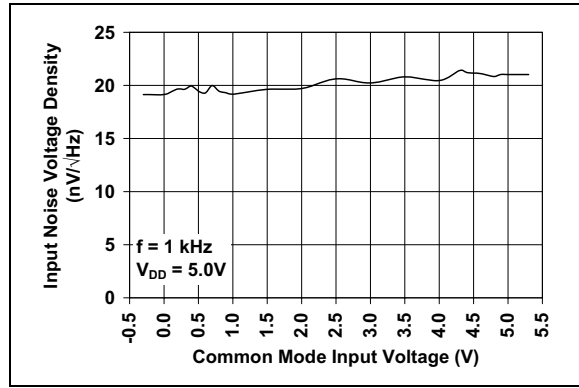
**FIGURE 2-19:** Maximum Output Voltage Swing vs. Frequency.



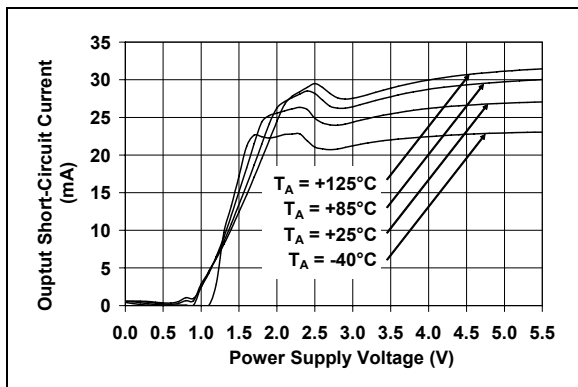
**FIGURE 2-22:** Slew Rate vs. Temperature.



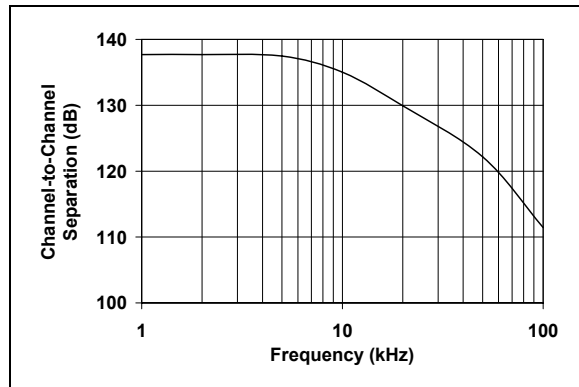
**FIGURE 2-20:** Input Noise Voltage Density vs. Frequency.



**FIGURE 2-23:** Input Noise Voltage Density vs. Common Mode Input Voltage, with  $f = 1\text{ kHz}$ .



**FIGURE 2-21:** Output Short Circuit Current vs. Supply Voltage.

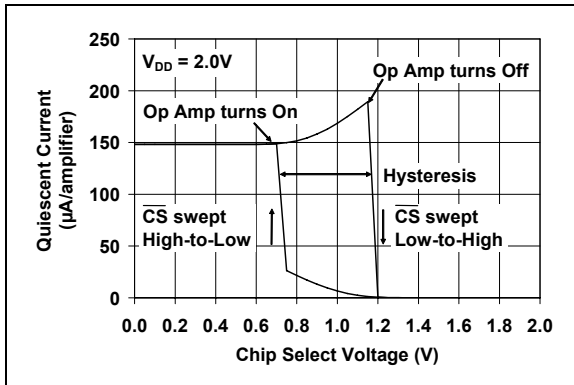


**FIGURE 2-24:** Channel-to-Channel Separation vs. Frequency (MCP6272 and MCP6274).

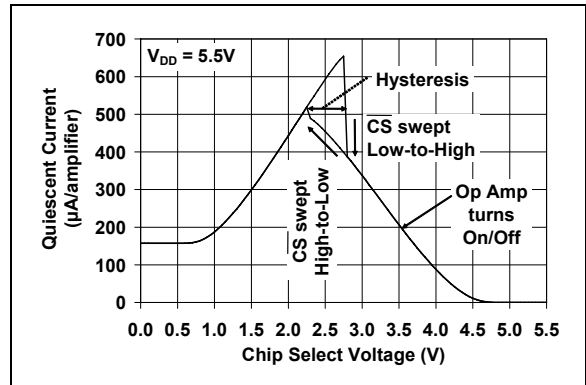


## TYPICAL PERFORMANCE CURVES (Continued)

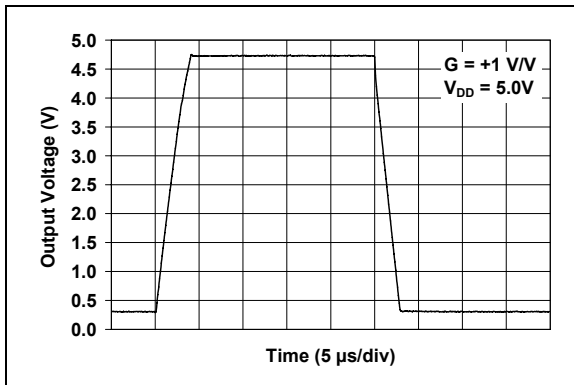
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{CM} = +2.0\text{V}$  to  $+5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$ , and  $\overline{\text{CS}}$  is tied low.



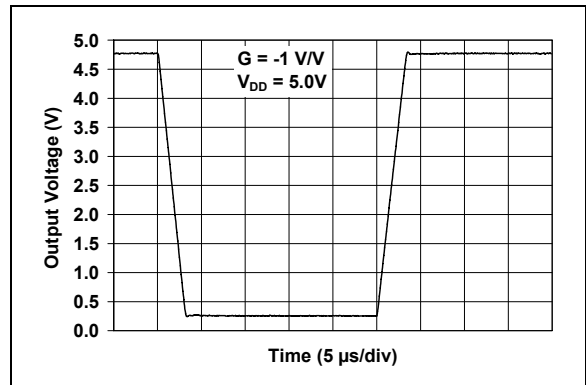
**FIGURE 2-25:** Quiescent Current vs. Chip Select ( $\overline{\text{CS}}$ ) Voltage, with  $V_{DD} = 2.0\text{V}$  (MCP6273 and MCP6275 only).



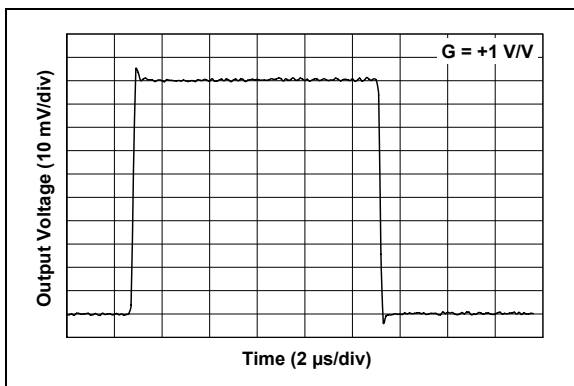
**FIGURE 2-28:** Quiescent Current vs. Chip Select ( $\overline{\text{CS}}$ ) Voltage, with  $V_{DD} = 5.5\text{V}$  (MCP6273 and MCP6275 only).



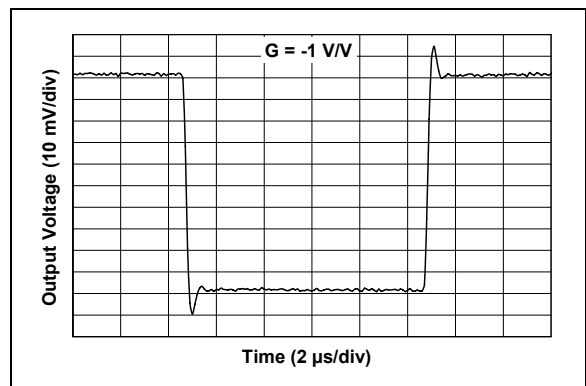
**FIGURE 2-26:** Large Signal Non-inverting Pulse Response.



**FIGURE 2-29:** Large Signal Inverting Pulse Response.



**FIGURE 2-27:** Small Signal Non-inverting Pulse Response.

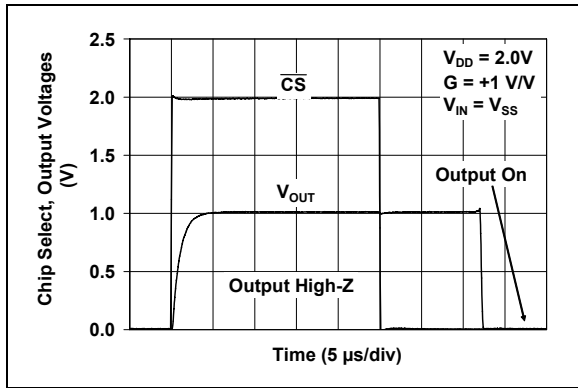


**FIGURE 2-30:** Small Signal Inverting Pulse Response.

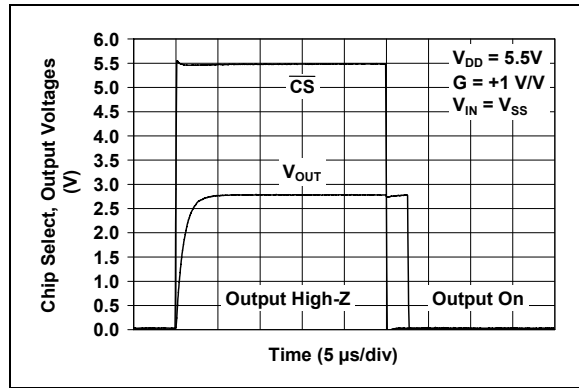
# MCP6271/1R/2/3/4/5

## TYPICAL PERFORMANCE CURVES (Continued)

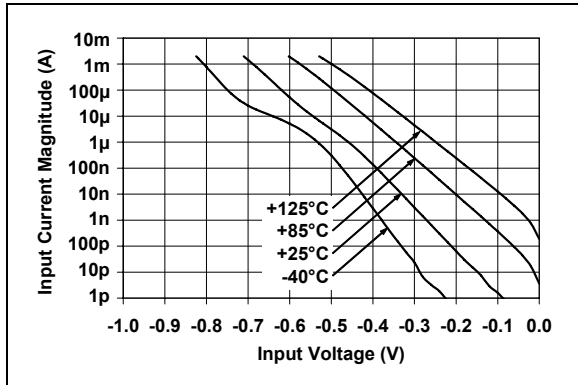
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{\text{CM}} = +2.0\text{V}$  to  $+5.5\text{V}$ ,  $V_{\text{SS}} = \text{GND}$ ,  $V_{\text{CM}} = V_{\text{DD}}/2$ ,  $V_{\text{OUT}} \approx V_{\text{DD}}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_{\text{DD}}/2$ ,  $C_L = 60\text{ pF}$ , and  $\overline{\text{CS}}$  is tied low.



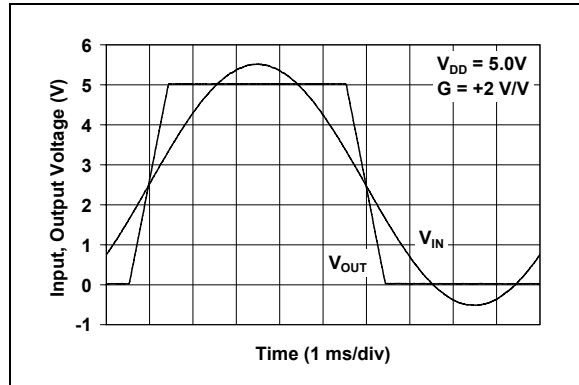
**FIGURE 2-31:** Chip Select ( $\overline{\text{CS}}$ ) to Amplifier Output Response Time, with  $V_{\text{DD}} = 2.0\text{V}$  (MCP6273 and MCP6275 only).



**FIGURE 2-33:** Chip Select ( $\overline{\text{CS}}$ ) to Amplifier Output Response Time, with  $V_{\text{DD}} = 5.5\text{V}$  (MCP6273 and MCP6275 only).



**FIGURE 2-32:** Input Current vs. Input Voltage.



**FIGURE 2-34:** The MCP6271/1R/2/3/4/5 Show no Phase Reversal.

## 3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in [Table 3-1](#) (single op amps) and [Table 3-2](#) (dual and quad op amps).

**TABLE 3-1: PIN FUNCTION TABLE FOR SINGLE OP AMPS**

MCP6271 (PDIP, SOIC, MSOP)	MCP6271 (SOT-23-5)	MCP6271R (SOT-23-5)	MCP6273 (PDIP, SOIC, MSOP)	MCP6273 (SOT-23-6)	Symbol	Description
2	4	4	2	4	$V_{IN-}$	Inverting Input
3	3	3	3	3	$V_{IN+}$	Non-inverting Input
4	2	5	4	2	$V_{SS}$	Negative Power Supply
6	1	1	6	1	$V_{OUT}$	Analog Output
7	5	2	7	6	$V_{DD}$	Positive Power Supply
—	—	—	8	5	$\overline{CS}$	Chip Select
1,5,8	—	—	1,5	—	NC	No Internal Connection

**TABLE 3-2: PIN FUNCTION TABLE FOR DUAL AND QUAD OP AMPS**

MCP6272	MCP6274	MCP6275	Symbol	Description
1	1	—	$V_{OUTA}$	Analog Output (op amp A)
2	2	2	$V_{INA-}$	Inverting Input (op amp A)
3	3	3	$V_{INA+}$	Non-inverting Input (op amp A)
8	4	8	$V_{DD}$	Positive Power Supply
5	5	—	$V_{INB+}$	Non-inverting Input (op amp B)
6	6	6	$V_{INB-}$	Inverting Input (op amp B)
7	7	7	$V_{OUTB}$	Analog Output (op amp B)
—	8	—	$V_{OUTC}$	Analog Output (op amp C)
—	9	—	$V_{INC-}$	Inverting Input (op amp C)
—	10	—	$V_{INC+}$	Non-inverting Input (op amp C)
4	11	4	$V_{SS}$	Negative Power Supply
—	12	—	$V_{IND+}$	Non-inverting Input (op amp D)
—	13	—	$V_{IND-}$	Inverting Input (op amp D)
—	14	—	$V_{OUTD}$	Analog Output (op amp D)
—	—	1	$V_{OUTA} / V_{INB+}$	Analog Output (op amp A)/Non-inverting Input (op amp B)
—	—	5	$\overline{CS}$	Chip Select

### 3.1 Analog Outputs

The output pins are low impedance voltage sources.

### 3.2 Analog Inputs

The non-inverting and inverting inputs are high impedance CMOS inputs with low bias currents.

### 3.3 MCP6275's $V_{OUTA}/V_{INB+}$ Pin

For the MCP6275 only, the output of op amp A is connected directly to the non-inverting input of op amp B; this is the  $V_{OUTA}/V_{INB+}$  pin. This connection makes it possible to provide a  $\overline{CS}$  pin for duals in 8-pin packages.

### 3.4 $\overline{CS}$ Digital Input

This is a CMOS, Schmitt triggered input that places the part into a low power mode of operation.

### 3.5 Power Supply ( $V_{SS}$ and $V_{DD}$ )

The positive power supply ( $V_{DD}$ ) is 2.0V to 5.5V higher than the negative power supply ( $V_{SS}$ ). For normal operation, the other pins are between  $V_{SS}$  and  $V_{DD}$ .

Typically, these parts are used in a single (positive) supply configuration. In this case,  $V_{SS}$  is connected to ground and  $V_{DD}$  is connected to the supply.  $V_{DD}$  will need a local bypass capacitor (typically 0.01  $\mu$ F to 0.1  $\mu$ F) within 2 mm of the  $V_{DD}$  pin. These parts need to use a bulk capacitor (within 100 mm), which can be shared with nearby analog parts.

# MCP6271/1R/2/3/4/5

## 4.0 APPLICATION INFORMATION

The MCP6271/1R/2/3/4/5 family of op amps is manufactured using Microchip's state of the art CMOS process, specifically designed for low cost, low power and general purpose applications. The low supply voltage, low quiescent current and wide bandwidth make the MCP6271/1R/2/3/4/5 ideal for battery powered applications.

### 4.1 Rail-to-Rail Inputs

The input stage of the MCP6271/1R/2/3/4/5 op amps uses two differential CMOS input stages in parallel. One operates at low common mode input voltage ( $V_{CM}$ , which is approximately equal to  $V_{IN+}$  and  $V_{IN-}$  in normal operation) and the other at high  $V_{CM}$ . With this topology, the input operates with  $V_{CM}$  up to 0.3V past either supply rail (see Figure 2-7 and Figure 2-10). The input offset voltage ( $V_{OS}$ ) is measured at  $V_{CM} = V_{SS} - 0.3V$  and  $V_{DD} + 0.3V$  to ensure proper operation.

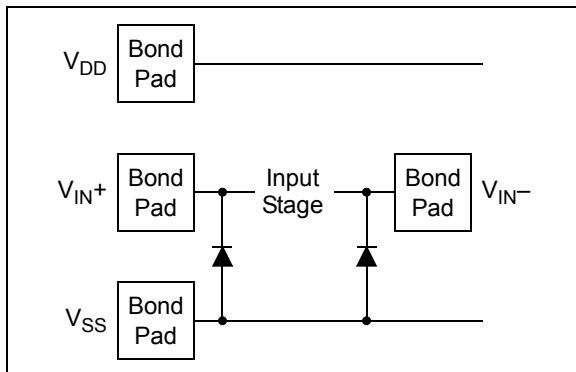
The transition between the two input stage occurs when  $V_{CM} \approx V_{DD} - 1.1V$  (see Figure 2-3 and Figure 2-6). For the best distortion and gain linearity, with non-inverting gains, avoid this region of operation.

#### 4.1.1 PHASE REVERSAL

The input devices are designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-34 shows an input voltage exceeding both supplies with no phase inversion.

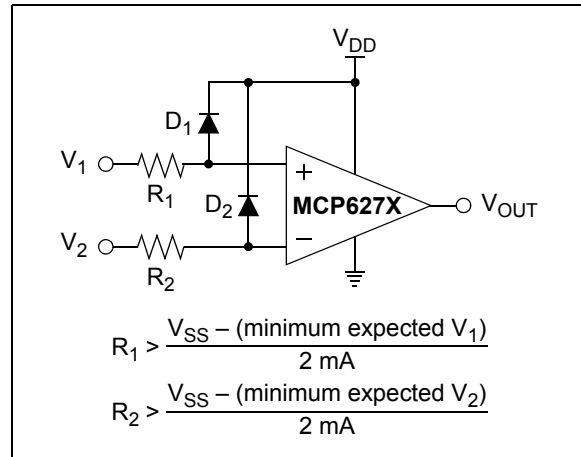
#### 4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current ( $I_B$ ). The input ESD diodes clamp the inputs when they try to go more than one diode drop below  $V_{SS}$ . They also clamp any voltages that go too far above  $V_{DD}$ ; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.



**FIGURE 4-1:** Simplified Analog Input ESD Structures.

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents (and voltages) at the input pins (see **Absolute Maximum Ratings †** at the beginning of Section 1.0 "Electrical Characteristics"). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins ( $V_{IN+}$  and  $V_{IN-}$ ) from going too far below ground, and the resistors  $R_1$  and  $R_2$  limit the possible current drawn out of the input pins. Diodes  $D_1$  and  $D_2$  prevent the input pins ( $V_{IN+}$  and  $V_{IN-}$ ) from going too far above  $V_{DD}$ , and dump any currents onto  $V_{DD}$ . When implemented as shown, resistors  $R_1$  and  $R_2$  also limit the current through  $D_1$  and  $D_2$ .



**FIGURE 4-2:** Protecting the Analog Inputs.

It is also possible to connect the diodes to the left of the resistor  $R_1$  and  $R_2$ . In this case, the currents through the diodes  $D_1$  and  $D_2$  need to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins ( $V_{IN+}$  and  $V_{IN-}$ ) should be very small.

A significant amount of current can flow out of the inputs (through the ESD diodes) when the common mode voltage ( $V_{CM}$ ) is below ground ( $V_{SS}$ ); see Figure 2-32. Applications that are high impedance may need to limit the useable voltage range.

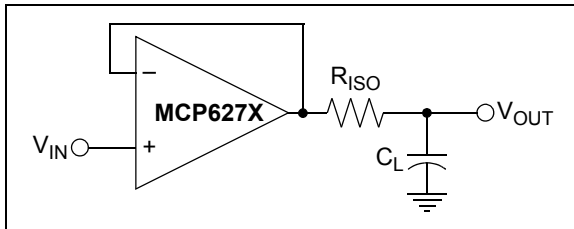
### 4.2 Rail-to-Rail Output

The output voltage range of the MCP6271/1R/2/3/4/5 op amps is  $V_{DD} - 15 \text{ mV}$  (min.) and  $V_{SS} + 15 \text{ mV}$  (max.) when  $R_L = 10 \text{ k}\Omega$  is connected to  $V_{DD}/2$  and  $V_{DD} = 5.5V$ . Refer to Figure 2-17 for more information.

## 4.3 Capacitive Loads

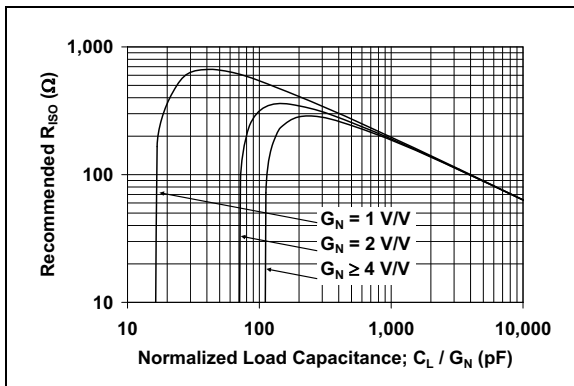
Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. A unity gain buffer ( $G = +1$ ) is the most sensitive to capacitive loads, though all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g.,  $> 100$  pF when  $G = +1$ ), a small series resistor at the output ( $R_{ISO}$  in Figure 4-3) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.



**FIGURE 4-3:** Output Resistor,  $R_{ISO}$  stabilizes large capacitive loads.

Figure 4-4 gives recommended  $R_{ISO}$  values for different capacitive loads and gains. The x-axis is the normalized load capacitance ( $C_L/G_N$ ), where  $G_N$  is the circuit's noise gain. For non-inverting gains,  $G_N$  and the Signal Gain are equal. For inverting gains,  $G_N$  is  $1 + |\text{Signal Gain}|$  (e.g.,  $-1$  V/V gives  $G_N = +2$  V/V).



**FIGURE 4-4:** Recommended  $R_{ISO}$  Values for Capacitive Loads.

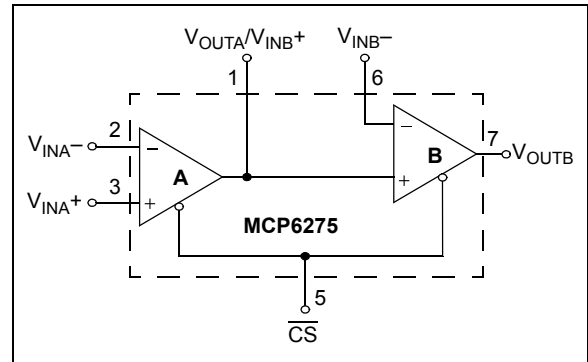
After selecting  $R_{ISO}$  for your circuit, double check the resulting frequency response peaking and step response overshoot. Modify  $R_{ISO}$ 's value until the response is reasonable. Bench evaluation and simulations with the MCP6271/1R/2/3/4/5 SPICE macro model are helpful.

## 4.4 MCP6273/5 Chip Select ( $\overline{CS}$ )

The MCP6273 and MCP6275 are single and dual op amps with Chip Select ( $\overline{CS}$ ), respectively. When  $\overline{CS}$  is pulled high, the supply current drops to  $0.7 \mu\text{A}$  (typ.) and flows through the  $\overline{CS}$  pin to  $V_{SS}$ . When this happens, the amplifier output is put into a high impedance state. By pulling  $\overline{CS}$  low, the amplifier is enabled. The  $\overline{CS}$  pin has a  $5 \text{ M}\Omega$  (typ.) pull-down resistor connected to  $V_{SS}$ , so it will go low if the  $\overline{CS}$  pin is left floating. Figure 1-1 shows the output voltage and supply current response to a  $\overline{CS}$  pulse.

## 4.5 Cascaded Dual Op Amps (MCP6275)

The MCP6275 is a dual op amp with Chip Select ( $\overline{CS}$ ). The Chip Select input is available on what would be the non-inverting input of a standard dual op amp (pin 5). This pin is available because the output of op amp A connects to the non-inverting input of op amp B, as shown in Figure 4-5. The Chip Select input, which can be connected to a microcontroller I/O line, puts the device in low power mode. Refer to Section 4.4 "MCP6273/5 Chip Select ( $\overline{CS}$ )".



**FIGURE 4-5:** Cascaded Gain Amplifier.

The output of op amp A is loaded by the input impedance of op amp B, which is typically  $10^{13} \Omega \parallel 6 \text{ pF}$ , as specified in the DC specification table (Refer to Section 4.3 "Capacitive Loads" for further details regarding capacitive loads).

The common mode input range of these op amps is specified in the data sheet as  $V_{SS} - 300 \text{ mV}$  and  $V_{DD} + 300 \text{ mV}$ . However, since the output of op amp A is limited to  $V_{OL}$  and  $V_{OH}$  (20 mV from the rails with a  $10 \text{ k}\Omega$  load), the non-inverting input range of op amp B is limited to the common mode input range of  $V_{SS} + 20 \text{ mV}$  and  $V_{DD} - 20 \text{ mV}$ .

# MCP6271/1R/2/3/4/5

## 4.6 Unused Amplifiers

An unused op amp in a quad package (MCP6274) should be configured as shown in Figure 4-6. These circuits prevent the output from toggling and causing crosstalk. In Circuit A,  $R_1$  and  $R_2$  produce a voltage within its output voltage range ( $V_{OH}$ ,  $V_{OL}$ ). The op amp buffers this voltage, which can be used elsewhere in the circuit. Circuit B uses the minimum number of components and operates as a comparator.

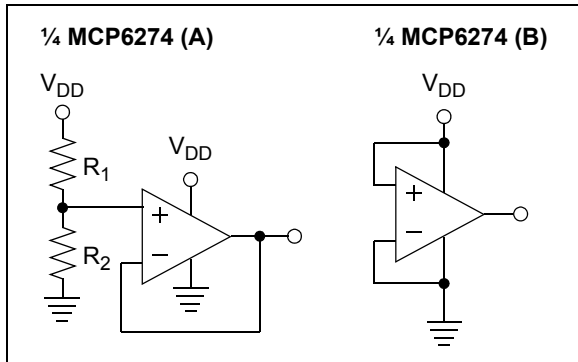


FIGURE 4-6: Unused Op Amps.

## 4.7 Supply Bypass

With this family of operational amplifiers, the power supply pin ( $V_{DD}$  for single supply) should have a local bypass capacitor (i.e., 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$ ) within 2 mm for good, high frequency performance. It also needs a bulk capacitor (i.e., 1  $\mu\text{F}$  or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with nearby analog parts.

## 4.8 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is  $10^{12}\Omega$ . A 5V difference would cause 5 pA of current to flow. This is greater than the MCP6271/1R/2/3/4/5 family's bias current at 25°C (1 pA, typ.).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is illustrated in Figure 4-7.

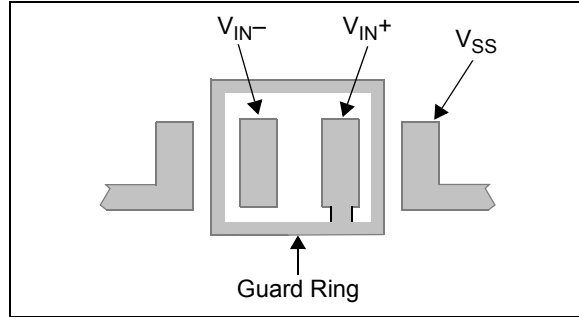


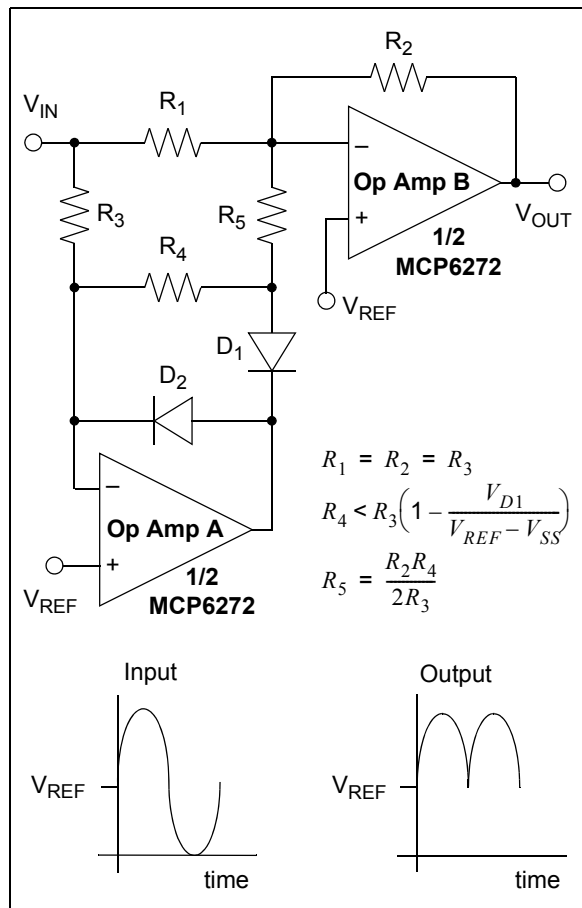
FIGURE 4-7: Example Guard Ring Layout for Inverting Gain.

1. For Inverting Gain and Transimpedance Amplifiers (convert current to voltage, such as photo detectors):
  - a) Connect the guard ring to the non-inverting input pin ( $V_{IN+}$ ). This biases the guard ring to the same reference voltage as the op amp (e.g.,  $V_{DD}/2$  or ground).
  - b) Connect the inverting pin ( $V_{IN-}$ ) to the input with a wire that does not touch the PCB surface.
2. Non-inverting Gain and Unity Gain Buffer:
  - a) Connect the non-inverting pin ( $V_{IN+}$ ) to the input with a wire that does not touch the PCB surface.
  - b) Connect the guard ring to the inverting input pin ( $V_{IN-}$ ). This biases the guard ring to the common mode input voltage.

## 4.9 Application Circuits

### 4.9.1 ACTIVE FULL-WAVE RECTIFIER

The MCP6271/1R/2/3/4/5 family of amplifiers can be used in applications such as an Active Full-Wave Rectifier or an Absolute Value circuit, as shown in Figure 4-8. The amplifier and feedback loops in this active voltage rectifier circuit eliminate the diode drop problem that exists in a passive voltage rectifier. This circuit behaves as a follower (the output follows the input) as long as the input signal is more positive than the reference voltage. If the input signal is more negative than the reference voltage, however, the circuit behaves as an inverting amplifier. Therefore, the output voltage will always be above the reference voltage, regardless of the input signal.

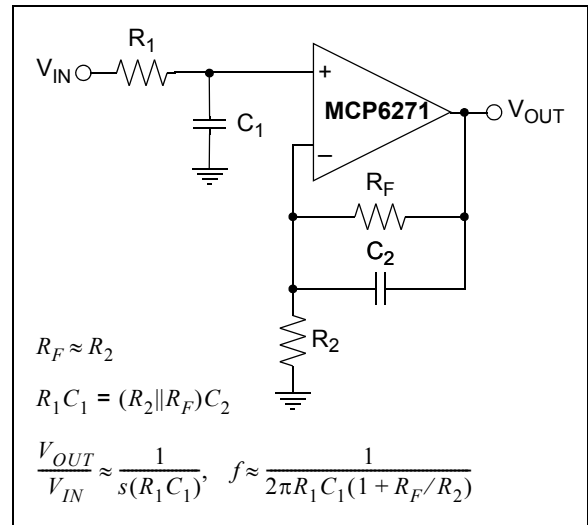


**FIGURE 4-8:** Active Full-wave Rectifier.

The design equations give a gain of  $\pm 1$  from  $V_{IN}$  to  $V_{OUT}$ , and produce rail-to-rail outputs.

### 4.9.2 LOSSY NON-INVERTING INTEGRATOR

The non-inverting integrator shown in Figure 4-9 is easy to build. It saves one op amp over the typical Miller integrator plus inverting amplifier configuration. The phase accuracy of this integrator depends on the matching of the input and feedback resistor-capacitor time constants.  $R_F$  makes this a lossy integrator (it has finite gain at DC), and makes this integrator stable by itself.



**FIGURE 4-9:** Non-Inverting Integrator.

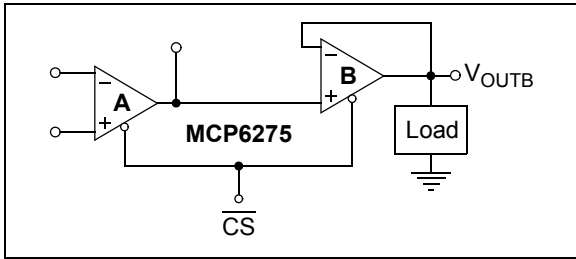
# MCP6271/1R/2/3/4/5

## 4.9.3 CASCADED OP AMP APPLICATIONS

The MCP6275 provides the flexibility of Low power mode for dual op amps in an 8-pin package. The MCP6275 eliminates the added cost and space in a battery powered application by using two single op amps with Chip Select ( $\overline{CS}$ ) lines or a 10-pin device with one  $\overline{CS}$  line for both op amps. Since the two op amps are internally cascaded, this device cannot be used in circuits that require active or passive elements between the two op amps. However, there are several applications where this op amp configuration with a  $\overline{CS}$  line becomes suitable. The circuits below show possible applications for this device.

### 4.9.3.1 Load Isolation

With the cascaded op amp configuration, op amp B can be used to isolate the load from op amp A. In applications where op amp A is driving capacitive or low resistive loads in the feedback loop (such as an integrator or filter circuit) the op amp may not have sufficient source current to drive the load. In this case, op amp B can be used as a buffer.



**FIGURE 4-10:** Isolating the Load with a Buffer.

### 4.9.3.2 Cascaded Gain

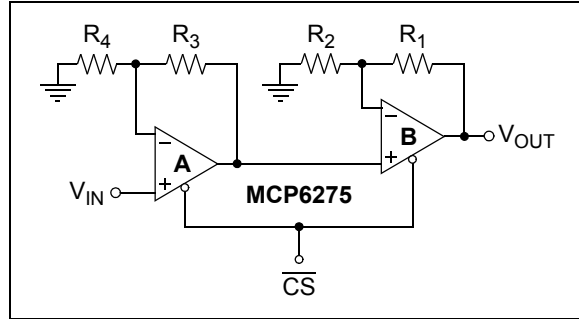
Figure 4-11 shows a cascaded gain circuit configuration with Chip Select. Op amps A and B are configured in a non-inverting amplifier configuration. In this configuration, it is important to note that the input offset voltage of op amp A is amplified by the gain of op amp A and B, as shown below:

$$V_{OUT} = V_{IN}G_A G_B + V_{OSA}G_A G_B + V_{OSB}G_B$$

Where:

- $G_A$  = op amp A gain
- $G_B$  = op amp B gain
- $V_{OSA}$  = op amp A input offset voltage
- $V_{OSB}$  = op amp B input offset voltage

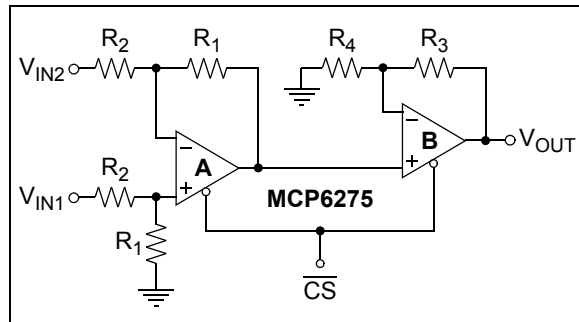
Therefore, it is recommended that you set most of the gain with op amp A and use op amp B with relatively small gain (e.g., a unity gain buffer).



**FIGURE 4-11:** Cascaded Gain Circuit Configuration.

### 4.9.3.3 Difference Amplifier

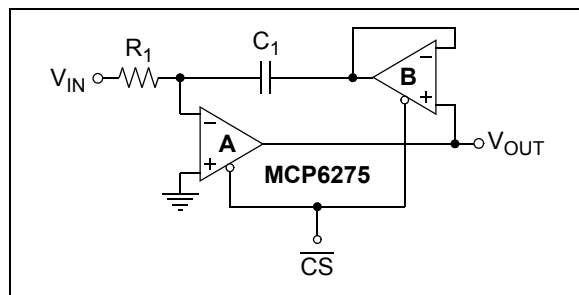
Figure 4-12 shows op amp A configured as a difference amplifier with Chip Select. In this configuration, it is recommended that well matched resistors (e.g., 0.1%) be used to increase the Common Mode Rejection Ratio (CMRR). Op amp B can be used to provide additional gain and isolate the load from the difference amplifier.



**FIGURE 4-12:** Difference Amplifier Circuit.

### 4.9.3.4 Inverting Integrator with Active Compensation and Chip Select

Figure 4-13 uses an active compensator (op amp B) to compensate for the non-ideal op amp characteristics introduced at higher frequencies. This circuit uses op amp B as a unity gain buffer to isolate the integration capacitor  $C_1$  from op amp A and drives the capacitor with a low impedance source. Since both op amps are matched very well, they provide a high quality integrator.

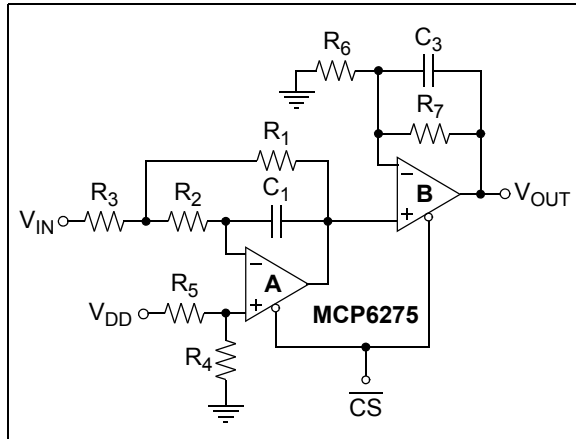


**FIGURE 4-13:** Integrator Circuit with Active Compensation.



## 4.9.3.5 Second Order MFB with an Extra Pole-Zero Pair

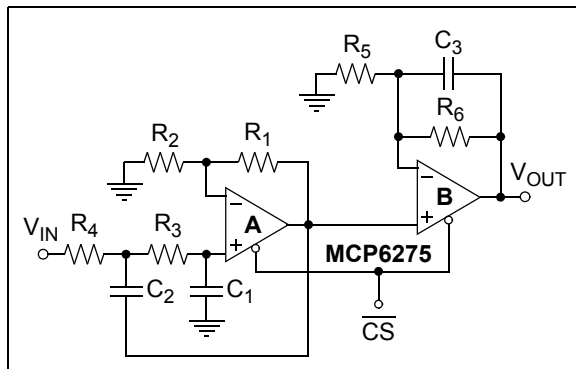
Figure 4-14 is a second order multiple feedback low-pass filter with Chip Select. Use the FilterLab<sup>®</sup> software from Microchip Technology Inc. to determine the R and C values for op amp A's second order filter. Op amp B can be used to add a pole-zero pair using  $C_3$ ,  $R_6$  and  $R_7$ .



**FIGURE 4-14:** Second Order Multiple Feedback Low-Pass Filter with an Extra Pole-Zero Pair.

## 4.9.3.6 Second Order Sallen-Key with an Extra Pole-Zero Pair

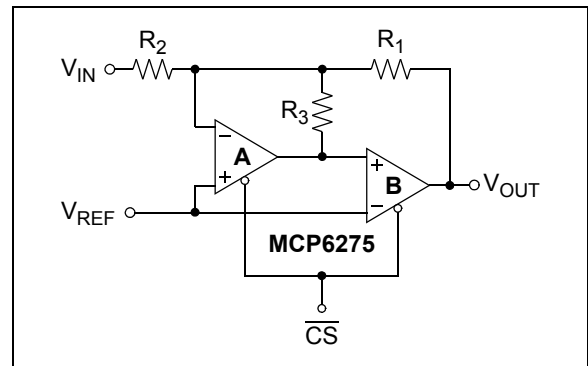
Figure 4-15 is a second order Sallen-Key low-pass filter with Chip Select. Use the Filterlab<sup>®</sup> software from Microchip to determine the R and C values for op amp A's second order filter. Op amp B can be used to add a pole-zero pair using  $C_3$ ,  $R_5$  and  $R_6$ .



**FIGURE 4-15:** Second Order Sallen-Key Low-Pass Filter with an Extra Pole-Zero Pair and Chip Select.

## 4.9.3.7 Capacitorless Second Order Low-Pass filter with Chip Select

The low-pass filter shown in Figure 4-16 does not require external capacitors and uses only three external resistors; the op amp's GBWP sets the corner frequency.  $R_1$  and  $R_2$  are used to set the circuit gain.  $R_3$  is used to set the Q. To avoid gain peaking in the frequency response, Q needs to be low (lower values need to be selected for  $R_3$ ). Note that the amplifier bandwidth varies greatly over temperature and process. This configuration, however, provides a low cost solution for applications with high bandwidth requirements.



**FIGURE 4-16:** Capacitorless Second Order Low-Pass Filter with Chip Select.

# MCP6271/1R/2/3/4/5

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## 5.0 DESIGN TOOLS

Microchip provides the basic design tools needed for the MCP6271/1R/2/3/4/5 family of op amps.

### 5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6271/1R/2/3/4/5 op amps is available on our web site at [www.microchip.com](http://www.microchip.com). This model is intended to be an initial design tool that works well in the op amp's linear region of operation at room temperature. See the macro model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

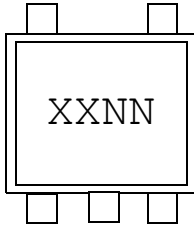
### 5.2 FilterLab<sup>®</sup> Software

Microchip's FilterLab software is an innovative tool that simplifies analog active filter (using op amps) design. It is available free of charge from our web site at [www.microchip.com](http://www.microchip.com). The FilterLab software tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information

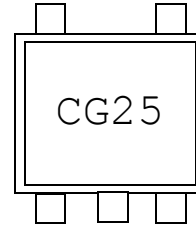
5-Lead SOT-23 (MCP6271 and MCP6271R)



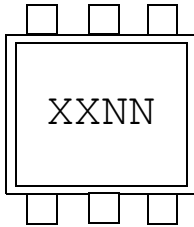
Device	Code
MCP6271	CGNN
MCP6271R	ETNN

**Note:** Applies to 5-Lead SOT-23

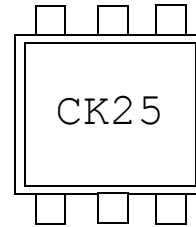
Example:



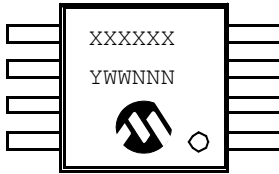
6-Lead SOT-23 (MCP6273)



Example:



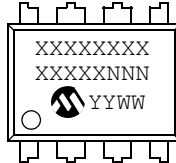
8-Lead MSOP



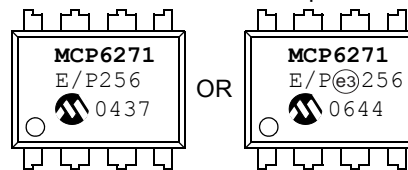
Example:



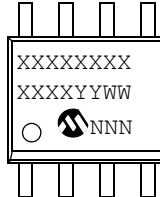
8-Lead PDIP (300 mil)



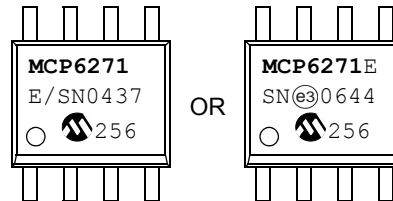
Example:



8-Lead SOIC (150 mil)



Example:



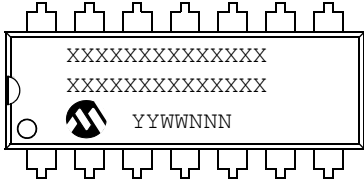
<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	③	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (③) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

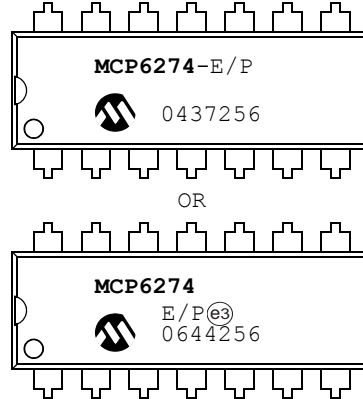
# MCP6271/1R/2/3/4/5

## Package Marking Information (Continued)

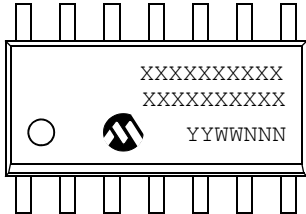
14-Lead PDIP (300 mil) (MCP6274)



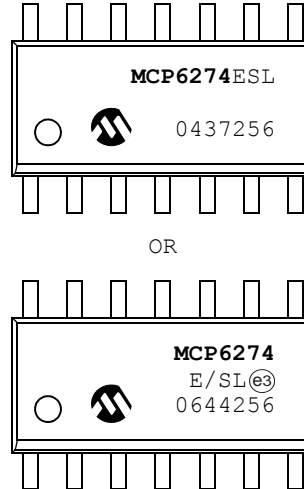
Example:



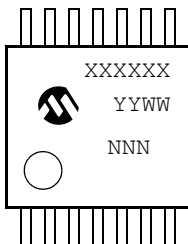
14-Lead SOIC (150 mil) (MCP6274)



Example:



14-Lead TSSOP (MCP6274)



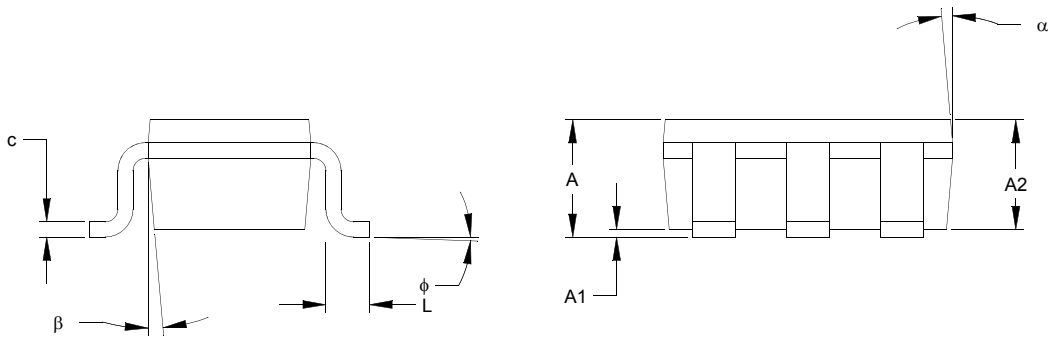
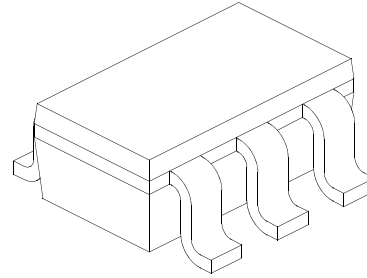
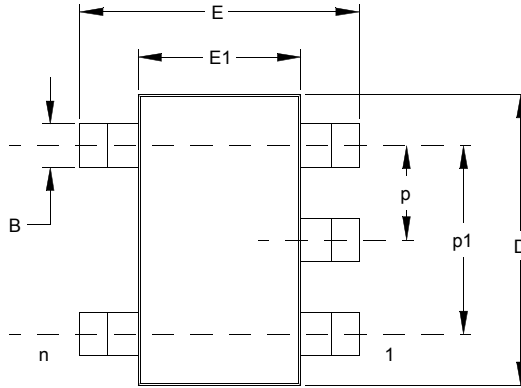
Example:



# MCP6271/1R/2/3/4/5

## 5-Lead Plastic Small Outline Transistor (OT) (SOT-23)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	f	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	a	0	5	10	0	5	10
Mold Draft Angle Bottom	b	0	5	10	0	5	10

\* Controlling Parameter

**Notes:**

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

EIAJ Equivalent: SC-74A

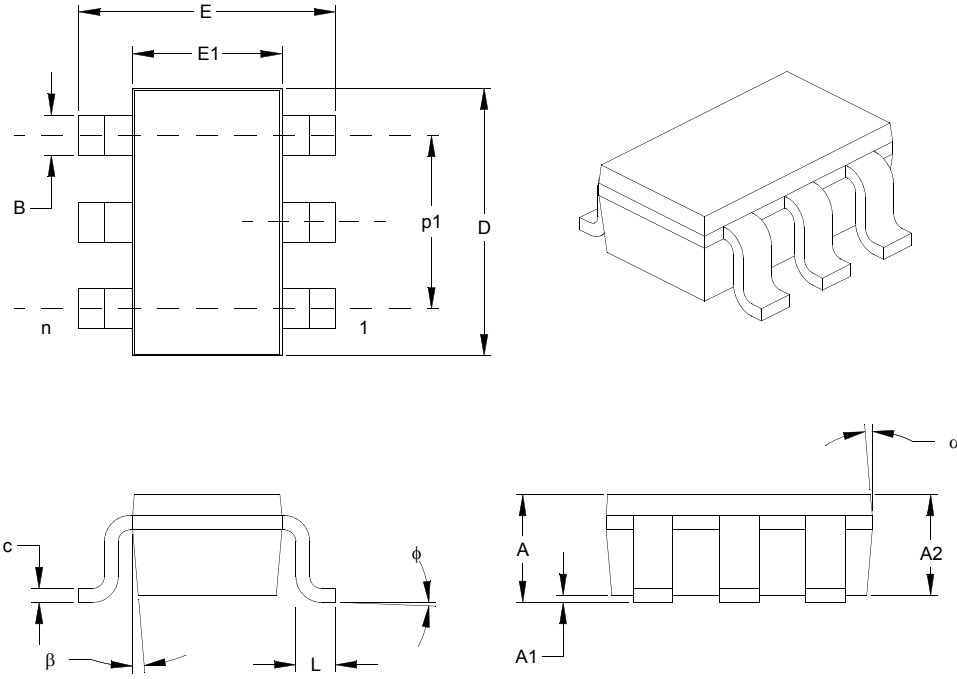
Drawing No. C04-091

Revised 09-12-05

# MCP6271/1R/2/3/4/5

## 6-Lead Plastic Small Outline Transistor (CH) (SOT-23)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	6			6		
Pitch	p	.038 BSC			0.95 BSC		
Outside lead pitch	p1	.075 BSC			1.90 BSC		
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	φ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter

**Notes:**

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

See ASME Y14.5M

JEITA (formerly EIAJ) equivalent: SC-74A

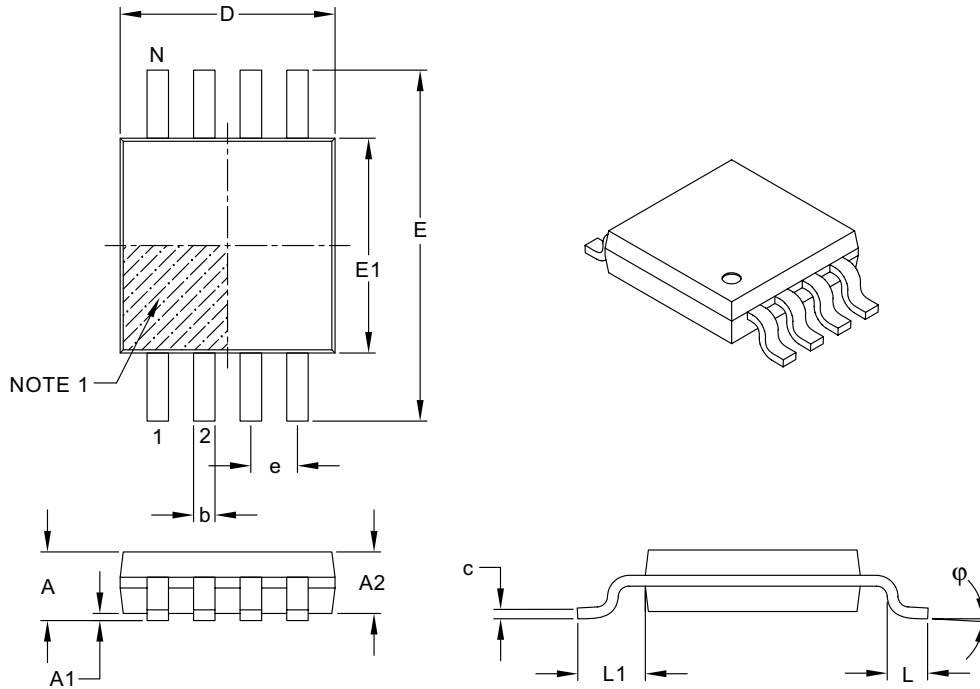
Drawing No. C04-120

Revised 09-12-05

# MCP6271/1R/2/3/4/5

## 8-Lead Plastic Micro Small Outline Package (MS) (MSOP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	—	—	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	—	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Foot Angle	$\phi$	0°	—	8°
Lead Thickness	c	0.08	—	0.23
Lead Width	b	0.22	—	0.40

### Notes:

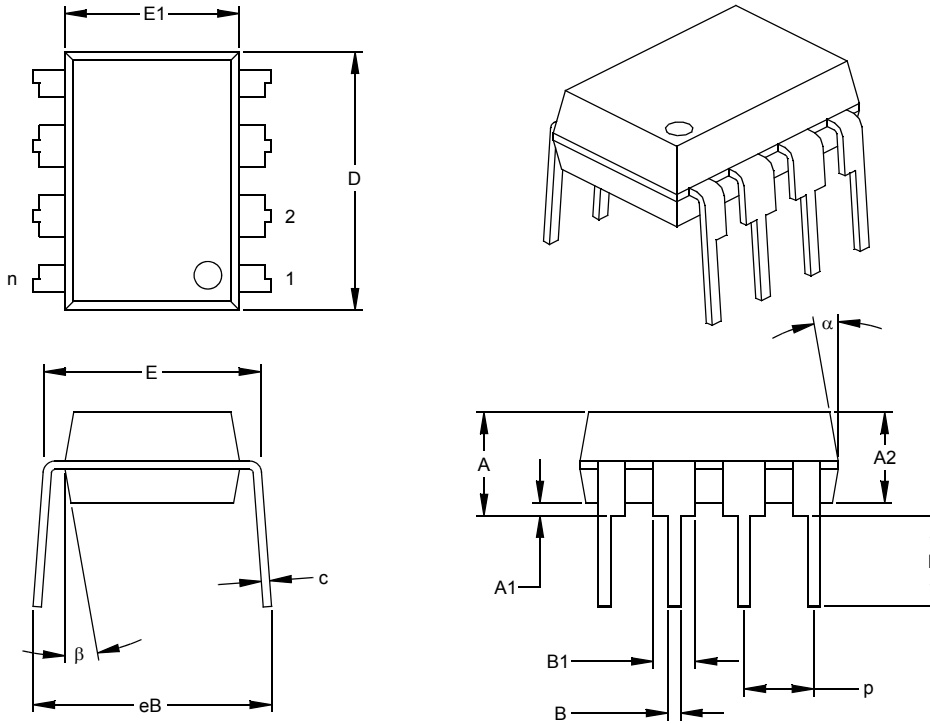
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-111, Sept. 8, 2006

# MCP6271/1R/2/3/4/5

## 8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

\* Controlling Parameter  
 § Significant Characteristic

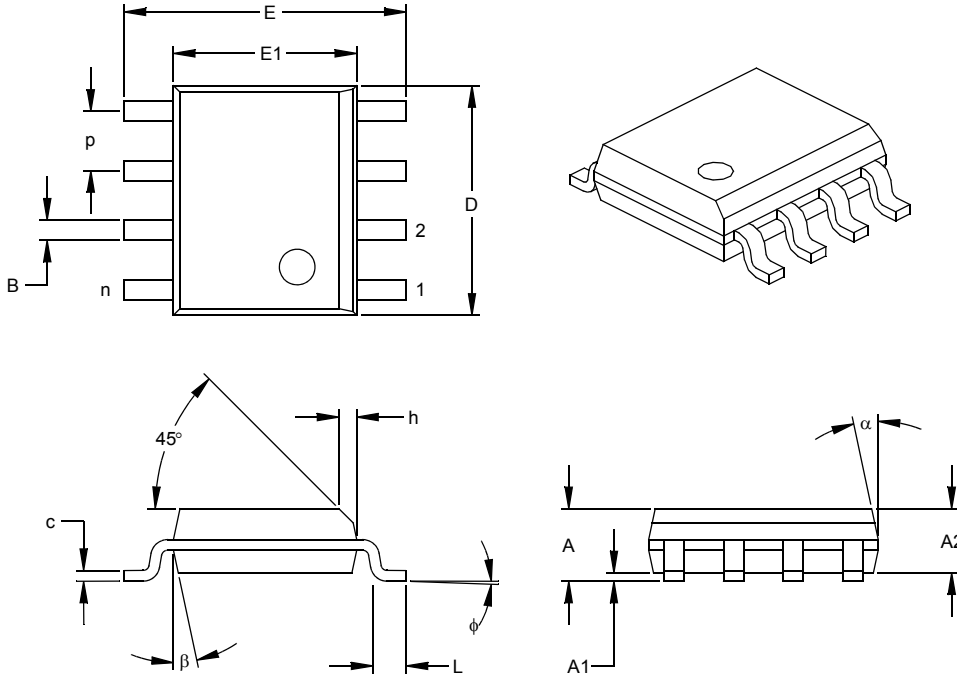
Notes:  
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.  
 JEDEC Equivalent: MS-001  
 Drawing No. C04-018



# MCP6271/1R/2/3/4/5

## 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter

§ Significant Characteristic

**Notes:**

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

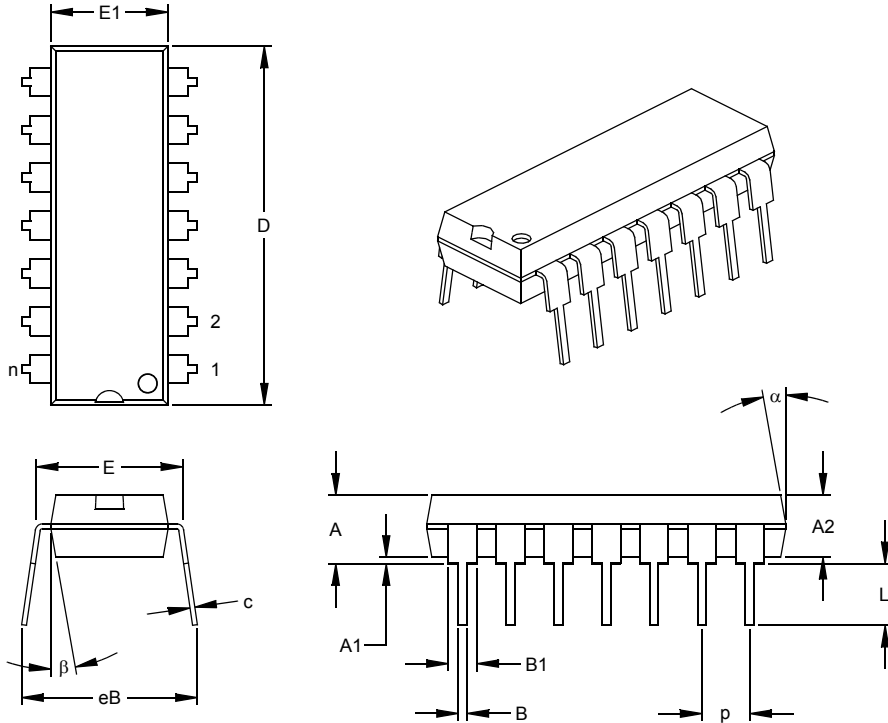
JEDEC Equivalent: MS-012

Drawing No. C04-057

# MCP6271/1R/2/3/4/5

## 14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

\* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

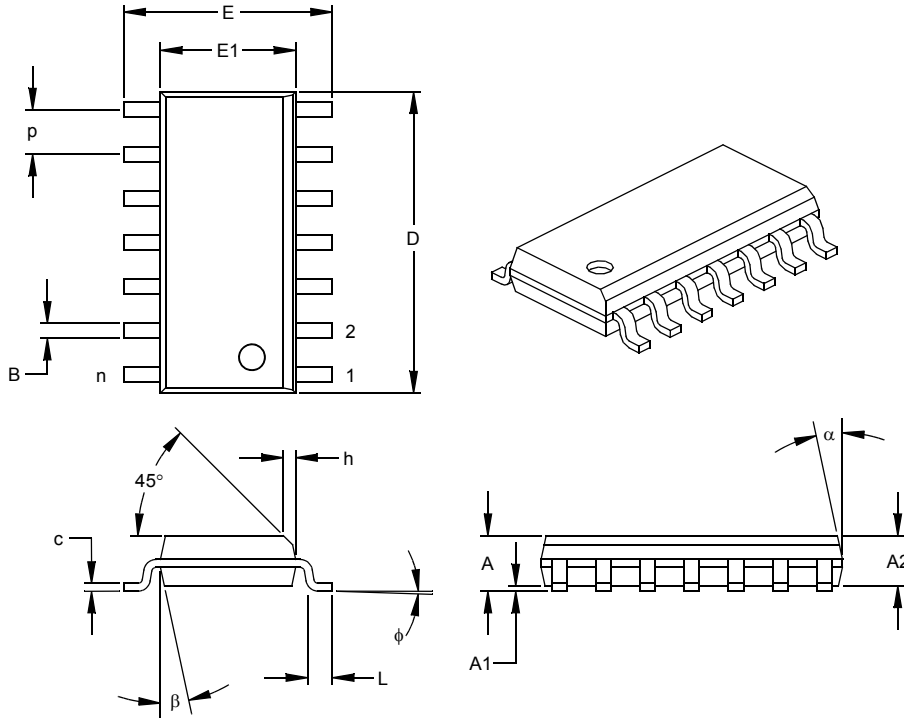
JEDEC Equivalent: MS-001

Drawing No. C04-005

# MCP6271/1R/2/3/4/5

## 14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	14			14		
Pitch	p	.050			1.27		
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter

§ Significant Characteristic

**Notes:**

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

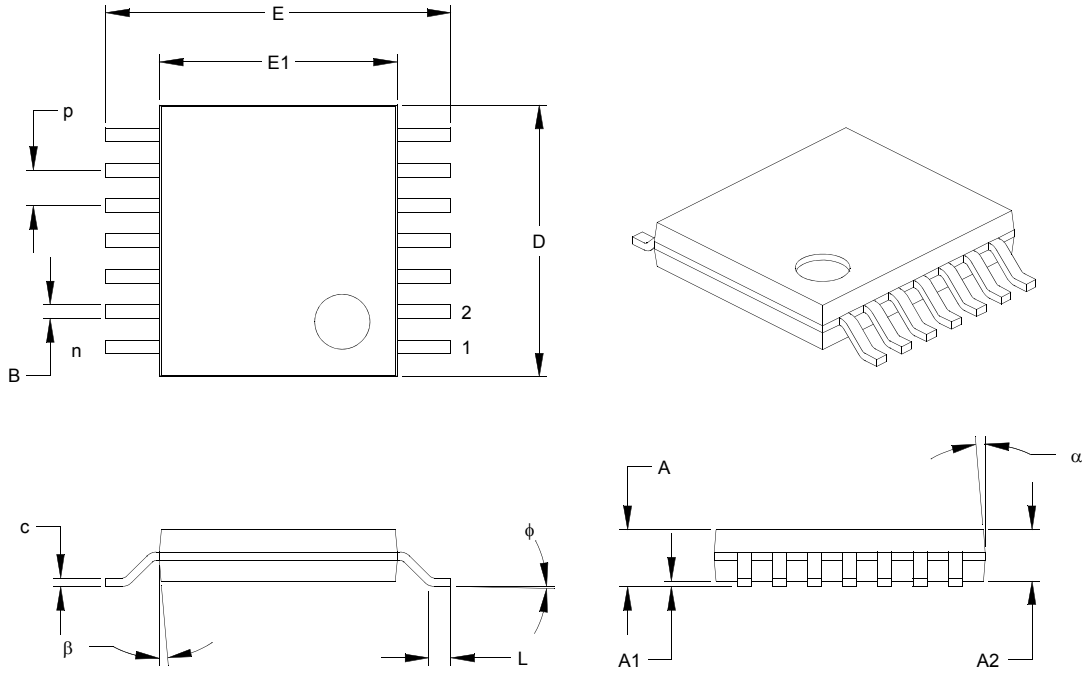
Drawing No. C04-065

Revised 7-20-06

# MCP6271/1R/2/3/4/5

## 14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	14			14		
Pitch	P	.026 BSC			0.65 BSC		
Overall Height	A	.039	.041	.043	1.00	1.05	1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0°	4°	8°	0°	4°	8°
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	12° REF			12° REF		
Mold Draft Angle Bottom	β	12° REF			12° REF		

\* Controlling Parameter

**Notes:**

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.
- BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
See ASME Y14.5M
- REF: Reference Dimension, usually without tolerance, for information purposes only.  
See ASME Y14.5M
- JEDEC Equivalent: MO-153 AB-1
- Drawing No. C04-087

Revised: 08-17-05

## APPENDIX A: REVISION HISTORY

### Revision E (December 2006)

The following is the list of modifications:

1. Updated specifications (**Section 1.0 “Electrical Characteristics”**):
  - a) Clarified Absolute Maximum Analog Input Voltage and Current specifications.
  - b) Clarified  $V_{CMR}$ ,  $V_{OL}$ ,  $V_{OH}$ , and PM specifications.
  - c) Corrected the typical  $E_{ni}$ .
2. Added plots on Common Mode Input Range behavior vs. temperature and supply voltage (**Section 2.0 “Typical Performance Curves”**).
3. Added applications writeup on unused op amps and corrected description of floating  $\overline{CS}$  pin behavior (**Section 4.0 “Application Information”**).
4. Updated package information (**Section 6.0 “Packaging Information”**):
  - a) Corrected package markings.
  - b) Added disclaimer to package outline drawings.

### Revision D (December 2004)

The following is the list of modifications:

1. Added SOT-23-5 packages for the DSTEMP and MCP6271R single op amps.
2. Added SOT-23-6 packages for the DSTEMP single op amp.
3. Added **Section 3.0 “Pin Descriptions”**.
4. Corrected application circuits (**Section 4.9 “Application Circuits”**).
5. Added SOT-23-5 and SOT-23-6 packages and corrected package marking information (**Section 6.0 “Packaging Information”**).
6. Added Appendix A: Revision History.

### Revision C (June 2004)

### Revision B (October 2003)

### Revision A (June 2003)

- Original data sheet release.

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	-	<u>X</u>	<u>/XX</u>	
Device		Temperature Range	Package	
Device:	MCP6271:	Single Op Amp		
	MCP6271T:	Single Op Amp (Tape and Reel) (SOIC, MSOP, SOT-23-5)		
	MCP6271RT:	Single Op Amp (Tape and Reel) (SOT-23-5)		
	MCP6272:	Dual Op Amp		
	MCP6272T:	Dual Op Amp (Tape and Reel) (SOIC, MSOP)		
	MCP6273:	Single Op Amp with Chip Select		
	MCP6273T:	Single Op Amp with Chip Select (Tape and Reel) (SOIC, MSOP, SOT-23-6)		
	MCP6274:	Quad Op Amp		
	MCP6274T:	Quad Op Amp (Tape and Reel) (SOIC, TSSOP)		
	MCP6275:	Dual Op Amp with Chip Select		
	MCP6275T:	Dual Op Amp with Chip Select (Tape and Reel) (SOIC, MSOP)		
Temperature Range:	E	= -40°C to +125°C		
Package:	OT	= Plastic Small Outline Transistor (SOT-23), 5-lead (MCP6271, MCP6271R)		
	CH	= Plastic Small Outline Transistor (SOT-23), 6-lead (MCP6273)		
	MS	= Plastic MSOP, 8-lead		
	P	= Plastic DIP (300 mil Body), 8-lead, 14-lead		
	SN	= Plastic SOIC, (150 mil Body), 8-lead		
	SL	= Plastic SOIC (150 mil Body), 14-lead		
	ST	= Plastic TSSOP (4.4 mm Body), 14-lead		
				<b>Examples:</b>
	a)	MCP6271-E/SN:	Extended Temperature, 8LD SOIC package.	
	b)	MCP6271-E/MS:	Extended Temperature, 8LD MSOP package.	
	c)	MCP6271-E/P:	Extended Temperature, 8LD PDIP package.	
	d)	MCP6271T-E/OT:	Tape and Reel, Extended Temperature, 5LD SOT-23 package.	
	a)	MCP6271RT-E/OT:	Tape and Reel, Extended Temperature, 5LD SOT-23 package.	
	a)	MCP6272-E/SN:	Extended Temperature, 8LD SOIC package.	
	b)	MCP6272-E/MS:	Extended Temperature, 8LD MSOP package.	
	c)	MCP6272-E/P:	Extended Temperature, 8LD PDIP package.	
	d)	MCP6272T-E/SN:	Tape and Reel, Extended Temperature, 8LD SOIC package.	
	a)	MCP6273-E/SN:	Extended Temperature, 8LD SOIC package.	
	b)	MCP6273-E/MS:	Extended Temperature, 8LD MSOP package.	
	c)	MCP6273-E/P:	Extended Temperature, 8LD PDIP package.	
	d)	MCP6273T-E/CH:	Extended Temperature, 6LD SOT-23 package.	
	a)	MCP6274-E/P:	Extended Temperature, 14LD PDIP package.	
	b)	MCP6274T-E/SL:	Tape and Reel, Extended Temperature, 14LD SOIC package.	
	c)	MCP6274-E/SL:	Extended Temperature, 14LD SOIC package.	
	d)	MCP6274-E/ST:	Extended Temperature, 14LD TSSOP package.	
	a)	MCP6275-E/SN:	Extended Temperature, 8LD SOIC package.	
	b)	MCP6275-E/MS:	Extended Temperature, 8LD MSOP package.	
	c)	MCP6275-E/P:	Extended Temperature, 8LD PDIP package.	
	d)	MCP6275T-E/SN:	Tape and Reel, Extended Temperature, 8LD SOIC package.	

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