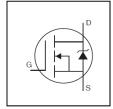
AUTOMOTIVE GRADE

AUIRFR3710Z

HEXFET® Power MOSFET

Features

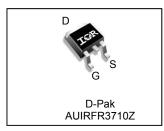
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- · Repetitive Avalanche Allowed up to Timax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



V _{DSS}	100V
R _{DS(on)} max.	18mΩ
I _{D (Silicon Limited)}	56A
D (Package Limited)	42A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



G	D	S
Gate	Drain	Source

Base part number	Standard Pack			Orderable Part Number	
Base part number	Package Type	Form	Quantity	Orderable Part Number	
ALUDED27107	D. Dok	Tube	75	AUIRFR3710Z	
AUIRFR3710Z	D-Pak	Tape and Reel Left	3000	AUIRFR3710ZTRL	

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units		
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	56			
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	39	A		
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Package Limited) 42				
I _{DM}	Pulsed Drain Current ①	220			
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	140	W		
	Linear Derating Factor	0.95	W/°C		
V_{GS}	Gate-to-Source Voltage	± 20	V		
E _{AS}	Single Pulse Avalanche Energy (Thermally Limited) ② 150		mJ		
E _{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ®	200			
I _{AR}	Avalanche Current ①	See Fig.15,16, 12a, 12b			
E _{AR}	Repetitive Avalanche Energy ©		mJ		
T_J	Operating Junction and -55 to + 175				
T _{STG}	Storage Temperature Range				
	Soldering Temperature, for 10 seconds (1.6mm from case)	300			

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{ heta JC}$	Junction-to-Case ®		1.05	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ∅		50	°C/W
$R_{\theta JA}$	Junction-to-Ambient		110	

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2015-11-23

^{*}Qualification standards can be found at www.infineon.com



Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		0.088		V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance		15	18	mΩ	V _{GS} = 10V, I _D = 33A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0		4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
gfs	Forward Trans conductance	39			S	$V_{DS} = 25V, I_{D} = 33A$ ③
	Drain to Course Leakage Current			20		$V_{DS} = 100V, V_{GS} = 0V$
I _{DSS}	Drain-to-Source Leakage Current			250	μA	$V_{DS} = 100V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
	Gate-to-Source Forward Leakage			200	n ^	V _{GS} = 20V
IGSS	Gate-to-Source Reverse Leakage			-200	nA	V _{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

		-	-		
Total Gate Charge		69	100		I _D = 33A
Gate-to-Source Charge		15		nC	$V_{DS} = 80V$
Gate-to-Drain Charge		25			V _{GS} = 10V3
Turn-On Delay Time		14			$V_{DD} = 50V$
Rise Time		43		no	I _D = 33A
Turn-Off Delay Time		53		115	$R_G = 6.8\Omega$
Fall Time		42			V _{GS} = 10V③
Internal Drain Inductance		4.5			Between lead, 6mm (0.25in.)
Internal Source Inductance		7.5			from package and center of die contact
Input Capacitance		2930			$V_{GS} = 0V$
Output Capacitance		290			$V_{DS} = 25V$
Reverse Transfer Capacitance		180		nΕ	f = 1.0MHz
Output Capacitance		1200		рΓ	$V_{GS} = 0V$, $V_{DS} = 1.0V$ $f = 1.0MHz$
Output Capacitance		180			$V_{GS} = 0V$, $V_{DS} = 80V$ $f = 1.0MHz$
Effective Output Capacitance		430			$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V $
	Gate-to-Source Charge Gate-to-Drain Charge Turn-On Delay Time Rise Time Turn-Off Delay Time Fall Time Internal Drain Inductance Internal Source Inductance Input Capacitance Output Capacitance Reverse Transfer Capacitance Output Capacitance Output Capacitance Output Capacitance Output Capacitance Output Capacitance	Gate-to-Source Charge —— Gate-to-Drain Charge —— Turn-On Delay Time —— Rise Time —— Turn-Off Delay Time —— Fall Time —— Internal Drain Inductance —— Input Capacitance —— Output Capacitance —— Reverse Transfer Capacitance —— Output Capacitance ——	Gate-to-Source Charge — 15 Gate-to-Drain Charge — 25 Turn-On Delay Time — 14 Rise Time — 43 Turn-Off Delay Time — 53 Fall Time — 42 Internal Drain Inductance — 4.5 Internal Source Inductance — 7.5 Input Capacitance — 2930 Output Capacitance — 180 Output Capacitance — 1200 Output Capacitance — 180	Gate-to-Source Charge — 15 — Gate-to-Drain Charge — 25 — Turn-On Delay Time — 14 — Rise Time — 43 — Turn-Off Delay Time — 53 — Fall Time — 42 — Internal Drain Inductance — 4.5 — Internal Source Inductance — 7.5 — Input Capacitance — 2930 — Output Capacitance — 290 — Reverse Transfer Capacitance — 180 — Output Capacitance — 1200 — Output Capacitance — 180 —	Gate-to-Source Charge — 15 — nC Gate-to-Drain Charge — 25 — Turn-On Delay Time — 14 — Rise Time — 43 — Turn-Off Delay Time — 53 — Fall Time — 42 — Internal Drain Inductance — 4.5 — Internal Source Inductance — 7.5 — Input Capacitance — 2930 — Output Capacitance — 290 — Reverse Transfer Capacitance — 180 — Output Capacitance — 1200 — Output Capacitance — 180 —

Diode Characteristics

	Parameter	Min.	Тур.	Max.	Units	Conditions
	Continuous Source Current			56		MOSFET symbol
I _S	(Body Diode)			50	_	showing the
ı	Pulsed Source Current			220	A	integral reverse
I _{SM}	(Body Diode) ①			220		p-n junction diode.
V_{SD}	Diode Forward Voltage			1.3	V	$T_J = 25^{\circ}C, I_S = 33A, V_{GS} = 0V$ ③
t _{rr}	Reverse Recovery Time		35	53	ns	$T_J = 25^{\circ}C$, $I_F = 33A$, $V_{DD} = 50V$
Q _{rr}	Reverse Recovery Charge		41	62	nC	di/dt = 100A/µs ③
t _{on}	Forward Turn-On Time	Intrinsio	turn-or	n time is	negligil	ole (turn-on is dominated by L _S +L _D)

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

- \oplus C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
- © Limited by T_{Jmax}, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population, starting $T_J = 25$ °C, L = 0.28mH, R_G = 25Ω, I_{AS} = 33A, V_{GS} =10V.
- When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994

 \otimes R₀ is measured at T_J approximately 90°C.



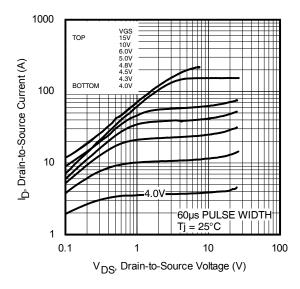


Fig. 1 Typical Output Characteristics

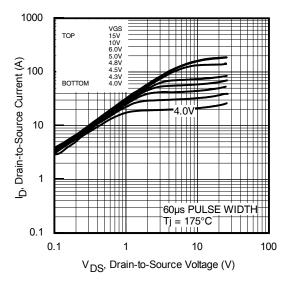


Fig. 2 Typical Output Characteristics

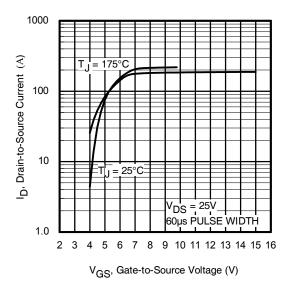


Fig. 3 Typical Transfer Characteristics

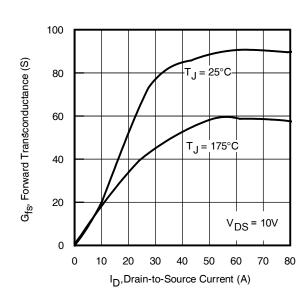


Fig. 4 Typical Forward Trans conductance Vs. Drain Current



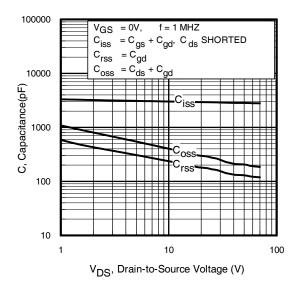


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

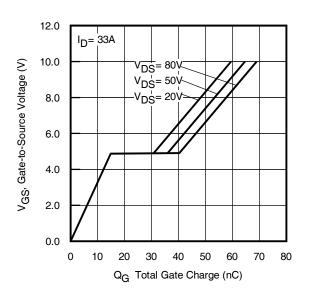


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

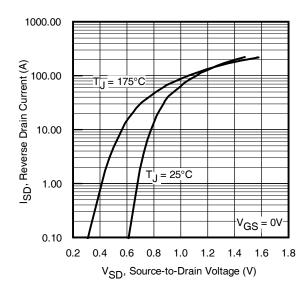


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

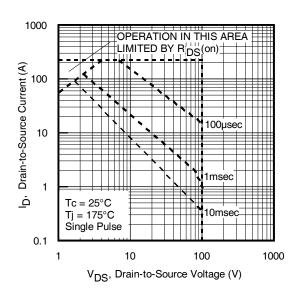
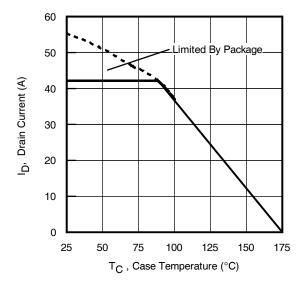


Fig 8. Maximum Safe Operating Area

4





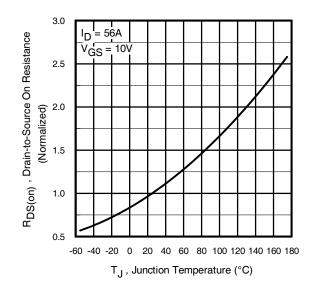


Fig 9. Maximum Drain Current Vs. Case Temperature

Fig 10. Normalized On-Resistance Vs. Temperature

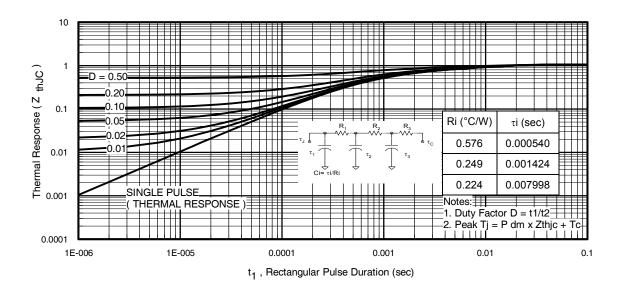


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



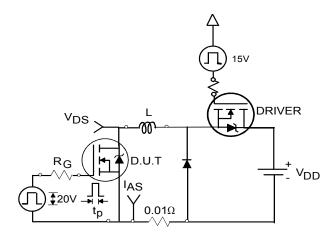


Fig 12a. Unclamped Inductive Test Circuit

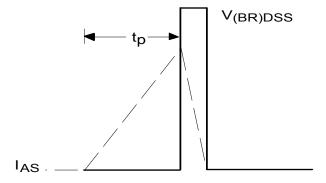


Fig 12b. Unclamped Inductive Waveforms

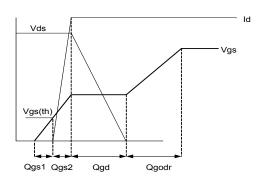


Fig 13a. Gate Charge Waveform

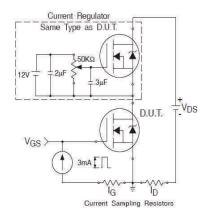


Fig 13b. Gate Charge Test Circuit

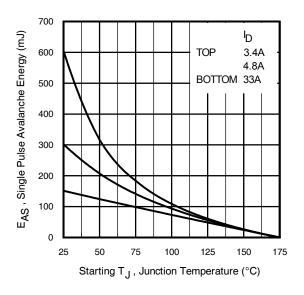


Fig 12c. Maximum Avalanche Energy vs. Drain Current

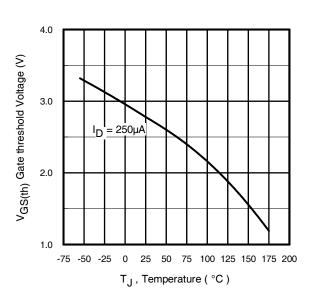


Fig 14. Threshold Voltage Vs. Temperature



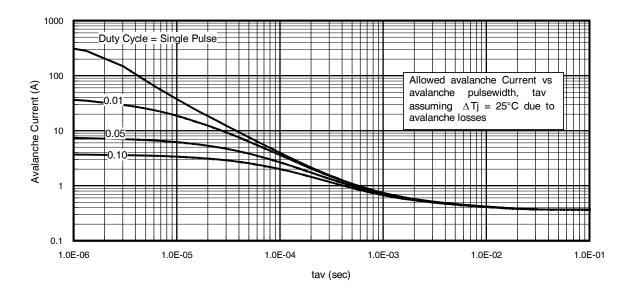


Fig 15. Typical Avalanche Current Vs. Pulse width

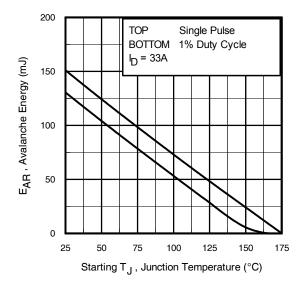


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:

(For further info, see AN-1005 at www.infineon.com)

- Avalanche failures assumption:
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{imax}. This is validated for every part type.
- 2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
- 3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
- 4. PD (ave) = Average power dissipation per single avalanche pulse.
- BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
- 6. Iav = Allowable avalanche current.
- 7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).

tav = Average time in avalanche.

D = Duty cycle in avalanche = tav ·f

ZthJC(D, tav) = Transient thermal resistance, see Figures 13)

$$\begin{split} P_{D \; (ave)} &= 1/2 \; (\; 1.3 \cdot BV \cdot I_{av}) = \Delta T / \; Z_{thJC} \\ I_{av} &= 2\Delta T / \; [1.3 \cdot BV \cdot Z_{th}] \\ E_{AS \; (AR)} &= P_{D \; (ave)} \cdot t_{av} \end{split}$$

2015-11-23



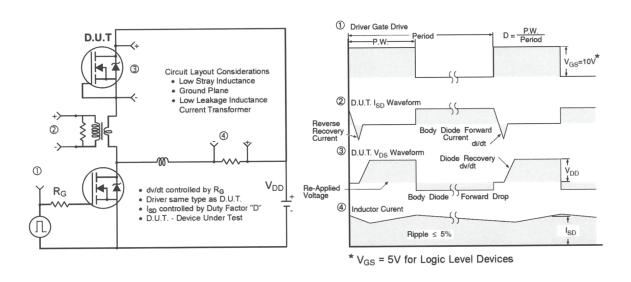
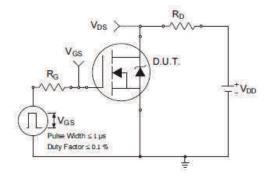
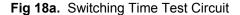


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs





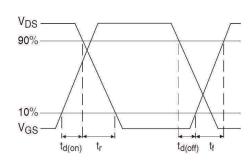
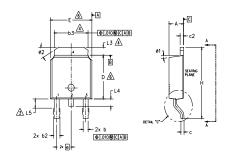


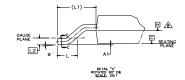
Fig 18b. Switching Time Waveforms

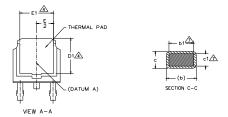


D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))









NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- 1 LEAD DIMENSION UNCONTROLLED IN L5.
- A- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.— SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- ⚠ DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- A- DIMENSION 61 & c1 APPLIED TO BASE METAL ONLY.
- ♠ DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

S Y M	DIMENSIONS					
В	MILLIM	ETERS	INC	HES	O T	
0 L	MIN.	MAX.	MIN.	MAX.	E S	
Α	2.18	2.39	.086	.094		
A1	_	0.13	-	.005		
b	0.64	0.89	.025	.035		
ь1	0.65	0.79	.025	.031	7	
b2	0.76	1.14	.030	.045		
b3	4.95	5.46	.195	.215	4	
С	0.46	0.61	.018	.024		
c1	0.41	0.56	.016	.022	7	
c2	0.46	0.89	.018	.035		
D	5.97	6.22	.235	.245	6	
D1	5.21	-	.205	-	4	
Ε	6.35	6.73	.250	.265	6	
E1	4.32	-	.170	-	4	
е	2.29	BSC	.090 BSC			
Н	9.40	10.41	.370	.410		
L	1.40	1.78	.055	.070		
L1	2.74	BSC	.108	REF.		
L2	0.51	BSC	.020	BSC		
L3	0.89	1.27	.035	.050	4	
L4	-	1.02	-	.040		
L5	1.14	1.52	.045	.060	3	
ø	0,	10°	0,	10°		
ø1	0,	15*	0,	15*		
ø2	25*	35*	25*	35*		

LEAD ASSIGNMENTS

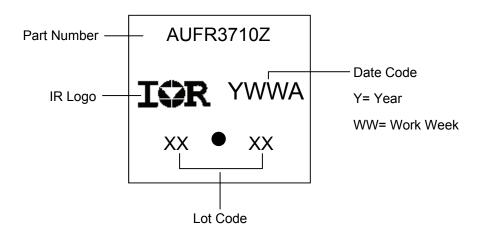
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE 4.- DRAIN

IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4. COLLECTOR

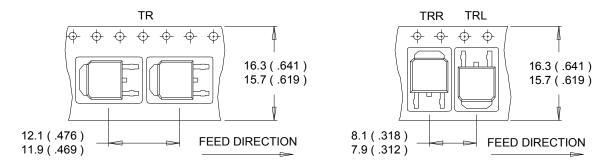
D-Pak (TO-252AA) Part Marking Information



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

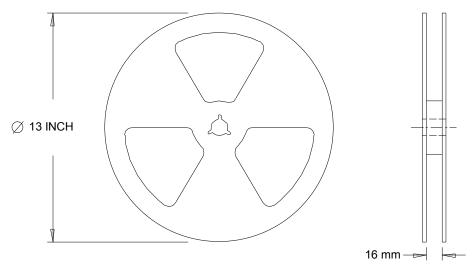


D-Pak (TO-252AA) Tape & Reel Information (Dimensions are shown in millimeters (inches))



NOTES:

- 1. CONTROLLING DIMENSION: MILLIMETER.
- 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
- 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/



Qualification Information

Industrial and Consumer qual	er(s) passed Automotive qualification. Infineon's lification level is granted by extension of the higher				
Industrial and Consumer qual	lification level is granted by extension of the higher				
Industrial and Consumer qual	lification level is granted by extension of the higher				
Automotive level.	MSI 1				
	MQI 1				
Moisture Sensitivity Level D-Pak	D-Pak MSL1				
Marking Market	Class M4 [†]				
Machine Model	AEC-Q101-002				
FOR Harris Bada Madal	Class H1C [†]				
ESD Human Body Model	AEC-Q101-001				
0	Class C3 [†]				
Charged Device Model AEC-Q101-005					
RoHS Compliant	Yes				

[†] Highest passing voltage.

Revision History

Date	Comments
11/23/2015	Updated datasheet with corporate template
11/23/2013	Corrected ordering table on page 1.

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