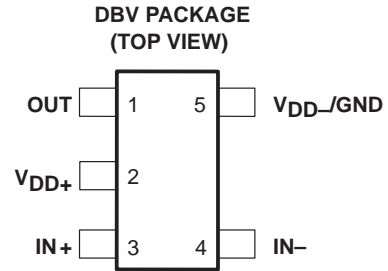


TLV2711, TLV2711Y
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- Output Swing Includes Both Supply Rails
- Low Noise . . . 21 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Very Low Power . . . 11 μA Per Channel Typ
- Common-Mode Input Voltage Range Includes Negative Rail
- Wide Supply Voltage Range 2.7 V to 10 V
- Available in the SOT-23 Package
- Macromodel Included



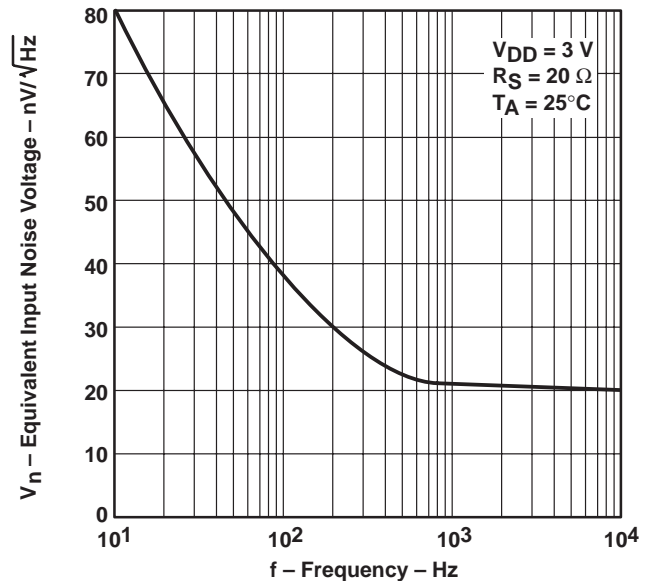
description

The TLV2711 is a single low-voltage operational amplifier available in the SOT-23 package. It consumes only 11 μA (typ) of supply current and is ideal for battery-power applications. Looking at Figure 1, the TLV2711 has a 3-V noise level of 21 nV/√Hz at 1 kHz; five times lower than competitive SOT-23 micropower solutions. The device exhibits rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLV2711 is fully characterized at 3 V and 5 V and is optimized for low-voltage applications.

The TLV2711, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs).

With a total area of 5.6mm², the SOT-23 package only requires one-third the board space of the standard 8-pin SOIC package. This ultra-small package allows designers to place single amplifiers very close to the signal source, minimizing noise pick-up from long PCB traces.

**EQUIVALENT INPUT NOISE VOLTAGE†
VS
FREQUENCY**



† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.
For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

Figure 1. Equivalent Input Noise Voltage Versus Frequency

AVAILABLE OPTIONS

| T _A | V _{IOmax} AT 25°C | PACKAGED DEVICES | SYMBOL | CHIP FORM‡ (Y) |
|----------------|----------------------------|------------------|--------|----------------|
| | | SOT-23 (DBV)† | | |
| 0°C to 70°C | 3 mV | TLV2711CDBV | VAJC | TLV2711Y |
| -40°C to 85°C | 3 mV | TLV2711IDBV | VAJI | |

† The DBV package available in tape and reel only.

‡ Chip forms are tested at T_A = 25°C only.



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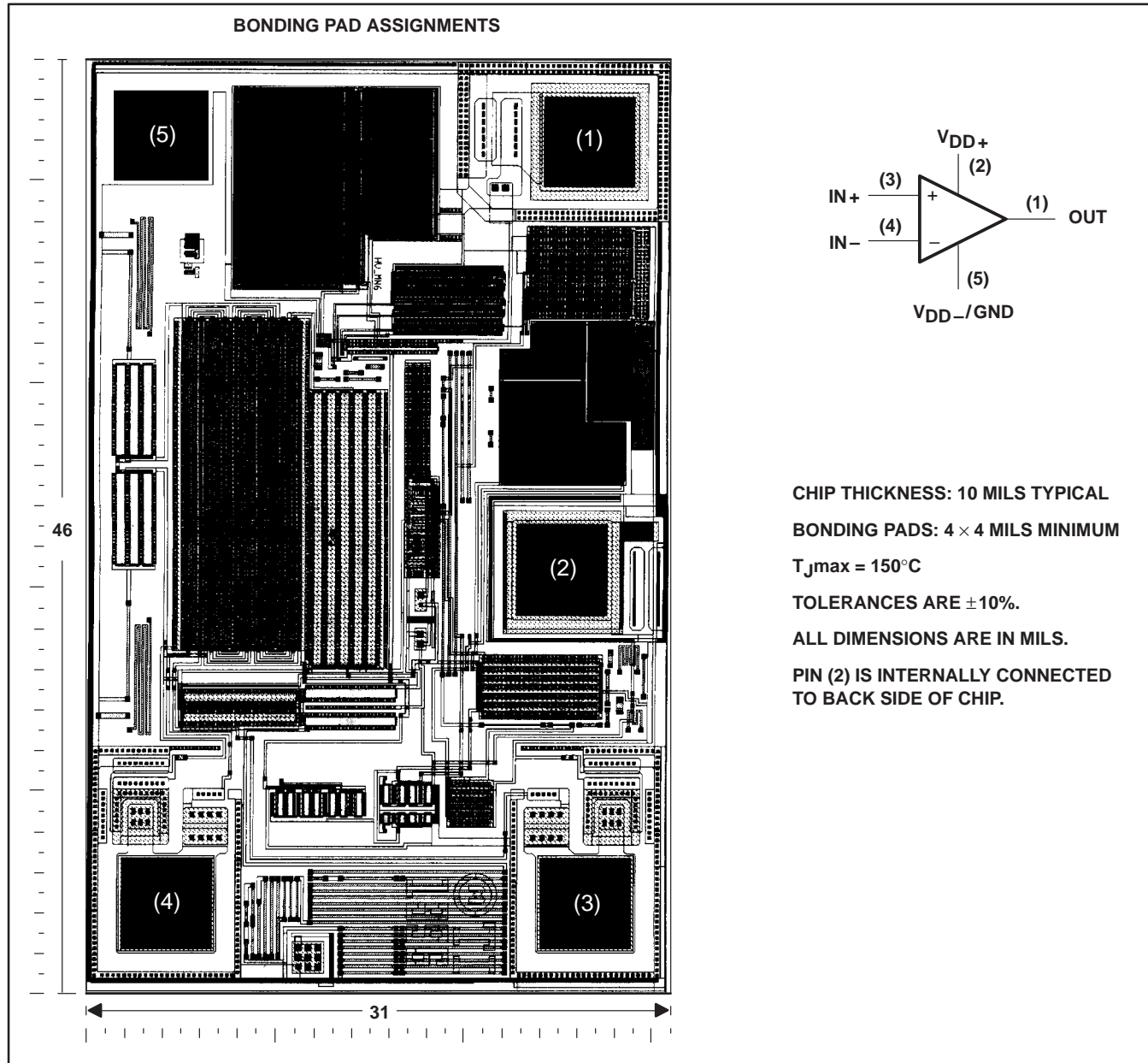
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TLV2711Y chip information

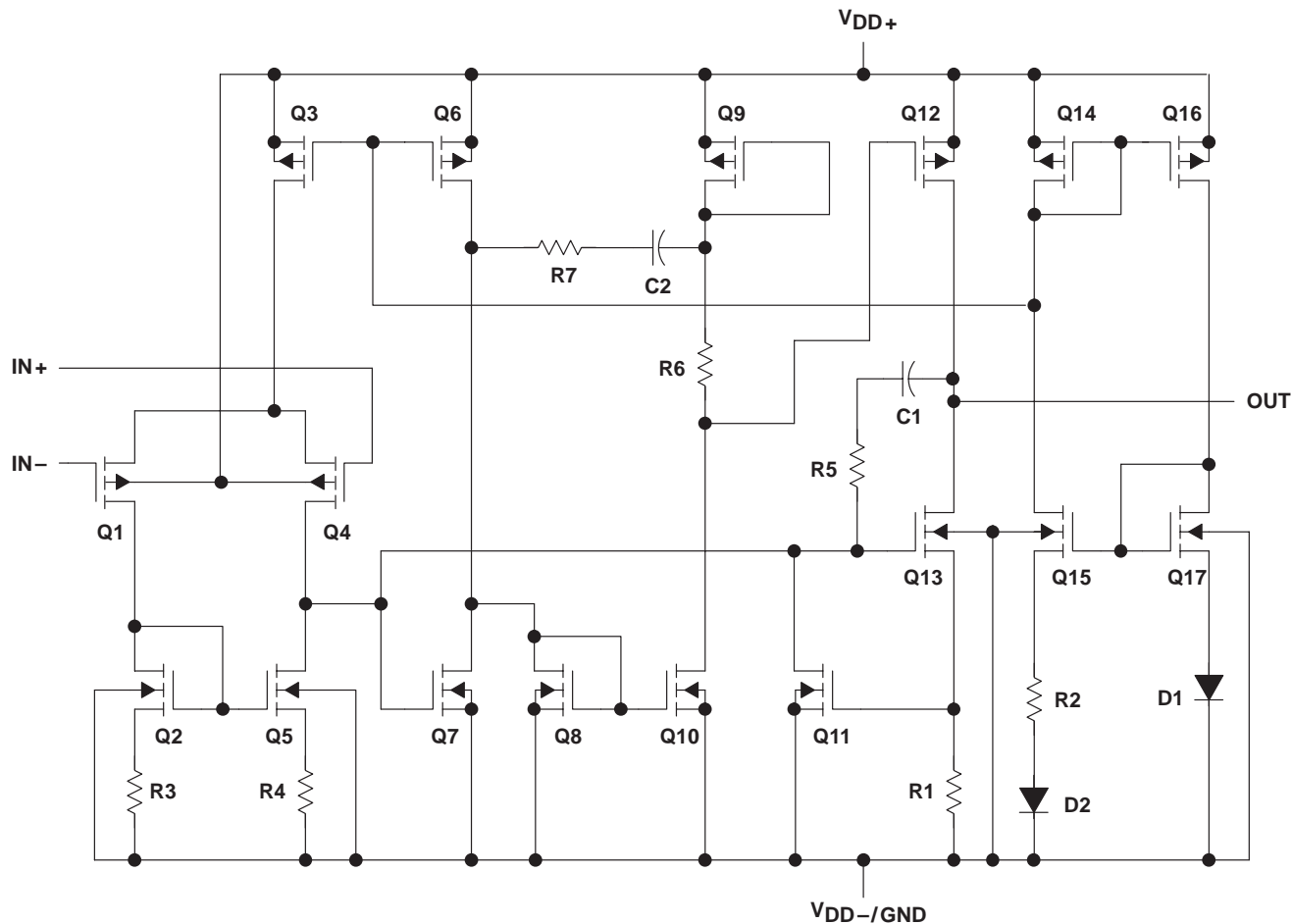
This chip, when properly assembled, displays characteristics similar to the TLV2711C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 10 MILS TYPICAL
BONDING PADS: 4 × 4 MILS MINIMUM
 $T_{jmax} = 150^{\circ}\text{C}$
TOLERANCES ARE $\pm 10\%$.
ALL DIMENSIONS ARE IN MILS.
PIN (2) IS INTERNALLY CONNECTED TO BACK SIDE OF CHIP.

equivalent schematic



| COMPONENT COUNT† | |
|------------------|----|
| Transistors | 23 |
| Diodes | 6 |
| Resistors | 11 |
| Capacitors | 2 |

† Includes both amplifiers and all ESD, bias, and trim circuitry

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|------------------------------|
| Supply voltage, V_{DD} (see Note 1) | 12 V |
| Differential input voltage, V_{ID} (see Note 2) | $\pm V_{DD}$ |
| Input voltage range, V_I (any input, see Note 1) | -0.3 V to V_{DD} |
| Input current, I_I (each input) | ± 5 mA |
| Output current, I_O | ± 50 mA |
| Total current into V_{DD+} | ± 50 mA |
| Total current out of V_{DD-} | ± 50 mA |
| Duration of short-circuit current (at or below) 25°C (see Note 3) | unlimited |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A : TLV2711C | 0°C to 70°C |
| TLV2711I | -40°C to 85°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DBV package | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to V_{DD-} .
 2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below $V_{DD-} - 0.3$ V.
 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|---|---|--|--|
| DBV | 150 mW | 1.2 mW/°C | 96 mW | 78 mW |

recommended operating conditions

| | TLV2711C | | TLV2711I | | UNIT |
|---------------------------------------|-----------|-----------------|-----------|-----------------|------|
| | MIN | MAX | MIN | MAX | |
| Supply voltage, V_{DD} (see Note 1) | 2.7 | 10 | 2.7 | 10 | V |
| Input voltage range, V_I | V_{DD-} | $V_{DD+} - 1.3$ | V_{DD-} | $V_{DD+} - 1.3$ | V |
| Common-mode input voltage, V_{IC} | V_{DD-} | $V_{DD+} - 1.3$ | V_{DD-} | $V_{DD+} - 1.3$ | V |
| Operating free-air temperature, T_A | 0 | 70 | -40 | 85 | °C |

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-} .



electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2711C | | | TLV2711I | | | UNIT |
|--|---|-----------------------------|------------|-------------|-----------|-------------|-------------------------|------|------------------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IO} Input offset voltage | $V_{DD\pm} = \pm 1.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$ | Full range | 0.4 | | 3 | 0.4 | | 3 | mV |
| $\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage | | | 1 | | | 1 | | | $\mu\text{V}/^\circ\text{C}$ |
| Input offset voltage long-term drift (see Note 4) | | 25°C | 0.003 | | 0.003 | | $\mu\text{V}/\text{mo}$ | | |
| I_{IO} Input offset current | | 25°C | 0.5 | | 60 | | pA | | |
| I_{IB} Input bias current | | Full range | 150 | | 150 | | | | |
| | | 25°C | 60 | | 60 | | | | |
| | | Full range | 1 | | 150 | | | | |
| V_{ICR} Common-mode input voltage range | $ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$ | 25°C | 0 to 2 | -0.3 to 2.2 | 0 to 2 | -0.3 to 2.2 | V | | |
| | | Full range | 0 to 1.7 | | 0 to 1.7 | | | | |
| V_{OH} High-level output voltage | $I_{OH} = -100\ \mu\text{A}$ | 25°C | 2.94 | | 2.94 | | V | | |
| | $I_{OH} = -250\ \mu\text{A}$ | 25°C | 2.85 | | 2.85 | | | | |
| | | Full range | 2.6 | | 2.6 | | | | |
| V_{OL} Low-level output voltage | $V_{IC} = 1.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ | 25°C | 15 | | 15 | | mV | | |
| | $V_{IC} = 1.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$ | 25°C | 150 | | 150 | | | | |
| | | Full range | 500 | | 500 | | | | |
| A_{VD} Large-signal differential voltage amplification | $V_{IC} = 1.5\text{ V}$, $V_O = 1\text{ V to }2\text{ V}$ | $R_L = 10\text{ k}\Omega$ ‡ | 25°C | 3 | 7 | 3 | 7 | V/mV | |
| | | | Full range | 1 | | 1 | | | |
| | | $R_L = 1\text{ M}\Omega$ ‡ | 25°C | 600 | | 600 | | | |
| $r_{i(d)}$ Differential input resistance | | 25°C | 10^{12} | | 10^{12} | | Ω | | |
| $r_{i(c)}$ Common-mode input resistance | | 25°C | 10^{12} | | 10^{12} | | Ω | | |
| $C_{i(c)}$ Common-mode input capacitance | $f = 10\text{ kHz}$, | 25°C | 5 | | 5 | | pF | | |
| z_o Closed-loop output impedance | $f = 7\text{ kHz}$, $A_V = 1$ | 25°C | 200 | | 200 | | Ω | | |
| $CMRR$ Common-mode rejection ratio | $V_{IC} = 0\text{ to }1.7\text{ V}$, $R_S = 50\ \Omega$, $V_O = 1.5\text{ V}$ | 25°C | 65 | 83 | | 65 | 83 | dB | |
| | | Full range | 60 | | 60 | | | | |
| k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$) | $V_{DD} = 2.7\text{ V to }8\text{ V}$, No load, $V_{IC} = V_{DD}/2$ | 25°C | 80 | 95 | | 80 | 95 | dB | |
| | | Full range | 80 | | 80 | | | | |
| I_{DD} Supply current | $V_O = 1.5\text{ V}$, No load | 25°C | 11 | | 25 | | μA | | |
| | | Full range | 30 | | 30 | | | | |

† Full range for the TLV2711C is 0°C to 70°C. Full range for the TLV2711I is -40°C to 85°C.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2711C | | | TLV2711I | | | UNIT | |
|-------------|---|---|----------|-------|-----|----------|-------|-----|------------------------|-----|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| SR | Slew rate at unity gain $V_O = 1.1\text{ V to }1.9\text{ V}$, $R_L = 10\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | 0.01 | 0.025 | | 0.01 | 0.025 | | V/ μ s | |
| | | Full range | 0.005 | | | 0.005 | | | | |
| V_n | Equivalent input noise voltage | f = 10 Hz | 80 | | | 80 | | | nV/ $\sqrt{\text{Hz}}$ | |
| | | f = 1 kHz | 22 | | | 22 | | | | |
| $V_{N(PP)}$ | Peak-to-peak equivalent input noise voltage | f = 0.1 Hz to 1 Hz | 660 | | | 660 | | | nV | |
| | | f = 0.1 Hz to 10 Hz | 880 | | | 880 | | | | |
| I_n | Equivalent input noise current | 25°C | 0.6 | | | 0.6 | | | fA/ $\sqrt{\text{Hz}}$ | |
| | Gain-bandwidth product | f = 10 kHz, $R_L = 10\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | 56 | | | 56 | | | kHz |
| BOM | Maximum output-swing bandwidth | $V_{O(PP)} = 1\text{ V}$, $R_L = 10\text{ k}\Omega$ ‡, $A_V = 1$, $C_L = 100\text{ pF}$ ‡ | 25°C | 7 | | | 7 | | | kHz |
| ϕ_m | Phase margin at unity gain | $R_L = 10\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡ | 25°C | 56° | | | 56° | | | |
| | Gain margin | | 25°C | 20 | | | 20 | | | dB |

† Full range is –40°C to 85°C.

‡ Referenced to 1.5 V



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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2711C | | | TLV2711I | | | UNIT |
|--|---|------------|-----------------------------|-------------|-----------|-------------|-------------------------|-----|------------------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IO} Input offset voltage | $V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$ | Full range | 0.45 | | 3 | 0.45 | | 3 | mV |
| $\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage | | | 0.5 | | | 0.5 | | | $\mu\text{V}/^\circ\text{C}$ |
| Input offset voltage long-term drift (see Note 4) | | 25°C | 0.003 | | 0.003 | | $\mu\text{V}/\text{mo}$ | | |
| I_{IO} Input offset current | | 25°C | 0.5 | 60 | 0.5 | 60 | pA | | |
| | | Full range | 150 | | 150 | | | | |
| I_{IB} Input bias current | 25°C | 1 | 60 | 1 | 60 | pA | | | |
| | Full range | 150 | | 150 | | | | | |
| V_{ICR} Common-mode input voltage range | $ V_{IO} \leq 5\text{ mV}$ $R_S = 50\ \Omega$ | 25°C | 0 to 4 | -0.3 to 4.2 | 0 to 4 | -0.3 to 4.2 | V | | |
| | | Full range | 0 to 3.5 | | 0 to 3.5 | | | | |
| V_{OH} High-level output voltage | $I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -250\ \mu\text{A}$ | 25°C | 4.95 | | 4.95 | | V | | |
| | | 25°C | 4.875 | | 4.875 | | | | |
| | | Full range | 4.6 | | 4.6 | | | | |
| V_{OL} Low-level output voltage | $V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ $V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$ | 25°C | 12 | | 12 | | mV | | |
| | | 25°C | 120 | | 120 | | | | |
| | | Full range | 500 | | 500 | | | | |
| A_{VD} Large-signal differential voltage amplification | $V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$ | 25°C | $R_L = 10\text{ k}\Omega$ ‡ | | 6 | 12 | V/mV | | |
| | | | Full range | | 3 | | | | |
| | | 25°C | $R_L = 1\text{ M}\Omega$ ‡ | | 800 | | 800 | | |
| $r_{i(d)}$ Differential input resistance | | 25°C | 10^{12} | | 10^{12} | | Ω | | |
| $r_{i(c)}$ Common-mode input resistance | | 25°C | 10^{12} | | 10^{12} | | Ω | | |
| $c_{i(c)}$ Common-mode input capacitance | $f = 10\text{ kHz}$, | 25°C | 5 | | 5 | | pF | | |
| z_o Closed-loop output impedance | $f = 7\text{ kHz}$, $A_V = 1$ | 25°C | 200 | | 200 | | Ω | | |
| CMRR Common-mode rejection ratio | $V_{IC} = 0\text{ to }2.7\text{ V}$, $R_S = 50\ \Omega$, $V_O = 2.5\text{ V}$ | 25°C | 70 | 83 | 70 | 83 | dB | | |
| | | Full range | 70 | | 70 | | | | |
| k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$) | $V_{DD} = 4.4\text{ V to }8\text{ V}$, No load, $V_{IC} = V_{DD}/2$ | 25°C | 80 | 95 | 80 | 95 | dB | | |
| | | Full range | 80 | | 80 | | | | |
| I_{DD} Supply current | $V_O = 2.5\text{ V}$, No load | 25°C | 13 | 25 | 13 | 25 | μA | | |
| | | Full range | 30 | | 30 | | | | |

† Full range for the TLV2711C is 0°C to 70°C. Full range for the TLV2711I is -40°C to 85°C.

‡ Referenced to 1.5 V

NOTE 5: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A † | TLV2711C | | | TLV2711I | | | UNIT |
|---|--|------------|----------|-------|-----|----------|-------|-----|------------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR Slew rate at unity gain | $V_O = 1.5\text{ V to }3.5\text{ V}, R_L = 10\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$ | 25°C | 0.01 | 0.025 | | 0.01 | 0.025 | | V/ μs |
| | | Full range | 0.005 | | | 0.005 | | | |
| V_n Equivalent input noise voltage | $f = 10\text{ Hz}$ | 25°C | 72 | | | 72 | | | nV/ $\sqrt{\text{Hz}}$ |
| | $f = 1\text{ kHz}$ | 25°C | 21 | | | 21 | | | |
| $V_{N(PP)}$ Peak-to-peak equivalent input noise voltage | $f = 0.1\text{ Hz to }1\text{ Hz}$ | 25°C | 600 | | | 600 | | | nV |
| | $f = 0.1\text{ Hz to }10\text{ Hz}$ | 25°C | 800 | | | 800 | | | |
| I_n Equivalent input noise current | | 25°C | 0.6 | | | 0.6 | | | fA/ $\sqrt{\text{Hz}}$ |
| Gain-bandwidth product | $f = 10\text{ kHz}, R_L = 10\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$ | 25°C | 65 | | | 65 | | | kHz |
| B_{OM} Maximum output-swing bandwidth | $V_{O(PP)} = 2\text{ V}, R_L = 10\text{ k}\Omega^\ddagger, A_V = 1, C_L = 100\text{ pF}^\ddagger$ | 25°C | 7 | | | 7 | | | kHz |
| ϕ_m Phase margin at unity gain | $R_L = 10\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$ | 25°C | 60° | | | 60° | | | |
| Gain margin | | 25°C | 22 | | | 22 | | | dB |

† Full range is -40°C to 85°C .

‡ Referenced to 1.5 V

electrical characteristics at $V_{DD} = 3\text{ V}, T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | TLV2711Y | | | UNIT |
|--|---|------------------------------------|-----|-----|---------------|
| | | MIN | TYP | MAX | |
| V_{IO} Input offset voltage | $V_{DD\pm} = \pm 1.5\text{ V}, V_O = 0, V_{IC} = 0, R_S = 50\ \Omega$ | 0.47 | | | mV |
| I_{IO} Input offset current | | 0.5 | | | pA |
| I_{IB} Input bias current | | 1 | | | pA |
| V_{ICR} Common-mode input voltage range | $ V_{IO} \leq 5\text{ mV}, R_S = 50\ \Omega$ | -0.3 to 2.2 | | | V |
| V_{OH} High-level output voltage | $I_{OH} = -100\ \mu\text{A}$ | 2.94 | | | V |
| | $I_{OH} = -200\ \mu\text{A}$ | 2.85 | | | |
| V_{OL} Low-level output voltage | $V_{IC} = 0, I_{OL} = 50\ \mu\text{A}$ | 15 | | | mV |
| | $V_{IC} = 0, I_{OL} = 500\ \mu\text{A}$ | 150 | | | |
| A_{VD} Large-signal differential voltage amplification | $V_{IC} = 1.5\text{ V}, V_O = 1\text{ V to }2\text{ V}$ | $R_L = 10\text{ k}\Omega^\ddagger$ | 7 | | V/mV |
| | | $R_L = 1\text{ M}\Omega^\ddagger$ | 600 | | |
| $r_{i(d)}$ Differential input resistance | | 10^{12} | | | Ω |
| $r_{i(c)}$ Common-mode input resistance | | 10^{12} | | | Ω |
| $c_{i(c)}$ Common-mode input capacitance | $f = 10\text{ kHz}$ | 5 | | | pF |
| z_o Closed-loop output impedance | $f = 7\text{ kHz}, A_V = 1$ | 200 | | | Ω |
| CMRR Common-mode rejection ratio | $V_{IC} = 0\text{ to }1.7\text{ V}, V_O = 1.5\text{ V}, R_S = 50\ \Omega$ | 83 | | | dB |
| k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD} = 2.7\text{ V to }8\text{ V}, V_{IC} = V_{DD}/2, \text{ No load}$ | 95 | | | dB |
| I_{DD} Supply current | $V_O = 1.5\text{ V}, \text{ No load}$ | 11 | | | μA |

† Referenced to 1.5 V



electrical characteristics at $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | TLV2711Y | | | UNIT |
|--|--|-----------------------------------|-----|-----|---------------|
| | | MIN | TYP | MAX | |
| V_{IO} Input offset voltage | $V_{DD} \pm \pm 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $V_O = 0$ | 0.45 | | | mV |
| I_{IO} Input offset current | | 0.5 | | | pA |
| I_{IB} Input bias current | | 1 | | | pA |
| V_{ICR} Common-mode input voltage range | $ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$ | -0.3 to 4.2 | | | V |
| V_{OH} High-level output voltage | $I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -250\ \mu\text{A}$ | 4.95 | | | V |
| | | 4.875 | | | |
| V_{OL} Low-level output voltage | $V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ | 12 | | | mV |
| | $V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$ | 120 | | | |
| A_{VD} Large-signal differential voltage amplification | $V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$ | $R_L = 10\text{ k}\Omega^\dagger$ | 12 | | V/mV |
| | | $R_L = 1\text{ M}\Omega^\dagger$ | 800 | | |
| $r_{i(d)}$ Differential input resistance | | 10^{12} | | | Ω |
| $r_{i(c)}$ Common-mode input resistance | | 10^{12} | | | Ω |
| $c_{i(c)}$ Common-mode input capacitance | $f = 10\text{ kHz}$ | 5 | | | pF |
| z_o Closed-loop output impedance | $f = 7\text{ kHz}$, $A_V = 1$ | 200 | | | Ω |
| CMRR Common-mode rejection ratio | $V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$ | 83 | | | dB |
| k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD} = 4.4\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load | 95 | | | dB |
| I_{DD} Supply current | $V_O = 2.5\text{ V}$, No load | 13 | | | μA |

† Referenced to 1.5 V

TYPICAL CHARACTERISTICS

Table of Graphs

| | | | FIGURE |
|-----------------|--|---|------------------------|
| V_{IO} | Input offset voltage | Distribution vs Common-mode input voltage | 2, 3 4, 5 |
| αV_{IO} | Input offset voltage temperature coefficient | Distribution | 6, 7 |
| I_{IB}/I_{IO} | Input bias and input offset currents | vs Free-air temperature | 8 |
| V_I | Input voltage | vs Supply voltage vs Free-air temperature | 9 10 |
| V_{OH} | High-level output voltage | vs High-level output current | 11, 14 |
| V_{OL} | Low-level output voltage | vs Low-level output current | 12, 13, 15 |
| $V_{O(PP)}$ | Maximum peak-to-peak output voltage | vs Frequency | 16 |
| I_{OS} | Short-circuit output current | vs Supply voltage vs Free-air temperature | 17 18 |
| V_O | Output voltage | vs Differential input voltage | 19, 20 |
| A_{VD} | Large-signal differential voltage amplification and phase margin | vs Load resistance vs Frequency vs Free-air temperature | 21 22, 23 24, 25 |
| z_o | Output impedance | vs Frequency | 26, 27 |
| CMRR | Common-mode rejection ratio | vs Frequency vs Free-air temperature | 28 29 |
| k_{SVR} | Supply-voltage rejection ratio | vs Frequency vs Free-air temperature | 30, 31 32 |
| I_{DD} | Supply current | vs Supply voltage | 33 |
| SR | Slew rate | vs Load capacitance vs Free-air temperature | 34 35 |
| V_O | Large-signal pulse response | vs Time | 36, 37, 38, 39 |
| | Inverting small-signal pulse response | | 40, 41 |
| | Small-signal pulse response | | 42, 43 |
| V_n | Equivalent input noise voltage | vs Frequency | 44, 45 |
| | Noise voltage (referred to input) | Over a 10-second period | 46 |
| THD + N | Total harmonic distortion plus noise | vs Frequency | 47 |
| | Gain-bandwidth product | vs Free-air temperature vs Supply voltage | 48 49 |
| ϕ_m | Phase margin | vs Frequency vs Load capacitance | 23, 24 50 |
| | Gain margin | vs Load capacitance | 51 |
| B_1 | Unity-gain bandwidth | vs Load capacitance | 52 |

TYPICAL CHARACTERISTICS

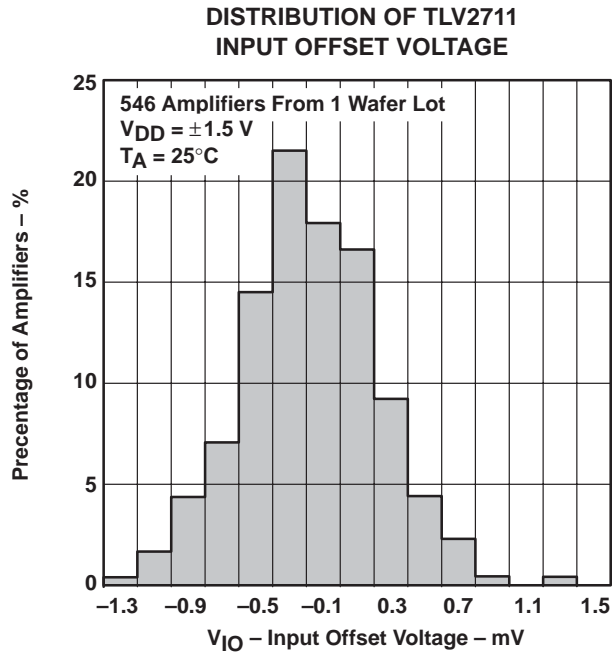


Figure 2

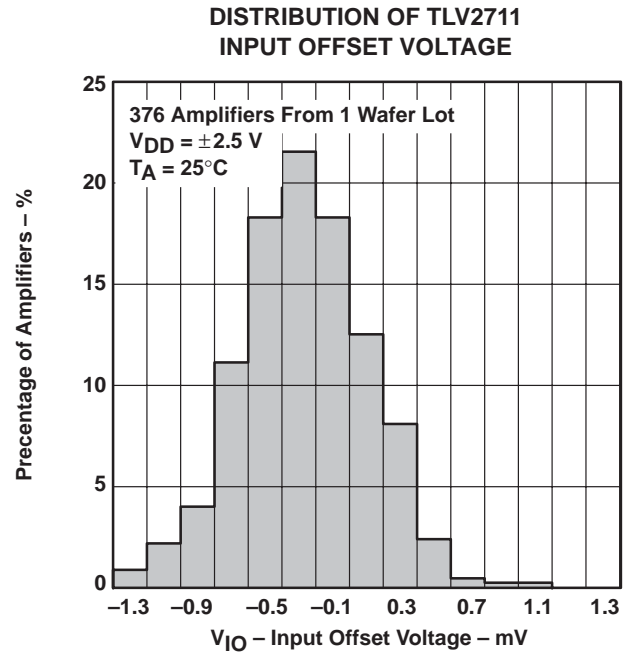


Figure 3

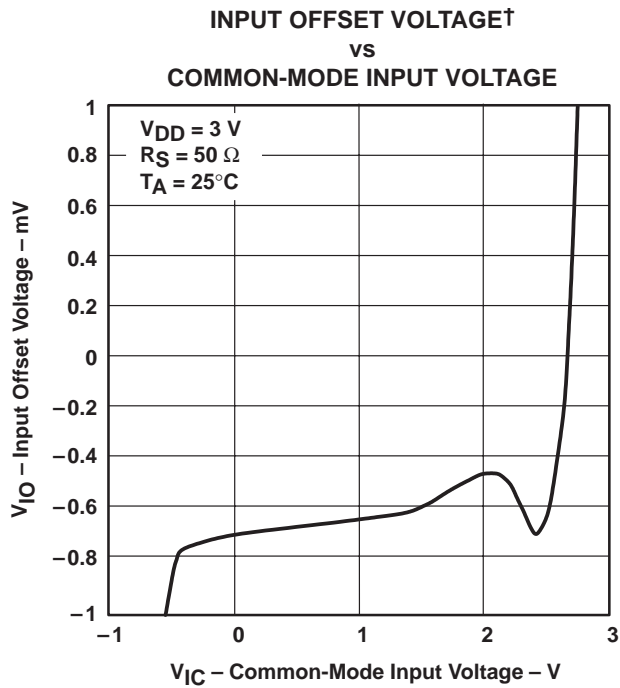


Figure 4

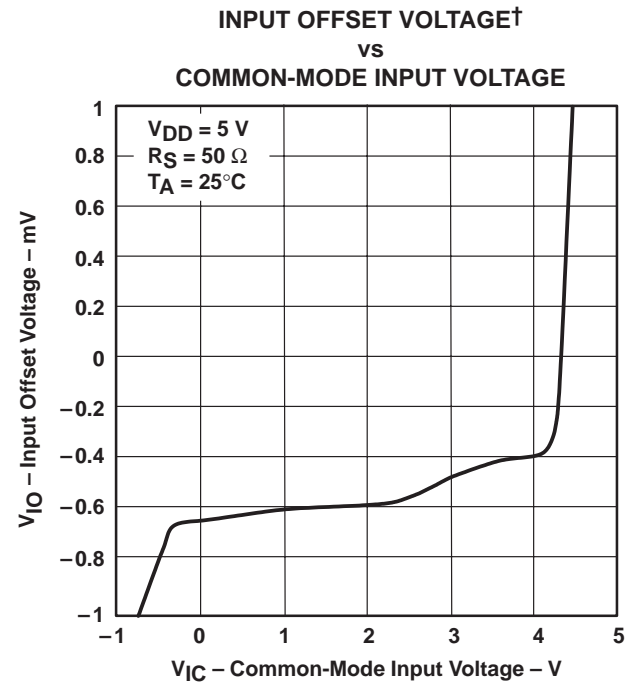


Figure 5

† For all curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 \text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

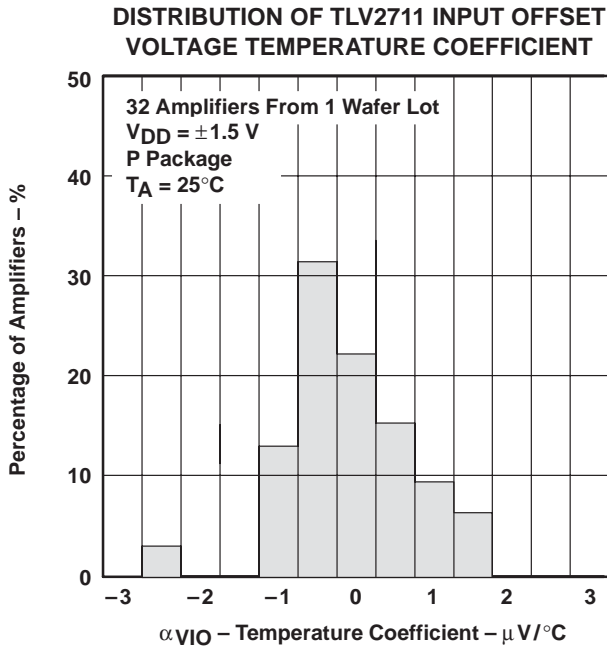


Figure 6

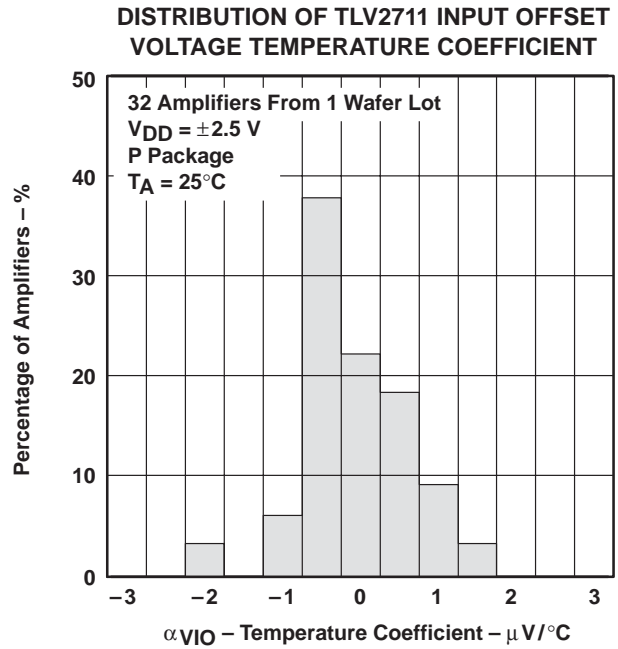


Figure 7

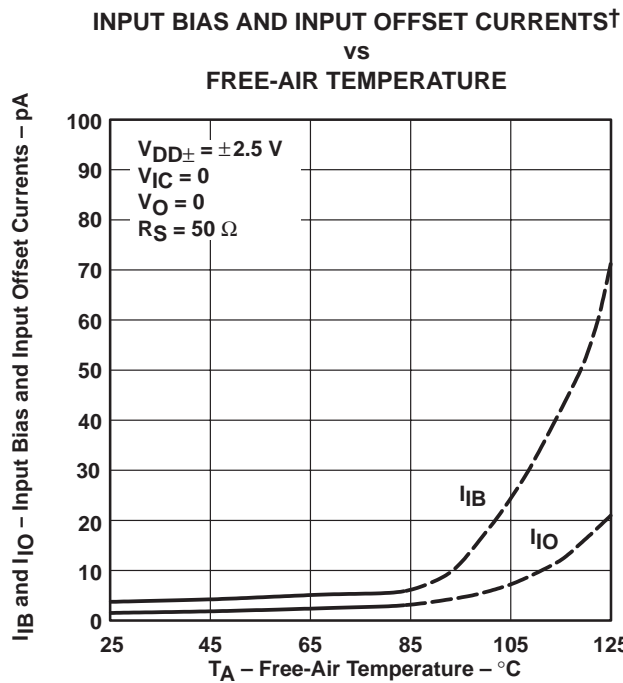


Figure 8

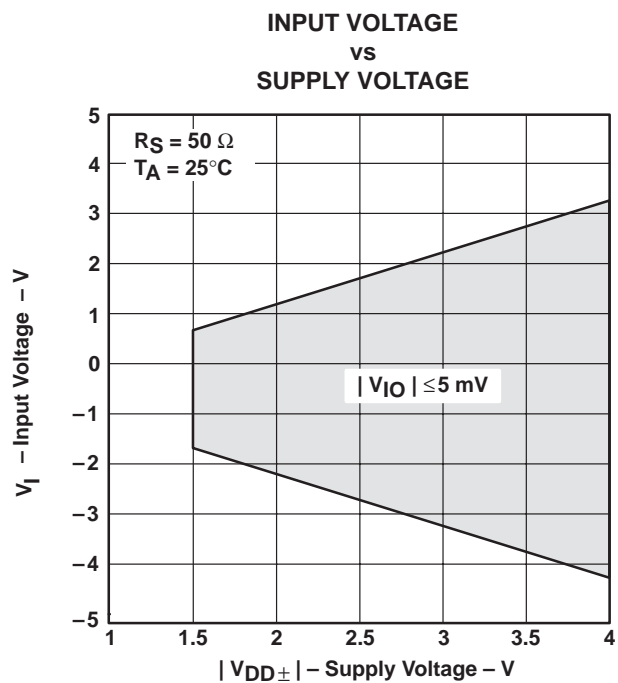
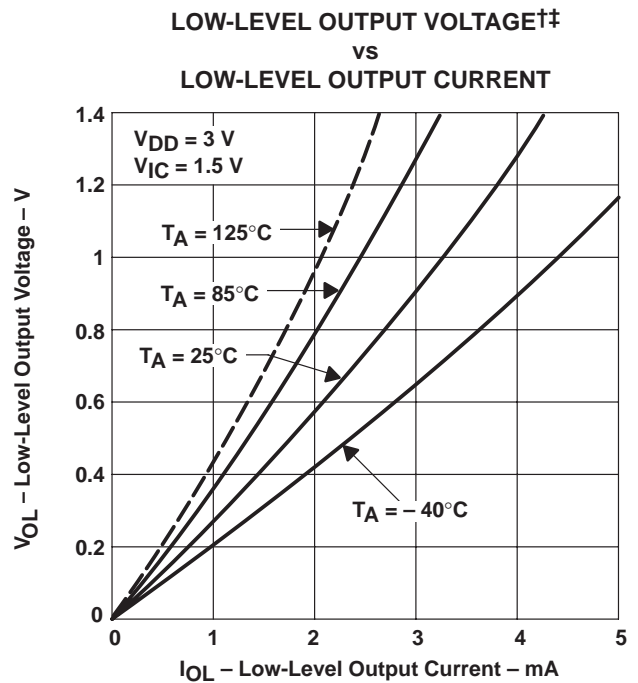
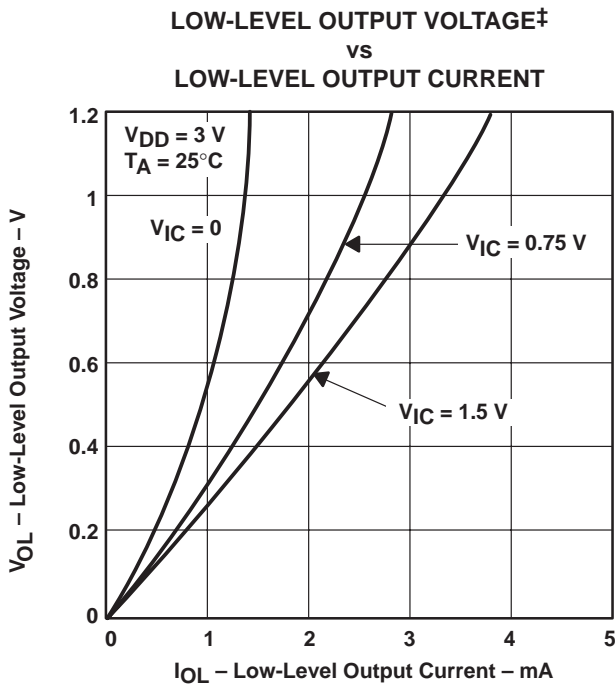
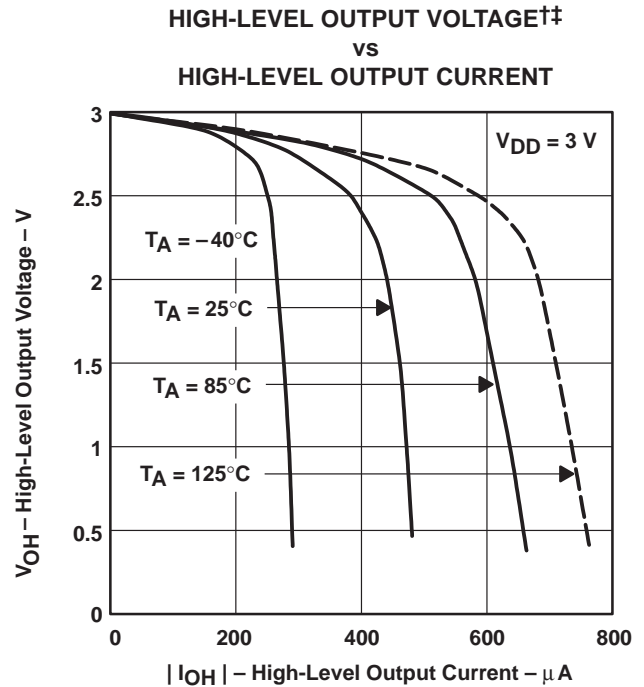
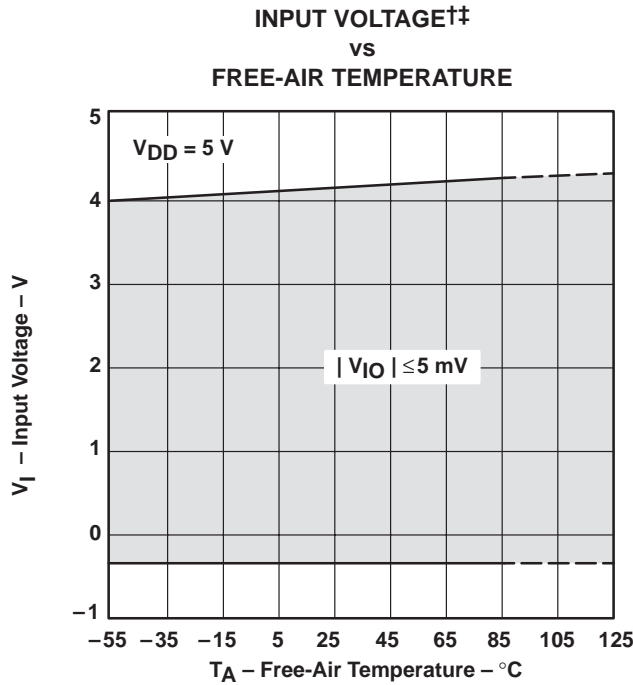


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

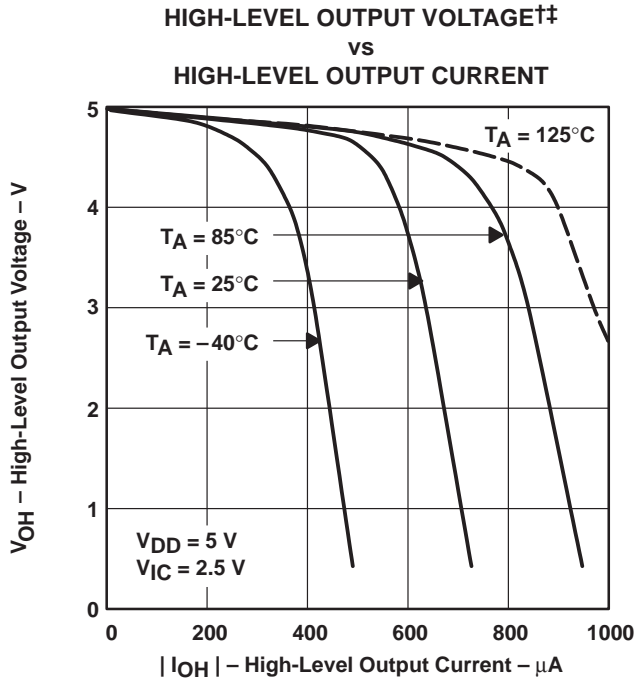


Figure 14

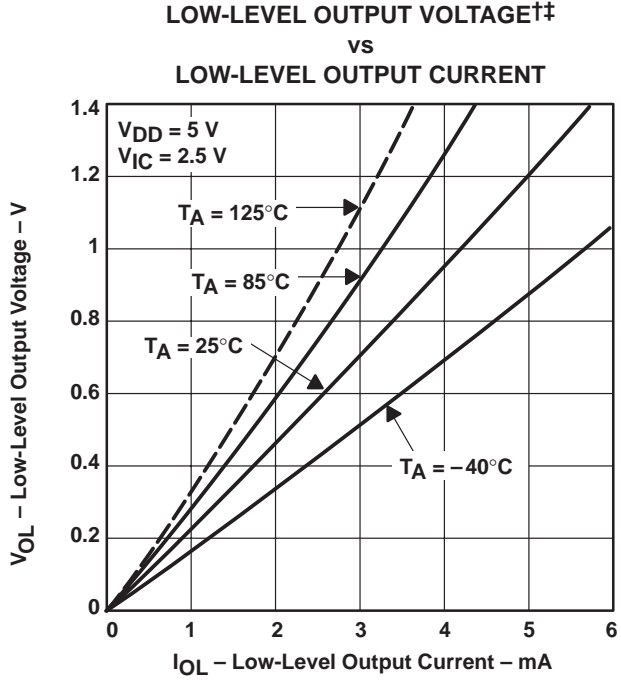


Figure 15

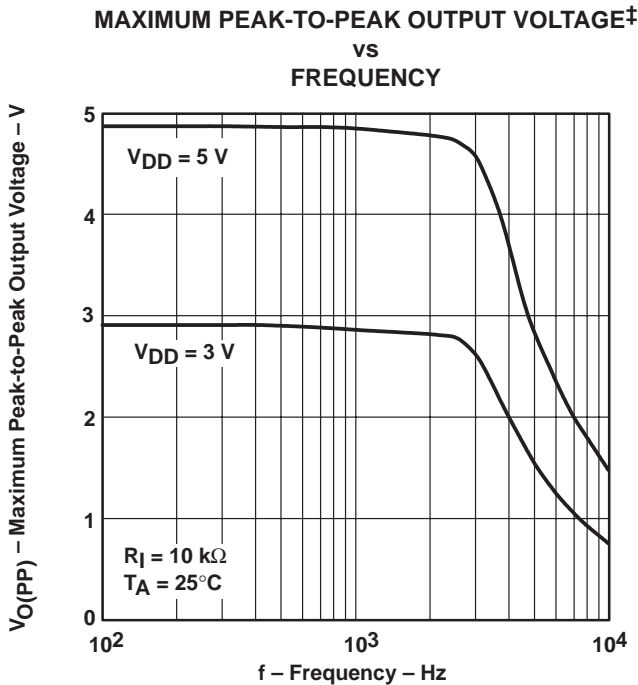


Figure 16

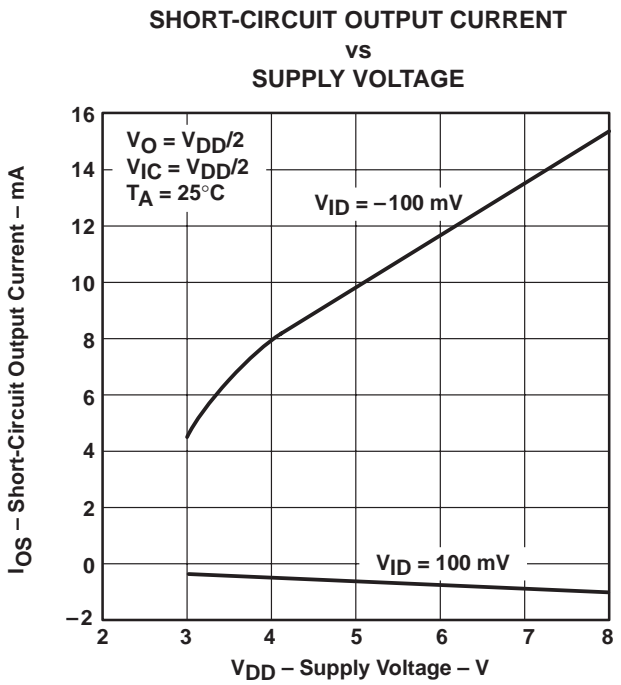
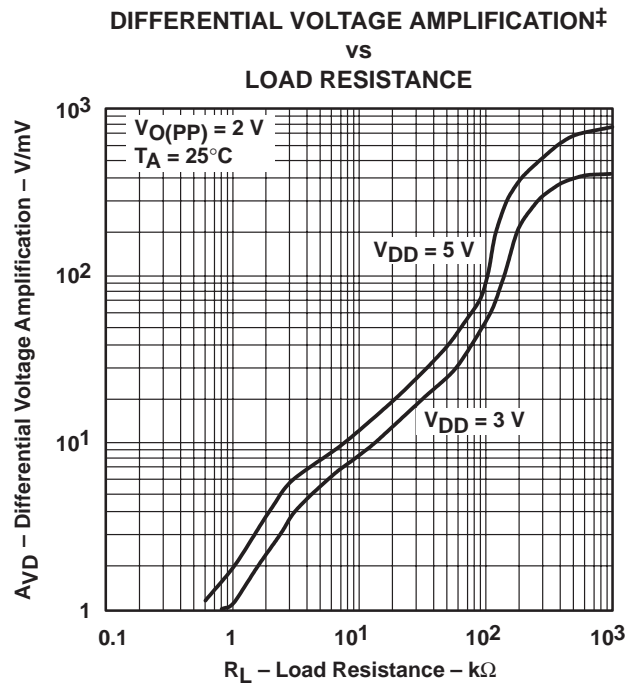
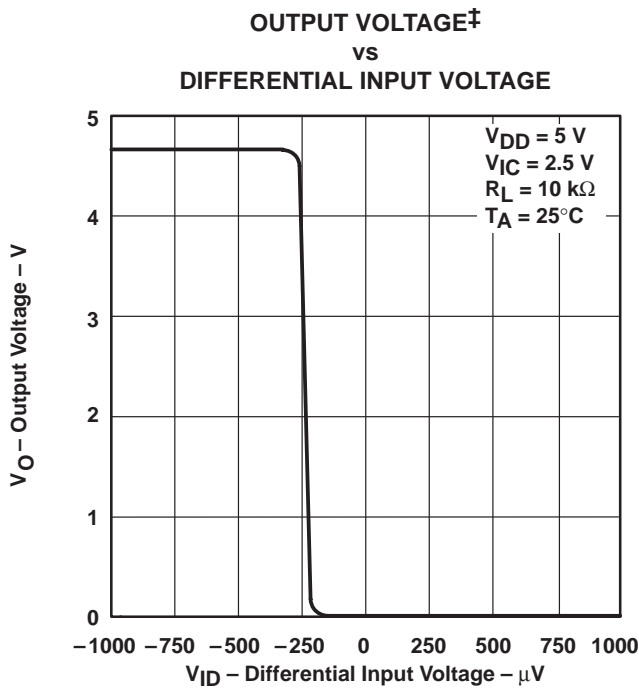
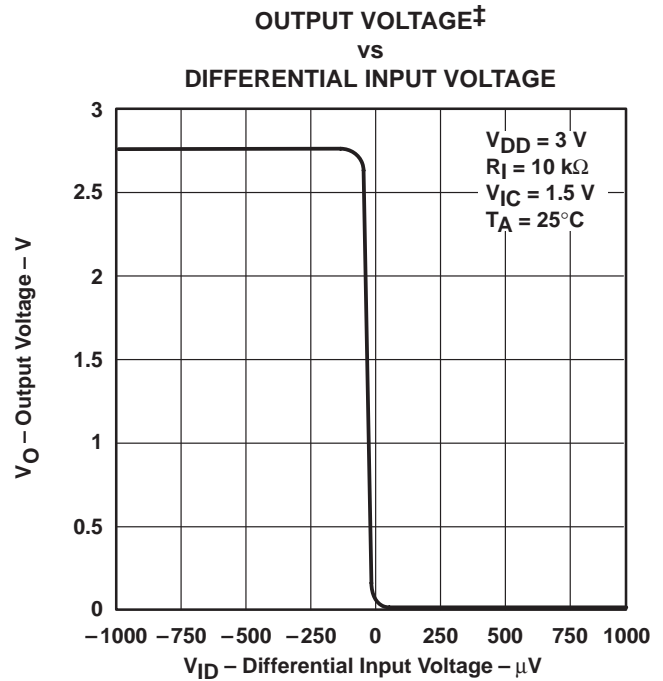
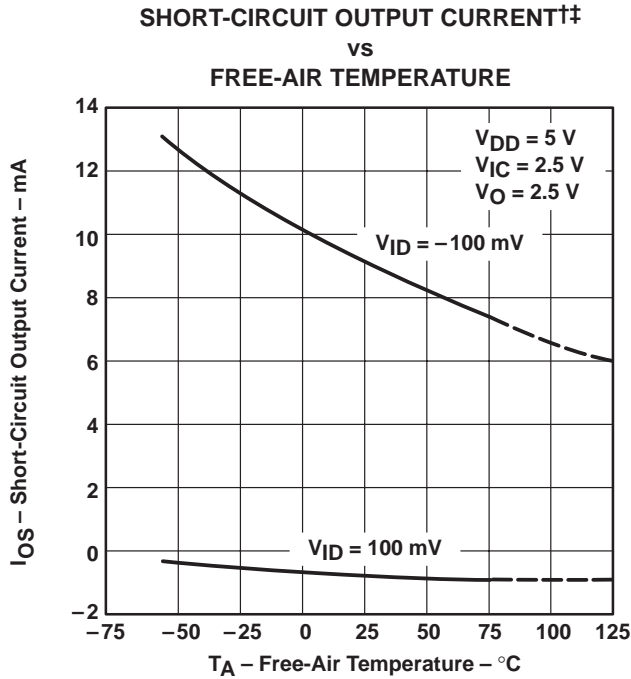


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V . For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V .

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
 AMPLIFICATION AND PHASE MARGIN†

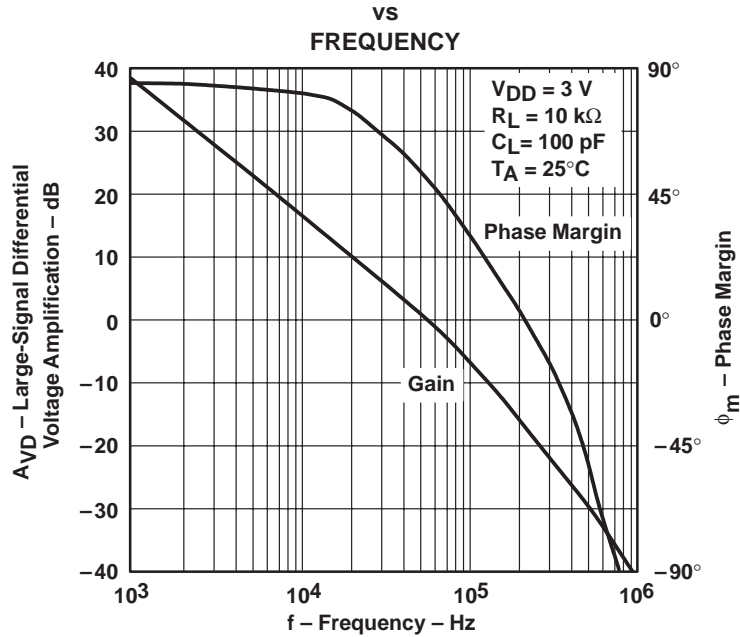


Figure 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
 AMPLIFICATION AND PHASE MARGIN†

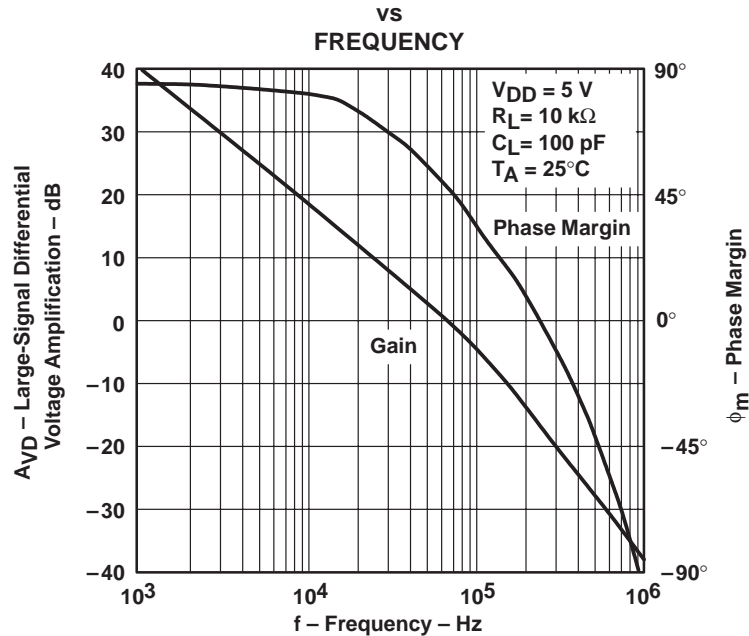


Figure 23

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

**LARGE-SIGNAL DIFFERENTIAL
 VOLTAGE AMPLIFICATION†‡
 vs
 FREE-AIR TEMPERATURE**

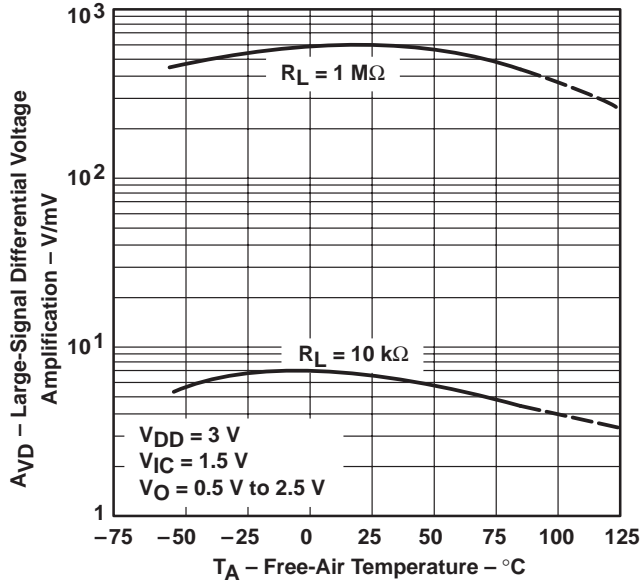


Figure 24

**LARGE-SIGNAL DIFFERENTIAL
 VOLTAGE AMPLIFICATION†‡
 vs
 FREE-AIR TEMPERATURE**

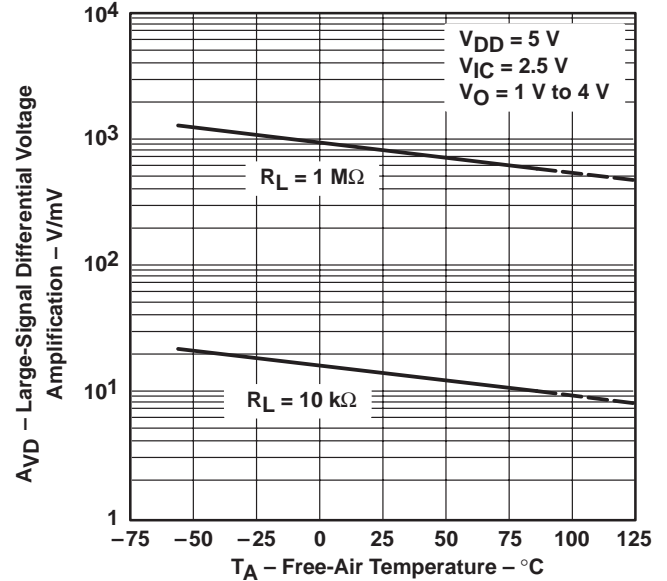


Figure 25

**OUTPUT IMPEDANCE‡
 vs
 FREQUENCY**

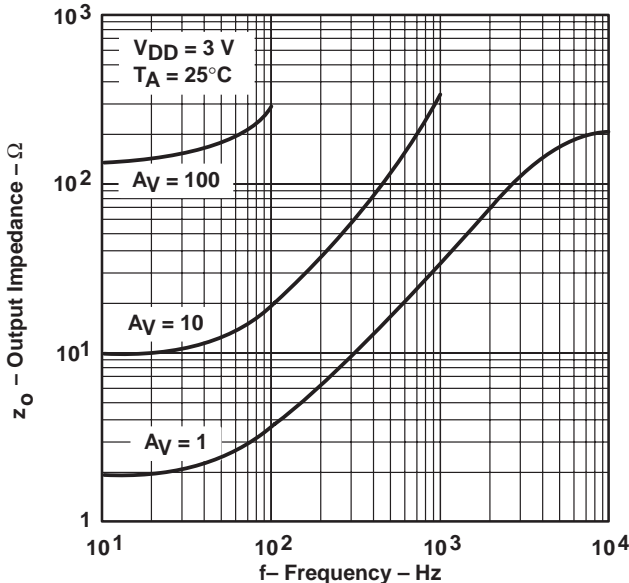


Figure 26

**OUTPUT IMPEDANCE‡
 vs
 FREQUENCY**

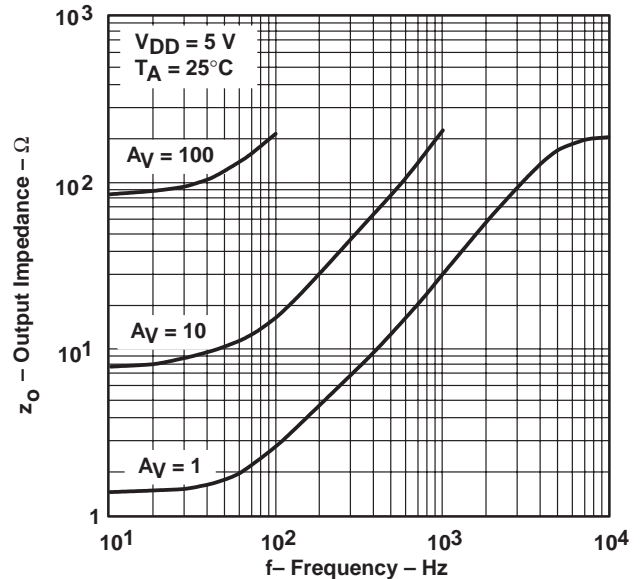


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

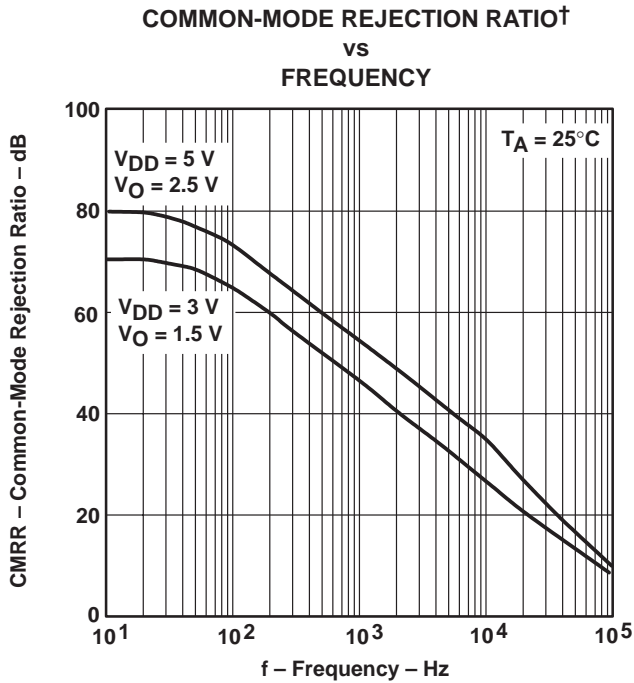


Figure 28

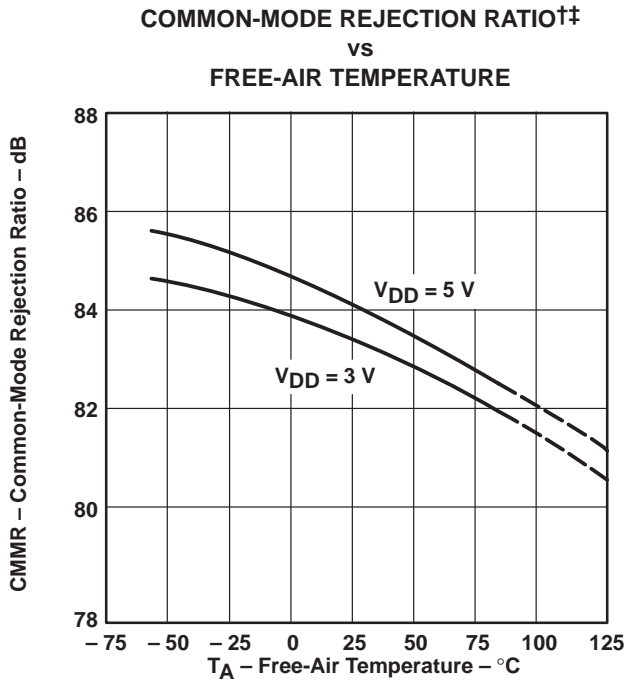


Figure 29

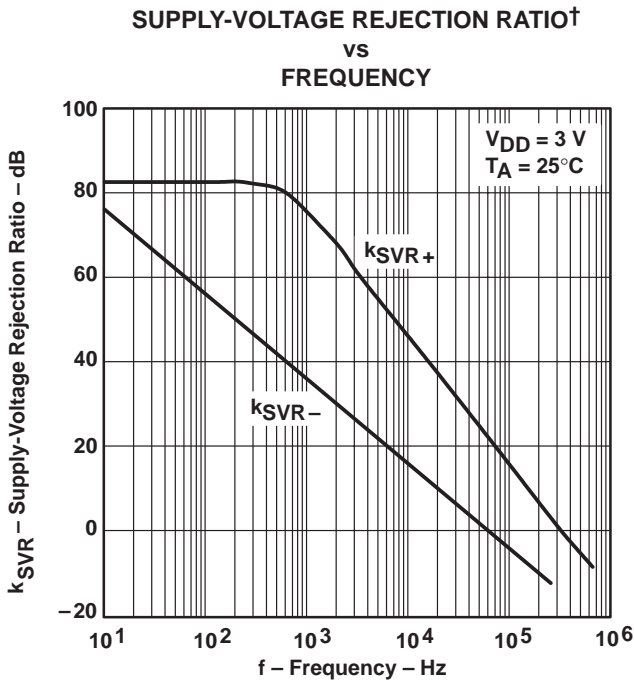


Figure 30

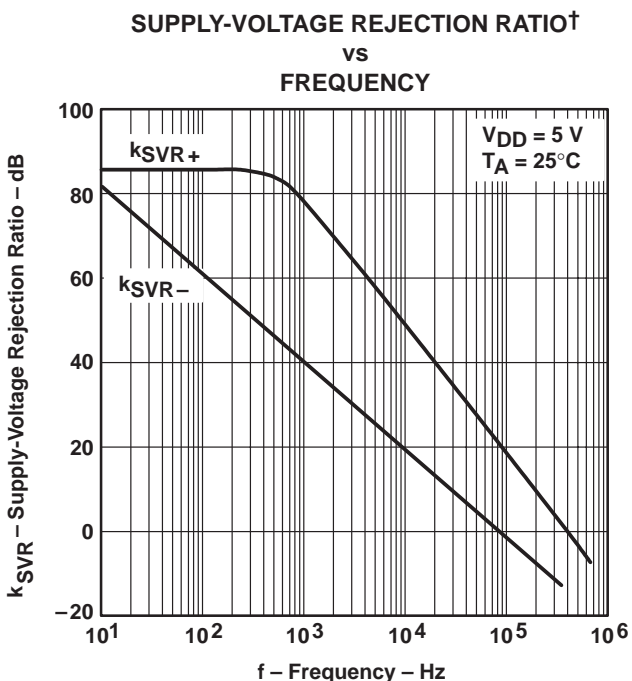
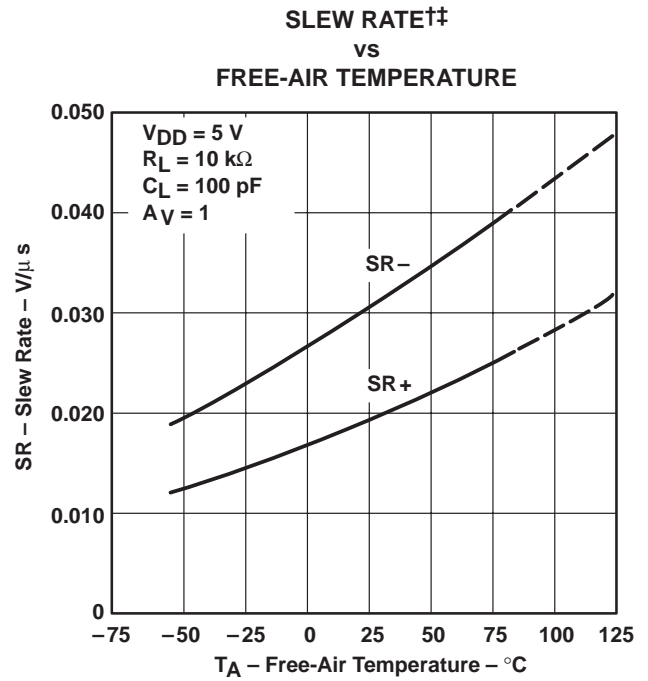
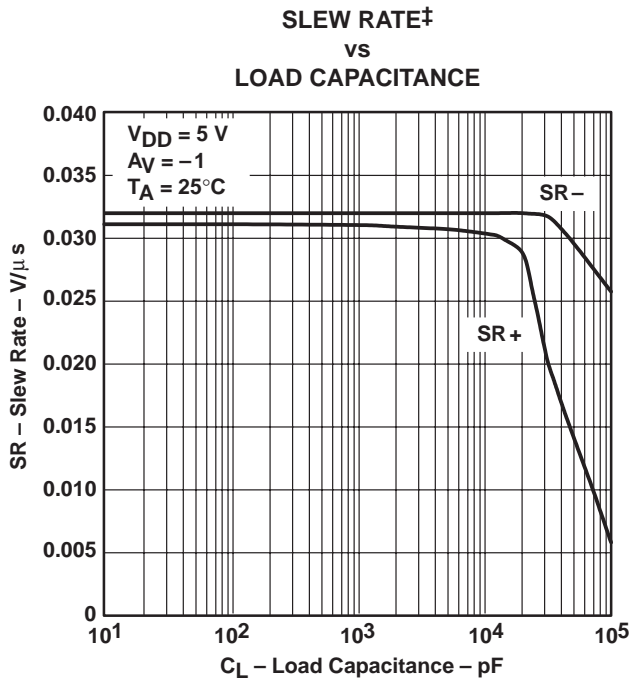
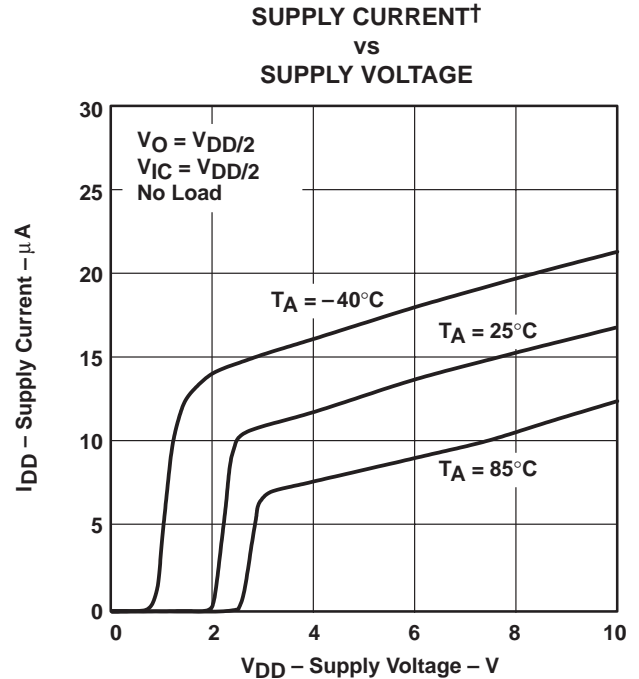
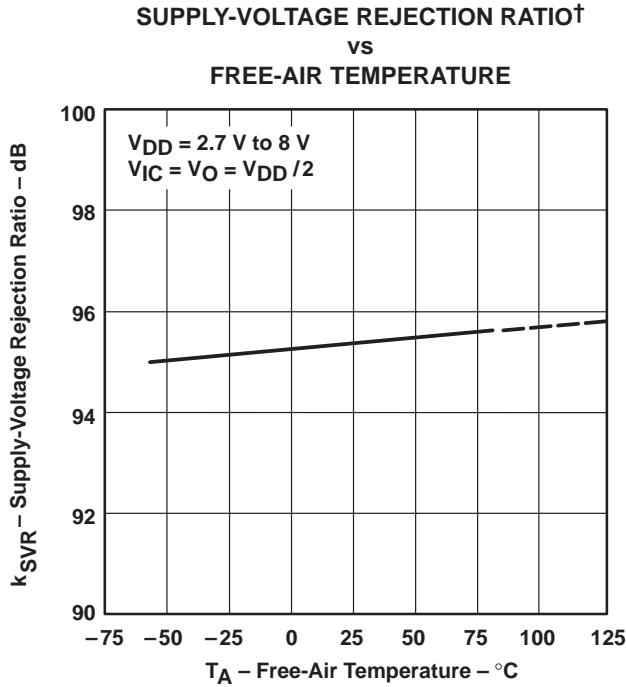


Figure 31

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.
 ‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE†

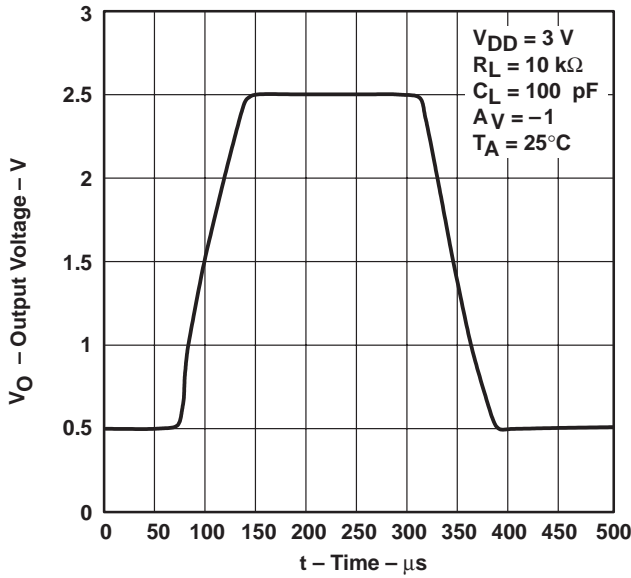


Figure 36

INVERTING LARGE-SIGNAL PULSE RESPONSE†

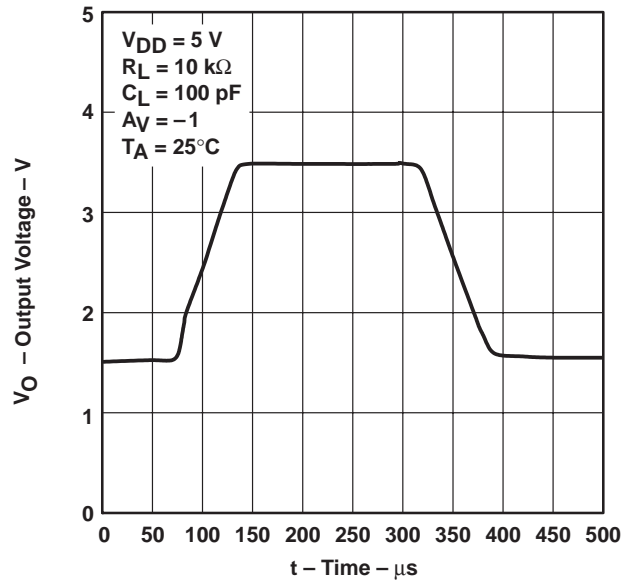


Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

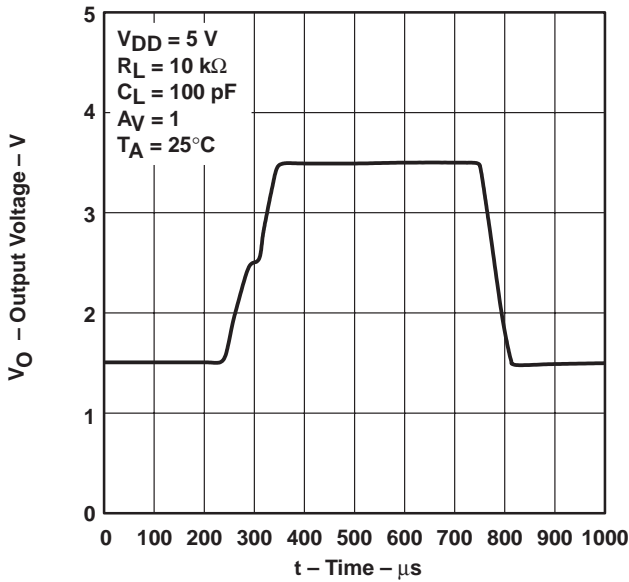


Figure 38

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

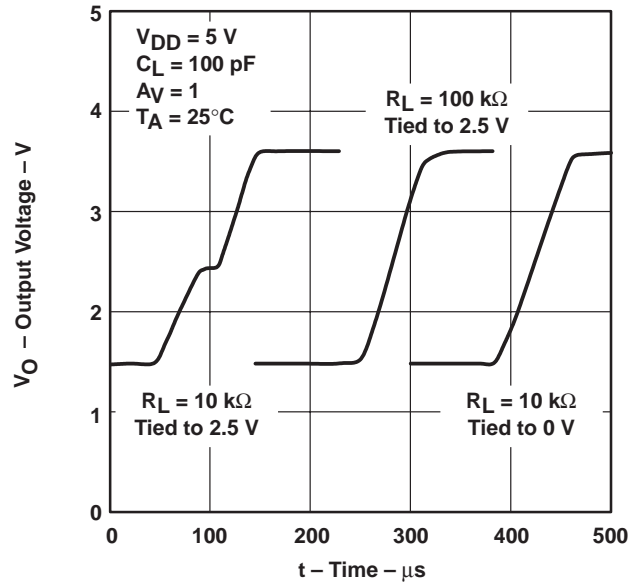


Figure 39

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

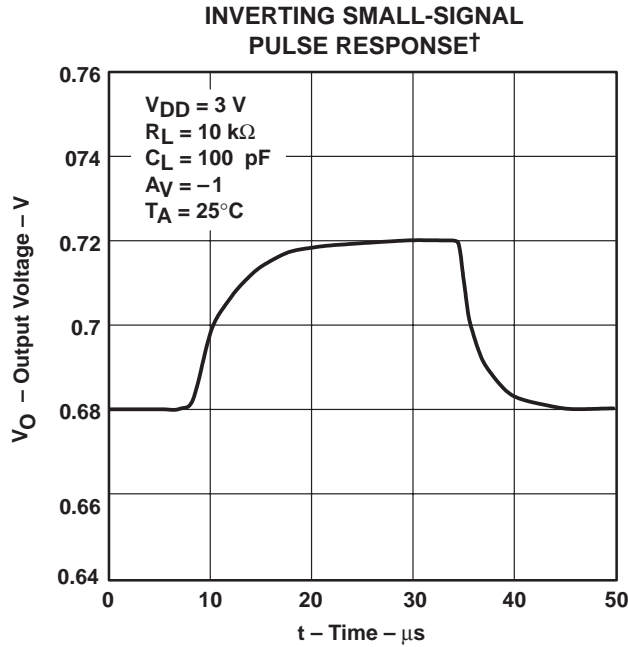


Figure 40

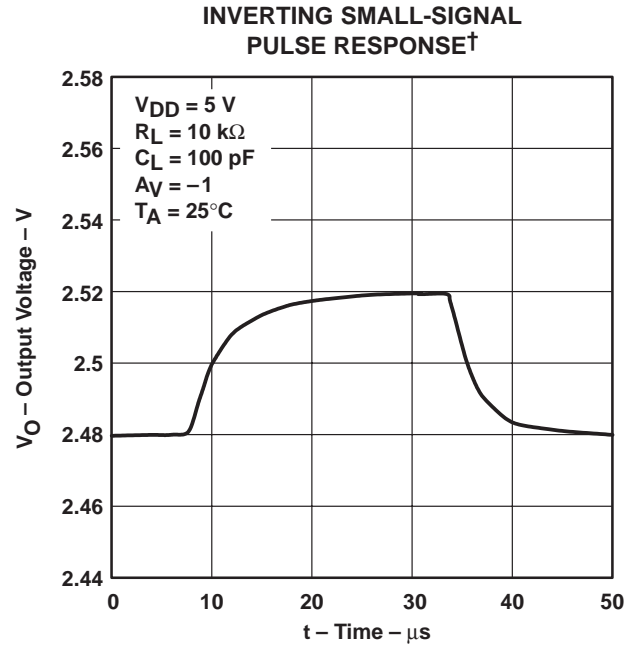


Figure 41

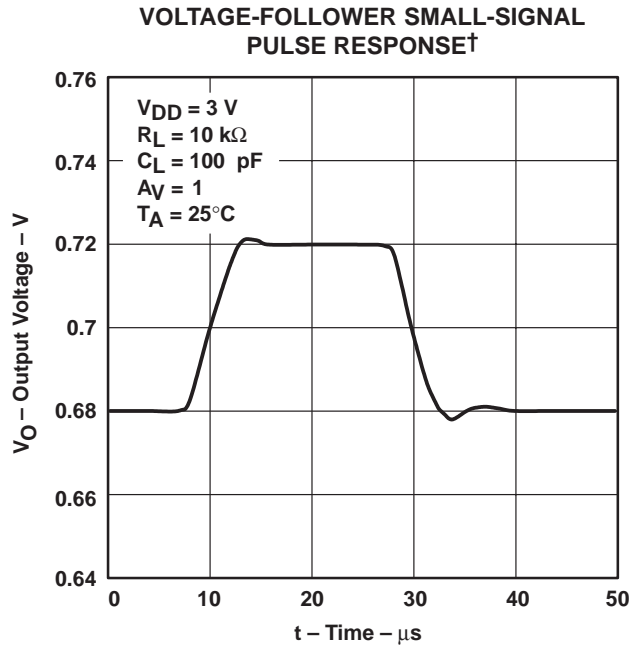


Figure 42

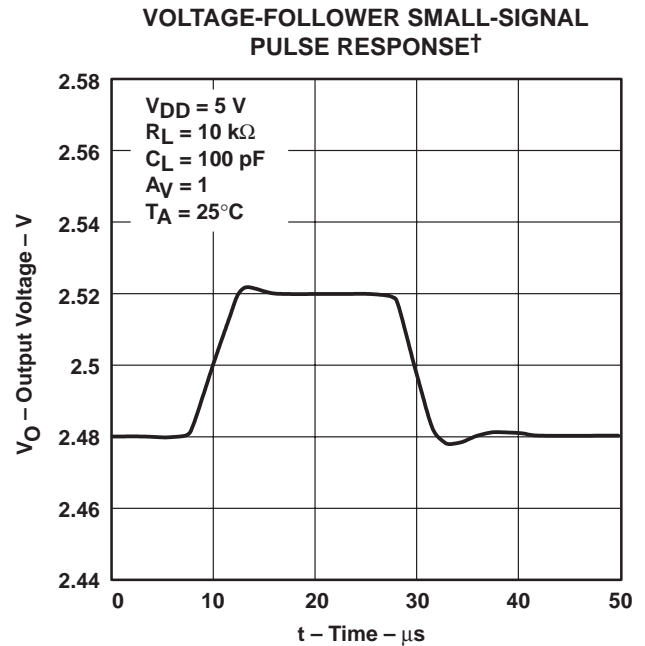


Figure 43

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE†
 VS
 FREQUENCY

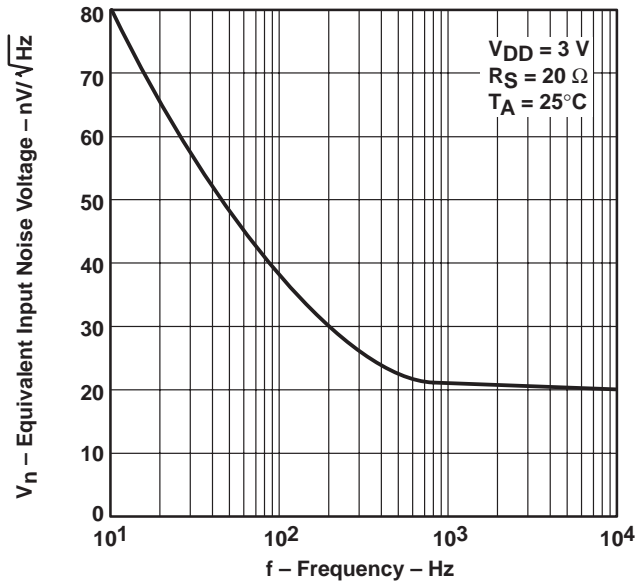


Figure 44

EQUIVALENT INPUT NOISE VOLTAGE†
 VS
 FREQUENCY

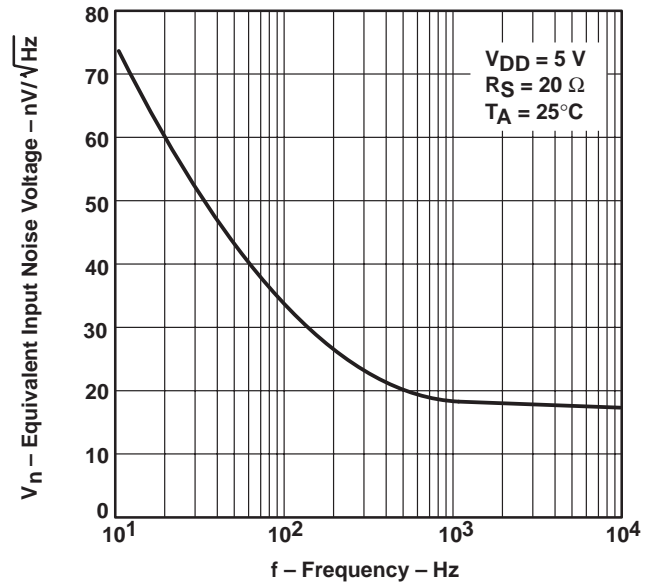


Figure 45

INPUT NOISE VOLTAGE OVER
 A 10-SECOND PERIOD†

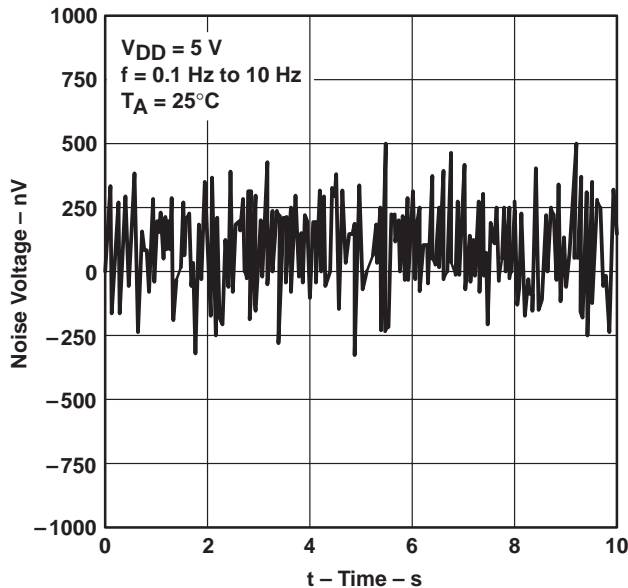


Figure 46

TOTAL HARMONIC DISTORTION PLUS NOISE†
 VS
 FREQUENCY

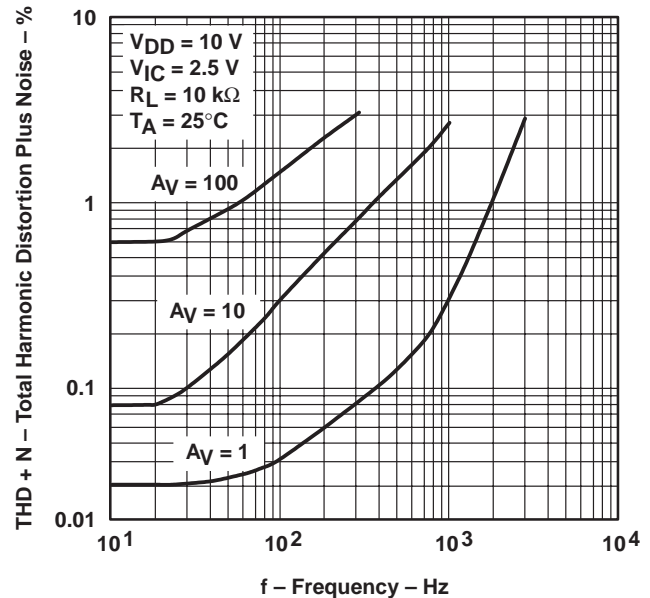
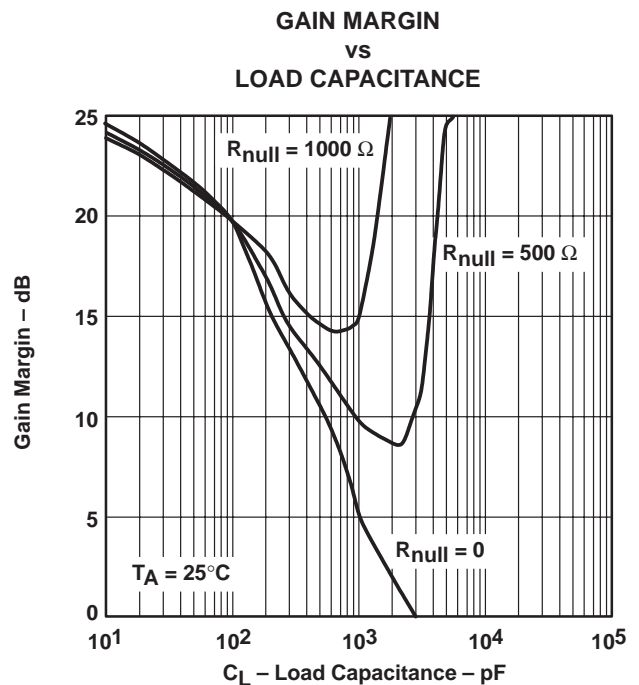
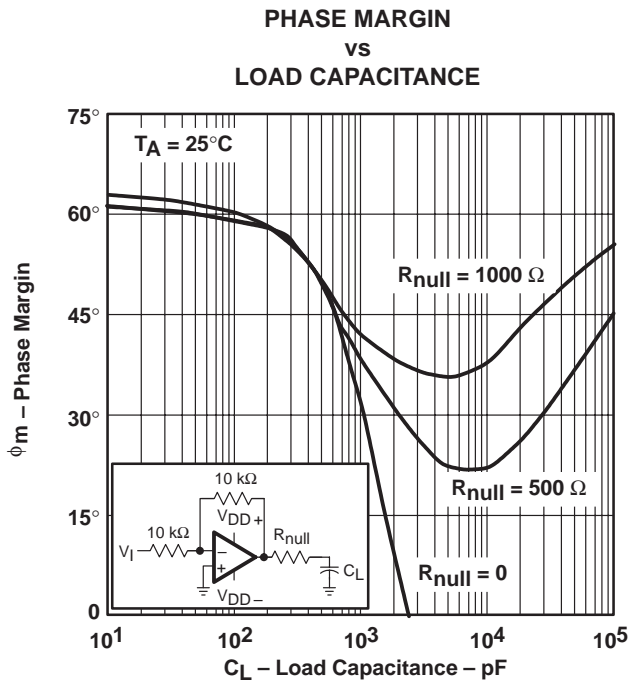
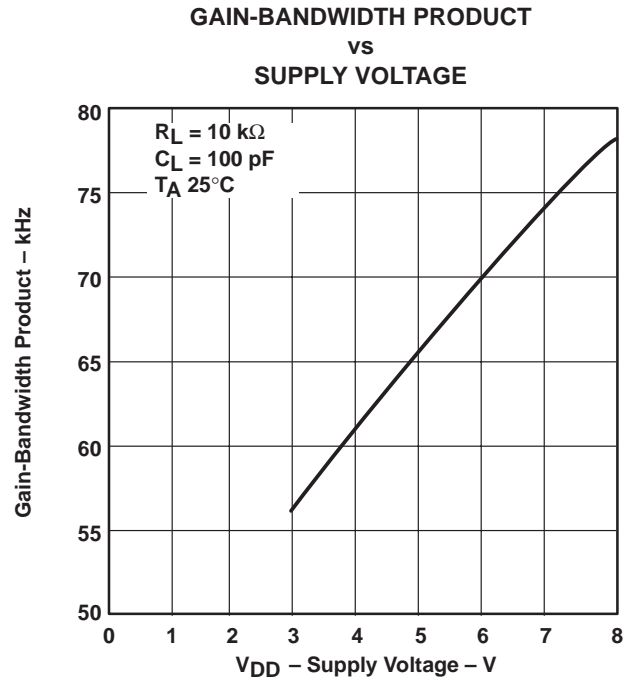
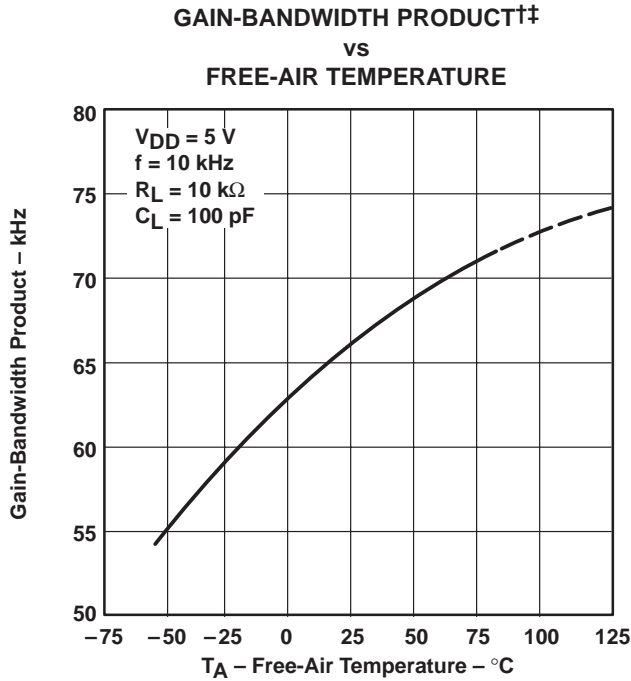


Figure 47

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

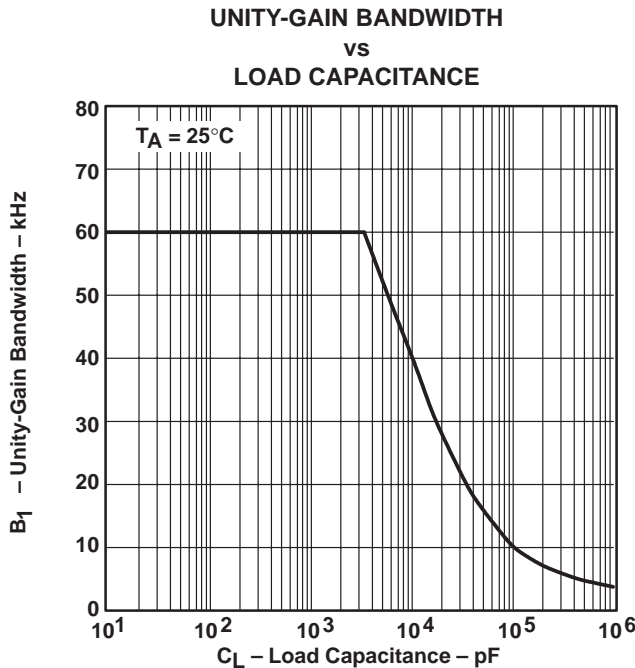


Figure 52

APPLICATION INFORMATION

driving large capacitive loads

The TLV2711 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 50 and Figure 51 illustrate its ability to drive loads up to 600 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 53) improves the gain and phase margins when driving large capacitive loads. Figure 50 and Figure 51 show the effects of adding series resistances of 500 Ω and 1000 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1} \left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L \right) \tag{1}$$

Where :

- $\Delta\phi_{m1}$ = Improvement in phase margin
- UGBW = Unity-gain bandwidth frequency
- R_{null} = Output series resistance
- C_L = Load capacitance



APPLICATION INFORMATION

driving large capacitive loads (continued)

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 52). To use equation 1, UGBW must be approximated from Figure 52.

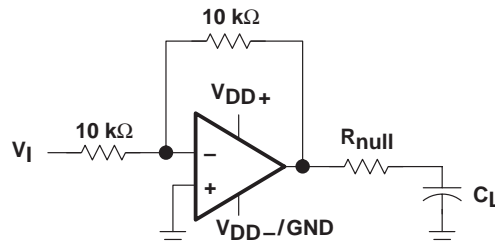


Figure 53. Series-Resistance Circuit

driving heavy dc loads

The TLV2711 is designed to provide better sinking and sourcing output currents than earlier CMOS rail-to-rail output devices. This device is specified to sink 500 μA and source 250 μA at $V_{\text{DD}} = 3\text{ V}$ and $V_{\text{DD}} = 5\text{ V}$ at a maximum quiescent I_{DD} of 25 μA . This provides a greater than 90% power efficiency.

When driving heavy dc loads, such as 10 k Ω , the positive edge under slewing conditions can experience some distortion. This condition can be seen in Figure 38. This condition is affected by three factors.

- Where the load is referenced. When the load is referenced to either rail, this condition does not occur. The distortion occurs only when the output signal swings through the point where the load is referenced. Figure 39 illustrates two 10-k Ω load conditions. The first load condition shows the distortion seen for a 10-k Ω load tied to 2.5 V. The third load condition shows no distortion for a 10-k Ω load tied to 0 V.
- Load resistance. As the load resistance increases, the distortion seen on the output decreases. Figure 39 illustrates the difference seen on the output for a 10-k Ω load and a 100-k Ω load with both tied to 2.5 V.
- Input signal edge rate. Faster input edge rates for a step input result in more distortion than with slower input edge rates.

TLV2711, TLV2711Y

Advanced LinCMOS™ RAIL-TO-RAIL

MICROPOWER SINGLE OPERATIONAL AMPLIFIERS

SLOS196A – AUGUST 1997 – REVISED MARCH 2001

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 6) and subcircuit in Figure 54 are generated using the TLV2711 typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

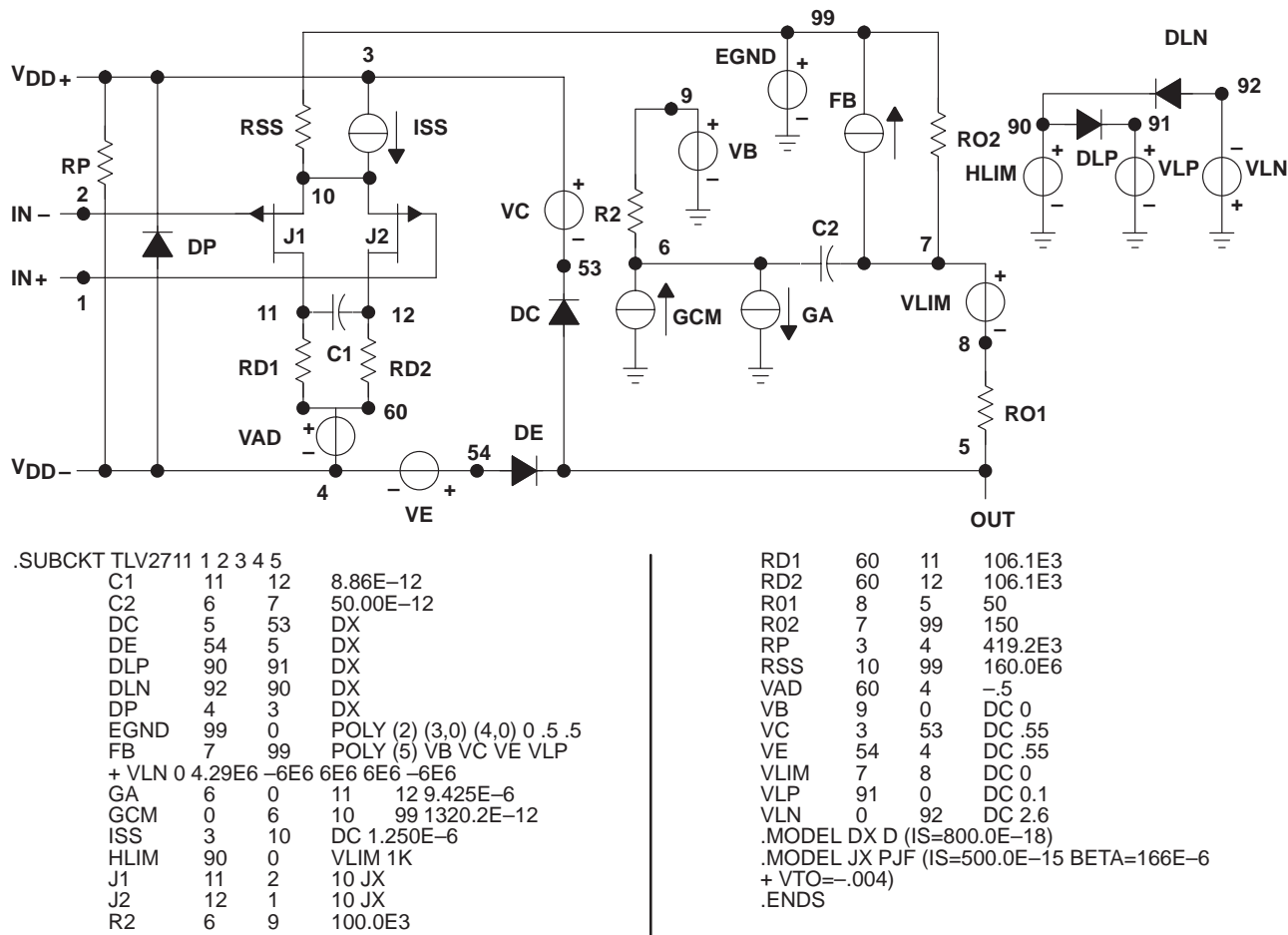


Figure 54. Boyle Macromodel and Subcircuit

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Macromodels, simulation models, or other models provided by TI, directly or indirectly, are not warranted by TI as fully representing all of the specification and operating characteristics of the semiconductor product to which the model relates.



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PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV2711CDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VAJC | Samples |
| TLV2711CDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VAJC | Samples |
| TLV2711CDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | | VAJC | Samples |
| TLV2711IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VAJI | Samples |
| TLV2711IDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VAJI | Samples |
| TLV2711IDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | | VAJI | Samples |
| TLV2711IDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | | VAJI | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV2711CDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2711CDBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2711IDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2711IDBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV2711CDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV2711CDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TLV2711IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV2711IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |

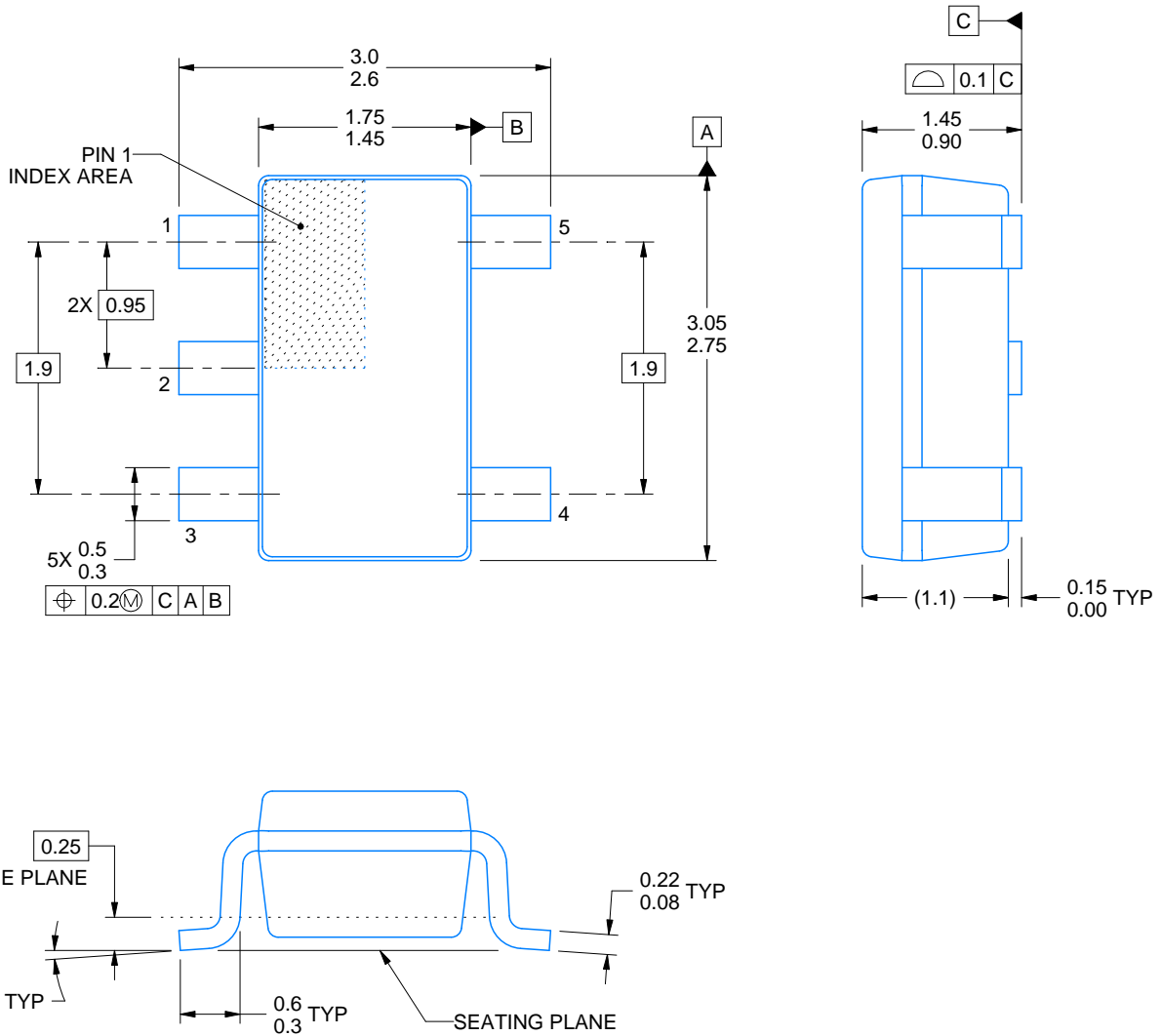


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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