

4-channel Electronic Volume with Input Selector

■GENERAL DESCRIPTION

The **NJW1192** is 4-channel Electronic Volume with input selector. It includes main volume, balance and fader trim, 3 stereo inputs and 1 mono input selector, loudness and tone control.

The **NJW1192** performs low noise and low distortion characteristics with resistance ladder type electrical volume.

All of internal status and variables are controlled by I²C BUS interface.

■PACKAGE OUTLINE

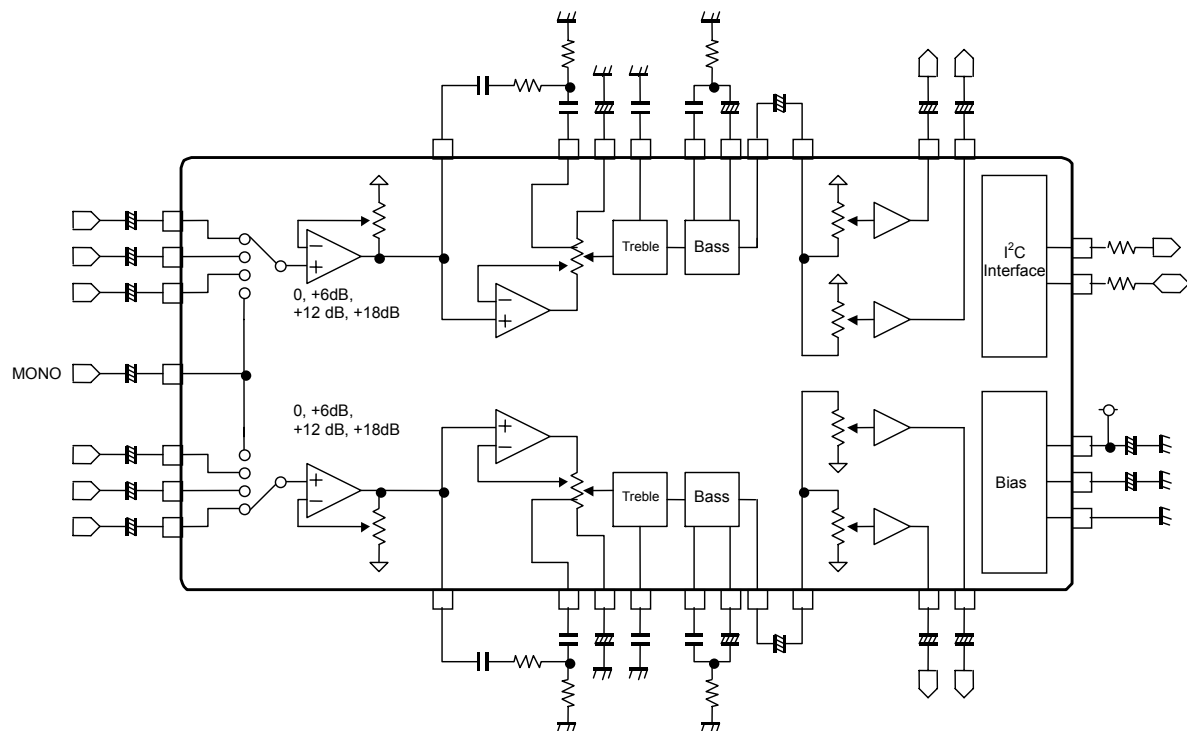


NJW1192V

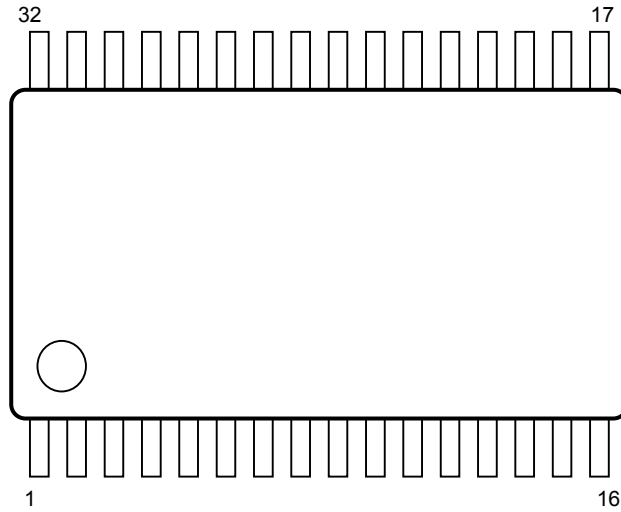
■FEATURES

- Operating Voltage 7.5 to 13V
- I²C BUS Interface
- Low Output Noise -103dBV typ.
- Low Distortion 0.005% typ.
- 3ch Stereo & 1ch Monaural Input Selector
- Tone Control Bass / Treble
- Main Volume
- Balance & Fader
- Bi-CMOS Technology
- Package Outline SSOP32

■BLOCK DIAGRAM



■PIN FUNCTION



No.	SYMBOL	FUNCTION	No.	SYMBOL	FUNCTION
1	GND	Ground	17	SDA	I ² C Data Input / Acknowledge Output
2	VREF	Reference Voltage	18	RL_OUT	Lch Rear Vol. Output
3	IN1R	Rch Input 1	19	FL_OUT	Lch Front Vol. Output
4	IN2R	Rch Input 2	20	VOL2IN_L	Lch 2 nd Vol. Input
5	IN3R	Rch Input 3	21	TONEOUT_L	Lch Tone Output
6	CAPR	Rch Volume DC cut Capacitor	22	DCCL	Lch Tone Bass DC cut Capacitor
7	TAP1R	Rch Loudness High Freq. Time Constant	23	TLCL	Lch Tone Bass Time Constant
8	TAP2R	Rch Loudness Low Freq. Time Constant	24	THCL	Lch Tone Treble Time Constant
9	THCR	Rch Tone Treble Time Constant	25	TAP2L	Lch Loudness Low Freq. Time Constant
10	TLCR	Rch Tone Bass Time Constant	26	TAP1L	Lch Loudness High Freq. Time Constant
11	DCCR	Rch Tone Bass DC cut Capacitor	27	CAPL	Lch Volume DC cut Capacitor
12	TONEOUT_R	Rch Tone Output	28	IN3L	Lch Input 3
13	VOL2IN_R	Rch 2 nd Vol. Input	29	IN2L	Lch Input 2
14	FR_OUT	Rch Front Vol. Output	30	IN1L	Lch Input 1
15	RR_OUT	Rch Rear Vol. Output	31	INMONO	Monaural Input
16	SCL	I ² C Clock Input	32	V+	Power Supply

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V ⁺	15	V
Power Dissipation	P _D	800 <small>NOTE: EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting</small>	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-40 to +125	°C

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V+=9V, R_g=600Ω, R_L=47kΩ, Vin=1.5Vrms, f=1kHz, all controls flat(Gv=0dB) unless otherwise specified)

PARAMETER	SYMBOL	Condition	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V ⁺		7.5	9.0	13.0	V
Supply Current	I _{CC}	No Signal	-	14	19	mA
Reference Voltage	V _{REF}	No Signal	4.0	4.5	5.0	V
Maximum Input Voltage	V _{IM}	VOL1=-20dB THD=1%	2.0	2.4	-	Vrms
Maximum Output Voltage 1	V _{OM1}	THD=1%	2.0	2.4	-	Vrms
Maximum Output Voltage 2	V _{OM2}	THD=1%, f=50kHz	1.5	2.4	-	Vrms
Input Gain	G _{vin}	VOL1=0dB, INPUT GAIN=+18dB Vin=0.1Vrms	+16	+18	+20	dB
Voltage Gain 1	G _{V1}	VOL1=+6dB, INPUT GAIN=0dB Vin=0.1Vrms	+5	+6	+7	dB
Voltage Gain 2	G _{V2}		-1	0	1	dB
Voltage Gain 3	G _{V3}	VOL1=-68dB, f=10kHz	-71	-68	-64	dB
Voltage Gain 4	G _{V4}	VOL2FL,FR,BL,BR=-42dB	-45	-42	-39	dB
Mute Level	Mute	VOL2FL,FR,BL,BR=Mute Filter : 400Hz to 30kHz	-	-100	-90	dB
Channel Balance	G _{CB}		-1	0	1	dB
Total Harmonic Distortion	THD	BW : 400Hz to 30kHz	-	0.005	0.01	%
Output Noise Voltage 1	V _{NO1}	Rg=0Ω, Filter : A-weighted	-	-103 (7)	-90 (32)	dBV (μVrms)
Output Noise Voltage 2	V _{NO2}	VOL2FL,FR,BL,BR=Mute Rg=0Ω, Filter : A-weighted	-	-108 (4)	-95 (17.8)	dBV (μVrms)
Cross Talk	CT	Selected Input : No signal Rg=0Ω Unselected Input : Input signal Filter : 400Hz to 30kHz	90	100	-	dB
Channel Separation	CS	Rg=0Ω, Filter : 400Hz to 30kHz	90	100	-	dB

◆ LOUDNESS

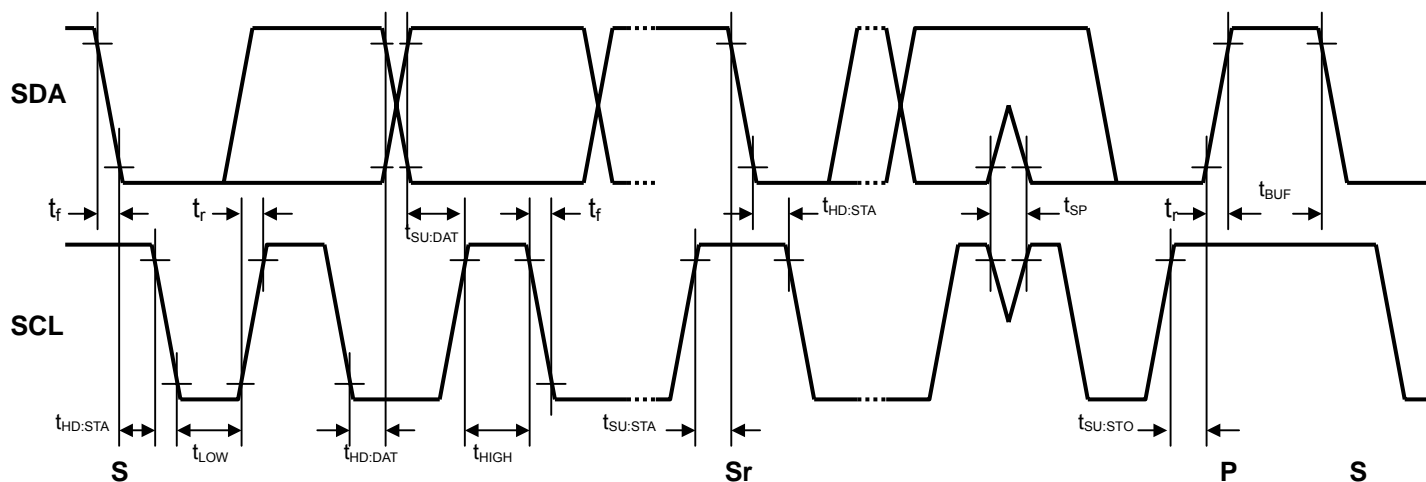
Maximum Low Boost Level	G _{LDL}	Loudness=ON, VOL1=-24dB, f=40Hz	9.5	12	14.5	dB
Maximum High Boost Level	G _{LDH}	Loudness=ON, VOL1=-24dB, f=10kHz	2.5	5	7.5	dB

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V+=9V, R_G=600Ω, R_L=47kΩ, Vin=1.5Vrms, f=1kHz, all controls flat(Gv=0dB) unless otherwise specified)

PARAMETER	SYMBOL	Condition	MIN.	TYP.	MAX.	UNIT
◆TONE						
Treble Boost Level	G _{HBST}	BCT="1", TREB="111", f=10kHz Vin=0.1Vrms	11.5	14.0	16.5	dB
Treble Flat Level	G _{HFLT}	TREB="000", f=10kHz	-2.0	0.0	2.0	dB
Treble Cut Level	G _{HCUT}	BCT="0", TREB="111", f=10kHz	-16.5	-14.0	-11.5	dB
Bass Boost Level	G _{LBST}	BCB="1", BASS="111", f=100Hz Vin=0.1Vrms	11.5	14.0	16.5	dB
Bass Flat Level	G _{LFLT}	BASS="000", f=100Hz	-2.0	0.0	2.0	dB
Bass Cut Level	G _{LCUT}	BCB="0", BASS="111", f=100Hz	-16.5	-14.0	-11.5	dB

■TIMING ON THE I²C BUS (SDA,SCL)



■CHARACTERISTICS OF I/O STAGES FOR I²C BUS (SDA,SCL)

I²C BUS Load Conditions

STANDARD MODE : Pull up resistance 4k Ω (Connected to +5V), Load capacitance 200pF (Connected to GND)

FAST MODE : Pull up resistance 4k Ω (Connected to +5V), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	Standard mode			Fast mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Low Level Input Voltage	V _{IL}	0.0	-	1.5	0.0	-	1.5	V
High Level Input Voltage	V _{IH}	2.5	-	5.5	2.5	-	5.5	V
Low level output voltage (3mA at SDA pin)	V _{OL}	0	-	0.4	0	-	0.4	V
Input current each I/O pin with an input voltage between 0.1V _{DD} and 0.9V _{DDmax}	I _i	-10	-	10	-10	-	10	μ A

■CHARACTERISTICS OF BUS LINES (SDA,SCL) FOR I²C-BUS DEVICES

PARAMETER	SYMBOL	Standard mode			Fast mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
SCL clock frequency	f _{SCL}	-	-	100	-	-	400	kHz
Hold time (repeated) START condition.	t _{HD:STA}	4.0	-	-	0.6	-	-	μs
Low period of the SCL clock	t _{LOW}	4.7	-	-	1.3	-	-	μs
High period of the SCL clock	t _{HIGH}	4.0	-	-	0.6	-	-	μs
Set-up time for a repeated START condition	t _{SU:STA}	4.7	-	-	0.6	-	-	μs
Data hold time ^{NOTE)}	t _{HD:DAT}	0	-	-	0	-	-	μs
Data set-up time	t _{SU:DAT}	250	-	-	100	-	-	ns
Rise time of both SDA and SCL signals	t _r	-	-	1000	-	-	300	ns
Fall time of both SDA and SCL signals	t _f	-	-	300	-	-	300	ns
Set-up time for STOP condition	t _{SU:STO}	4.0	-	-	0.6	-	-	μs
Bus free time between a STOP and START condition	t _{BUF}	4.7	-	-	1.3	-	-	μs
Capacitive load for each bus line	C _b	-	-	400	-	-	400	pF
Noise margin at the Low level	V _{nL}	0.5	-	-	0.5	-	-	V
Noise margin at the High level	V _{nH}	1	-	-	1	-	-	V

C_b ; total capacitance of one bus line in pF.

NOTE). Data hold time : t_{HD:DAT}

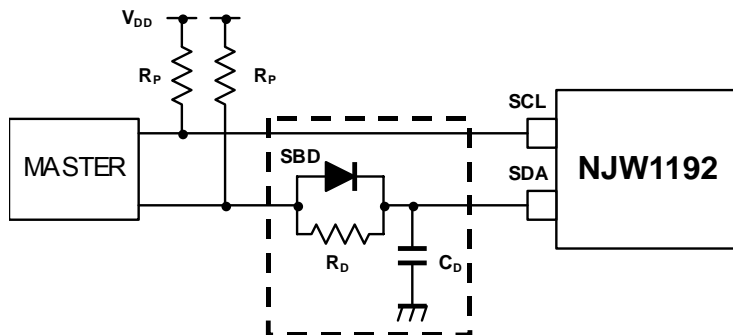
Please hold the Data Hold Time (t_{HD:DAT}) to 300ns or more to avoid status of unstable at SCL falling edge.

The SDA block in the NJW1192 does not hold data. Add external data-delay-circuit of the SDA terminal, in case of not providing a hold time of at least 300nsec for the SDA in the master device.

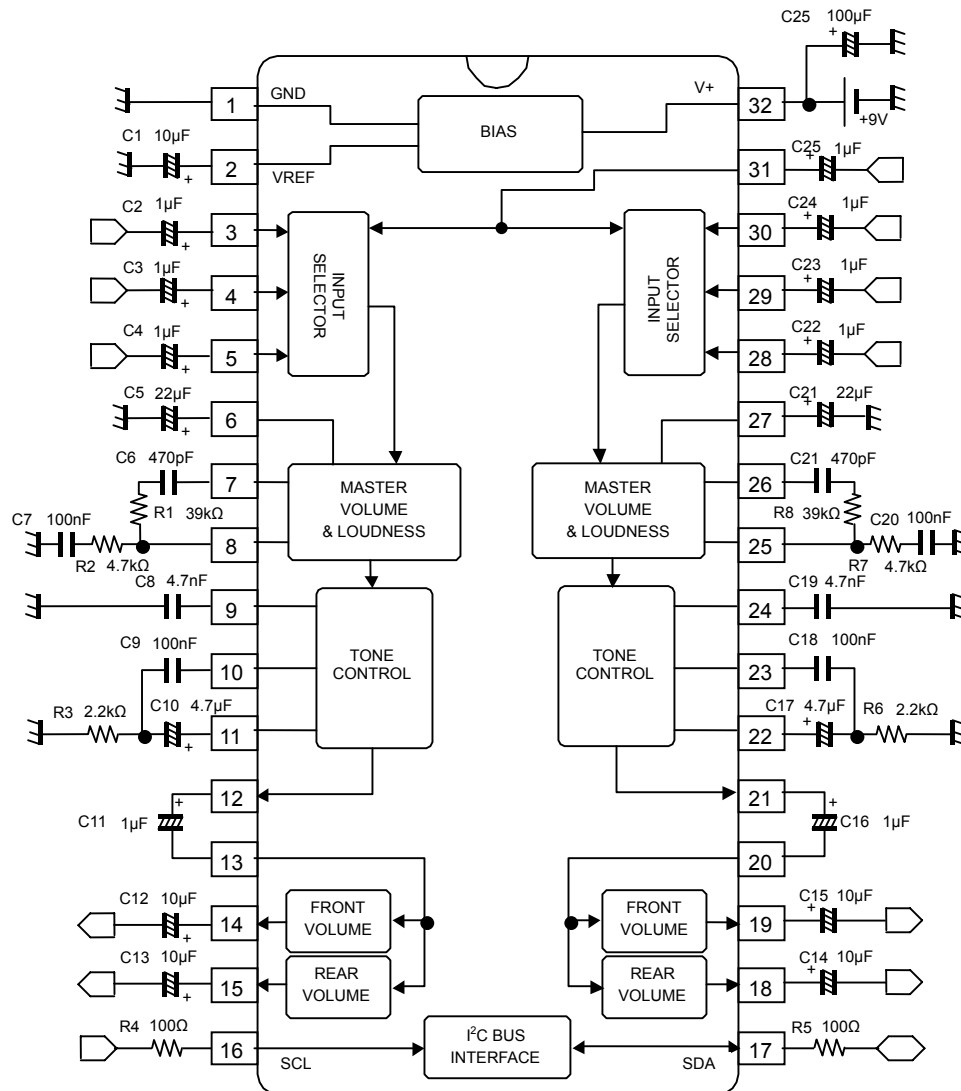
The time-consists of the data-delay-circuit of the SDA terminal are as follows.

- (a) Low level → High level : $T_{LH} \approx R_P * C_D$
- (b) High level → Low level : $T_{HL} \approx R_D * C_D$

In addition, Schottky barrier diode (SBD) influences a Low level at the Acknowledge. Therefore choose the low forward voltage (V_f) as much as possible.



APPLICATION CIRCUIT



APPLICATION NOTES

Pin No.	Function	Note
2	Vref	C1 can be adjusted rise and fall time of reference voltage at power on and off. Take care that the reduced C1 makes sensitive to ripple of power supply.
3-5, 28-31	Inputs	The input impedance is designed about 48k ohms. The ground line should be inserted between each input lines to avoid cross talk.
6,27	Volume DC cut capacitor terminals	The wiring pattern between these terminals and capacitors should be shortened to prevent the generating of wiring resistance. C5, C21 affect pop-noise when "VOL1" or "Tone Bass" are immediately controlled after powered. Though reducing the capacity of C5, C21 may reduce pop-noise, it affects bass frequency characteristic on volume1 attenuation (See Page.22 Voltage Gain vs. Frequency characteristics). Use Pre Charge function for reducing pop-noise.(See Page.14)
7,8,25,26	Loudness filter Taps	Loudness frequency can be adjusted with external parts (See Page.7). Especially, 8 and 25 pins should be kept from large signal lines such as digital signal lines or the other sound signal lines to avoid the digitaly noise or cross talk in Loudness mode.
9,10,11,22,23,24	Tone filter terminals	Tone Bass and Treble cut off frequency can be adjusted with external parts (See Page.7). These pins should be kept from large signal lines such as digital signal lines or the other sound signal lines to avoid the digitaly noise or cross talk in Loudness mode.
12,21	Tone outputs	Output impedance is designed about 50 ohms.
13,20	Balance Fader volume inputs	Input impedance is designed about 24k ohms.
14,15,18,19	Balance Fader volume outputs	Output impedance is designed about 50 ohms.
16,17	I²C control signal ports	These terminals should be inserted resistance about 100 ohms between terminal and signal sources to reduce the digitaly noise. These lines should be kept from analog signal lines and or near by the chip to avoid digitaly noises. Inserted ground line between analog line and digital line should be recommended.

APPLICATION NOTES

< Loudness fc adjustment >

Loudness High and Low Boost cut off frequencies are able to adjust with the external parts as shown in fig.A. They are given by the functions below.

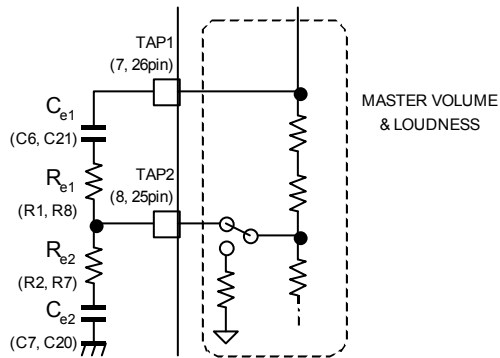


fig. A Loudness circuit

$$\text{High Boost cut off frequency: } f_{CH} = \frac{1}{2\pi R_{e1} \cdot C_{e1}} \text{ (Hz)}$$

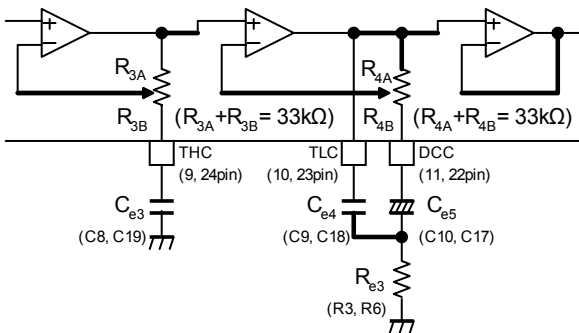
$$\text{Low Boost cut off frequency: } f_{CL} = \frac{1}{2\pi R_{e2} \cdot C_{e2}} \text{ (Hz)}$$

<NOTE>

R_{e2} should be fixed to 4.7kΩ for the precise level of volume in Loudness mode.

< Tone fc adjustment >

Tone High and Low cut off frequencies are able to adjust with the external parts as shown in fig.B. They are given by the functions below. .



(Boost)

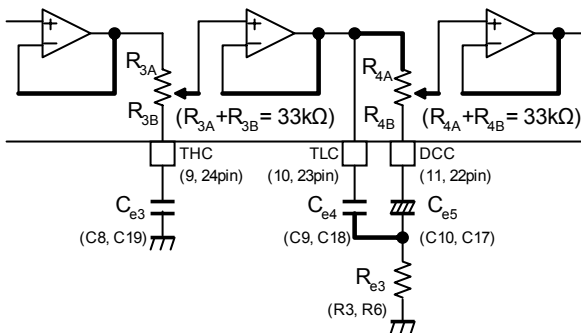
$$\text{Treble cut off frequency: } f_{CT} = \frac{1}{2\pi R_{3B} \cdot C_{e3}} \text{ (Hz)}$$

($R_{3B}=5.5\text{k}\Omega$ at 14dB set)

$$\text{Bass cut off frequency: } f_{CBL} = \frac{(R_{4B} + R_{e3})}{2\pi(R_{4A} + R_{4B}) \cdot R_{e3} \cdot C_{e4}} \text{ (Hz)}$$

$$\left[\text{DC cut off frequency: } f_{DC} = \frac{1}{2\pi(R_{4B} + R_{e3}) \cdot C_{e5}} \text{ (Hz)} \right]$$

($R_{4B}=3.3\text{k}\Omega$ at 14dB set)



(Cut)

fig. B Tone circuit

■TERMINAL DESCRIPTION

No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
2	VREF	Reference Voltage		$V+/2$
3 4 5 30 29 28	IN1R IN2R IN3R IN1L IN2L IN3L	Rch Input 1 Rch Input 2 Rch Input 3 Lch Input 1 Lch Input 2 Lch Input 3		$V+/2$
6 27	CAPR CAPL	Rch Volume DC cut Capacitor Lch Volume DC cut Capacitor		$V+/2$
7 26	TAP1R TAP1L	Rch Loudness High Freq. Time Constant Lch Loudness High Freq. Time Constant		$V+/2$

■TERMINAL DESCRIPTION

No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
8 25	TAP2R TAP2L	Rch Loudness Low Freq. Time Constant Lch Loudness Low Freq. Time Constant		V+/2
9 24	THCR THCL	Rch Tone Treble Time Constant Lch Tone Treble Time Constant		V+/2
10 23	TLCR TLCL	Rch Tone Bass Time Constant Lch Tone Bass Time Constant		V+/2
11 22	DCCR DCCL	Rch Tone Bass DC cut Capacitor Lch Tone Bass DC cut Capacitor		V+/2

■TERMINAL DESCRIPTION

No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
12 14 15 19 18 21	TONEOUT_R FR_OUT RR_OUT FL_OUT RL_OUT TONEOUT_L	Rch Tone Output Rch Front Vol. Output Rch Rear Vol. Output Lch Front Vol. Output Lch Rear Vol. Output Lch Tone Output		V+/2
13 20	VOL2IN_R VOL2IN_L	Rch 2 nd Vol. Input Lch 2 nd Vol. Input		V+/2
16	SCL	I ² C Clock Input		-
17	SDA	I ² C Data Input / Acknowledge Output		-

■TERMINAL DESCRIPTION

No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
31	INMONO	Monaural Input		V+/2

■ DEFINITION OF I²C REGISTER

◆ I²C BUS FORMAT



S: Starting Term
 A: Acknowledge Bit
 P: Ending Term

◆ SLAVE ADDRESS

Slave Address								Hex
MSB				LSB				-
1	0	0	0	0	0	0	0	80(h)

◆ CONTROL REGISTER TABLE

The select address sets each function (Volume, Loudness, Balance, Fader, Tone Control, Input Selector).
 The auto increment function cycles the select address as follows.
 00H→01H→02H→03H→04H→00H

<Write Mode>

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	Input Gain				VOL1			
01H	VOL2FL (Front Left)				VOL2FR (Front Right)			
02H	VOL2RL (Rear Left)				VOL2RR (Rear Right)			
03H	BCB	Tone Bass			BCT	Tone Treble		
04H	FLMute	FRMute	RLMute	RRMute	Input Selector		Loudness	Test *

* Test : Set D0=0 in usually.
 (For device check use only)

◆ CONTROL REGISTER DEFAULT VALUE

Control register default value is all "0".

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	0	0	0	0	0	0	0	0
01H	0	0	0	0	0	0	0	0
02H	0	0	0	0	0	0	0	0
03H	0	0	0	0	0	0	0	0
04H	0	0	0	0	0	0	0	0

■ INSTRUCTION CODE

a) MAIN VOLUME (VOL1, Input Gain) SETTING

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	Input Gain			VOL1				

- Input Gain : 0dB, +6dB, +12dB, +18dB
- VOL1 : Volume 1 Level setting +6 to -30dB (1dB/Step), -30 to -68dB (2dB/Step), Mute

b) BALANCE, FADER VOLUME (VOL2FL,FR,RL,RR) SETTING

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
01H	VOL2FL				VOL2FR			
02H	VOL2RL				VOL2RR			

- VOL2FL,FR,RL,RR : 0,-2,-4,-6,-8,-10,-12,-16,-18,-20,-24,-32,-34,-36,-38,-42 dB

c) TONE SETTING

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
03H	BCB	TONE BASS			BCT	TONE TREBLE		

- BCB : Boost cut select for Bass control
 "0" : Cut
 "1" : Boost
- TONE BASS : BASS Level Setting
 Cut Level : -14 to 0dB(2dB/Step)
 Boost Level : 0 to +14dB(2dB/Step)
- BCT : Boost cut select for Treble control
 "0" : Cut
 "1" : Boost
- TONE TREBLE : TREBLE Level Setting
 Cut Level : -14 to 0dB(2dB/Step)
 Boost Level : 0 to +14dB(2dB/Step)

d) INPUT SELECTOR SETTING

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
04H	FLMute	FRMute	RLMute	RRMute	Input Selector		Loudness	Test

- FLMute, FRMute, RLMute, RRMute : VOL2FL,FR,RL,RR Mute
- Input Selector: INPUT1 to 3 and MONO
- Loudness : Loudness ON/OFF
- Test : For device check use only. Set D0 = 0 in usual.

■VOL1(Select Address : 00H)

Gain(dB)	VOL1					
	D5	D4	D3	D2	D1	D0
0	1	1	1	1	1	1
-1	1	1	1	1	1	0
-2	1	1	1	1	0	1
-3	1	1	1	1	0	0
-4	1	1	1	0	1	1
-5	1	1	1	0	1	0
-6	1	1	1	0	0	1
-7	1	1	1	0	0	0
-8	1	1	0	1	1	1
-9	1	1	0	1	1	0
-10	1	1	0	1	0	1
-11	1	1	0	1	0	0
-12	1	1	0	0	1	1
-13	1	1	0	0	1	0
-14	1	1	0	0	0	1
-15	1	1	0	0	0	0
-16	1	0	1	1	1	1
-17	1	0	1	1	1	0
-18	1	0	1	1	0	1
-19	1	0	1	1	0	0
-20	1	0	1	0	1	1
-21	1	0	1	0	1	0
-22	1	0	1	0	0	1
-23	1	0	1	0	0	0
-24	1	0	0	1	1	1
-25	1	0	0	1	1	0
-26	1	0	0	1	0	1
-27	1	0	0	1	0	0
-28	1	0	0	0	1	1
-29	1	0	0	0	1	0
-30	1	0	0	0	0	1
-32	1	0	0	0	0	0
-34	0	1	1	1	1	1
-36	0	1	1	1	1	0
-38	0	1	1	1	0	1
-40	0	1	1	1	0	0
-42	0	1	1	0	1	1
-44	0	1	1	0	1	0
-46	0	1	1	0	0	1
-48	0	1	1	0	0	0
-50	0	1	0	1	1	1
-52	0	1	0	1	1	0
-54	0	1	0	1	0	1
-56	0	1	0	1	0	0
-58	0	1	0	0	1	1
-60	0	1	0	0	1	0
-62	0	1	0	0	0	1
-64	0	1	0	0	0	0
-66	0	0	1	1	1	1
-68	0	0	1	1	1	0
Mute	0	0	1	1	0	1
Mute	0	0	1	1	0	0
Mute	0	0	1	0	1	1
Mute	0	0	1	0	1	0
Mute	0	0	1	0	0	1
Mute	0	0	1	0	0	0
0	0	0	0	1	1	1
+1	0	0	0	1	1	0
+2	0	0	0	1	0	1
+3	0	0	0	1	0	0
+4	0	0	0	0	1	1
+5	0	0	0	0	1	0
+6	0	0	0	0	0	1
Pre Charge*	0	0	0	0	0	0

* Pre Charge : Charge the DC cut capacitor of VOL1 (CAPL, CAPR) and Tone Bass (DCCL, DCCR) for reducing pop-noise when "VOL1" or "Tone Bass" are immediately controlled after powered.
 This device should be provided the Pre Charge time of at least 2 sec for reducing pop-noise under application circuit condition.

■INPUT GAIN (Select Address : 00H)

Gain(dB)	INPUT GAIN	
	D7	D6
0	0	0
+6	0	1
+12	1	0
+18	1	1

■VOL2 FL,FR (Select Address : 01H) : Front Channel
 VOL2 RL,RR (Select Address : 02H) : Rear Channel

Gain(dB)	VOL2					
	Lch	D7	D6	D5	D4	
	Rch	D3	D2	D1	D0	
0		1	1	1	1	
-2		1	1	1	0	
-4		1	1	0	1	
-6		1	1	0	0	
-8		1	0	1	1	
-10		1	0	1	0	
-12		1	0	0	1	
-16		1	0	0	0	
-18		0	1	1	1	
-20		0	1	1	0	
-24		0	1	0	1	
-32		0	1	0	0	
-34		0	0	1	1	
-36		0	0	1	0	
-38		0	0	0	1	
-42		0	0	0	0	

■TONE (Select Address : 03H)

Cut/Boost Select	BCB
	D7
	BCT
	D3
Cut	0
Boost	1

		TONE BASS		
		D6	D5	D4
Cut Gain(dB)	Boost Gain(dB)	TONE TREBLE		
		D2	D1	D0
-14	14	1	1	1
-12	12	1	1	0
-10	10	1	0	1
-8	8	1	0	0
-6	6	0	1	1
-4	4	0	1	0
-2	2	0	0	1
0	0	0	0	0

■VOL2 MUTE (Select Address : 04H)

Mute Setting	FL Mute
	D7
	FR Mute
	D6
	RL Mute
	D5
RR Mute	
D4	
Mute	0
Active	1

■INPUT SELECTOR (Select Address : 04H)

	Input Selector	
	D3	D2
INPUT 1	0	0
INPUT 2	0	1
INPUT 3	1	0
MONO	1	1

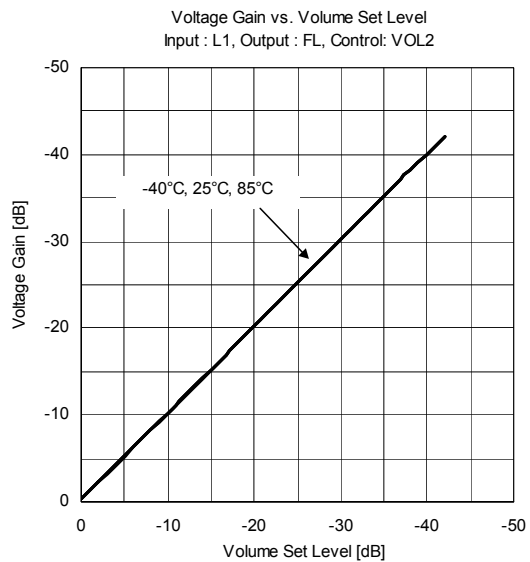
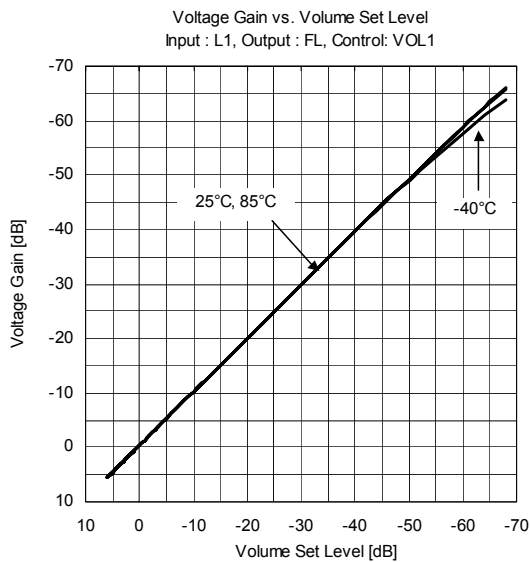
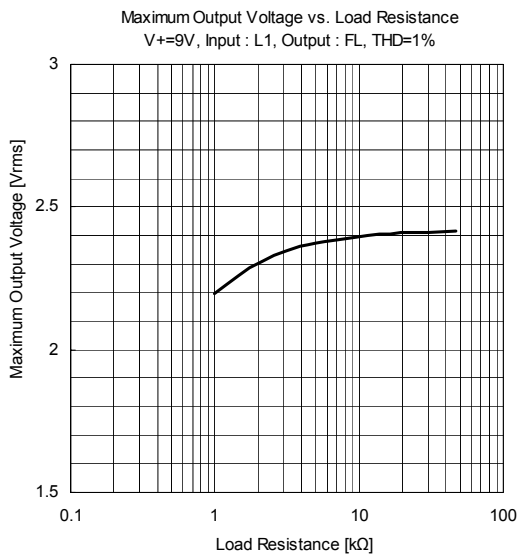
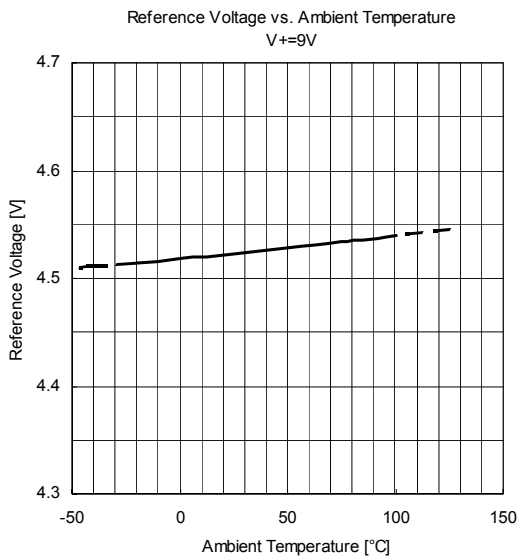
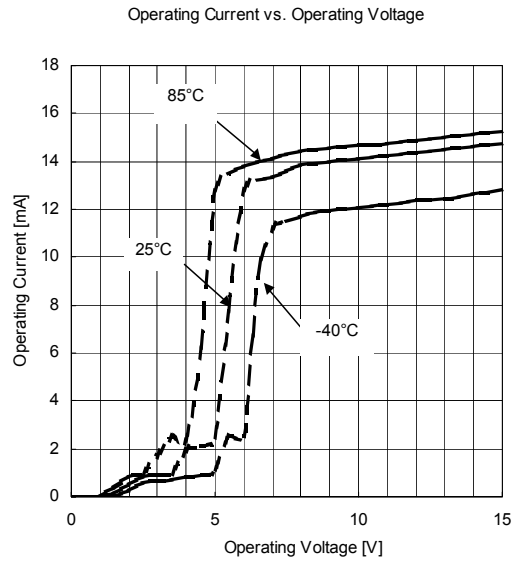
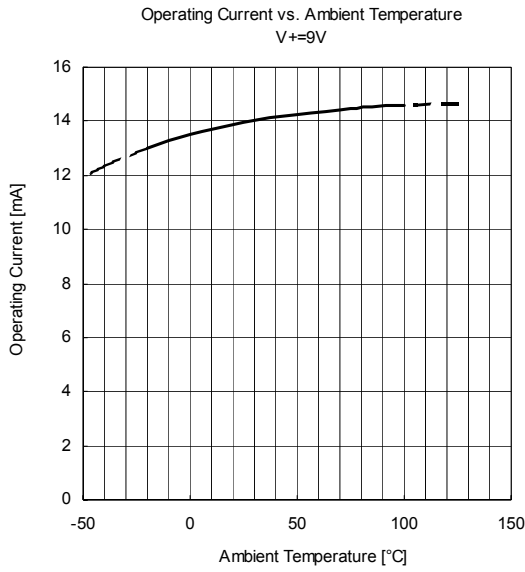
■LOUDNESS (Select Address : 04H)

Loudness Setting	Loudness D1
OFF	0
ON	1

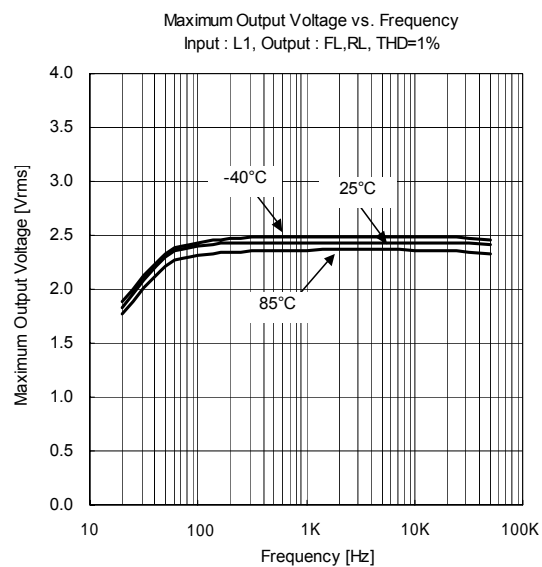
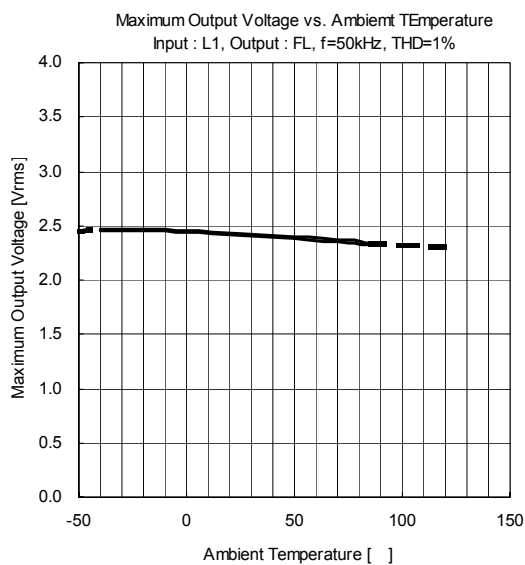
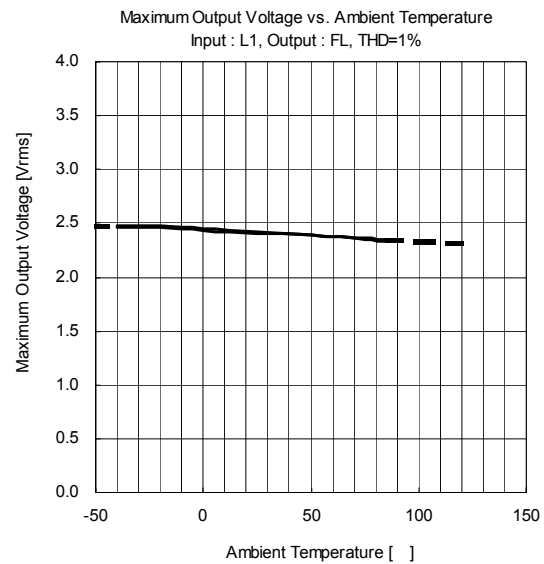
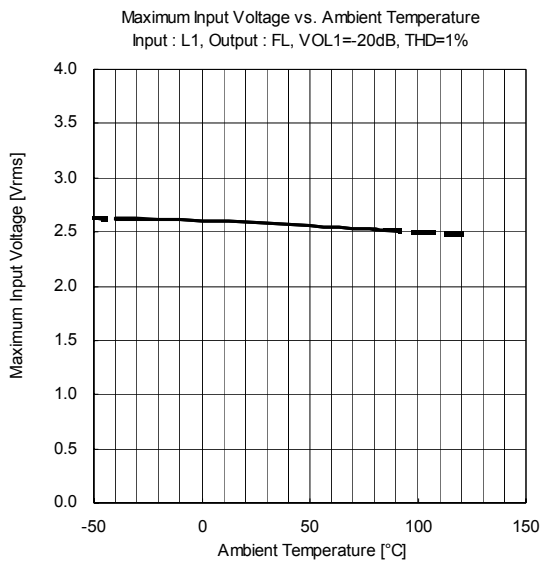
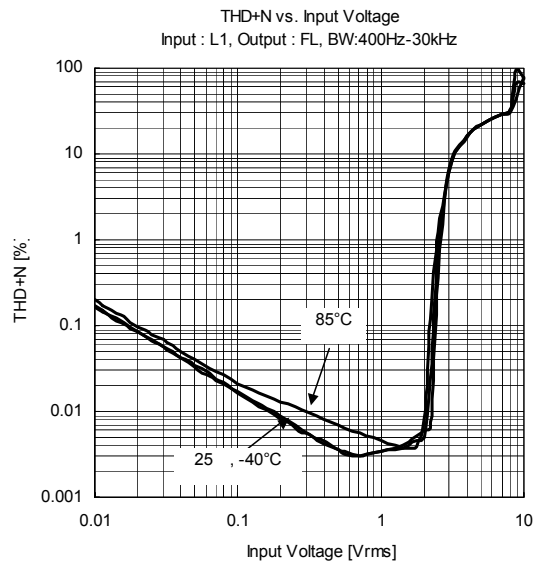
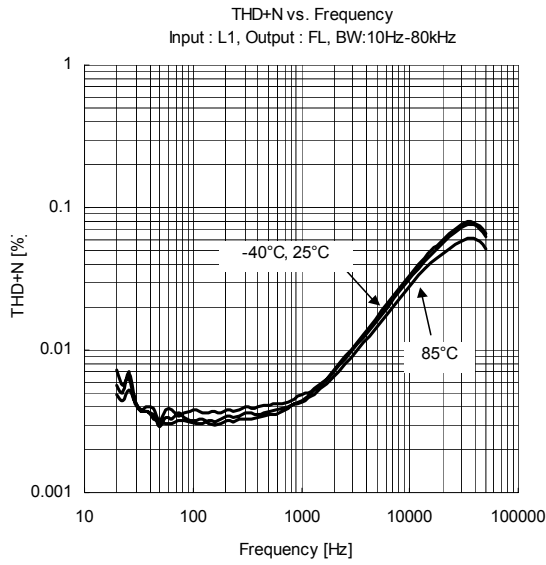
■TEST (Select Address : 04H) * FOR DEVICE CHECK USE ONLY.

	Test
	D0
Normal	0
Test Mode	1

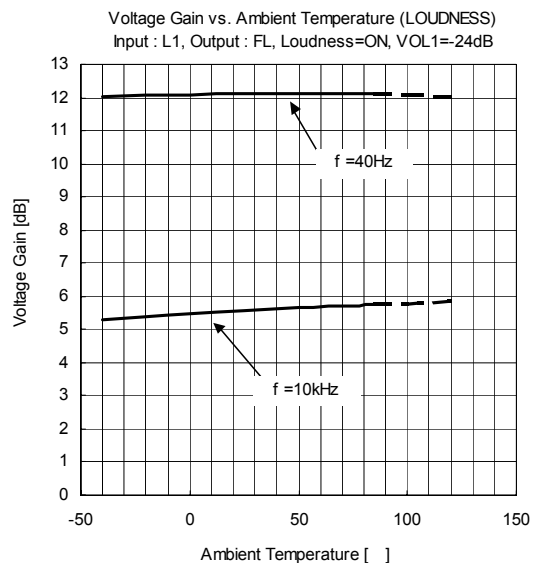
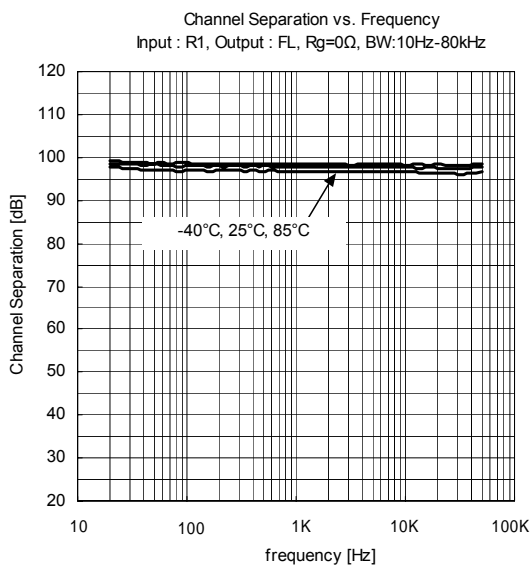
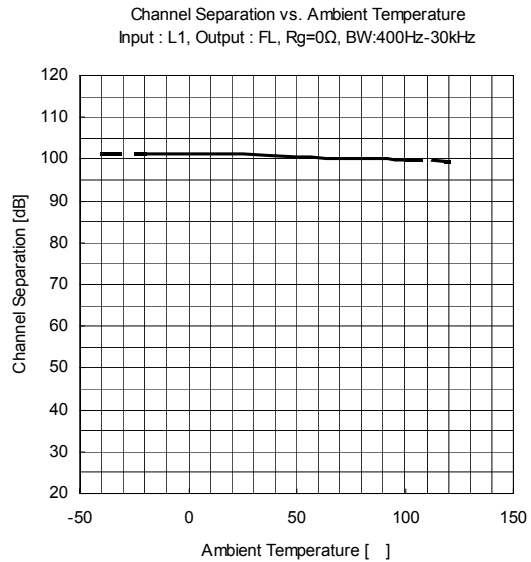
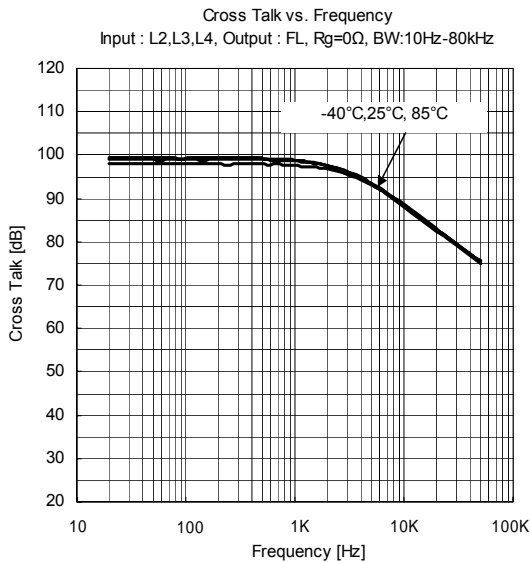
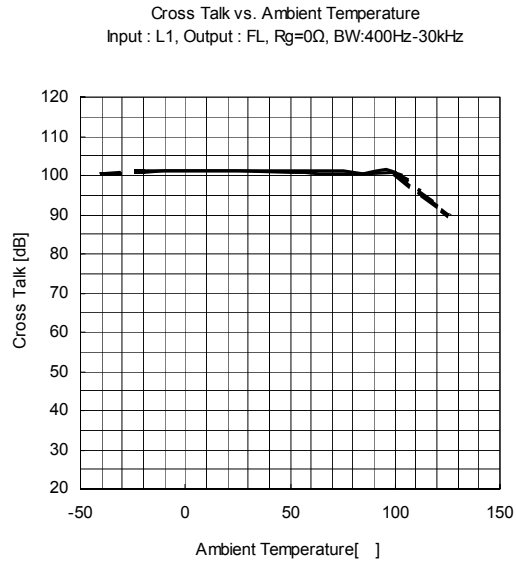
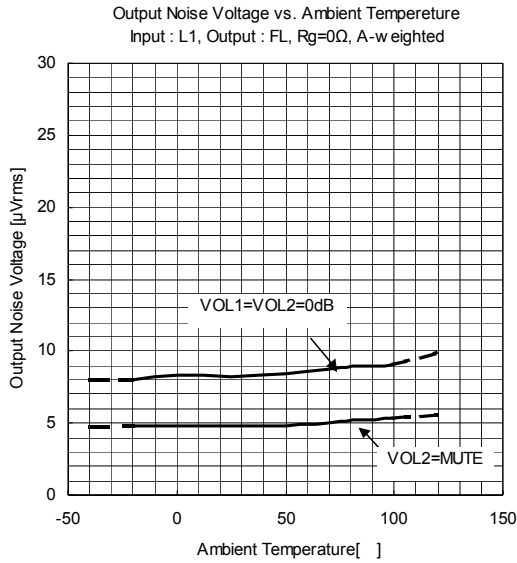
■ TYPICAL CHARACTERISTICS



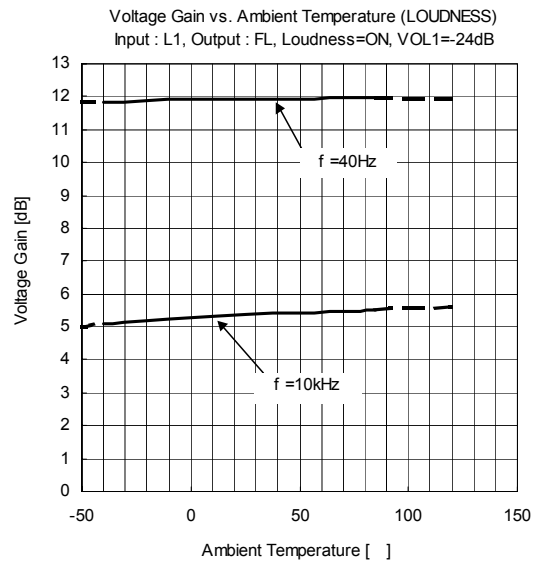
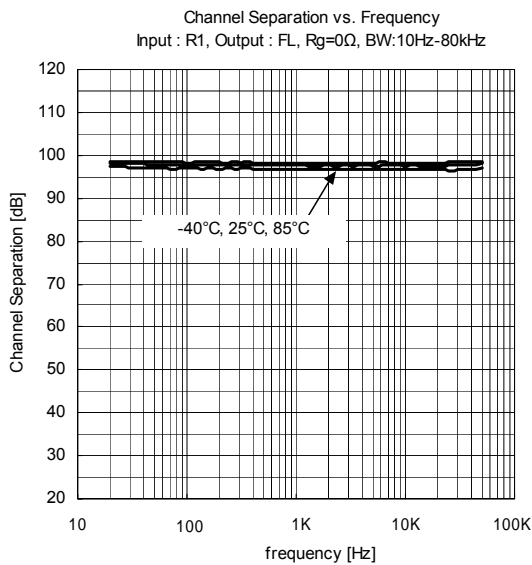
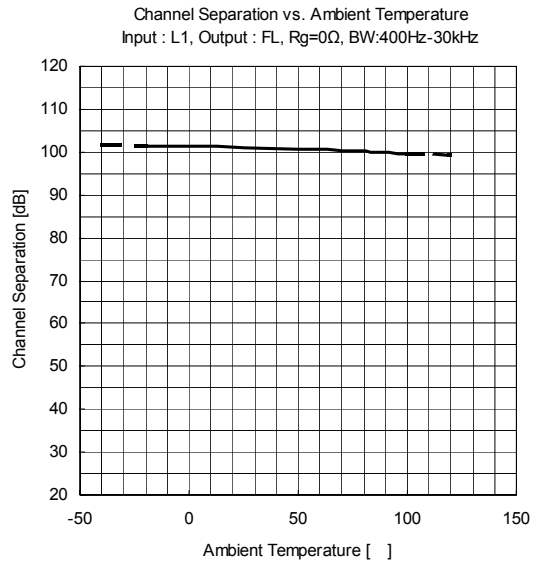
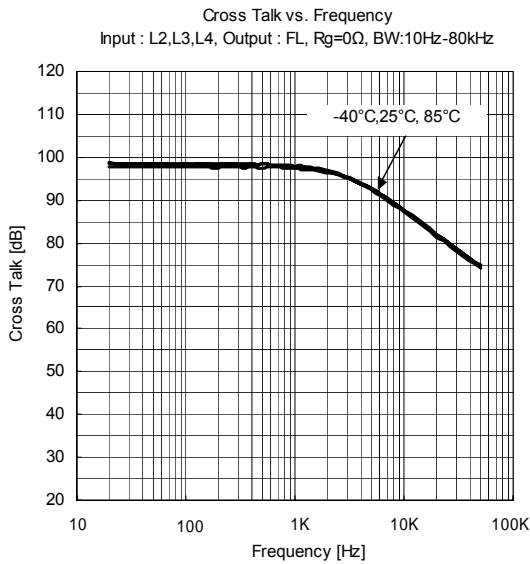
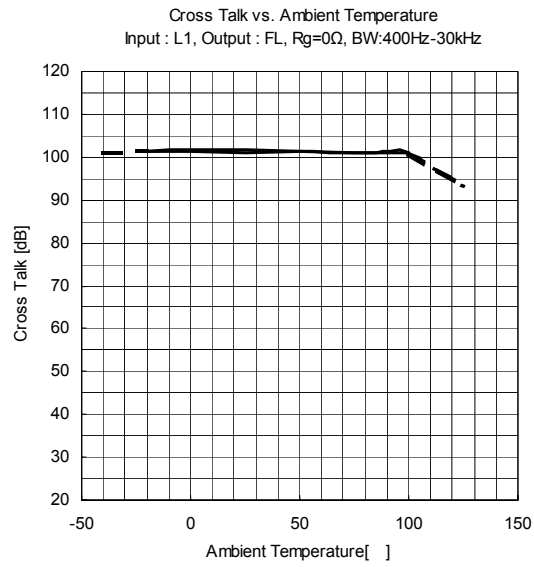
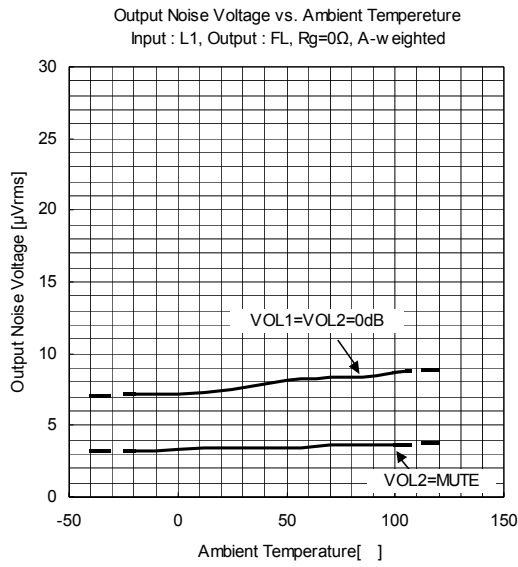
■ TYPICAL CHARACTERISTICS



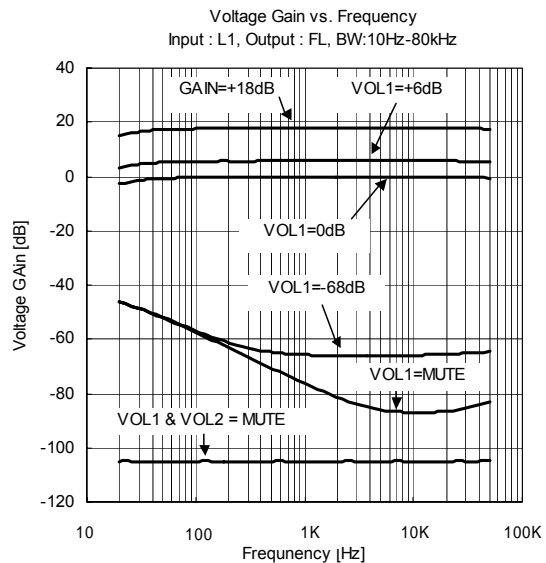
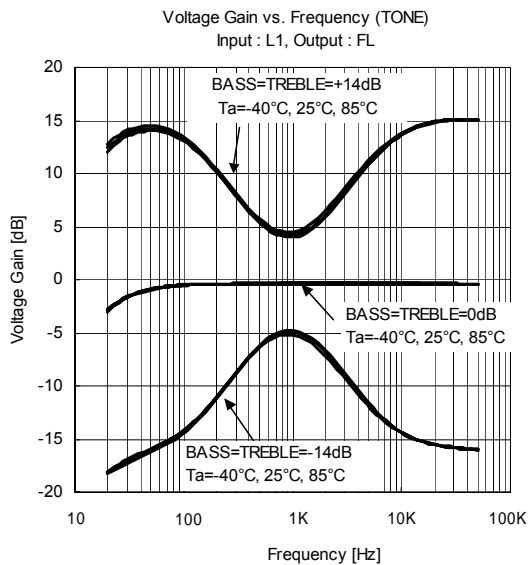
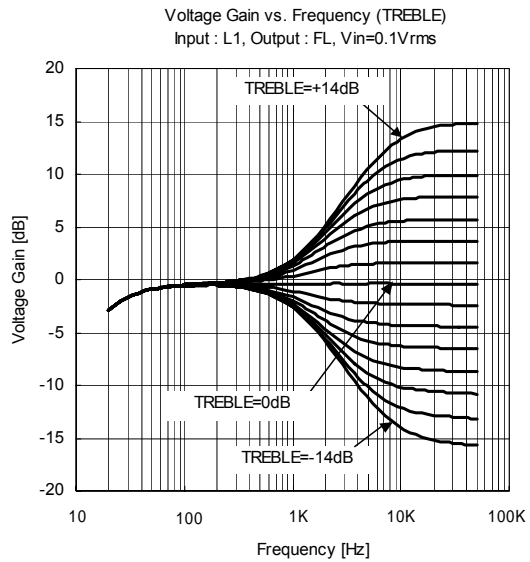
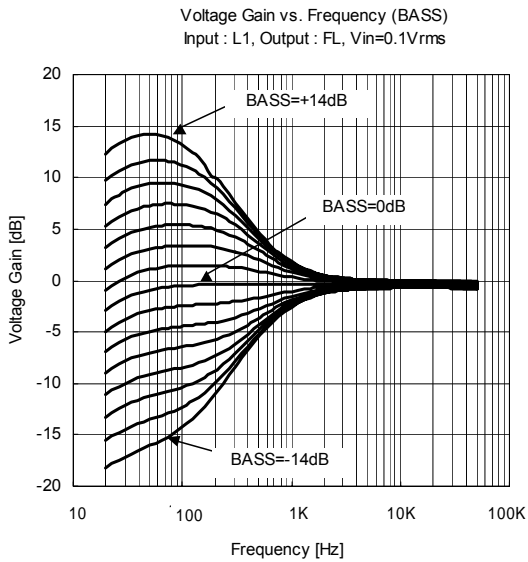
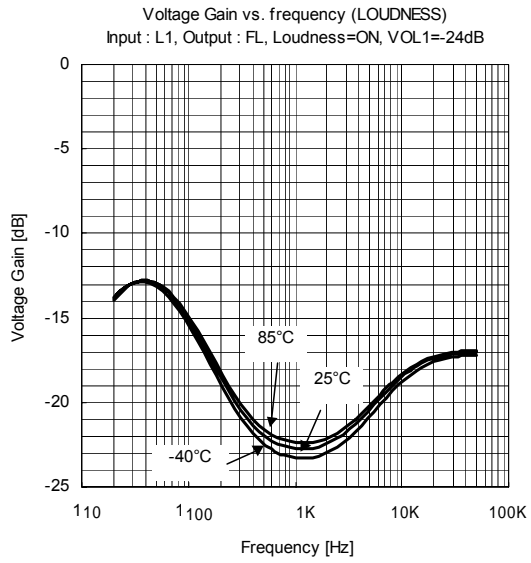
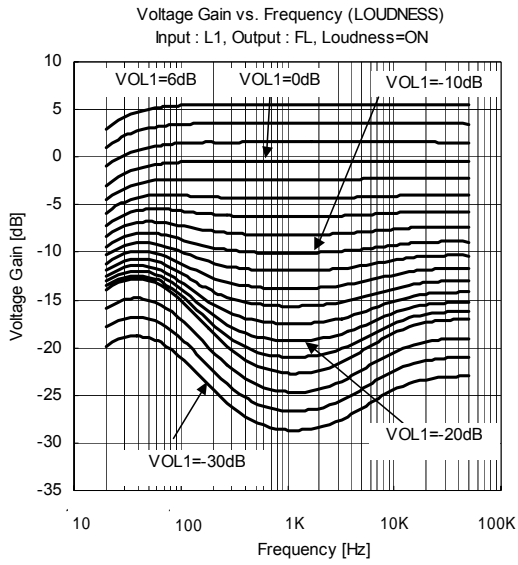
■ TYPICAL CHARACTERISTICS



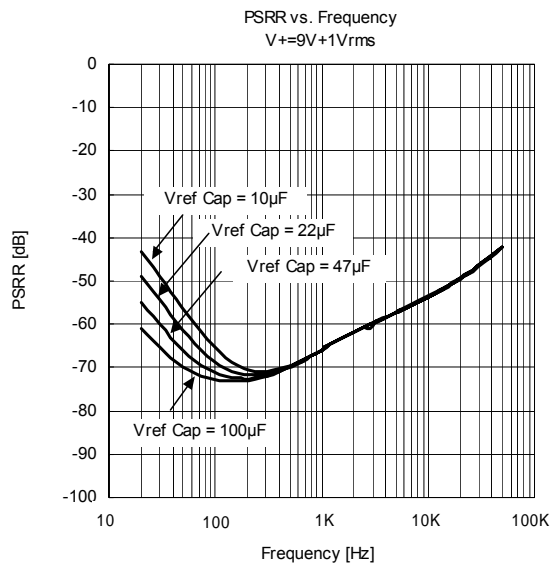
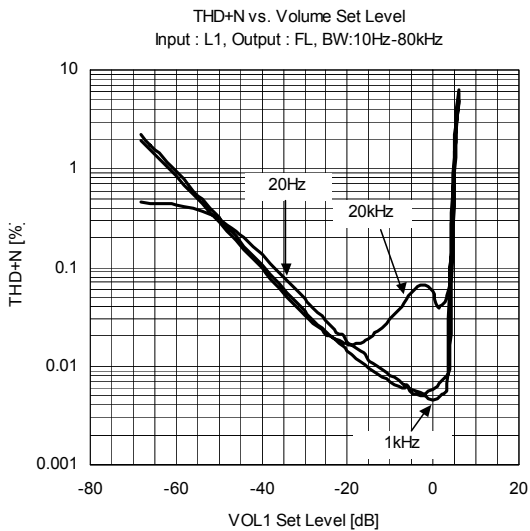
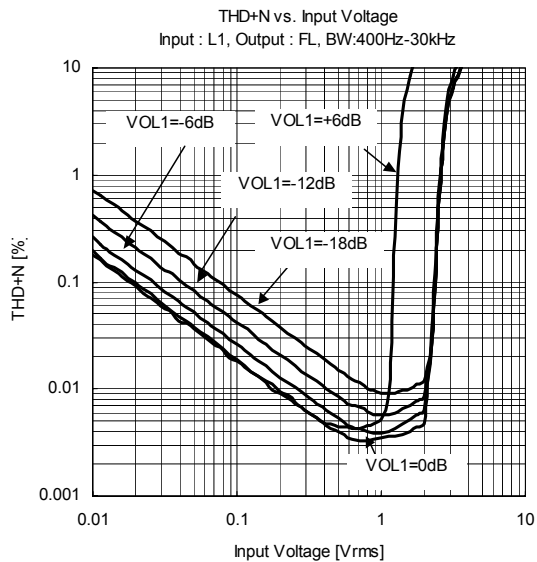
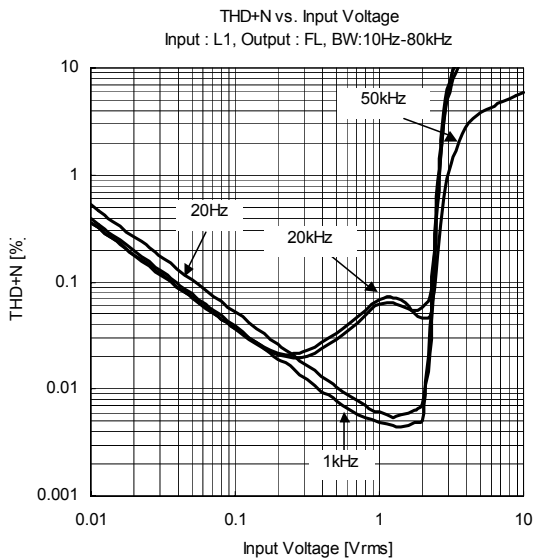
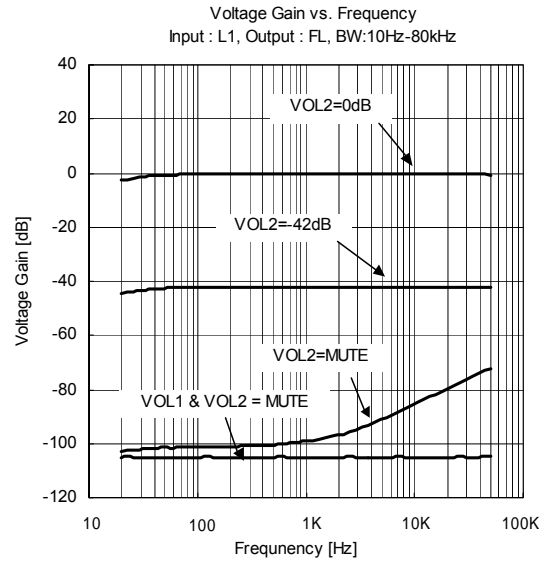
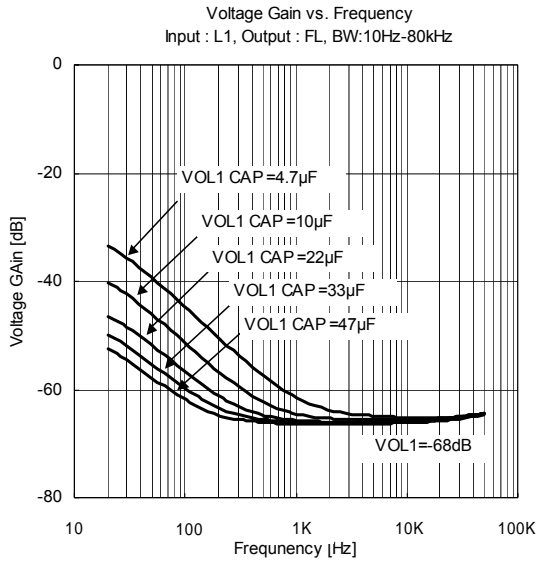
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS



■NOTE

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