PCA9545A Low Voltage 4-channel I²C and SMbus Switch With Interrupt Logic and Reset Functions

1 Features

- 1-of-4 Bidirectional Translating Switches
- I²C Bus and SMBus Compatible
- Four Active-Low Interrupt Inputs
- Active-Low Interrupt Output
- Active-Low Reset Input
- Two Address Terminals, Allowing up to Four Devices on the I²C Bus
- Channel Selection via I²C Bus, in Any Combination
- Power-Up With All Switch Channels Deselected
- Low R_{ON} Switches
- Allows Voltage-Level Translation Between 1.8-V, 2.5-V, 3.3-V, and 5-V Buses
- No Glitch on Power-Up
- Supports Hot Insertion
- Low Standby Current
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5.5 V Tolerant Inputs
- 0 to 400-kHz Clock Frequency
- Latch-Up Performance Exceeds 100 mA per JESD 78
- ESD Protection Exceeds JESD 22
  – 2000-V Human-Body Model (A114-A)
  – 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products With I²C Slave Address Conflicts (e.g. Multiple, Identical Temp Sensors)

3 Description

The PCA9545A is a quad bidirectional translating switch controlled via the I²C bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register. Four interrupt inputs ($\overline{\text{INT3}}$–$\overline{\text{INT0}}$), one for each of the downstream pairs, are provided. One interrupt ($\overline{\text{INT}}$) output acts as an AND of the four interrupt inputs.

An active-low reset ($\overline{\text{RESET}}$) input allows the PCA9545A to recover from a situation in which one of the downstream I²C buses is stuck in a low state. Pulling $\overline{\text{RESET}}$ low resets the I²C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

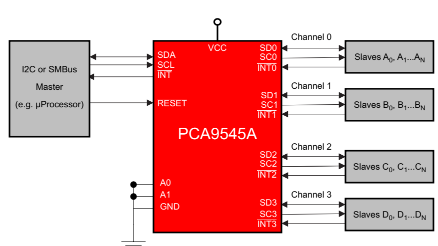
The pass gates of the switches are constructed such that the VCC terminal can be used to limit the maximum high voltage, which will be passed by the PCA9545A. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5 V tolerant.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCA9545A	TSSOP (20)	6.50 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Application Diagram



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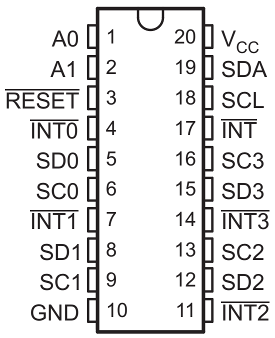
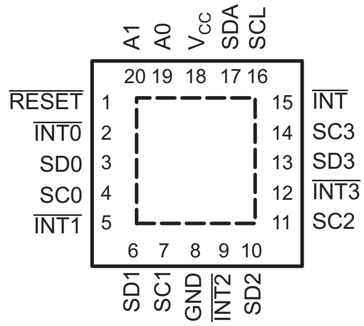
• Added Added $\overline{\text{RESET}}$ Errata section.	12
• Added Power-On Reset Errata section.	20

6 Pin Configuration and Functions

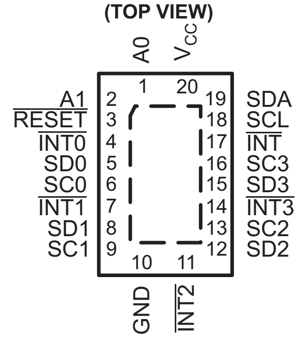
DGV, DW, OR PW PACKAGE (TOP VIEW)



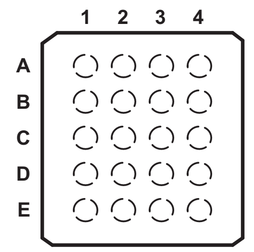
RGW PACKAGE (TOP VIEW)



RGY PACKAGE (TOP VIEW)



GQN OR ZQN PACKAGE (TOP VIEW)



Pin Functions

PIN				DESCRIPTION
NAME	DGV, DW, PW, AND RGY	RGW	GQN AND ZQN	
A0	1	19	A2	Address input 0. Connect directly to V_{CC} or ground.
A1	2	20	A1	Address input 1. Connect directly to V_{CC} or ground.
$\overline{\text{RESET}}$	3	1	B3	Active-low reset input. Connect to V_{DPUM}(1) through a pull-up resistor, if not used.
$\overline{\text{INT0}}$	4	2	B1	Active-low interrupt input 0. Connect to V_{DPU0}(1) through a pull-up resistor.
SD0	5	3	C2	Serial data 0. Connect to V_{DPU0}(1) through a pull-up resistor.
SC0	6	4	C1	Serial clock 0. Connect to V_{DPU0}(1) through a pull-up resistor.
$\overline{\text{INT1}}$	7	5	D3	Active-low interrupt input 1. Connect to V_{DPU1}(1) through a pull-up resistor.
SD1	8	6	D1	Serial data 1. Connect to V_{DPU1}(1) through a pull-up resistor.
SC1	9	7	E2	Serial clock 1. Connect to V_{DPU1}(1) through a pull-up resistor.
GND	10	8	E1	Ground
$\overline{\text{INT2}}$	11	9	E3	Active-low interrupt input 2. Connect to V_{DPU2}(1) through a pull-up resistor.
SD2	12	10	E4	Serial data 2. Connect to V_{DPU2}(1) through a pull-up resistor.
SC2	13	11	D2	Serial clock 2. Connect to V_{DPU2}(1) through a pull-up resistor.
$\overline{\text{INT3}}$	14	12	D4	Active-low interrupt input 3. Connect to V_{DPU3}(1) through a pull-up resistor.
SD3	15	13	C3	Serial data 3. Connect to V_{DPU3}(1) through a pull-up resistor.
SC3	16	14	C4	Serial clock 3. Connect to V_{DPU3}(1) through a pull-up resistor.
$\overline{\text{INT}}$	17	15	B2	Active-low interrupt output. Connect to V_{DPUM}(1) through a pull-up resistor.
SCL	18	16	B4	Serial clock line. Connect to V_{DPUM}(1) through a pull-up resistor.
SDA	19	17	A4	Serial data line. Connect to V_{DPUM}(1) through a pull-up resistor.
VCC	20	18	A3	Supply power

(1) V_{DPUX} is the pull-up reference voltage for the associated data line. V_{DPUM} is the master I^2C reference voltage while V_{DPU0}-V_{DPU3} are the slave channel reference voltages.

7 Specifications

7.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range[2]		–0.5	7	V
I_I	Input current			±20	mA
I_O	Output current			±25	mA
	Continuous current through V_{CC}			±100	mA
	Continuous current through GND			±100	mA
θ_{JA}	Package thermal impedance[3]	DGV package		92	°C/W
		DW package		58	
		GQN/ZQN package		78	
		PW package		83	
		RGW package		TBD	
		RGY package		47	
P_{tot}	Total power dissipation			400	mW
T_A	Operating free-air temperature range		–40	85	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CC}$	6	V
		A1, A0, $\overline{\text{INT3}}$–$\overline{\text{INT0}}$, $\overline{\text{RESET}}$	$0.7 \times V_{CC}$	$V_{CC} + 0.5$	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	$0.3 \times V_{CC}$	V
		A1, A0, $\overline{\text{INT3}}$–$\overline{\text{INT0}}$, $\overline{\text{RESET}}$	–0.5	$0.3 \times V_{CC}$	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

7.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP[(1)]	MAX	UNIT
V_{POR}	Power-on reset voltage[(2)]		No load, $V_I = V_{CC}$ or GND	V_{POR}		1.6	2.1	V
V_{pass}	Switch output voltage		$V_{SWin} = V_{CC}$, $I_{SWout} = –100\ \mu A$	5 V		3.6		V
				4.5 V to 5.5 V	2.6		4.5	
				3.3 V		1.9		
				3 V to 3.6 V	1.6		2.8	
				2.5 V		1.5		
				2.3 V to 2.7 V	1.1		2	
I_{OH}	$\overline{INT}$		$V_O = V_{CC}$	2.3 V to 5.5 V			10	μA
I_{OL}	SCL, SDA		$V_{OL} = 0.4$ V	2.3 V to 5.5 V	3	7		mA
			$V_{OL} = 0.6$ V		6	10		
	$\overline{INT}$		$V_{OL} = 0.4$ V		3			
I_I	SCL, SDA		$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			±1	μA
	SC3–SC0, SD3–SD0						±1	
	A1, A0						±1	
	$\overline{INT3}$–$\overline{INT0}$						±1	
	$\overline{RESET}$						±1	
I_{CC}	Operating mode	$f_{SCL} = 100$ kHz	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		3	12	μA
				3.6 V		3	11	
				2.7 V		3	10	
	Standby mode	Low inputs	V_I = GND, $I_O = 0$	5.5 V		0.3	1	
				3.6 V		0.1	1	
				2.7 V		0.1	1	
		High inputs	$V_I = V_{CC}$, $I_O = 0$	5.5 V		0.3	1	
				3.6 V		0.1	1	
				2.7 V		0.1	1	
ΔI_{CC}	Supply-current change	$\overline{INT3}$–$\overline{INT0}$	One $\overline{INT3}$–$\overline{INT0}$ input at 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V		8	15	μA
			One $\overline{INT3}$–$\overline{INT0}$ input at $V_{CC} – 0.6$ V, Other inputs at V_{CC} or GND			8	15	
		SCL, SDA	SCL or SDA input at 0.6 V, Other inputs at V_{CC} or GND			8	15	
			SCL or SDA input at $V_{CC} – 0.6$ V, Other inputs at V_{CC} or GND			8	15	
C_i	A1, A0		$V_I = V_{CC}$ or GND	2.3 V to 5.5 V		4.5	6	pF
	$\overline{INT3}$–$\overline{INT0}$					4.5	6	
	$\overline{RESET}$					4.5	5.5	
$C_{io(OFF)}$[(3)]	SCL, SDA		$V_I = V_{CC}$ or GND, Switch OFF	2.3 V to 5.5 V		15	19	pF
	SC3–SC0, SD3–SD0					6	8	
R_{ON}	Switch on-state resistance		$V_O = 0.4$ V, $I_O = 15$ mA	4.5 V to 5.5 V	4	9	16	Ω
				3 V to 3.6 V	5	11	20	
			$V_O = 0.4$ V, $I_O = 10$ mA	2.3 V to 2.7 V	7	16	45	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}), $T_A = 25°C$.
(2) The power-on reset circuit resets the I^2C bus logic with $V_{CC} < V_{POR}$. V_{CC} must be lowered to 0.2 V to reset the device.
(3) $C_{io(ON)}$ depends on the device capacitance and load that is downstream from the device.

7.5 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
			MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency		0	100	0	400	kHz
t_{sch}	I²C clock high time		4		0.6		μs
t_{scl}	I²C clock low time		4.7		1.3		μs
t_{sp}	I²C spike time			50		50	ns
t_{sds}	I²C serial-data setup time		250		100		ns
t_{sdh}	I²C serial-data hold time		0 (1)		0 (1)		μs
t_{icr}	I²C input rise time			1000	$20 + 0.1C_b$ (2)	300	ns
t_{icf}	I²C input fall time			300	$20 + 0.1C_b$ (2)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	$20 + 0.1C_b$ (2)	300	ns
t_{buf}	I²C bus free time between stop and start		4.7		1.3		μs
t_{sts}	I²C start or repeated start condition setup		4.7		0.6		μs
t_{sth}	I²C start or repeated start condition hold		4		0.6		μs
t_{sps}	I²C stop condition setup		4		0.6		μs
$t_{vdL(Data)}$	Valid-data time (high to low) (3)	SCL low to SDA output low valid		1		1	μs
$t_{vdH(Data)}$	Valid-data time (low to high) (3)	SCL low to SDA output high valid		0.6		0.6	μs
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		1		1	μs
C_b	I²C bus capacitive load			400		400	pF

(1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the V_{IH} min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.
(2) C_b = total bus capacitance of one bus line in pF
(3) Data taken using a 1-kΩ pull-up resistor and 50-pF load (see Figure 1)

7.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see Figure 3)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd} [(1)]	Propagation delay time	$R_{ON} = 20\ \Omega$, $C_L = 15$ pF	SDA or SCL	SDn or SCn		0.3	ns
		$R_{ON} = 20\ \Omega$, $C_L = 50$ pF				1	
t_{iv}	Interrupt valid time [(2)]		$\overline{\text{INTn}}$	$\overline{\text{INT}}$		4	µs
t_{ir}	Interrupt reset delay time [(2)]		$\overline{\text{INTn}}$	$\overline{\text{INT}}$		2	µs

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
(2) Data taken using a 4.7-kΩ pull-up resistor and 100-pF load (see Figure 3)

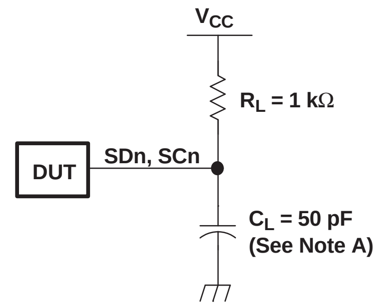
7.7 Interrupt and Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

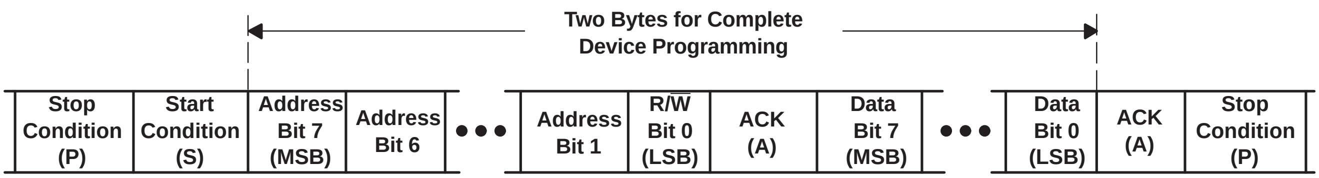
PARAMETER		MIN	MAX	UNIT
t_{PWRL}	Low-level pulse duration rejection of $\overline{\text{INTn}}$ inputs	1		µs
t_{PWRH}	High-level pulse duration rejection of $\overline{\text{INTn}}$ inputs	0.5		µs
t_{WL}	Pulse duration, $\overline{\text{RESET}}$ low	6		ns
t_{rst} [(1)]	$\overline{\text{RESET}}$ time (SDA clear)		500	ns
$t_{REC(STA)}$	Recovery time from $\overline{\text{RESET}}$ to start	0		ns

(1) t_{rst} is the propagation delay measured from the time the $\overline{\text{RESET}}$ pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of t_{WL}.

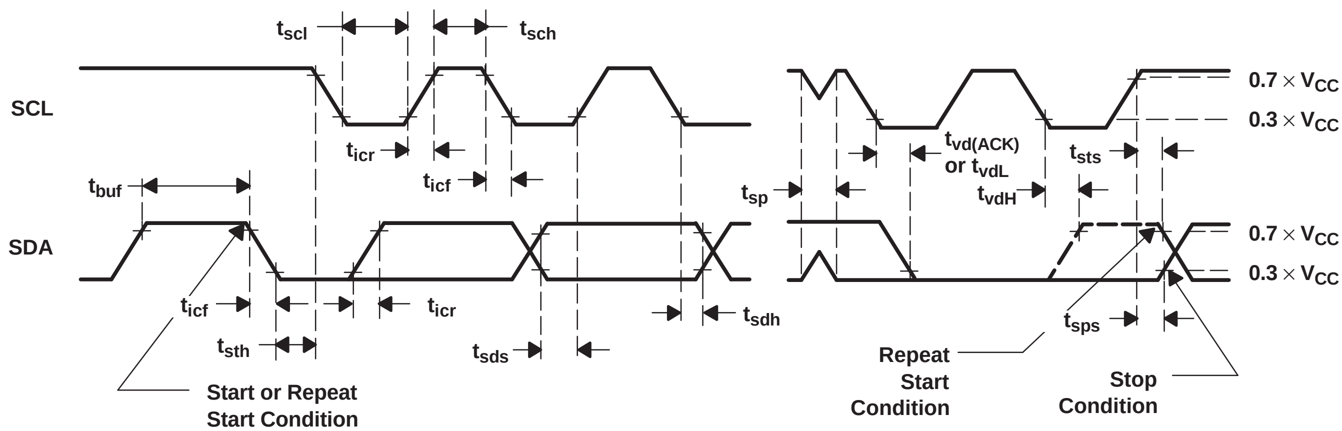
8 Parameter Measurement Information



I²C PORT LOAD CONFIGURATION



BYTE	DESCRIPTION
1	I²C address + R/W
2	Control register data



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 30 ns.

C. The outputs are measured one at a time, with one transition per measurement.

Figure 1. I²C Interface Load Circuit, Byte Descriptions, and Voltage Waveforms

Parameter Measurement Information (continued)

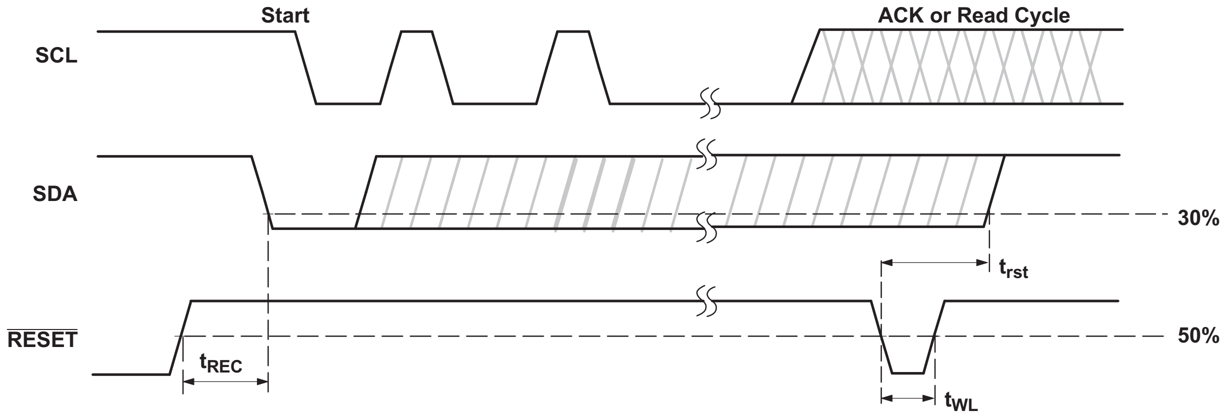
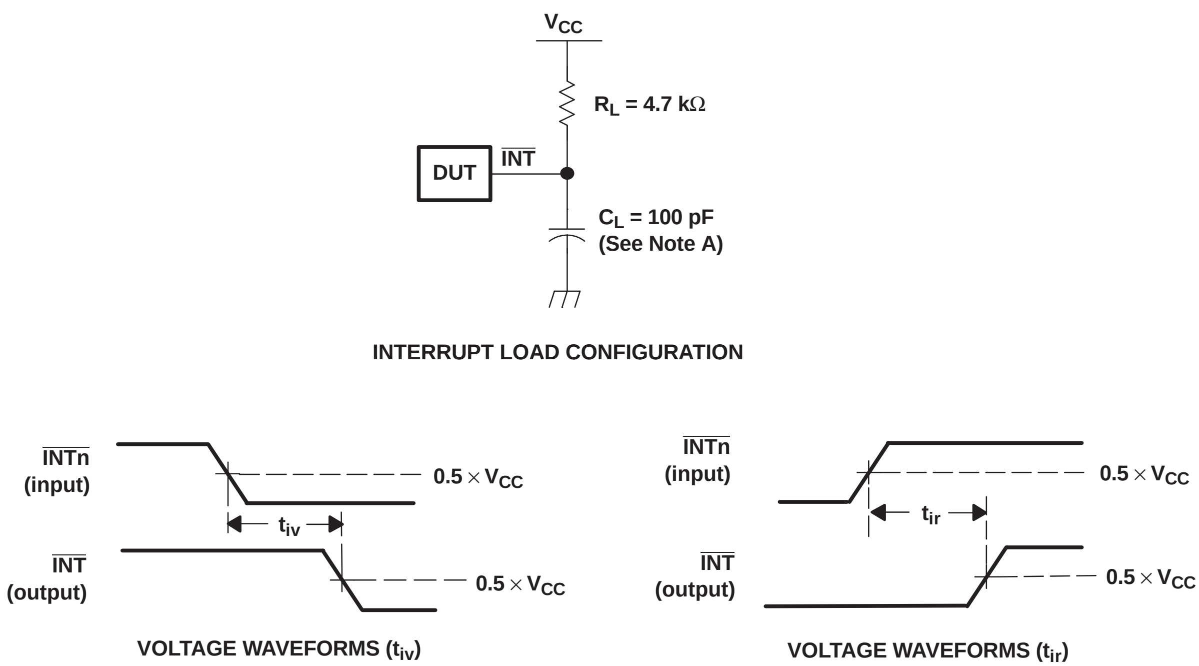


Figure 2. Reset Timing



A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 30 ns.

Figure 3. Interrupt Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

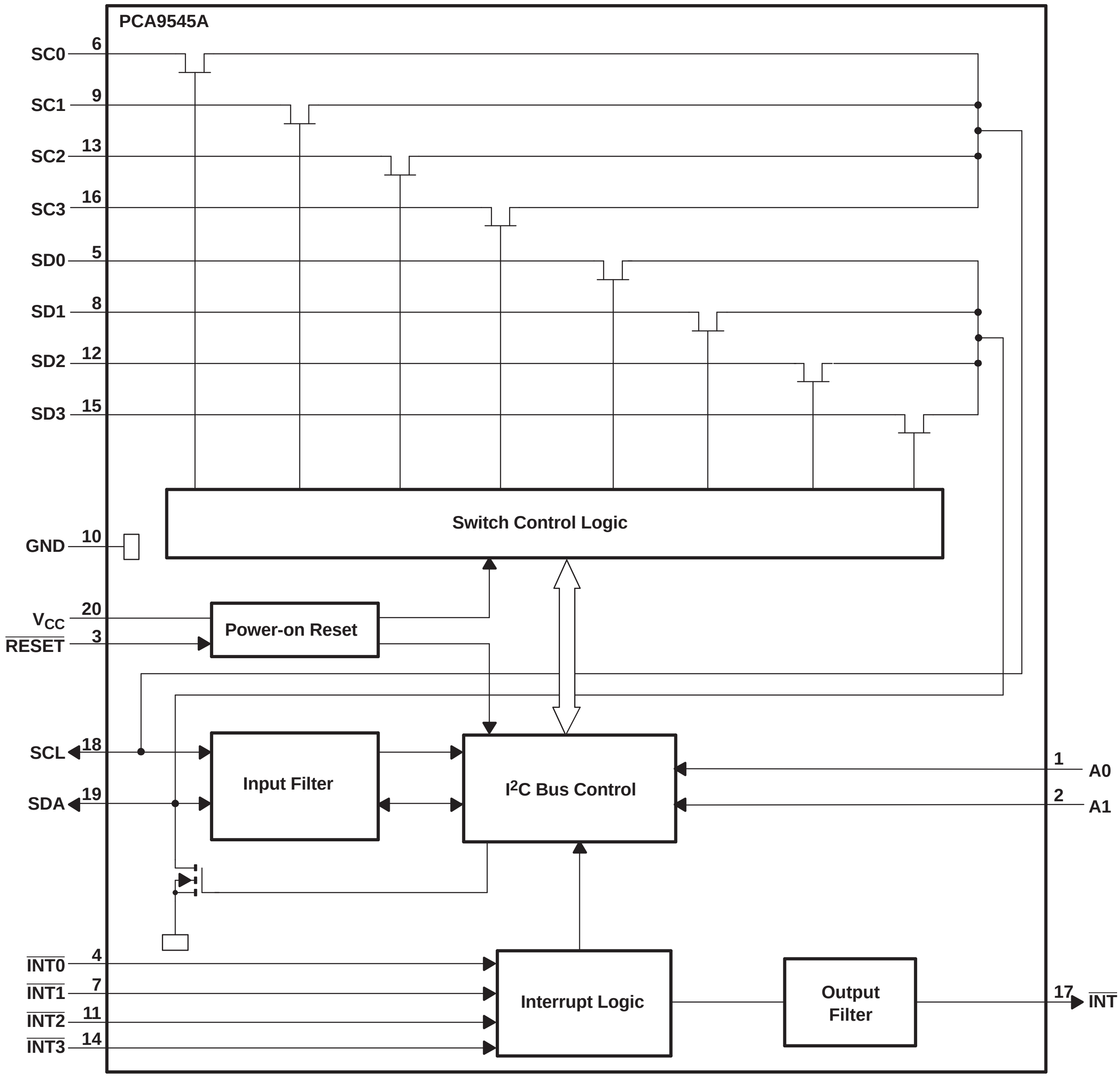
The PCA9545A is a 4-channel, bidirectional translating I²C switch. The master SCL/SDA signal pair is directed to four channels of slave devices, SC0/SD0-SC3/SD3. Any individual downstream channel can be selected as well as any combination of the four channels. The PCA9545A also supports interrupt signals in order for the master to detect an interrupt on the $\overline{INT}$ output terminal that can result from any of the slave devices connected to the $\overline{INT3}$-$\overline{INT0}$ input terminals.

The device offers an active-low $\overline{RESET}$ input which resets the state machine and allows the PCA9545A to recover should one of the downstream I²C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, V_{CC}, also known as a power-on reset (POR). Both the $\overline{RESET}$ function and a POR will cause all channels to be deselected.

The connections of the I²C data path are controlled by the same I²C master device that is switched to communicate with multiple I²C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0 and A1 terminals), a single 8-bit control register is written to or read from to determine the selected channels and state of the interrupts.

The PCA9545A may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

9.2 Functional Block Diagram



Pin numbers shown are for DGV, DW, PW, and RGY packages.

9.3 Feature Description

The PCA9545A is a 4-channel, bidirectional translating switch for I^{2}C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The PCA9545A features I^{2}C control using a single 8-bit control register in which the four least significant bits control the enabling and disabling of the 4 switch channels of I^{2}C data flow. The PCA9545A also supports interrupt signals for each slave channel and this data is held in the four most significant bits of the control register. Depending on the application, voltage translation of the I^{2}C bus can also be achieved using the PCA9545A to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I^{2}C bus enters a fault state, the PCA9545A can be reset to resume normal operation using the $\overline{\text{RESET}}$ pin feature or by a power-on reset which results from cycling power to the device.

9.4 Device Functional Modes

9.4.1 $\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input can be used to recover the PCA9545A from a bus-fault condition. The registers and the I^{2}C state machine within this device initialize to their default states if this signal is asserted low for a minimum of t_{WL}. All channels also are deselected in this case. $\overline{\text{RESET}}$ must be connected to V_{CC} through a pull-up resistor.

9.4.1.1 $\overline{\text{RESET}}$ Errata

If $\overline{\text{RESET}}$ voltage set higher than VCC, current will flow from $\overline{\text{RESET}}$ pin to VCC pin.

System Impact

VCC will be pulled above its regular voltage level

System Workaround

Design such that $\overline{\text{RESET}}$ voltage is same or lower than VCC

9.4.2 Power-On Reset

When power is applied to VCC, an internal power-on reset holds the PCA9545A in a reset condition until V_{CC} has reached V_{PORR}. At this point, the reset condition is released and the PCA9545A registers and I^{2}C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below at least V_{PORF} to reset the device.

Refer to the *Power-On Reset Errata* section.

9.5 Programming

9.5.1 I^{2}C Interface

The I^{2}C bus is for two-way two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer can be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse, as changes in the data line at this time are interpreted as control signals (see Figure 4).

Programming (continued)

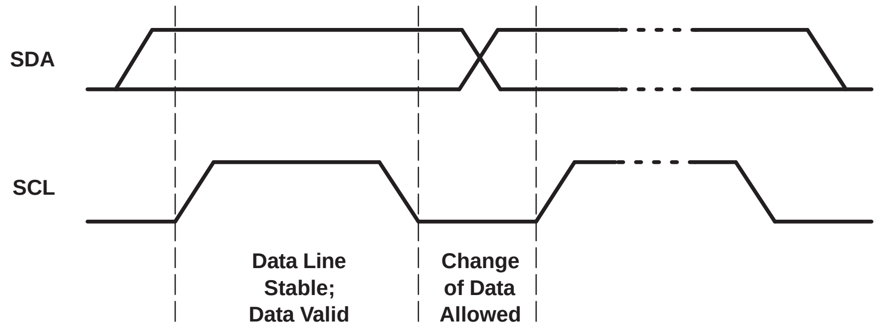


Figure 4. Bit Transfer

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 5).

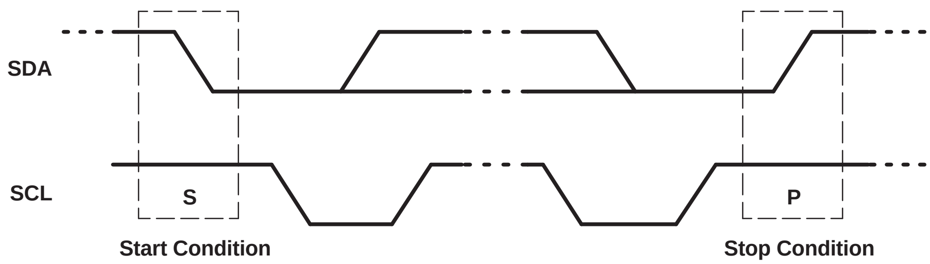


Figure 5. Definition of Start and Stop Conditions

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master, and the devices that are controlled by the master are the slaves (see Figure 6).

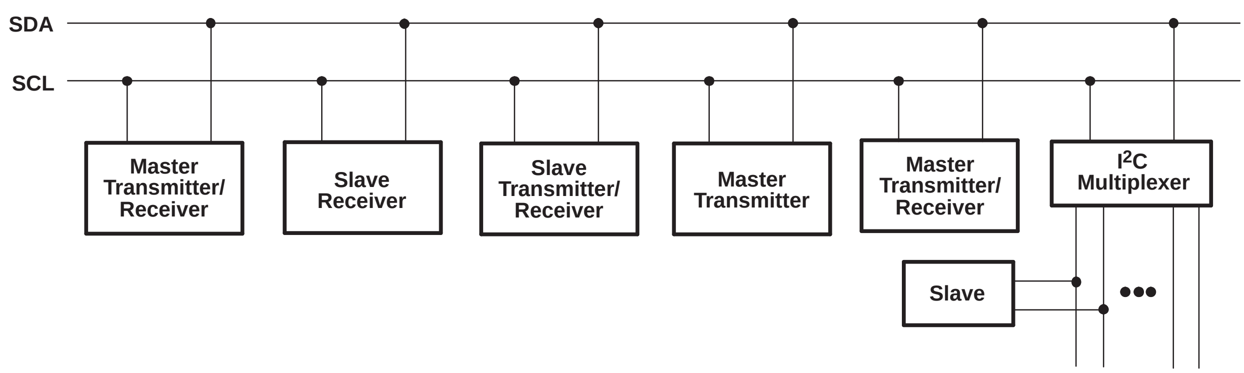


Figure 6. System Configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 7). Setup and hold times must be taken into account.

Programming (continued)

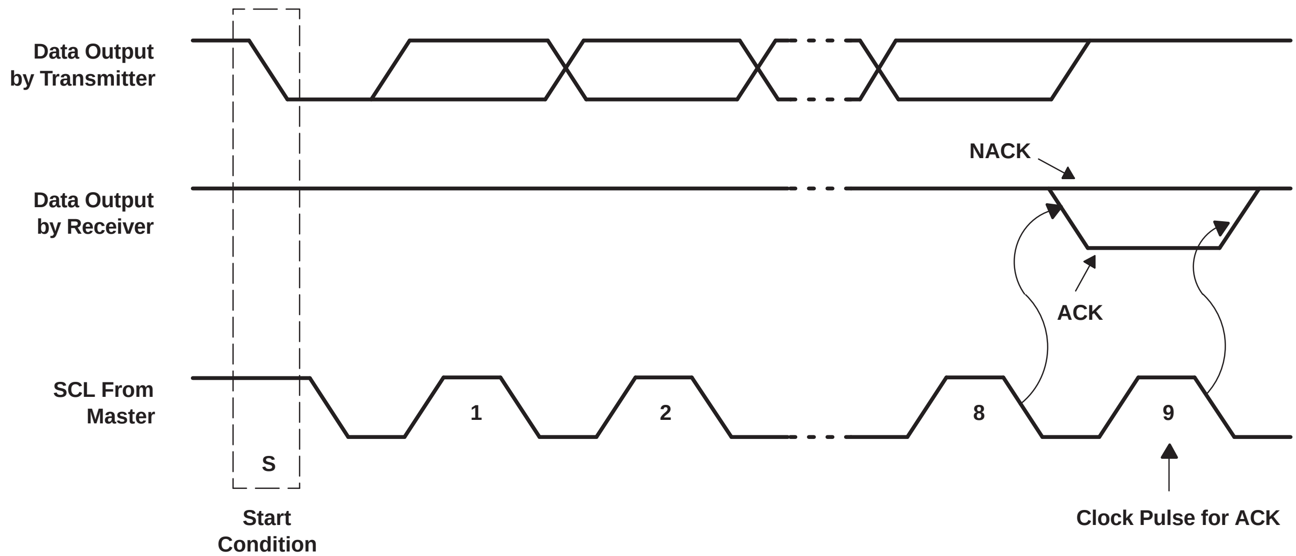


Figure 7. Acknowledgment on the I²C Bus

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

Data is transmitted to the PCA9545A control register using the write mode shown in Figure 8.

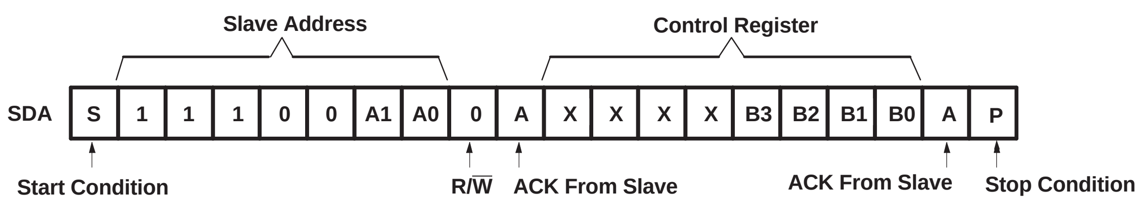


Figure 8. Write Control Register

Data is read from the PCA9545A control register using the read mode shown in Figure 9.

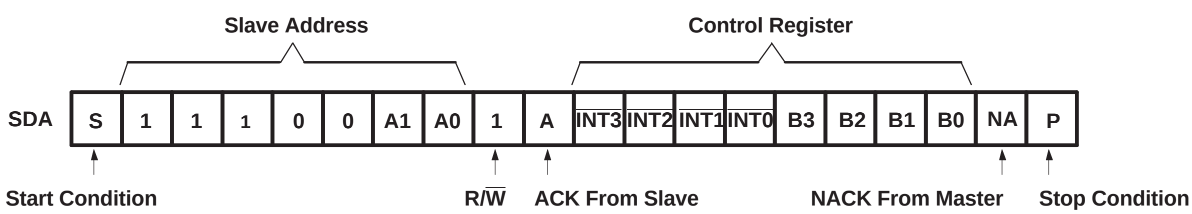


Figure 9. Read Control Register

9.6 Control Register

9.6.1 Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the PCA9545A is shown in Figure 10. To conserve power, no internal pull-up resistors are incorporated on the hardware-selectable address terminals, and they must be pulled high or low.

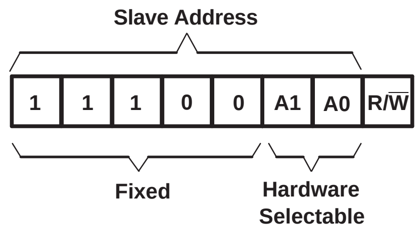


Figure 10. PCA9545A Address

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

9.6.2 Control Register Description

Following the successful acknowledgment of the slave address, the bus master sends a byte to the PCA9545A, which is stored in the control register (see Figure 11). If multiple bytes are received by the PCA9545A, it saves the last byte received. This register can be written and read via the I^2C bus.

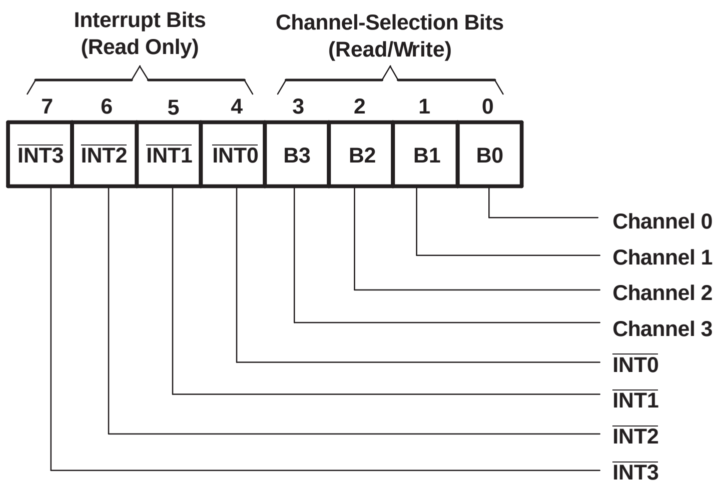


Figure 11. Control Register

9.6.3 Control Register Definition

One or several SCn/SDn downstream pairs, or channels, are selected by the contents of the control register (see Table 1). After the PCA9545A has been addressed, the control register is written. The four LSBs of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I^2C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition must occur always right after the acknowledge cycle.

Control Register (continued)

Table 1. Control Register Write (Channel Selection), Control Register Read (Channel Status)(1)

<table>
<tr><th>$\overline{\text{INT3}}$</th><th>$\overline{\text{INT2}}$</th><th>$\overline{\text{INT1}}$</th><th>$\overline{\text{INT0}}$</th><th>B3</th><th>B2</th><th>B1</th><th>B0</th><th>COMMAND</th></tr>
<tr><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>0</td><td>Channel 0 disabled</td></tr>
<tr><td>1</td><td>Channel 0 enabled</td></tr>
<tr><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>0</td><td rowspan="2">X</td><td>Channel 1 disabled</td></tr>
<tr><td>1</td><td>Channel 1 enabled</td></tr>
<tr><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>0</td><td rowspan="2">X</td><td rowspan="2">X</td><td>Channel 2 disabled</td></tr>
<tr><td>1</td><td>Channel 2 enabled</td></tr>
<tr><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>0</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>Channel 3 disabled</td></tr>
<tr><td>1</td><td>Channel 3 enabled</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>X</td><td>0</td><td>No channel selected,
power-up/reset default state</td></tr>
</table>

(1) Several channels can be enabled at the same time. For example, B3 = 0, B2 = 1, B1 = 1, B0 = 0 means that channels 0 and 3 are disabled, and channels 1 are 2 and enabled. Care should be taken not to exceed the maximum bus capacity.

9.6.4 Interrupt Handling

The PCA9545A provides four interrupt inputs (one for each channel) and one open-drain interrupt output (see Table 2). When an interrupt is generated by any device, it is detected by the PCA9545A and the interrupt output is driven low. The channel does not need to be active for detection of the interrupt. A bit also is set in the control register.

Bits 4–7 of the control register correspond to channels 0–3 of the PCA9545A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master then can address the PCA9545A and read the contents of the control register to determine which channel contains the device generating the interrupt. The master then can reconfigure the PCA9545A to select this channel and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs can be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to V_{CC}.

Table 2. Control Register Read (Interrupt)(1)

<table>
<tr><th>$\overline{\text{INT3}}$</th><th>$\overline{\text{INT2}}$</th><th>$\overline{\text{INT1}}$</th><th>$\overline{\text{INT0}}$</th><th>B3</th><th>B2</th><th>B1</th><th>B0</th><th>COMMAND</th></tr>
<tr><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>0</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>No interrupt on channel 0</td></tr>
<tr><td>1</td><td>Interrupt on channel 0</td></tr>
<tr><td rowspan="2">X</td><td rowspan="2">X</td><td>0</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>No interrupt on channel 1</td></tr>
<tr><td>1</td><td>Interrupt on channel 1</td></tr>
<tr><td rowspan="2">X</td><td>0</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>No interrupt on channel 2</td></tr>
<tr><td>1</td><td>Interrupt on channel 2</td></tr>
<tr><td>0</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>No interrupt on channel 3</td></tr>
<tr><td>1</td><td>Interrupt on channel 3</td></tr>
</table>

(1) Several interrupts can be active at the same time. For example, $\overline{\text{INT3}}$ = 0, $\overline{\text{INT2}}$ = 1, $\overline{\text{INT1}}$ = 1, $\overline{\text{INT0}}$ = 0 means that there is no interrupt on channels 0 and 3, and there is interrupt on channels 1 and 2.

10 Application and Implementation

10.1 Application Information

Applications of the PCA9545A will contain an I^2C (or SMBus) master device and up to four I^2C slave devices. The downstream channels are ideally used to resolve I^2C slave address conflicts. For example, if four identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0, 1, 2, and 3. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I^2C master can move on and read the next channel.

In an application where the I^2C bus will contain many additional slave devices that do not result in I^2C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches will be enabled simultaneously, additional design requirements must be considered (See *Design Requirements* and *Detailed Design Procedure*).

10.2 Typical Application

A typical application of the PCA9545A will contain anywhere from 1 to 5 separate data pull-up voltages, V_{DPUX} , one for the master device (V_{DPUM}) and one for each of the selectable slave channels (V_{DPU0} – V_{DPU3}). In the event where the master device and all slave devices operate at the same voltage, then the pass voltage, V_{pass} = V_{DPUX}. Once the maximum V_{pass} is known, V_{cc} can be selected easily using Figure 13. In an application where voltage translation is necessary, additional design requirements must be considered (See *Design Requirements*).

Figure 12 shows an application in which the PCA9545A can be used.

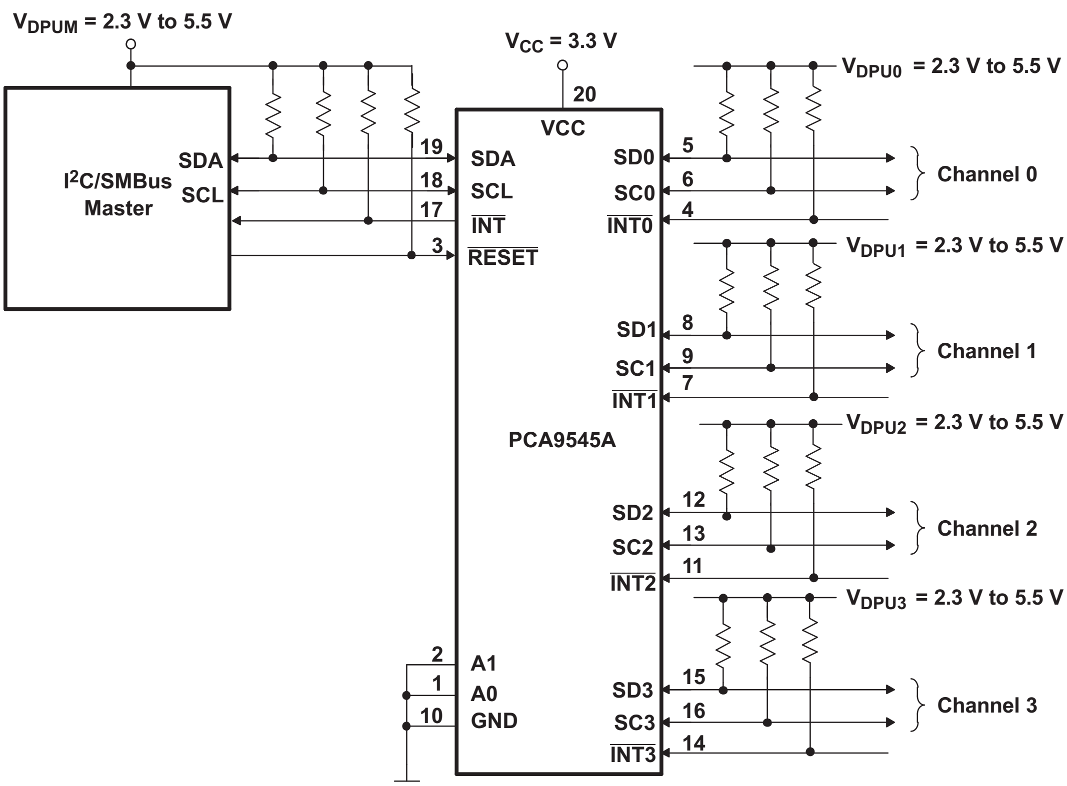


Figure 12. Typical Application Schematic

Typical Application (continued)

10.2.1 Design Requirements

The pull-up resistors on the $\overline{INT3}$-$\overline{INT0}$ terminals in the application schematic are not required in all applications. If the device generating the interrupt has an open-drain output structure or can be tri-stated, a pull-up resistor is required. If the device generating the interrupt has a push-pull output structure and cannot be tri-stated, a pull-up resistor is not required. The interrupt inputs should not be left floating in the application.

The A0 and A1 terminals are hardware selectable to control the slave address of the PCA9545A. These terminals may be tied directly to GND or V_{CC} in the application.

If multiple slave channels will be activated simultaneously in the application, then the total I_{OL} from SCL/SDA to GND on the master side will be the sum of the currents through all pull-up resistors, R_p.

The pass-gate transistors of the PCA9545A are constructed such that the V_{CC} voltage can be used to limit the maximum voltage that is passed from one I^2C bus to another.

Figure 13 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the *Electrical Characteristics* section of this data sheet). In order for the PCA9545A to act as a voltage translator, the V_{pass} voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V, V_{pass} must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 13, $V_{pass(max)}$ is 2.7 V when the PCA9545A supply voltage is 4 V or lower, so the PCA9545A supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 12).

10.2.2 Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors, R_p, for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of V_{DPUX}, $V_{OL,(max)}$, and I_{OL}:

$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I^2C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCA9545A, $C_{io(OFF)}$, the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If multiple channels will be activated simultaneously, each of the slaves on all channels will contribute to total bus capacitance.

Typical Application (continued)

10.2.3 PCA9545A Application Curves

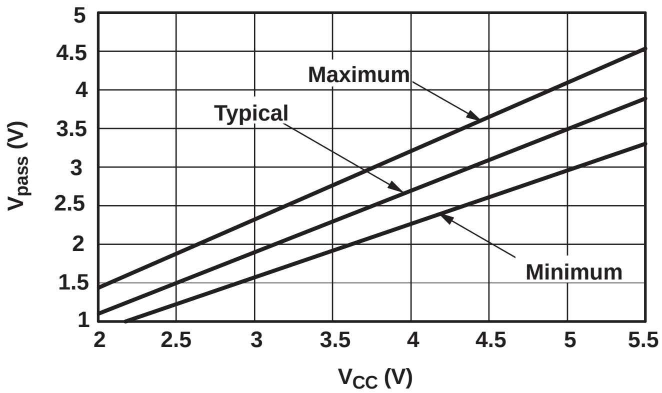
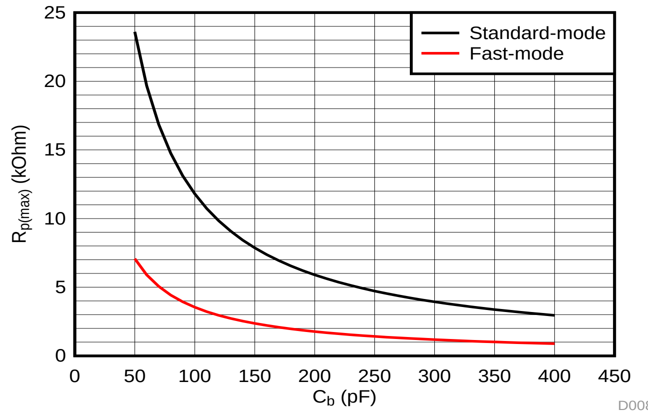


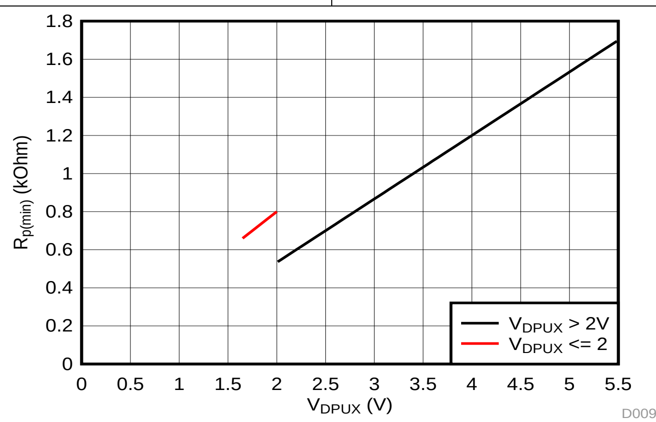
Figure 13. Pass-Gate Voltage (V_{pass}) vs Supply Voltage (V_{CC}) at Three Temperature Points



Standard-mode (f_{SCL}= 100 kHz, t_r = 1 µs)

Fast-mode (f_{SCL}= 400 kHz, t_r= 300 ns)

Figure 14. Maximum Pull-Up resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2*V_{DPUX}, I_{OL} = 2 mA when $V_{DPUX} \leq$ 2 V

V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{DPUX} > 2 V

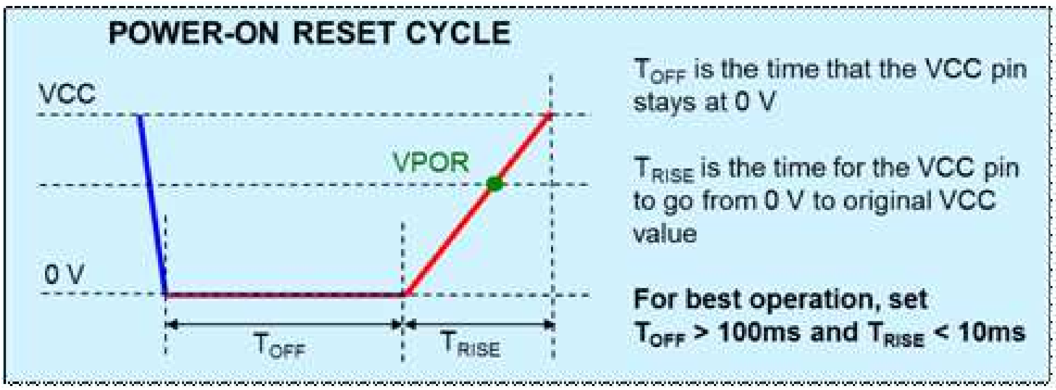
Figure 15. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{DPUX})

11 Power Supply Recommendations

The operating power-supply voltage range of the PCA9545A is 2.3 V to 5.5 V applied at the VCC pin. When the PCA9545A is powered on for the first time or anytime the device needs to be reset by cycling the power supply, the power-on reset requirements must be followed to ensure the I^2C bus logic is initialized properly.

11.1 Power-On Reset Errata

A power-on reset condition can be missed if the VCC ramps are outside specification listed below.



System Impact

If ramp conditions are outside timing allowances above, POR condition can be missed, causing the device to lock up.

12 Layout

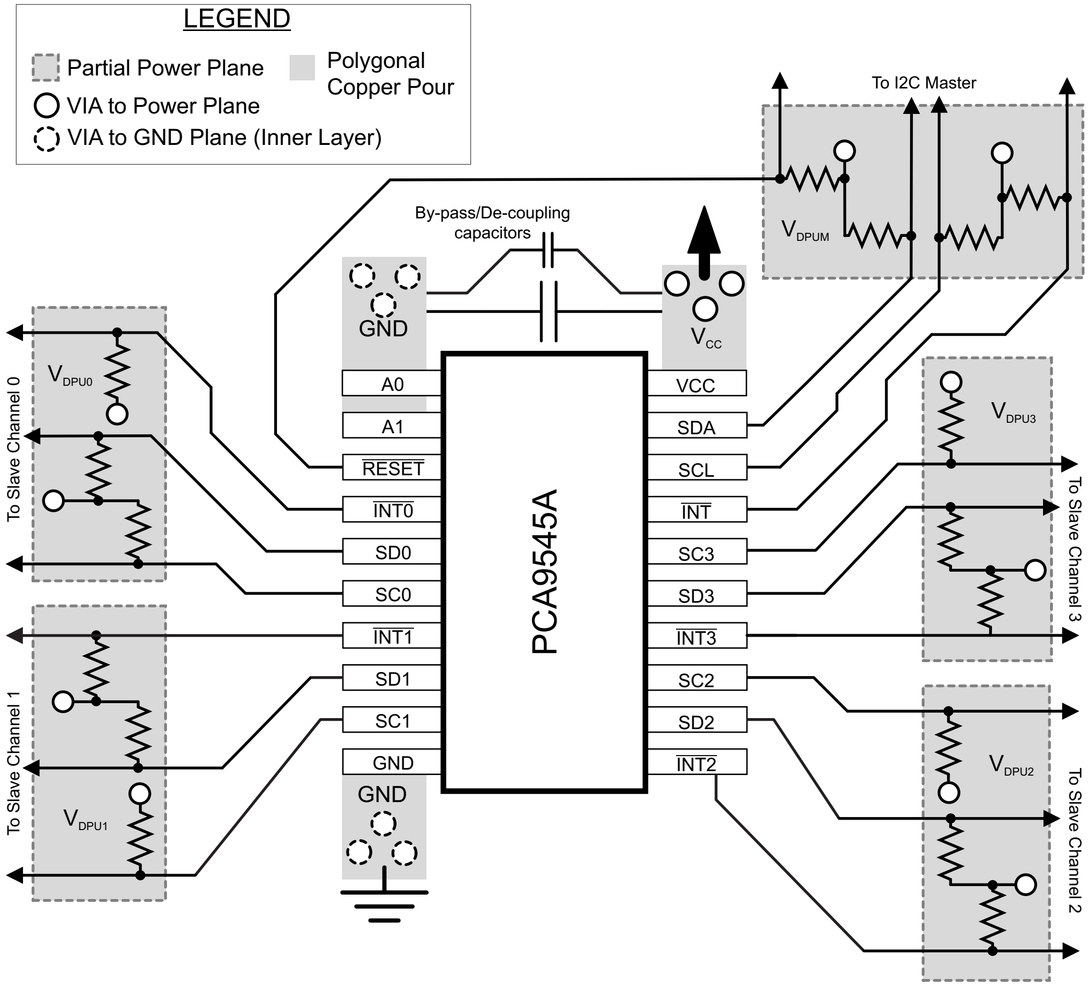
12.1 Layout Guidelines

For PCB layout of the PCA9545A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and terminals that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC terminal, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all V_{DPUX} voltages and V_{CC} could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V_{DPUM}, V_{DPU0}, V_{DPU1}, V_{DPU2}, and V_{DPU3} may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I^2C bus capacitance added by PCB parasitics, data lines (SCn, SDn and $\overline{\text{INTn}}$) should be a short as possible and the widths of the traces should also be minimized (e.g. 5-10 mils depending on copper weight).

12.2 Layout Example



13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9545ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9545A	Samples
PCA9545ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9545A	Samples
PCA9545APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD545A	Samples
PCA9545APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD545A	Samples
PCA9545APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD545A	Samples
PCA9545ARGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD545A	Samples
PCA9545ARGYRG4	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD545A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

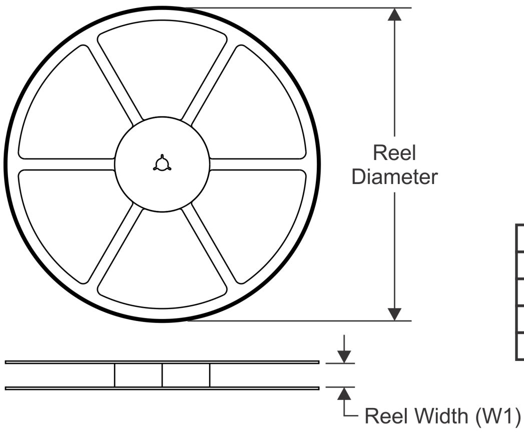
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

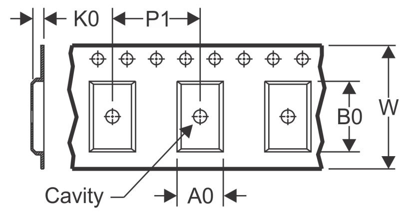
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

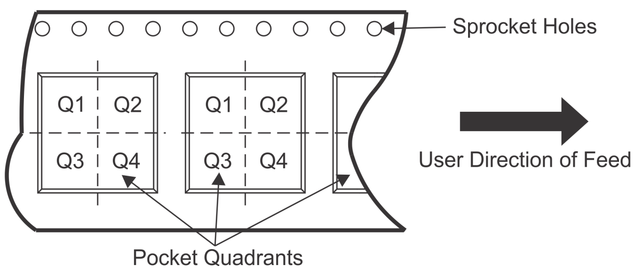


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

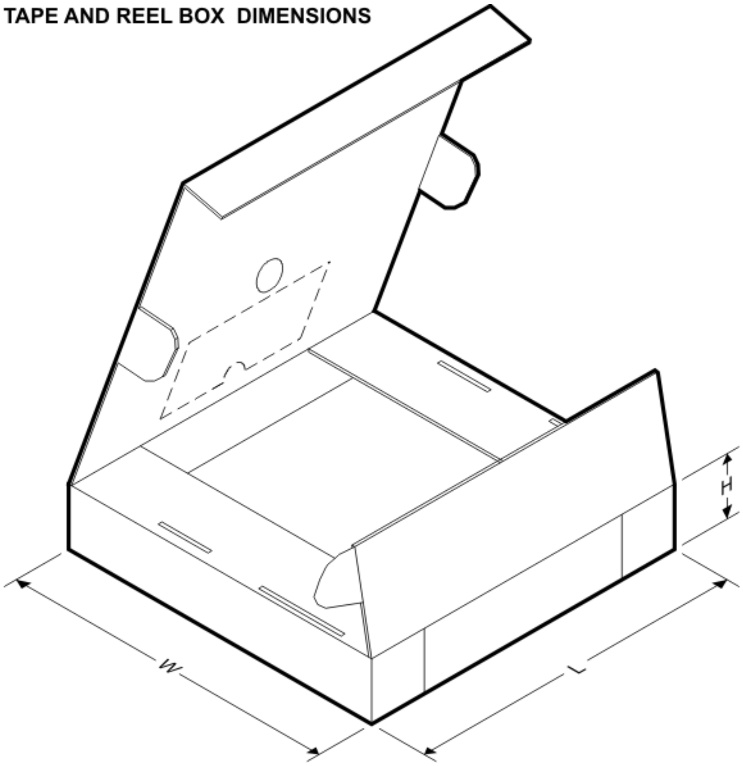
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9545ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
PCA9545APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
PCA9545APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
PCA9545ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

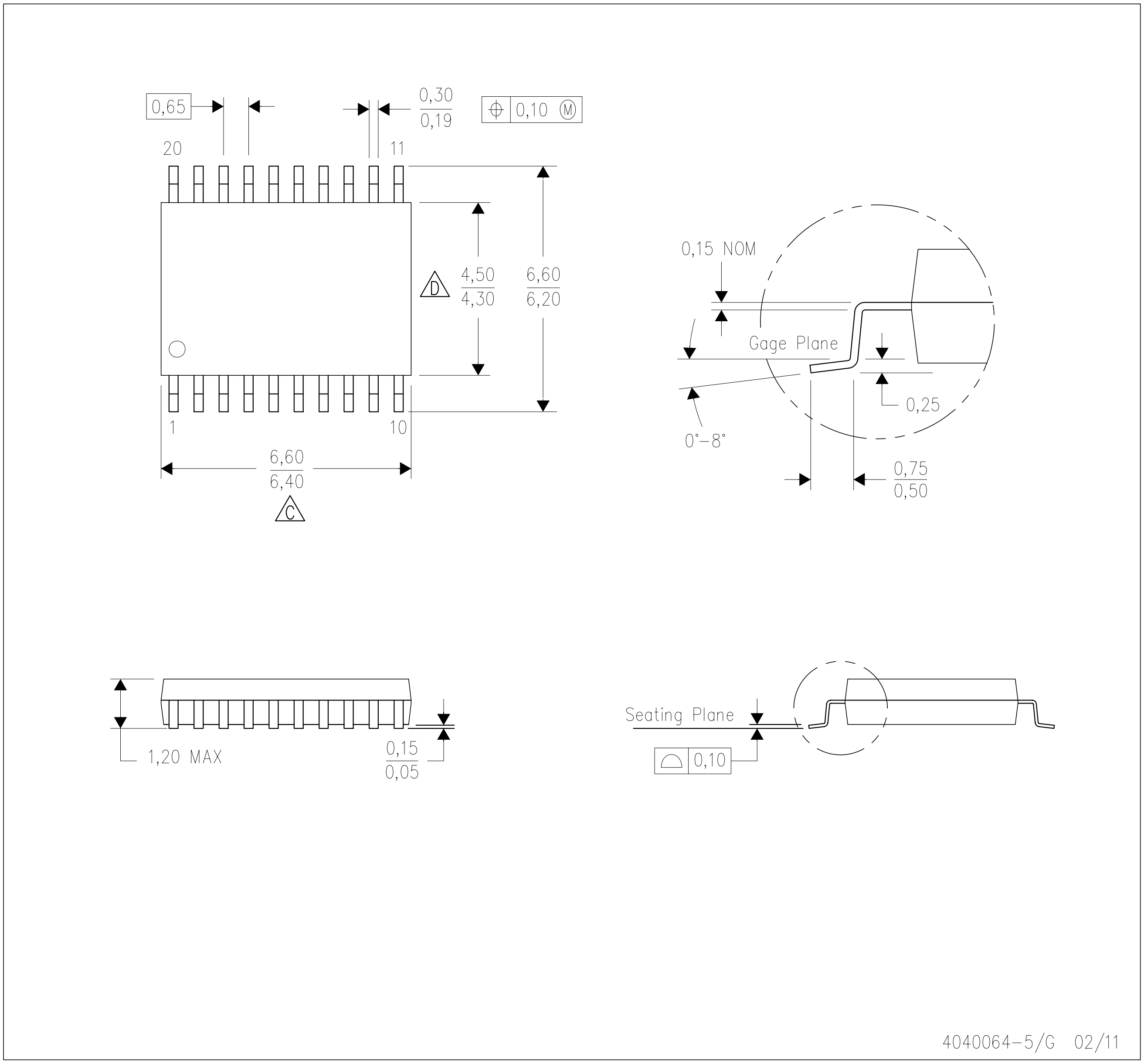
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9545ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
PCA9545APWR	TSSOP	PW	20	2000	367.0	367.0	38.0
PCA9545APWT	TSSOP	PW	20	250	367.0	367.0	38.0
PCA9545ARGYR	VQFN	RGY	20	3000	367.0	367.0	35.0

PW (R-PDSO-G20) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

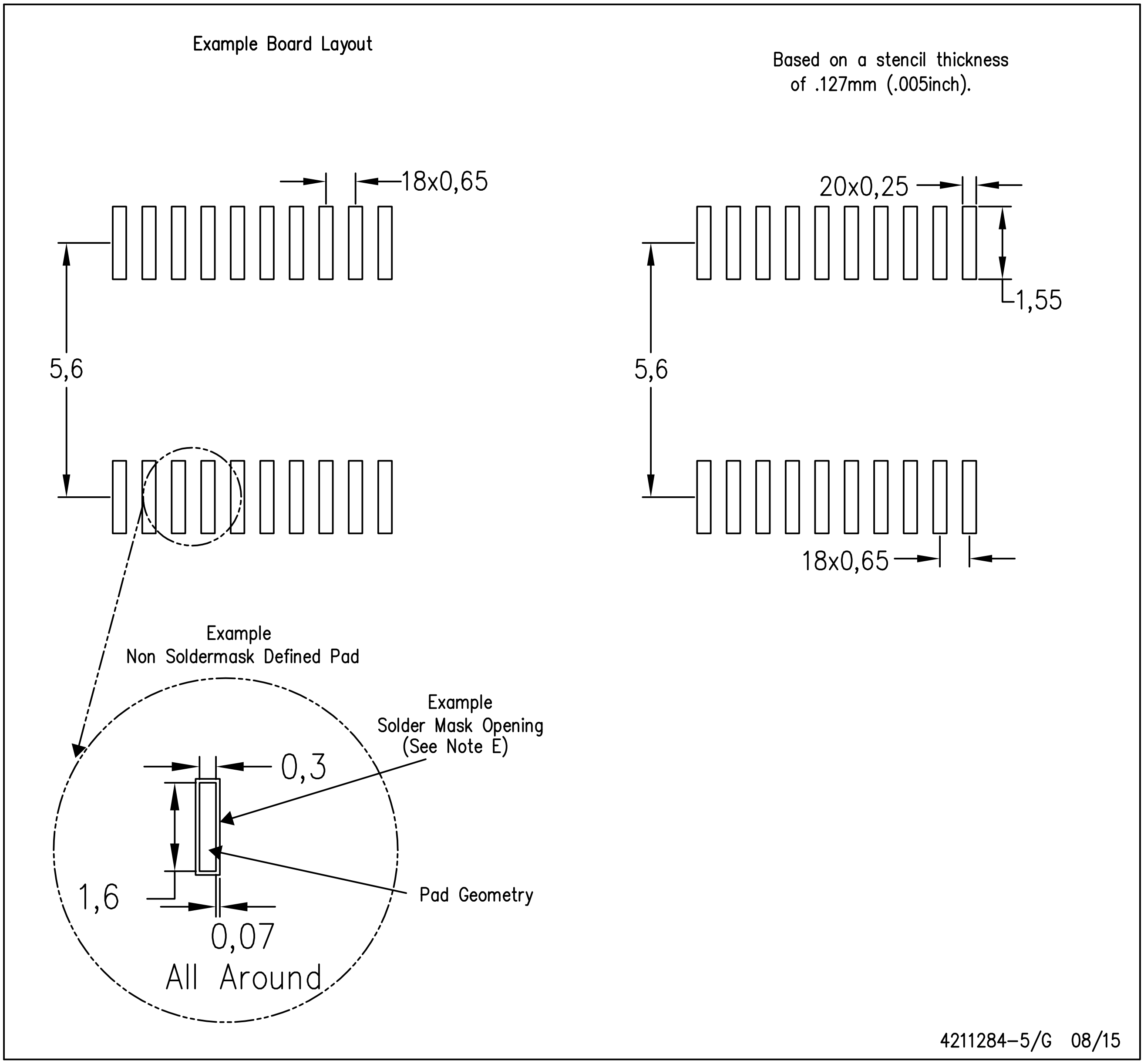
B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

PW (R-PDSO-G20) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

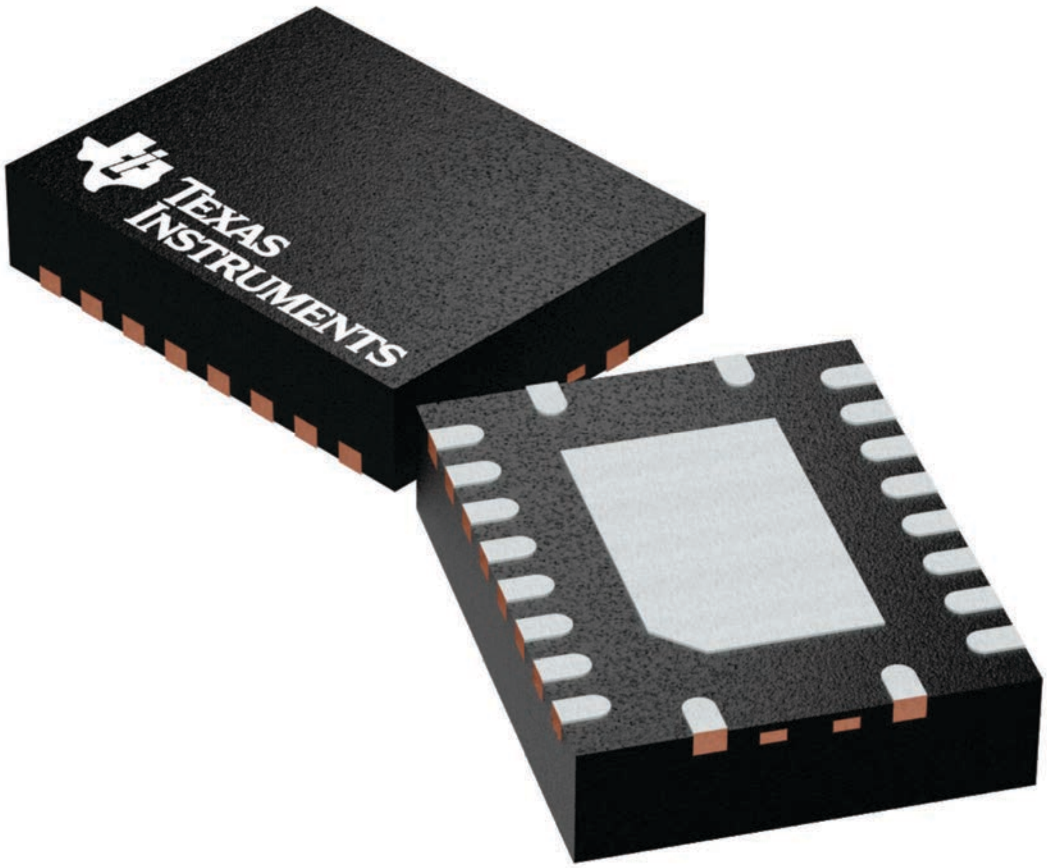
RGY 20

VQFN - 1 mm max height

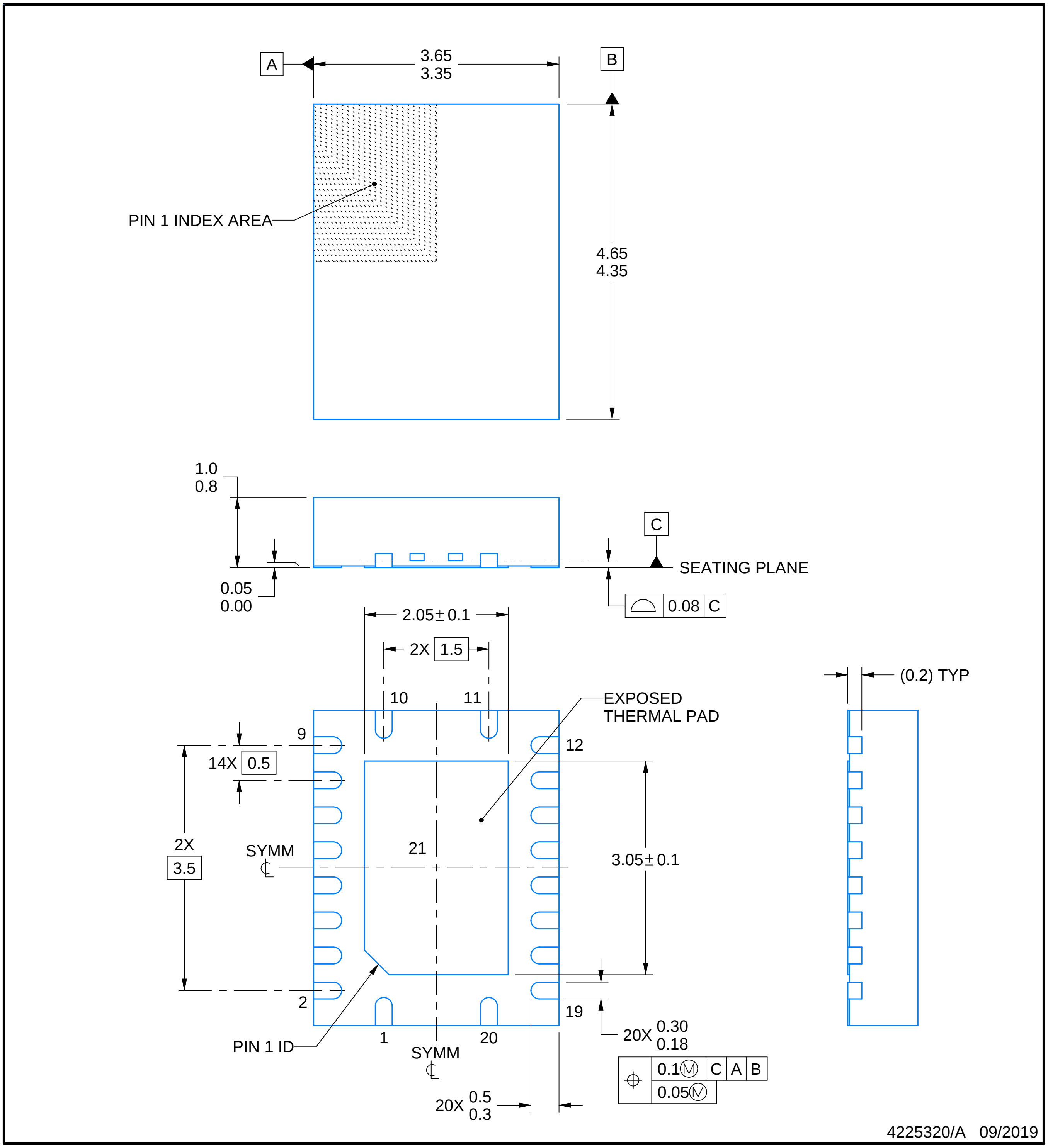
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

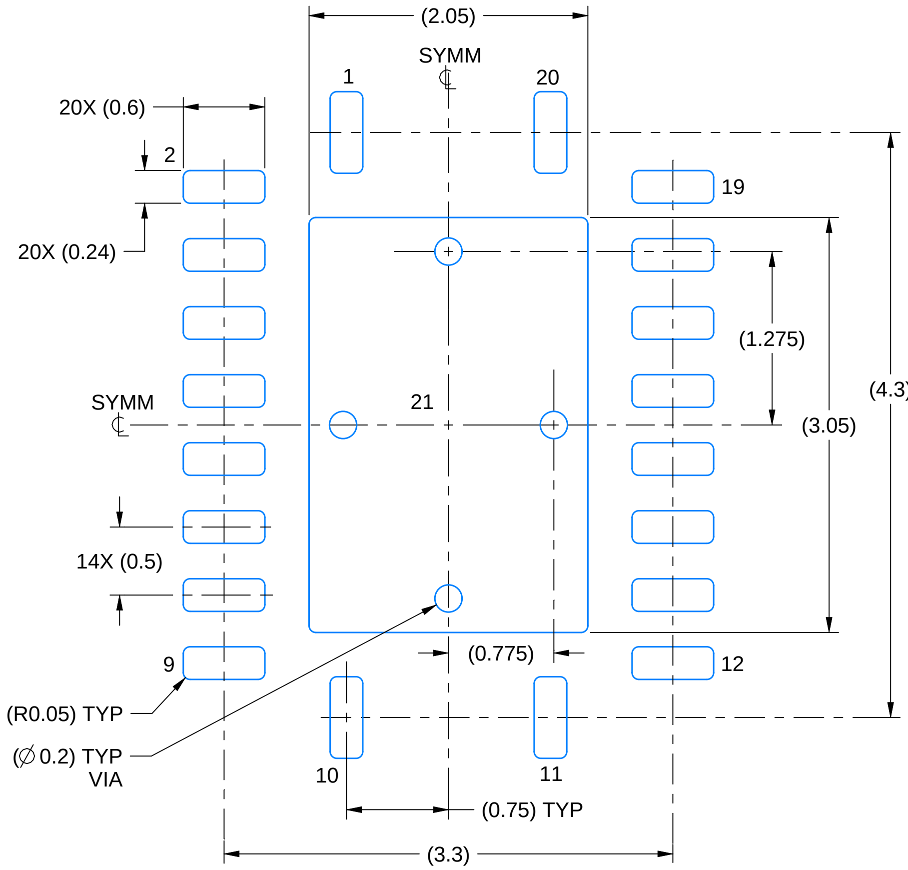


4225264/A

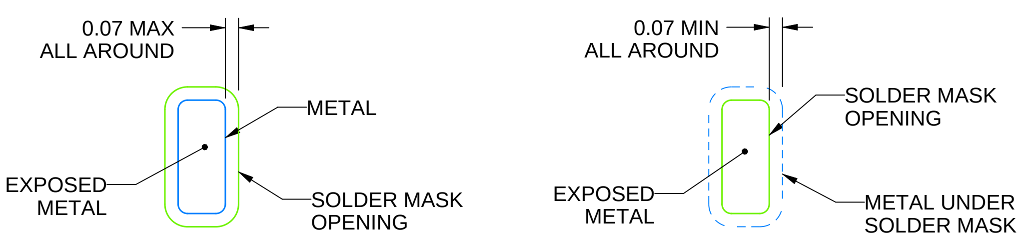


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

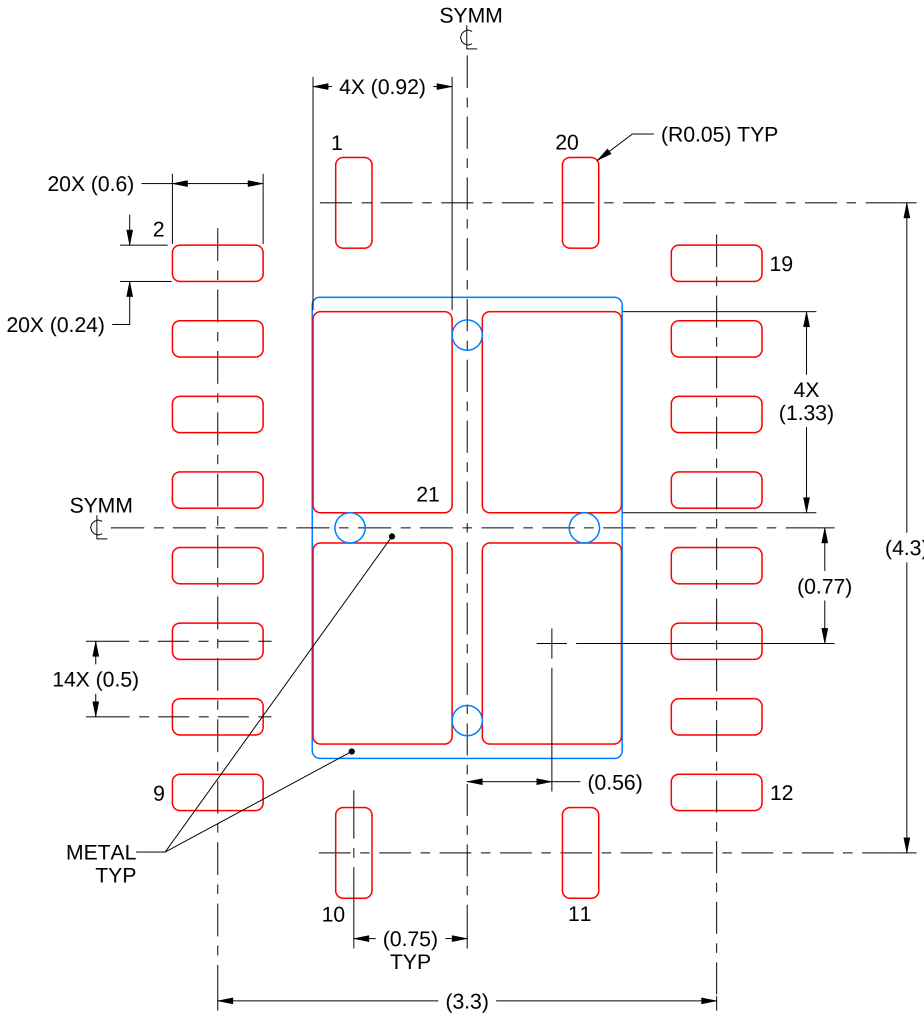
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



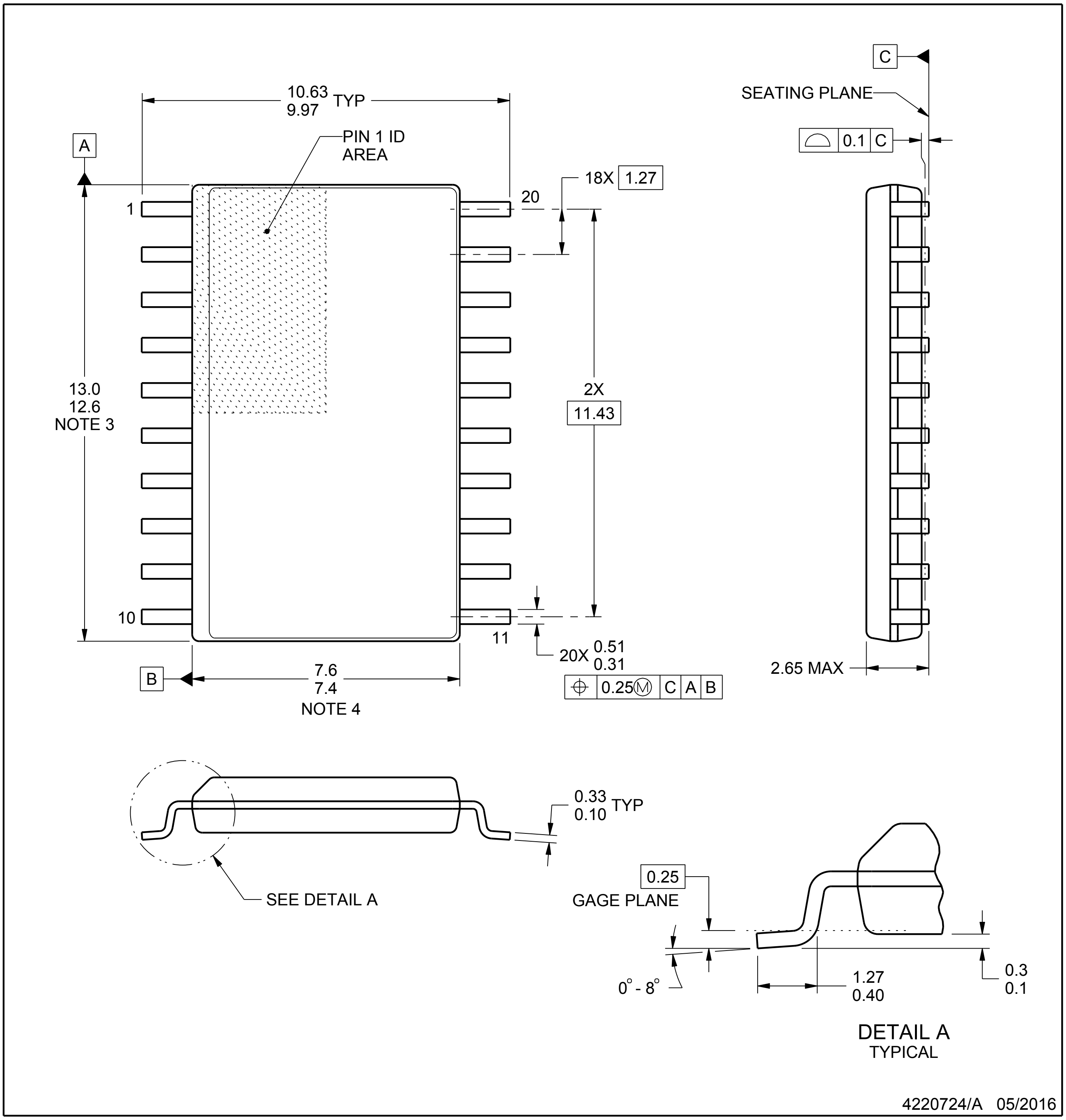
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

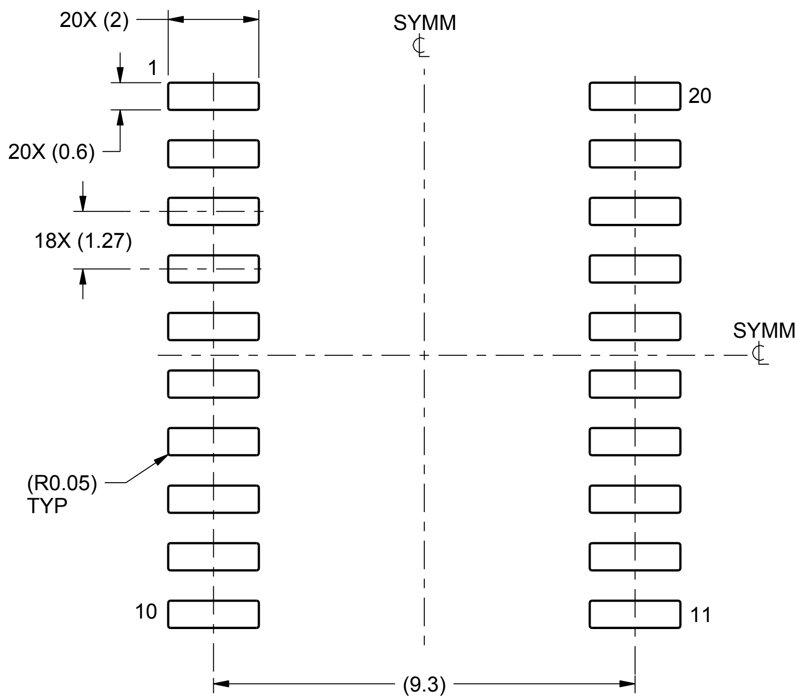
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

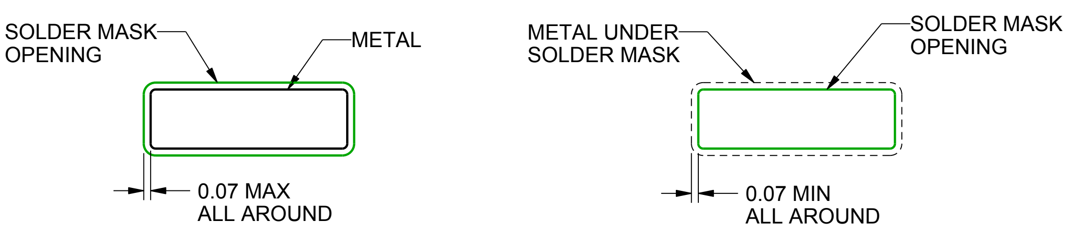


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK DEFINED

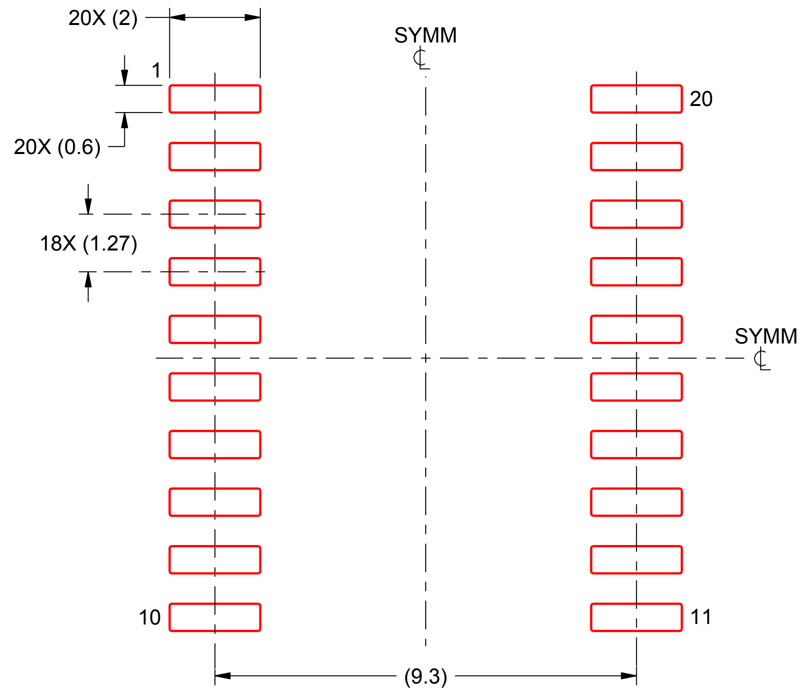
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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