TEXAS INSTRUMENTS

TPS82692, TPS82693, TPS826951
TPS82697, TPS82698

SLVSBF8C – MARCH 2013 – REVISED MAY 2015

TPS8269x High-Efficiency MicroSIP™ Step-Down Converter (Profile <1 mm)

1 Features

- Total Solution Size < 6.7 mm^2
- 95% Efficiency at 3-MHz Operation
- 23µA Quiescent Current
- High Duty-Cycle Operation
- *Best in Class* Load and Line Transient
- ±2% Total DC Voltage Accuracy
- Automatic PFM/PWM Mode Switching
- Low Ripple Light-Load PFM Mode
- Excellent AC Load Regulation
- Internal Soft Start, 200-µs Start-Up Time
- Integrated Active Power-Down Sequencing (Optional)
- Current Overload and Thermal Shutdown Protection
- Sub 1-mm Profile Solution

2 Applications

- Cell Phones, Smart-Phones
- Optical Data Modules
- Camera and Sensor Modules
- Wearable Devices
- LDO Replacement

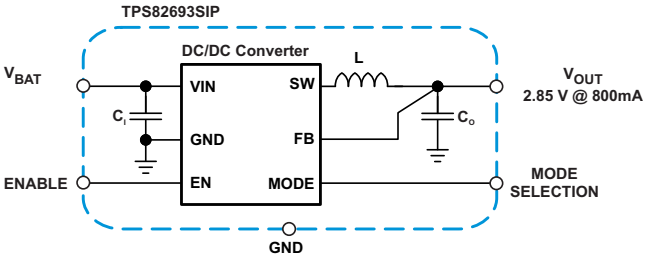
3 Description

The TPS8269xSIP device is a complete 500 mA / 800 mA, DC/DC step-down power supply intended for low-power applications. Included in the package are the switching regulator, inductor and input/output capacitors. No additional components are required to finish the design. The TPS8269xSIP is based on a high-frequency synchronous step-down dc-dc converter optimized for battery-powered portable applications. The MicroSIP™ DC/DC converter operates at a regulated 3-MHz switching frequency and enters the power-save mode operation at light load currents to maintain high efficiency over the entire load current range. The PFM mode extends the battery life by reducing the quiescent current to 23 µA (typical) during light load operation. For noise-sensitive applications, the device has PWM spread spectrum capability providing a lower noise regulated output, as well as low noise at the input. These features, combined with high PSRR and AC load regulation performance, make this device suitable to replace a linear regulator to obtain better power conversion efficiency. The TPS8269xSIP is packaged in a compact (2.9 mm × 2.3 mm) and low profile (1 mm) BGA package suitable for automated assembly by standard surface mount equipment.

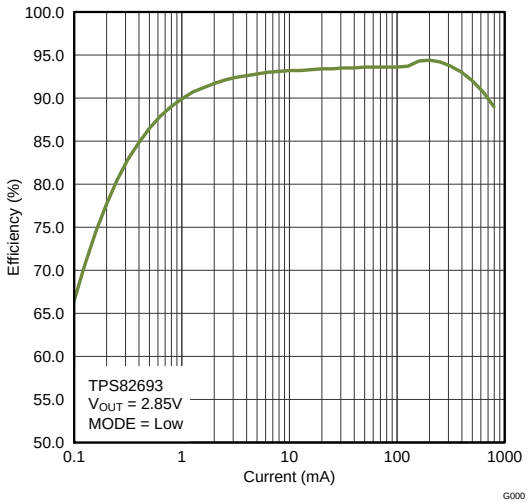
Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
TPS82692SIP	µSIP (8)	2,9mm × 2,3mm
TPS82693SIP	µSIP (8)	2,9mm × 2,3mm
TPS826951SIP	µSIP (8)	2,9mm × 2,3mm
TPS82697SIP	µSIP (8)	2,9mm × 2,3mm
TPS82698SIP	µSIP (8)	2,9mm × 2,3mm

Simplified Schematic



Efficiency vs Output Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2014) to Revision C — **Page**

- Added text to Device Comparison table for the TPS826951 device special features ... 4
- Moved T_{stg} spec from Handling Ratings to Absolute Maximum Ratings table ... 5
- Changed Handling Ratings table to ESD Ratings table ... 5

Changes from Revision A (July 2013) to Revision B — **Page**

- Global format to new data sheet standard ... 1
- Changed TPS82692, TPS826951 devices to production status. ... 4
- Changed Ordering Information table to "Device Comparison" table with cross reference to the POA at end of document. ... 4
- Moved Abs Max Ratings, Handling Ratings, Rec Oper Conditions, Thermal Info, and Elec Charactistics tables to the Specifications section ... 5
- Deleted Regulated DC Output Voltage parameters to electrical characteristics table for device TPS82692 ... 7
- Added efficiency graphs for device TPS82692 ... 11

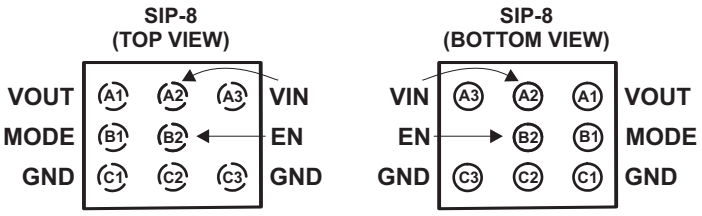
Changes from Original (March 2013) to Revision A **Page**

5 Device Comparison

PART NUMBER	OUTPUT VOLTAGE	SPECIFIC FEATURE	STATUS
TPS82692	2.2 V	800mA peak output current, spread spectrum frequency modulation	Production
TPS82693	2.85 V	800mA peak output current, spread spectrum frequency modulation, output discharge	Production
TPS826951	2.5 V	800mA peak output current, spread spectrum frequency modulation, output discharge	Production
TPS82697	2.8 V	800mA peak output current	Production
TPS82698	3 V	800mA peak output current, spread spectrum frequency modulation, output discharge	Production

6 Pin Configuration and Functions

8-Bump µSIP Package



Pin Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VOUT	A1	O	Power output terminal. Apply output load between this terminal and GND.
VIN	A2, A3	I	The VIN terminals supply current to the TPS8269xSIP's internal regulator.
EN	B2	I	This is the enable terminal of the device. Connecting this terminal to ground forces the converter into shutdown mode. Pulling this terminal to V_{IN} enables the device. This terminal must not be left floating and must be terminated.
MODE	B1	This is the mode selection terminal of the device. This terminal must not be left floating and must be terminated.	
			MODE = LOW: The device is operating in regulated frequency pulse width modulation mode (PWM) at high-load currents and in pulse frequency modulation mode (PFM) at light load currents. MODE = HIGH: Low-noise mode enabled, regulated frequency PWM operation forced.
GND	C1, C2, C3	–	Ground terminal.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Input Voltage	Voltage at VIN(2)(3), SW(3)		–0.3	6	V
	Voltage at VOUT(3)		–0.3	3.6	V
	Voltage at EN, MODE (3)		–0.3	V_{IN} + 0.3	V
Peak output current, I_O (4)		TPS82692, TPS82693, TPS826951, TPS82697, TPS62698		800(4)	mA
Power dissipation			Internally limited		
Operating temperature range, T_A (5)			–40	85	°C
Maximum internal operating temperature, $T_{INT(max)}$				125	°C
Storage temperature, T_{stg}			–55	125	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Operation above 4.8 V input voltage is not recommended over an extended period of time.
(3) All voltage values are with respect to network ground terminal.
(4) Limit to 50% Duty Cycle over Lifetime.
(5) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$. To achieve optimum performance, it is recommended to operate the device with a maximum junction temperature of 105°C.

7.2 ESD Ratings

		VALUE	UNIT
ESD	Human body model (HBM)	±2000	V
	Charged device model (CDM)	±1000	V

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range		2.3		4.8(1)	V
I_O	Output current range	TPS82692, TPS82693 TPS826951 TPS82697, TPS82698			800	mA
	Additional output capacitance (PFM/PWM)			0	4	µF
	Additional output capacitance (PWM)			0	7	µF
T_A	Ambient temperature		–40		85	°C
T_J	Operating junction temperature		–40		125	°C

(1) Operation above 4.8 V input voltage is not recommended over an extended period of time.

7.4 Thermal Information

THERMAL METRIC(1)		TPS82693/4/51/7/8/9 SIP (8-TERMINALS)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	83	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Thermal Information (continued)

THERMAL METRIC[1]		TPS82693/4/51/7/8/9 SIP (8-TERMINALS)	UNIT
θ_{JCtop}	Junction-to-case (top) thermal resistance	53	°C/W
θ_{JB}	Junction-to-board thermal resistance	-	°C/W
ψ_{JT}	Junction-to-top characterization parameter	-	°C/W
ψ_{JB}	Junction-to-board characterization parameter	-	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	-	°C/W

7.5 Electrical Characteristics

Minimum and maximum values are at V_{IN} = 2.3 V to 5.5 V, V_{OUT} = 2.85 V, EN = 1.8 V, AUTO mode and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V , V_{OUT} = 2.85 V, EN = 1.8 V, AUTO mode and T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_Q	Operating quiescent current	TPS8269x	I_O = 0mA. Device not switching		23	50	µA
		TPS8269x	I_O = 0mA, PWM mode		3.5		mA
$I_{(SD)}$	Shutdown current	TPS8269x	EN = GND		0.2	7	µA
UVLO	Undervoltage lockout threshold	TPS8269x			2.05	2.1	V
Protection							
	Thermal Shutdown	TPS8269x			140		°C
	Thermal Shutdown hysteresis	TPS8269x			10		°C
I_{LIM}	Peak Output Current Limit	TPS8269x			1000		mA
I_{SC}	Short Circuit Output Current Limit	TPS8269x			15		mA
ENABLE, MODE							
V_{IH}	High-level input voltage	TPS8269x		1			V
V_{IL}	Low-level input voltage					0.4	V
I_{lkg}	Input leakage current		Input connected to GND or VIN		0.01	1.5	µA
OSCILLATOR							
f_{SW}	Oscillator frequency	TPS8269x	I_O = 0mA, PWM mode. T_A = 25°C	2.7	3	3.3	MHz

Electrical Characteristics (continued)

Minimum and maximum values are at V_{IN} = 2.3 V to 5.5 V, V_{OUT} = 2.85 V, EN = 1.8 V, AUTO mode and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V , V_{OUT} = 2.85 V, EN = 1.8 V, AUTO mode and T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT							
V_{OUT}	Regulated DC output voltage	TPS82693 TPS82697	3.15V ≤ V_{IN} ≤ 4.8V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			3.25V ≤ V_{IN} ≤ 4.8V, 500mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			3.15V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			3.25V ≤ V_{IN} ≤ 5.5V, 500mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			3.15V ≤ V_{IN} ≤ 4.8V, 0mA ≤ I_O ≤ 500 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
			3.25V ≤ V_{IN} ≤ 4.8V, 500mA ≤ I_O ≤ 800 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
		TPS826951	2.9V ≤ V_{IN} ≤ 4.8V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			3.15V ≤ V_{IN} ≤ 4.8V, 500mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			2.9V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			3.15V ≤ V_{IN} ≤ 5.5V, 500mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			2.9V ≤ V_{IN} ≤ 4.8V, 0mA ≤ I_O ≤ 500 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
			3.15V ≤ V_{IN} ≤ 4.8V, 500mA ≤ I_O ≤ 800 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
		TPS82698	3.3V ≤ V_{IN} ≤ 4.8V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			3.45V ≤ V_{IN} ≤ 4.8V, 500mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			3.3V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			3.45V ≤ V_{IN} ≤ 5.5V, 500mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			3.3V ≤ V_{IN} ≤ 4.8V, 0mA ≤ I_O ≤ 500 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
			3.45V ≤ V_{IN} ≤ 4.8V, 500mA ≤ I_O ≤ 800 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
		TPS82692	2.5V ≤ V_{IN} ≤ 4.8V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			2.7V ≤ V_{IN} ≤ 4.8V, 500mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			2.5V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			2.7V ≤ V_{IN} ≤ 5.5V, 500mA ≤ I_O ≤ 800 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			2.5V ≤ V_{IN} ≤ 4.8V, 0mA ≤ I_O ≤ 500 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
			2.7V ≤ V_{IN} ≤ 4.8V, 500mA ≤ I_O ≤ 800 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
	Line regulation		V_{IN} = V_O + 0.5V (min 3.15V) to 5.5V I_O = 200 mA		0.18		%/V
	Load regulation		I_O = 0mA to 800 mA		–0.0002		%/mA
	Feedback input resistance	TPS8269x			480		kΩ

Electrical Characteristics (continued)

Minimum and maximum values are at V_{IN} = 2.3 V to 5.5 V, V_{OUT} = 2.85 V, EN = 1.8 V, AUTO mode and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V , V_{OUT} = 2.85 V, EN = 1.8 V, AUTO mode and T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_O	Power-save mode ripple voltage	TPS82693 TPS826951 TPS82697	I_O = 1mA C_O = 4.7µF X5R 6.3V 0402		30		mV_{PP}
		TPS82698	I_O = 1mA C_O = 4.7µF X5R 6.3V 0402		65		mV_{PP}
			I_O = 1mA C_O = 10µF X5R 6.3V 0603		25		mV_{PP}
		TPS82692	I_O = 1mA C_O = 10µF X5R 6.3V 0603		22		mV_{PP}
r_{DIS}	Discharge resistor for power-down sequence				120		Ω
	Start-up time	TPS82693 TPS826951 TPS82698 TPS82697	I_O = 0mA, Time from active EN to V_O		200		µs
		TPS82692	I_O = 0mA, Time from active EN to V_O		160		µs

7.6 Typical Characteristics

Table 1. Table Of Graphs

			FIGURE
η	Efficiency	vs Load current (TPS82699 V_{OUT} = 3.2V)	Figure 1, Figure 2, Figure 3
		vs Load current (TPS82693 V_{OUT} = 2.85V)	Figure 4, Figure 5, Figure 6
		vs Load current (TPS82697 V_{OUT} = 2.8V)	Figure 7, Figure 8
		vs Load current (TPS826951 V_{OUT} = 2.5V)	Figure 9, Figure 10
		vs Load current (TPS82698 V_{OUT} = 3.0V)	Figure 11, Figure 12
		vs Input Voltage (TPS82699 V_{OUT} = 3.2V)	Figure 15
		vs Input Voltage (TPS82692 V_{OUT} = 2.2V)	Figure 41, Figure 42
	Peak-to-peak output ripple voltage	vs Load current (TPS82699 V_{OUT} = 3.2V)	Figure 16, Figure 17
V_O	DC output voltage	vs Load Current (TPS82699 V_{OUT} = 3.2V)	Figure 18
		vs Load Current (TPS82693 V_{OUT} = 2.85V)	Figure 19, Figure 20
	Load transient response	TPS82699 V_{OUT} = 3.2V	Figure 28, Figure 29, Figure 30
		TPS826951 V_{OUT} = 2.5V	Figure 31, Figure 32
	AC load transient response	TPS82699 V_{OUT} = 3.2V	Figure 33, Figure 34, Figure 35, Figure 36
		TPS826951 V_{OUT} = 2.5V	Figure 37, Figure 38, Figure 39, Figure 40
		TPS82698 V_{OUT} = 3.0V	Figure 41, Figure 42, Figure 43
	PFM/PWM boundaries	vs Input voltage (TPS82699 V_{OUT} = 3.2V)	Figure 21
I_Q	Quiescent current	vs Input voltage	Figure 22
f_s	PWM switching frequency	vs Input voltage (TPS82699 V_{OUT} = 3.2V)	Figure 23
	Start-up	(TPS82699 V_{OUT} = 3.2V)	Figure 24, Figure 25
	Shut-Down		Figure 26

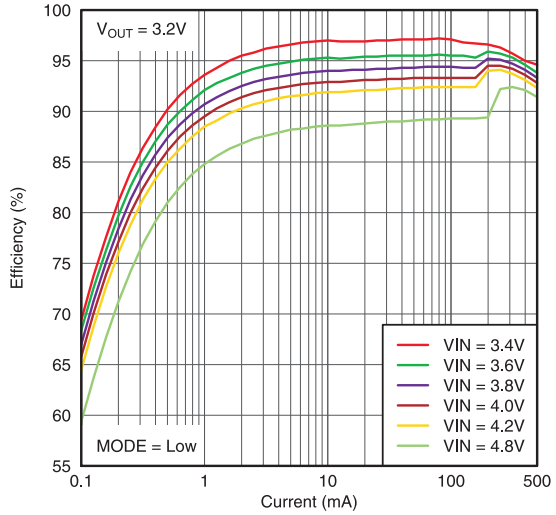


Figure 1. TPS82699 Efficiency vs Load Current

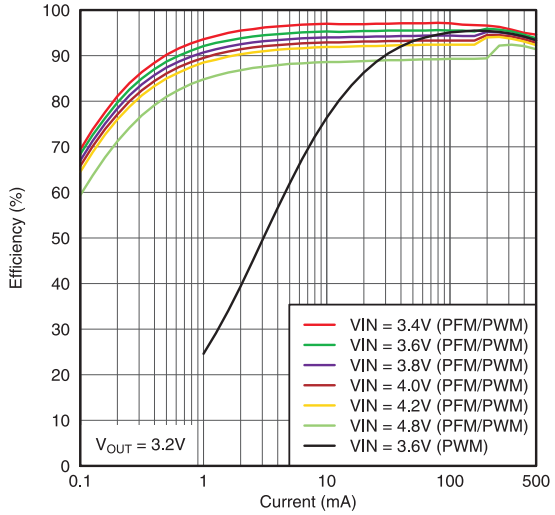


Figure 2. TPS82699 Efficiency vs Load Current

Typical Characteristics (continued)

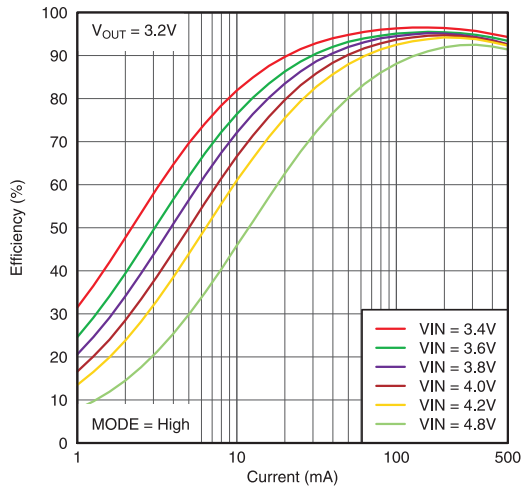


Figure 3. TPS82699 Efficiency vs Load Current

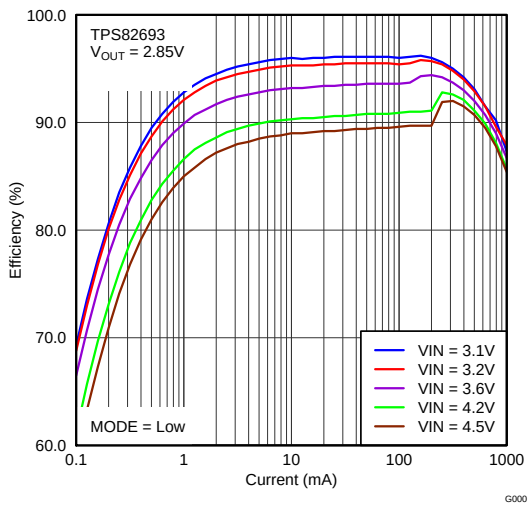


Figure 4. TPS82693 Efficiency vs Load Current

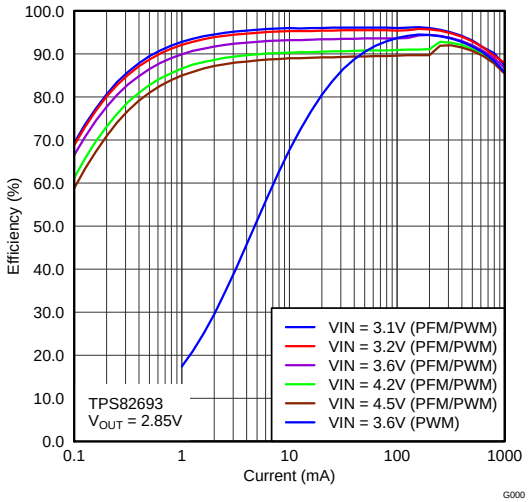


Figure 5. TPS82693 Efficiency vs Load Current

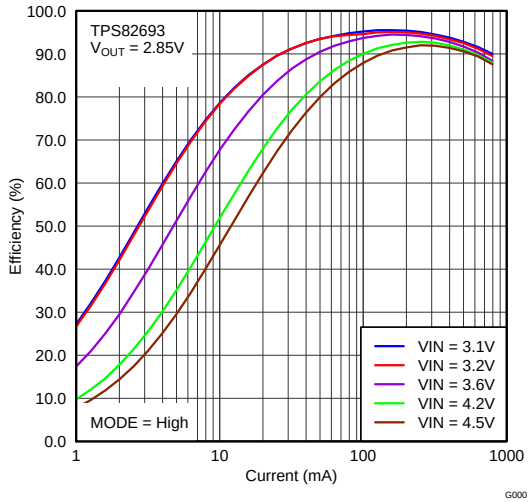


Figure 6. TPS82693 Efficiency vs Load Current

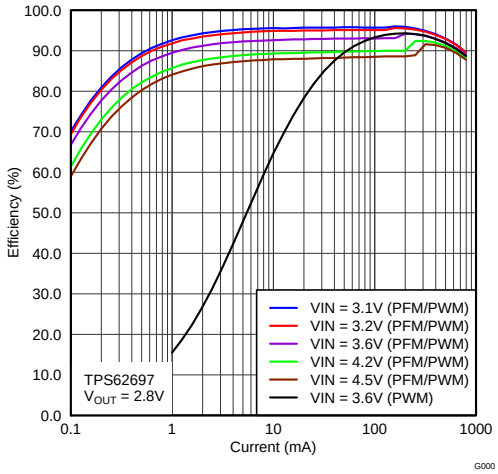


Figure 7. Efficiency vs Load Current Forced PWM Operation For Device TPS82697

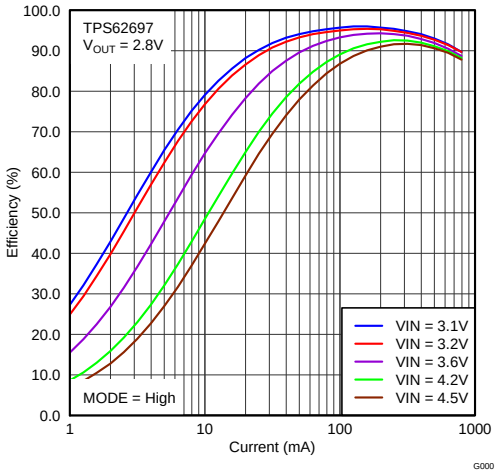


Figure 8. Efficiency vs Load Current Forced PWM Operation For Device TPS82697

Typical Characteristics (continued)

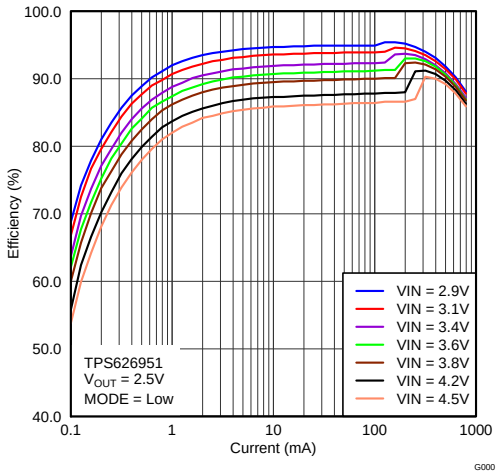


Figure 9. Efficiency vs Load Current PFM/PWM Operation For Device TPS826951

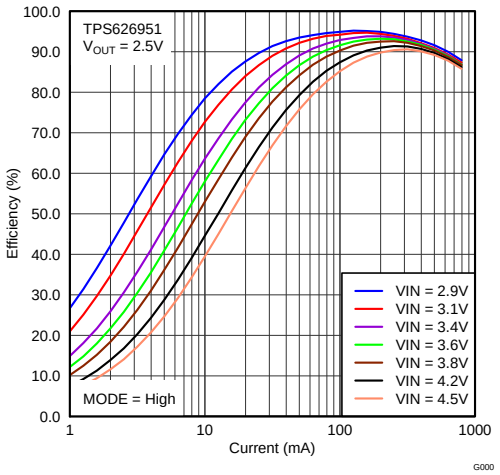


Figure 10. Efficiency vs Load Current Forced PWM Operation For Device TPS826951

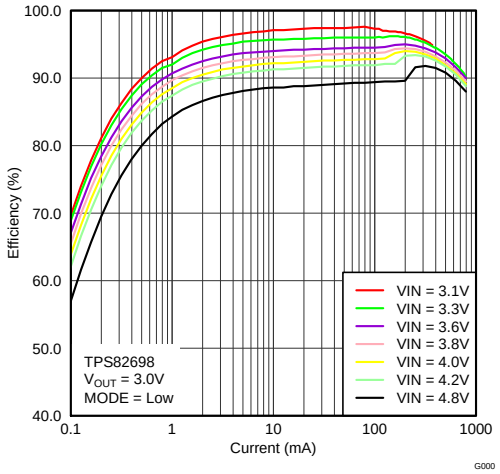


Figure 11. Efficiency vs Load Current PFM/PWM Operation For Device TPS82698

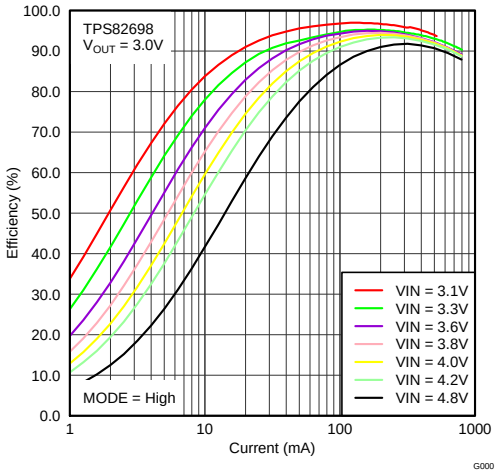


Figure 12. Efficiency vs Load Current Forced PWM Operation For Device TPS82698

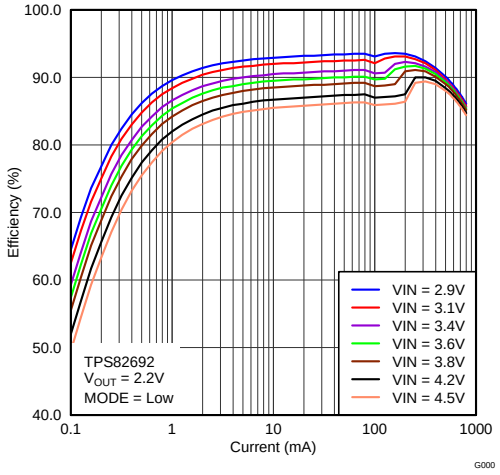


Figure 13. Efficiency vs Load Current PFM/PWM Operation For Device TPS82692

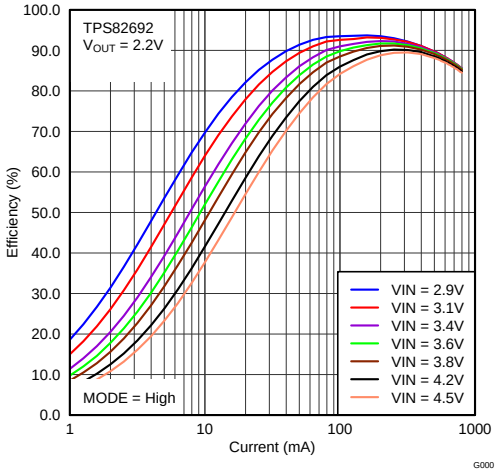


Figure 14. Efficiency vs Load Current PWM Operation For Device TPS82692

Typical Characteristics (continued)

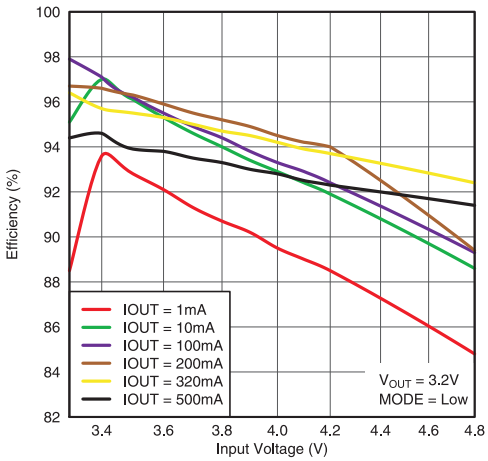


Figure 15. TPS82699 Efficiency vs Input Voltage

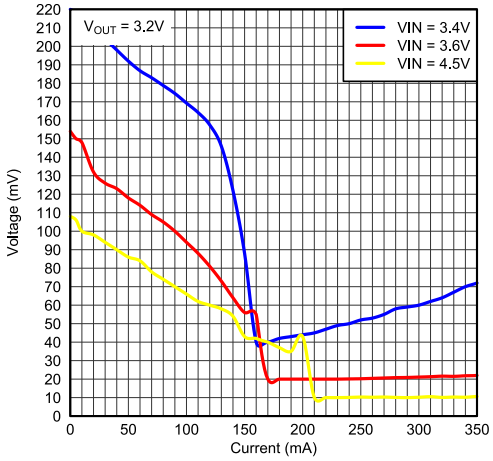


Figure 16. TPS82699 Peak-To-Peak Output Ripple Voltage vs Load Current

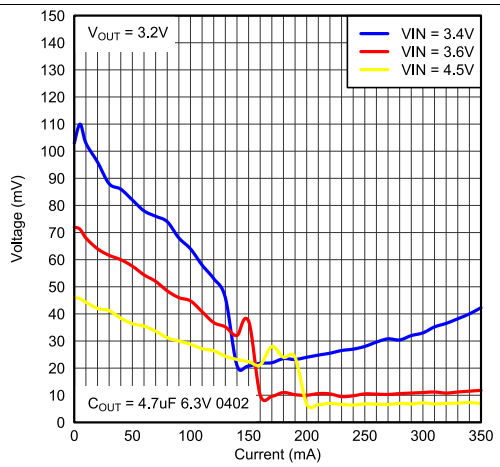


Figure 17. TPS82699 Peak-To-Peak Output Ripple Voltage vs Load Current

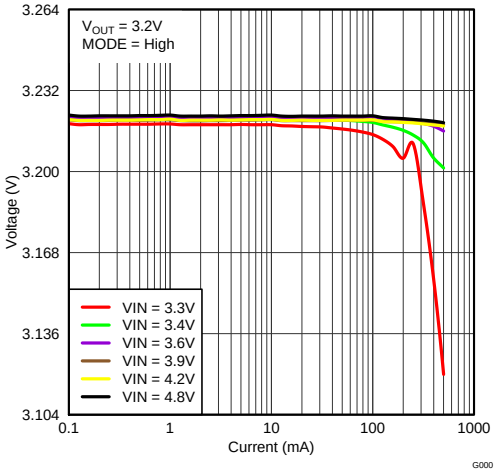


Figure 18. TPS82699 DC Output Voltage vs Load Current

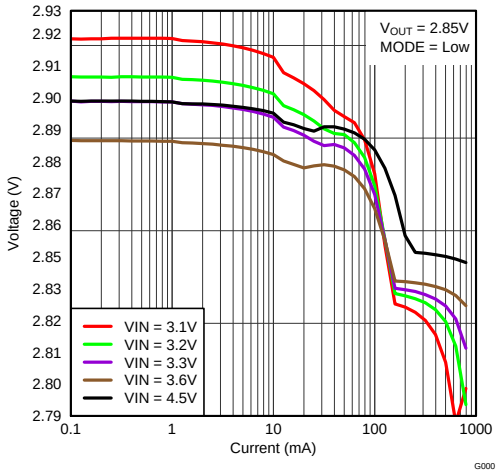


Figure 19. TPS82693 DC Output Voltage vs Load Current

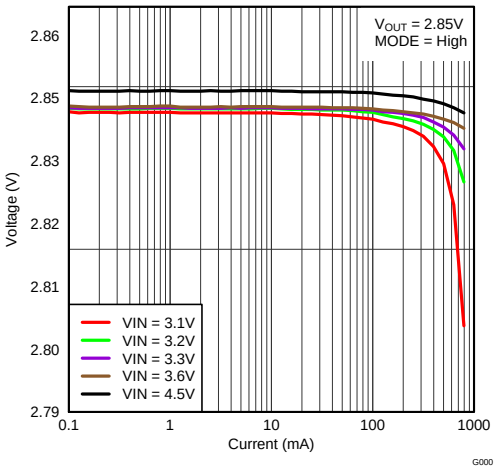


Figure 20. TPS82693dc Output Voltage vs Load Current

Typical Characteristics (continued)

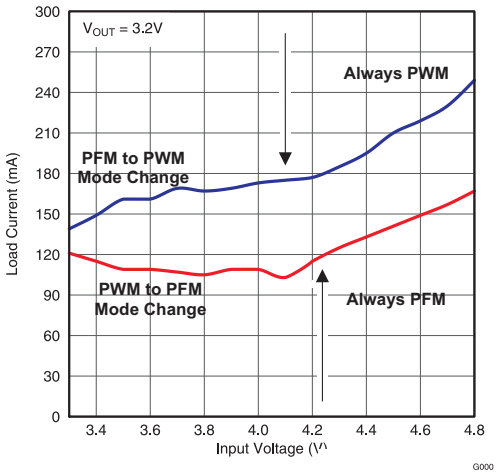


Figure 21. TPS82699 PFM/PWM Boundaries

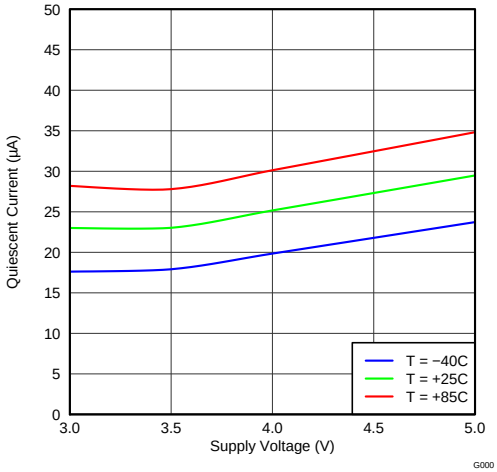


Figure 22. Quiescent Current vs Input Voltage

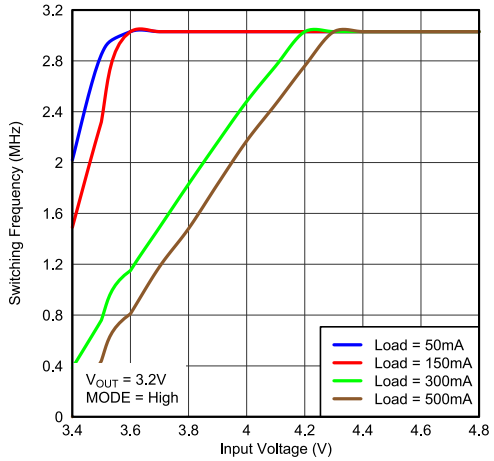


Figure 23. TPS82699 PWM Switching Frequency vs Input Voltage

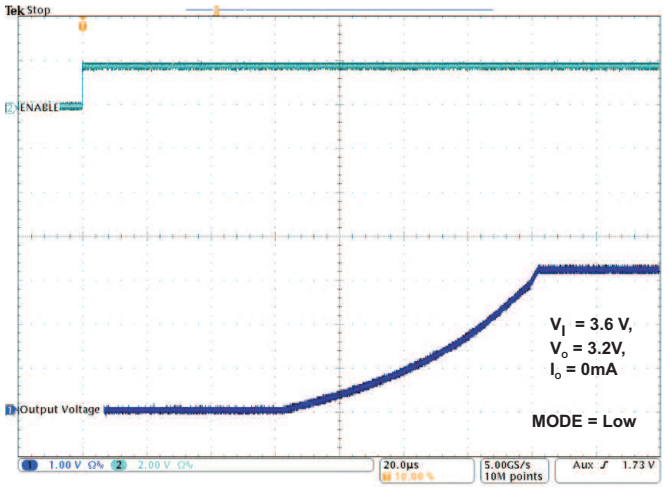


Figure 24. TPS82699 Start-Up

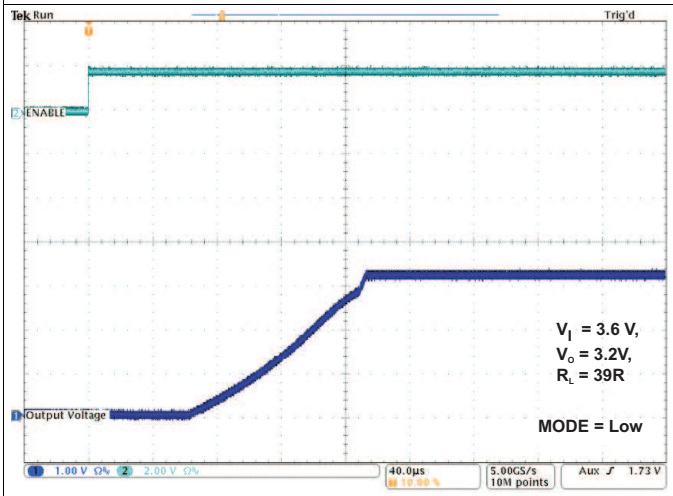


Figure 25. TPS82699 Start-Up

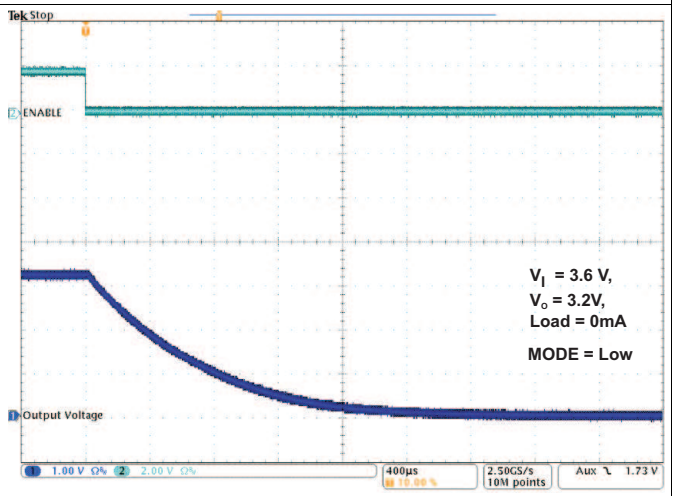


Figure 26. TPS82699 Shutdown

8 Parameter Measurement Information

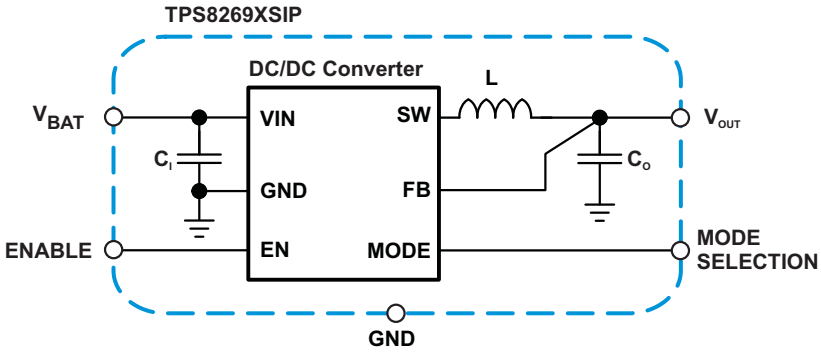


Figure 27. Circuit

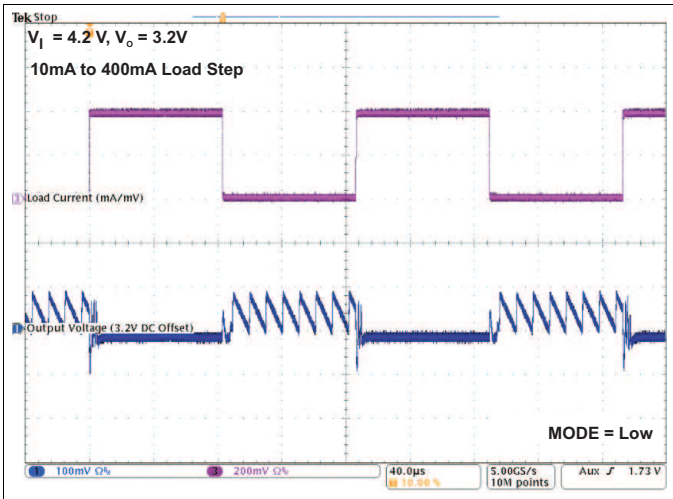


Figure 28. TPS8269 Load Transient Response In PFM/PWM Operation

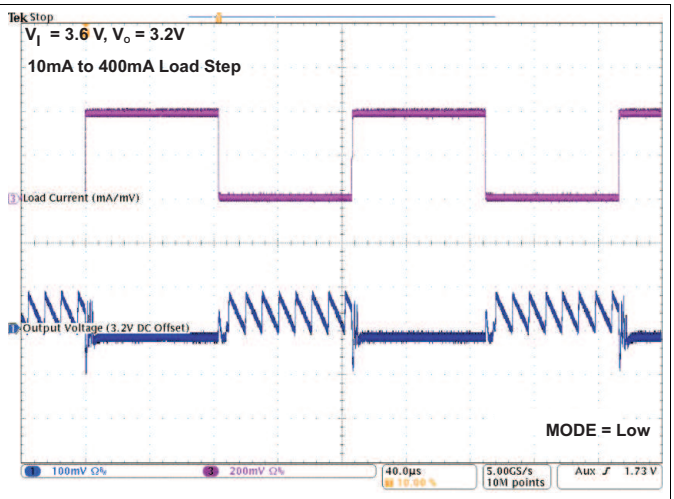


Figure 29. TPS82699 Load Transient Response In PFM/PWM Operation

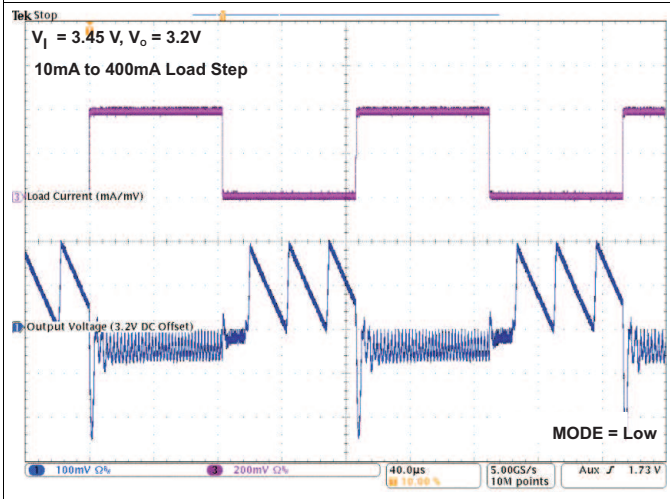


Figure 30. TPS82699 Load Transient Response In PFM/PWM Operation

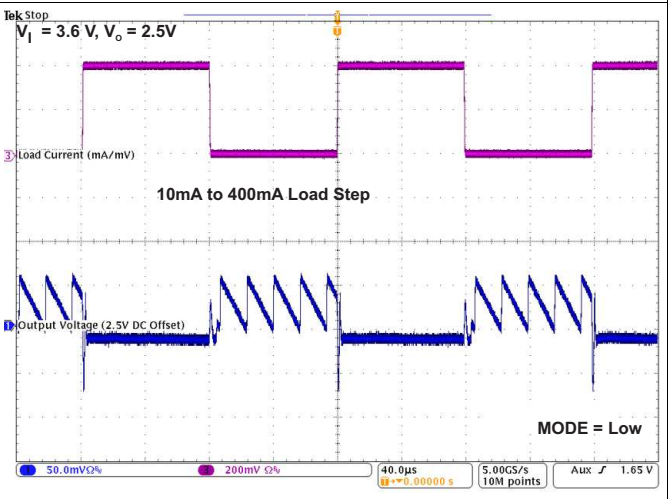


Figure 31. TPS826951 Load Transient Response In PFM/PWM Operation

Parameter Measurement Information (continued)

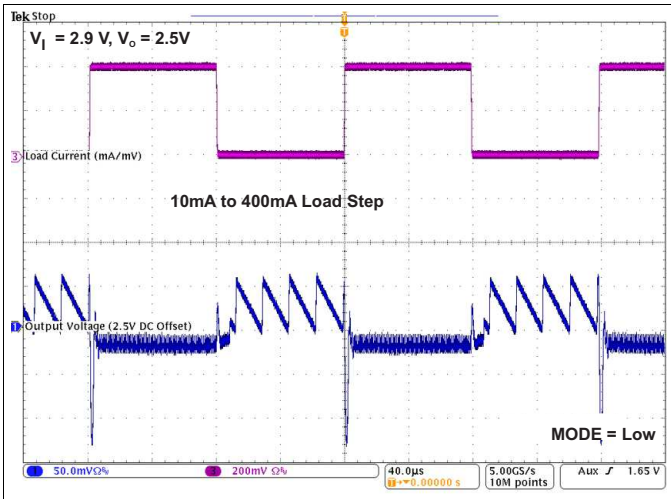


Figure 32. TPS826951 Load Transient Response In PFM/PWM Operation

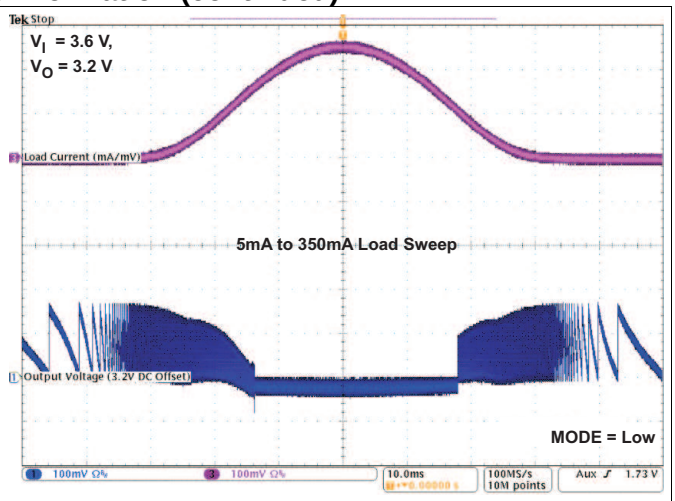


Figure 33. TPS82699 AC Load Transient Response

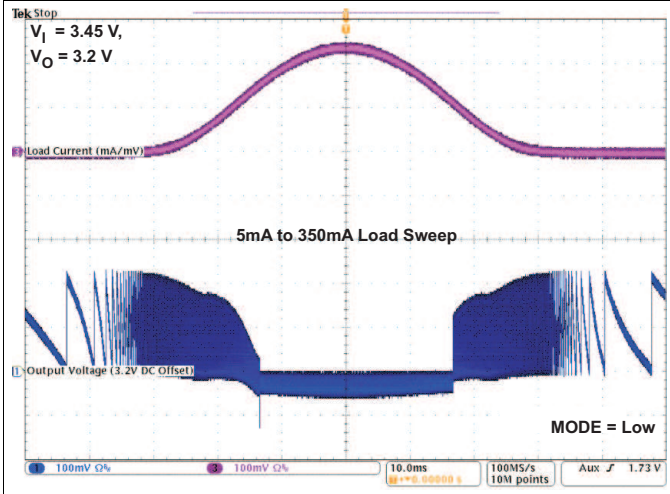


Figure 34. TPS82699 AC Load Transient Response

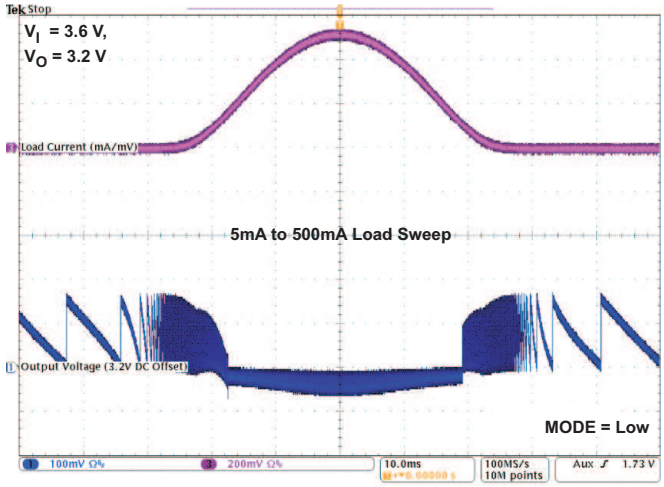


Figure 35. TPS82699 AC Load Transient Response

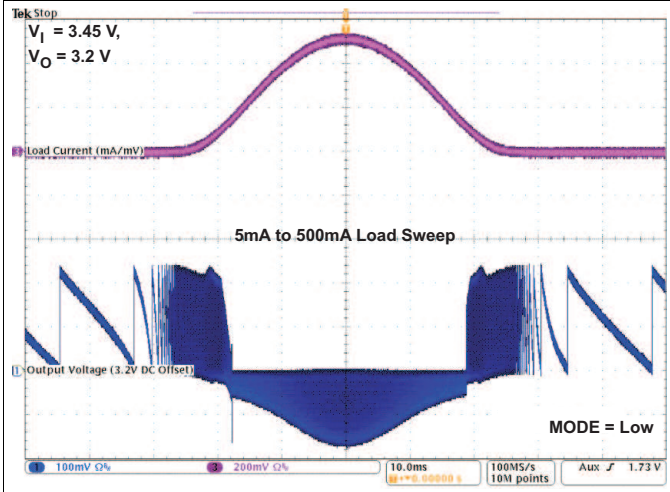


Figure 36. TPS82699 AC Load Transient Response

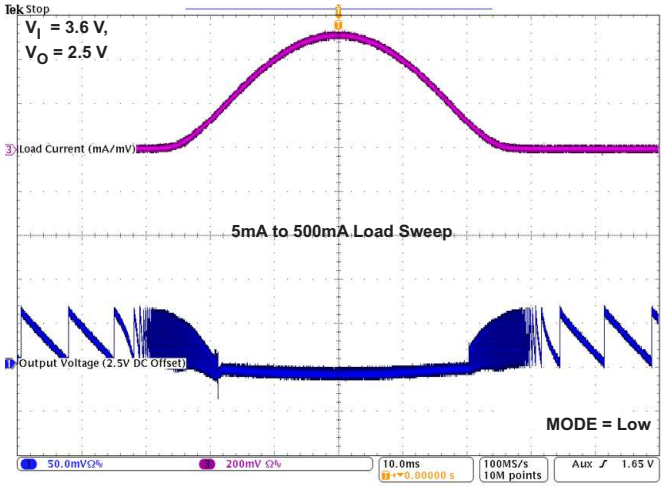


Figure 37. TPS826951 AC Load Transient Response

Parameter Measurement Information (continued)

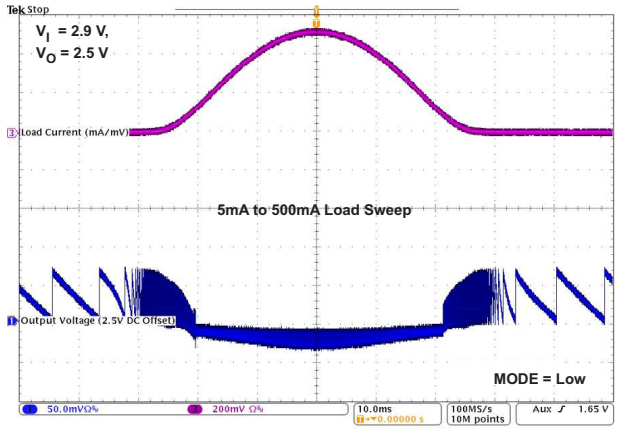


Figure 38. TPS826951 AC Load Transient Response

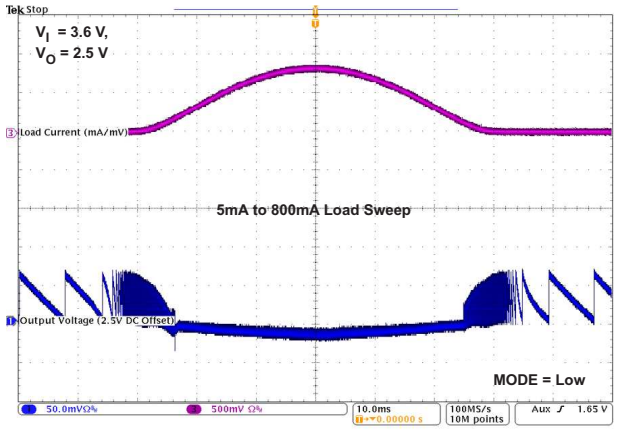


Figure 39. TPS826951 AC Load Transient Response

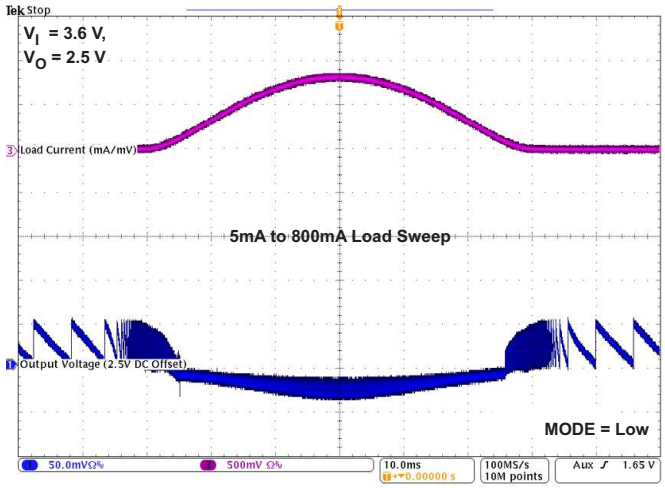


Figure 40. TPS826951 AC Load Transient Response

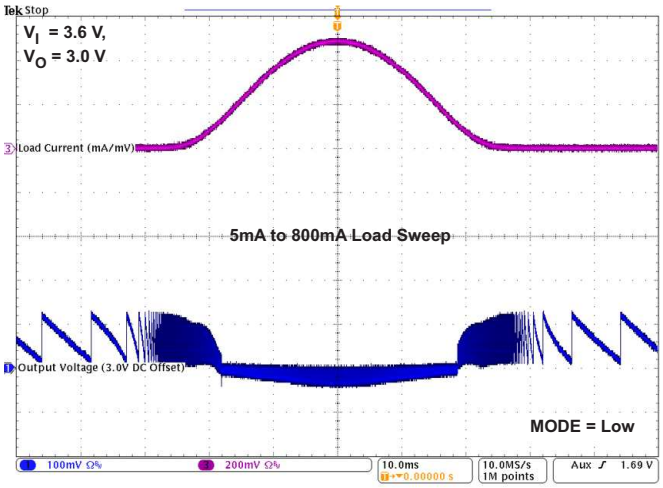


Figure 41. TPS82698 AC Load Transient Response

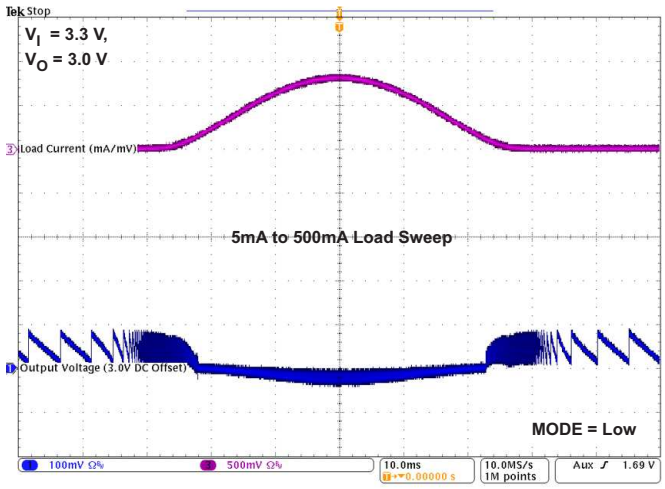


Figure 42. TPS82698 AC Load Transient Response

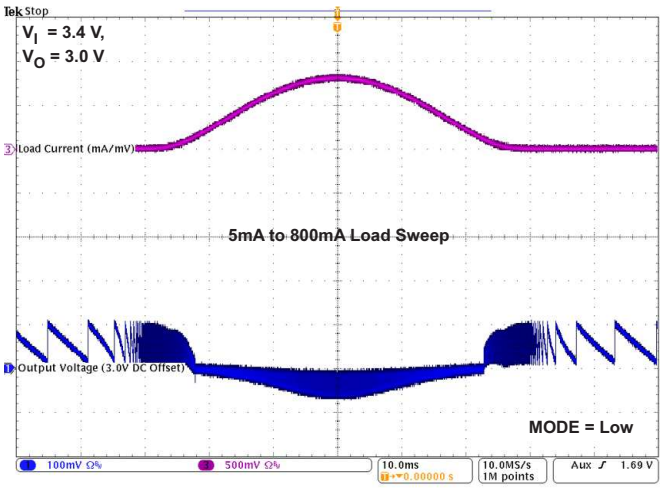


Figure 43. TPS82698 AC Load Transient Response

9 Detailed Description

9.1 Overview

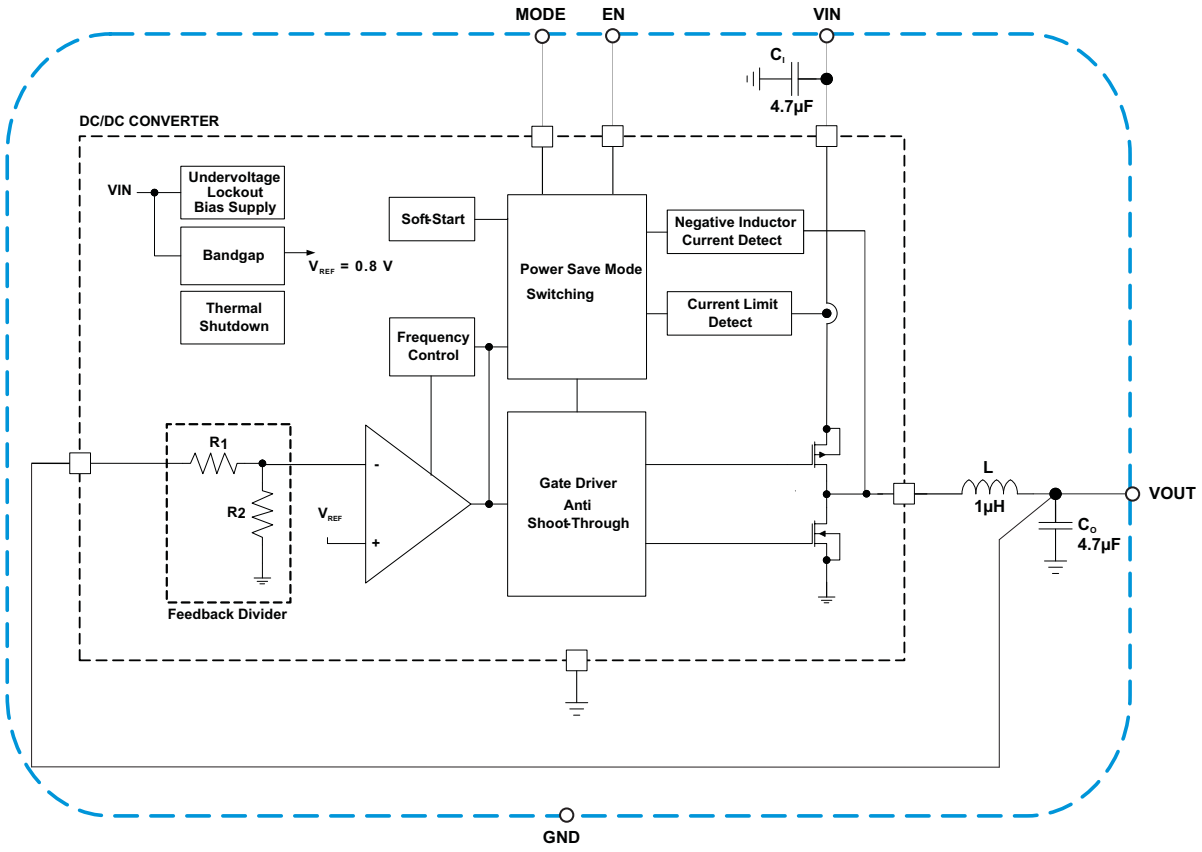
The TPS8269xSIP is a standalone synchronous step-down converter operating at a regulated 3-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents (up to 500 mA / 800mA output current). At light load currents, the TPS8269xSIP's converter operates in power-save mode with pulse frequency modulation (PFM).

The converter uses a unique frequency locked ring oscillating modulator to achieve *best-in-class* load and line response. One key advantage of the non-linear architecture is that there is no traditional feedback loop. The loop response to change in V_O is essentially instantaneous, which explains the transient response. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency lock loop (FLL) holds the switching frequency constant over a large range of operating conditions.

Combined with *best in class* load and line transient response characteristics, the low quiescent current of the device (ca. 23µA) allows to maintain high efficiency at light load, while preserving fast transient response for applications requiring tight output regulation.

The TPS8269xSIP integrates an input current limit to protect the device against heavy load or short circuits and features an undervoltage lockout circuit to prevent the device from misoperation at low input voltages.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power-Save Mode

If the load current decreases, the converter will enter power save mode operation automatically. During power-save mode the converter operates in discontinuous current (DCM) with a minimum of one pulse, which produces low output ripple compared with other PFM architectures.

Feature Description (continued)

When in power-save mode, the converter resumes its operation when the output voltage trips below the nominal voltage. It ramps up the output voltage with a minimum of one pulse and goes into power-save mode when the output voltage is within its regulation limits again.

PFM mode is left and PWM operation is entered as the output current can no longer be supported in PFM mode. As a consequence, the DC output voltage is typically positioned ca. 1.5% above the nominal output voltage and the transition between PFM and PWM is seamless.

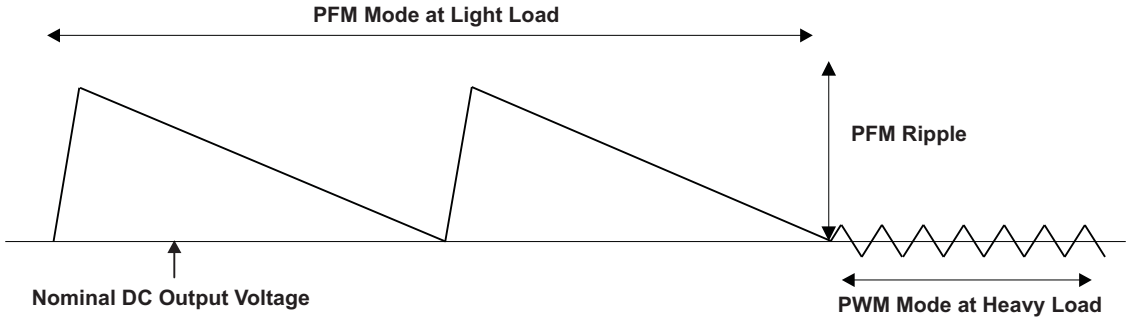


Figure 44. Operation In PFM Mode And Transfer To PWM Mode

9.3.2 Mode Selection

The MODE terminal allows to select the operating mode of the device. Connecting this terminal to GND enables the automatic PWM and power-save mode operation. The converter operates in regulated frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

Pulling the MODE terminal high forces the converter to operate in the PWM mode even at light load currents. The advantage is that the converter operates with a fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads.

For additional flexibility, it is possible to switch from power-save mode to PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

9.3.3 Soft Start

The TPS8269xSIP has an internal soft-start circuit that limits the inrush current during start-up. This limits input voltage drops when a battery or a high-impedance power source is connected to the input of the MicroSIP™ converter.

The soft-start system progressively increases the switching on-time from a minimum pulse-width of 35ns as a function of the output voltage. This mode of operation continues for approximately 100µs after enable. Should the output voltage not have reached its target value by that time, such as in the case of heavy load, the soft-start transitions to a second mode of operation.

If the output voltage has raised above 0.5V (approximately), the converter increases the input current limit thereby enabling the power supply to come-up properly. The start-up time mainly depends on the capacitance present at the output node and load current.

9.4 Device Functional Modes

9.4.1 Low Dropout, 100% Duty Cycle Operation

The device starts to enter 100% duty cycle mode once input and output voltage come close together. In order to maintain the output voltage, the DC/DC converter's high-side MOSFET is turned on 100% for one or more cycles.

Device Functional Modes (continued)

With further decreasing V_{IN} the high-side switch is constantly turned on, thereby providing a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

9.4.2 Enable

The TPS8269xSIP device starts operation when EN is set high and starts up with the soft start as previously described. For proper operation, the EN terminal must be terminated and must not be left floating.

Pulling the EN terminal low forces the device into shutdown. In this mode, all internal circuits are turned off and V_{IN} current reduces to the device leakage current, typically a few hundred nano amps.

The TPS8269xSIP device can actively discharge the output capacitor when it turns off (See *Device Comparison* table). The integrated discharge resistor has a typical resistance of 100 Ω. The required time to ramp-down the output voltage depends on the load current and the capacitance present at the output node.

10 Application and Implementation

10.1 Application Information

The TPS8269X devices are complete power supplies, optimized for and working within the given specification range without additional components or design steps. Further improvements can be achieved as described below.

10.2 Typical Application

10.2.1 Input Capacitor Selection

Because of the pulsating input current nature of the buck converter, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interference in other circuits in the system.

For most applications, the input capacitor that is integrated into the TPS8269x should be sufficient. If the application exhibits a noisy or erratic switching frequency, experiment with additional input ceramic capacitance to find a remedy.

The TPS8269x uses a tiny ceramic input capacitor. When a ceramic capacitor is combined with trace or cable inductance, such as from a wall adapter, a load step at the output can induce ringing at the VIN terminal. This ringing can couple to the output and be mistaken as loop instability or can even damage the part. In this circumstance, additional "bulk" capacitance, such as electrolytic or tantalum, should be placed between the input of the converter and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_I.

10.2.2 Output Capacitor Selection

The advanced, fast-response, voltage mode, control scheme of the TPS8269x allows the use of a tiny ceramic output capacitor (C_O). For most applications, the output capacitor integrated in the TPS8269x is sufficient.

At nominal load current, the device operates in PWM mode; the overall output voltage ripple is the sum of the voltage step that is caused by the output capacitor ESL and the ripple current that flows through the output capacitor impedance. At light loads, the output capacitor limits the output ripple voltage and provides holdup during large load transitions.

The TPS8269x is designed as a Point-Of-Load (POL) regulator, to operate stand-alone without requiring any additional capacitance. Adding a 4.7µF ceramic output capacitor (X7R or X5R dielectric) generally works from a converter stability point of view, helps to minimize the output ripple voltage in PFM mode and improves the converter's transient response under when input and output voltage are close together.

For best operation (i.e. optimum efficiency over the entire load current range, proper PFM/PWM auto transition), the TPS8269xSIP requires a minimum output ripple voltage in PFM mode. The typical output voltage ripple is ca. 1% of the nominal output voltage V_O. The PFM pulses are time controlled resulting in a PFM output voltage ripple and PFM frequency that depends (first order) on the capacitance seen at the MicroSiP™ DC/DC converter's output.

In applications requiring additional output bypass capacitors located close to the load, care should be taken to ensure proper operation. If the converter exhibits marginal stability or erratic switching frequency, experiment with additional low value series resistance (e.g. 50 to 100mΩ) in the output path to find a remedy.

Because the damping factor in the output path is directly related to several resistive parameters (e.g. inductor DCR, power-stage $r_{DS(on)}$, PWB DC resistance, load switches $r_{DS(on)}$ …) that are temperature dependant, the converter small and large signal behavior must be checked over the input voltage range, load current range and temperature range.

The easiest sanity test is to evaluate, directly at the converter’s output, the following aspects:

- PFM/PWM efficiency
- PFM/PWM and forced PWM load transient response

During the recovery time from a load transient, the output voltage can be monitored for settling time, overshoot or ringing that helps judge the converter’s stability. Without any ringing, the loop has usually more than 45° of phase margin.

11 Power Supply Recommendations

The TPS8269X MicroSIP™ devices are fully featured point of load power supplies. Use information given in *Application Information* to connect input and output circuitry appropriately. Even if electrical characteristics are based on measurements up to V_{IN}=5.5V, it is not recommended to operate at higher voltages than 4.8V permanently.

12 Layout

12.1 Layout Guidelines

In making the pad size for the SiP LGA balls, it is recommended that the layout use non-solder-mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 45 shows the appropriate diameters for a MicroSiP™ layout.

12.2 Layout Example

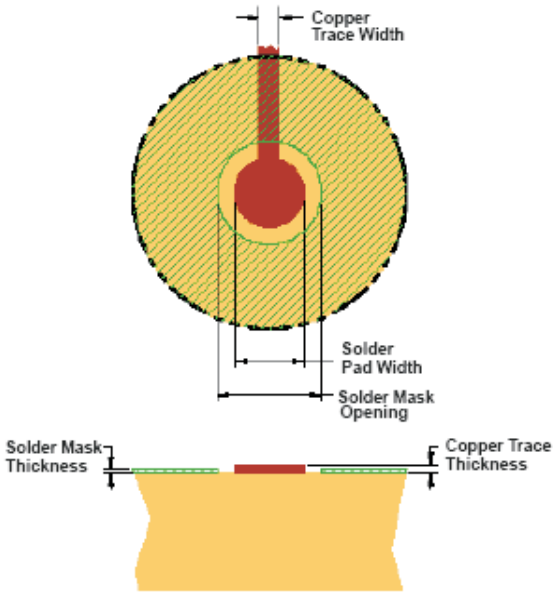


Figure 45. Recommended Land Pattern Image And Dimensions

SOLDER PAD DEFINITIONS (1)(2)(3)(4)	COPPER PAD	SOLDER MASK (5) OPENING	COPPER THICKNESS	STENCIL (6) OPENING	STENCIL THICKNESS
Non-solder-mask defined (NSMD)	0.30mm	0.360mm	1oz max (0.032mm)	0.34mm diameter	0.1mm thick

(1) Circuit traces from non-solder-mask defined PWB lands should be 75μm to 100μm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and affect reliability.
(2) Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
(3) Recommend solder paste is Type 3 or Type 4.
(4) For a PWB using a Ni/Au surface finish, the gold thickness should be less than 0.5mm to avoid a reduction in thermal fatigue performance.
(5) Solder mask thickness should be less than 20 μm on top of the copper circuit pattern.
(6) For best solder stencil performance use laser cut stencils with electro polishing. Chemically etched stencils give inferior solder paste volume control.

12.3 Surface Mount Information

The TPS8269x MicroSIP DC/DC converter uses an open frame construction that is designed for a fully automated assembly process and that features a large surface area for pick and place operations. See the "Pick Area" in the package drawings.

Package height and weight have been kept to a minimum thereby allowing the MicroSIP device to be handled similarly to a 0805 component.

See JEDEC/IPC standard J-STD-20b for reflow recommendations.

12.4 Thermal And Reliability Information

The TPS8269x output current may need to be de-rated if it is required to operate in a high ambient temperature or deliver a large amount of continuous power. The amount of current de-rating is dependent upon the input voltage, output power and environmental thermal conditions. Care should especially be taken in applications where the localized PWB temperature exceeds 65°C.

The TPS8269x die and inductor temperature should be kept lower than the maximum rating of 125°C, so care should be taken in the circuit layout to ensure good heat sinking. Sufficient cooling should be provided to ensure reliable operation.

Three basic approaches for enhancing thermal performance are listed below:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate the junction temperature, approximate the power dissipation within the TPS8269x by applying the typical efficiency stated in this datasheet to the desired output power; or, by taking a power measurement if you have an actual TPS8269x device or a TPS8269x evaluation module. Then calculate the internal temperature rise of the TPS8269x above the surface of the printed circuit board by multiplying the TPS8269x power dissipation by the thermal resistance.

The thermal resistance numbers listed in the Thermal Information table are based on modeling the MicroSIP™ package mounted on a high-K test board specified per JEDEC standard. For increased accuracy and fidelity to the actual application, it is recommended to run a thermal image analysis of the actual system. Figure 46 and Figure 47 are thermal images of TI's evaluation board with readings of the temperatures at specific locations on the device.

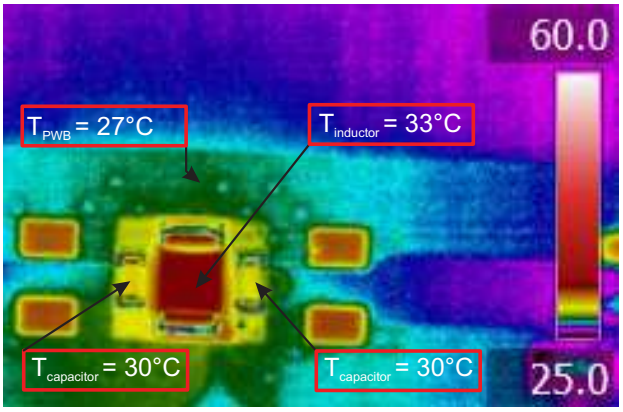


Figure 46. V=3.6v, V=2.85v, I=400ma 80mw Power Dissipation At Room Temp.-INOUTOUT

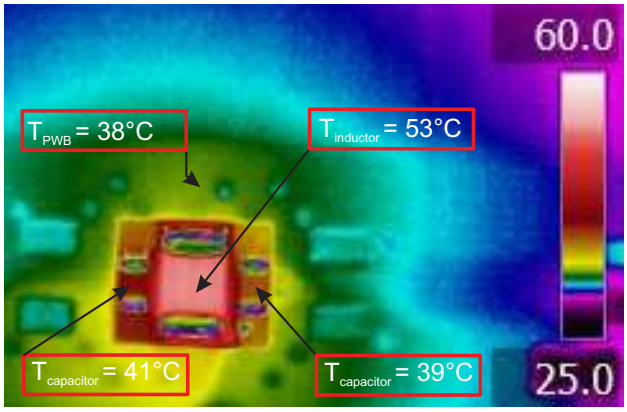


Figure 47. V=3.6v, V=2.85v, I=800ma 330mw Power Dissipation At Room Temp.-INOUTOUT

The TPS8269x is equipped with a thermal shutdown that will inhibit power switching at high junction temperatures. The activation threshold of this function, however, is above 125°C to avoid interfering with normal operation. Thus, it follows that prolonged or repetitive operation under a condition in which the thermal shutdown activates necessarily means that the components internal to the MicroSIP package are subjected to high temperatures for prolonged or repetitive intervals, which may damage or impair the reliability of the device.

MLCC capacitor reliability/lifetime is depending on temperature and applied voltage conditions. At higher temperatures, MLCC capacitors are subject to stronger stress. On the basis of frequently evaluated failure rates determined at standardized test conditions, the reliability of all MLCC capacitors can be calculated for their actual operating temperature and voltage.

Thermal And Reliability Information (continued)

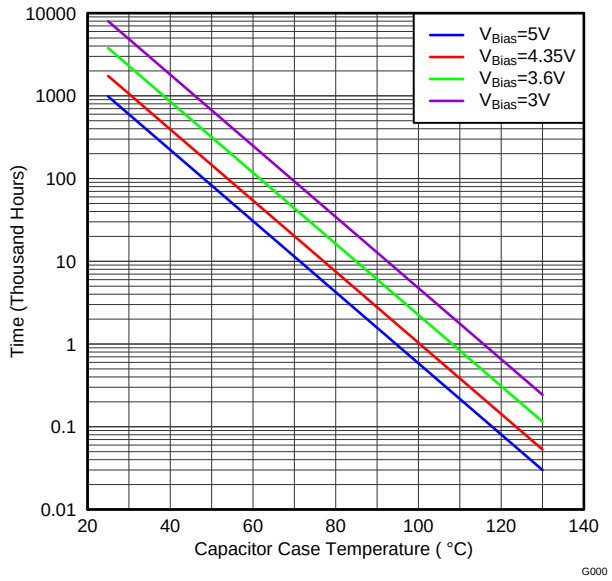


Figure 48. Capacitor Lifetime vs Capacitor Case Temperature

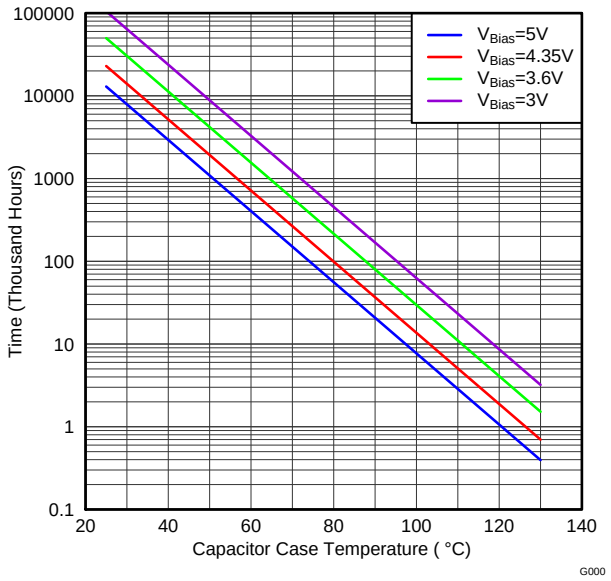
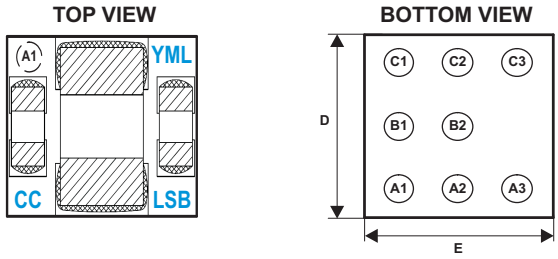


Figure 49. Capacitor B1 Lifetime vs Capacitor Case Temperature

Failures caused by systematic degradation can be described by the Arrhenius model. The most critical parameter (IR) is the Insulation Resistance (i.e. leakage current). The drop of IR below a lower limit (e.g., 1 MΩ) is used as the failure criterion, see Figure 48. Figure 49 (B1 life) defines the capacitor lifetime based on a failure rate reaching 1%. Note that the wear-out mechanisms occurring in the MLCC capacitors are not reversible but cumulative over time.

12.5 Package Summary

SIP Package



Code:

- CC — Customer Code (device/voltage specific)
- YML — Y: Year, M: Month, L: Lot trace code
- LSB — L: Lot trace code, S: Site code, B: Board locator

12.6 MicroSIP™

DC/DC Module Package Dimensioning

The TPS8269x device is available in an 8-bump ball grid array (BGA) package. The package dimensions are:

- D = 2,30 ±0,05 mm
- E = 2,90 ±0,05 mm

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

See ONET-10G-EVM

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS82692	Click here	Click here	Click here	Click here	Click here
TPS82693	Click here	Click here	Click here	Click here	Click here
TPS826951	Click here	Click here	Click here	Click here	Click here
TPS82697	Click here	Click here	Click here	Click here	Click here
TPS82698	Click here	Click here	Click here	Click here	Click here

13.3 Trademarks

MicroSIP is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

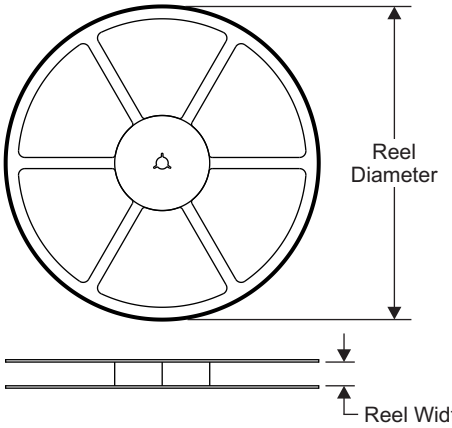
This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

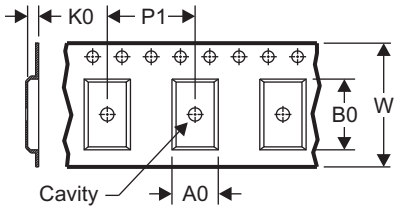
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

14.1 Tape and Reel Information

REEL DIMENSIONS

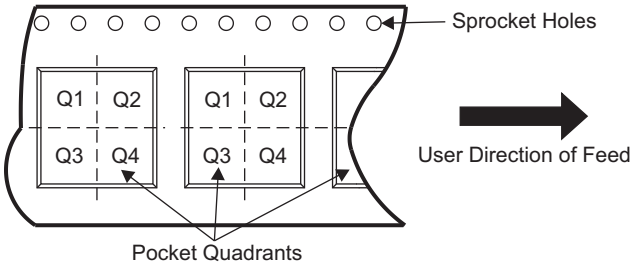


TAPE DIMENSIONS



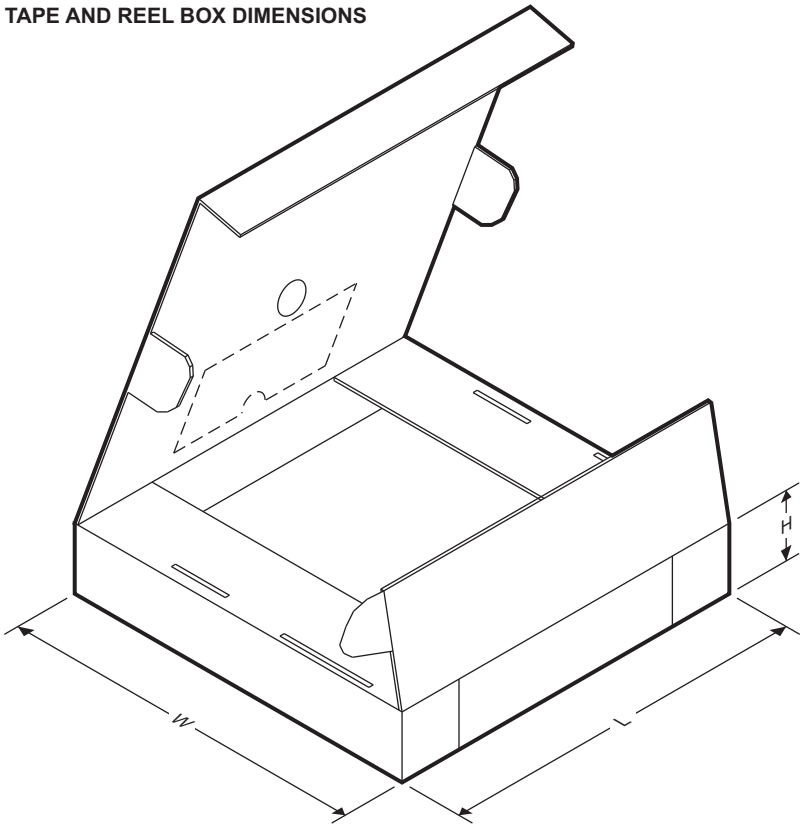
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS82692SIPR	uSIP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82692SIPT	uSIP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82693SIPR	uSIP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82693SIPT	uSIP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS826951SIPR	uSIP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS826951SIPT	uSIP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82697SIPR	uSIP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82697SIPT	uSIP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82698SIPR	uSIP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82698SIPT	uSIP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS82692SIPR	uSIP	SIP	8	3000	223	194	35
TPS82692SIPT	uSIP	SIP	8	250	223	194	35
TPS82693SIPR	uSIP	SIP	8	3000	223	194	35
TPS82693SIPT	uSIP	SIP	8	250	223	194	35
TPS826951SIPR	uSIP	SIP	8	3000	223	194	35
TPS826951SIPT	uSIP	SIP	8	250	223	194	35
TPS82697SIPR	uSIP	SIP	8	3000	223	194	35
TPS82697SIPT	uSIP	SIP	8	250	223	194	35
TPS82698SIPR	uSIP	SIP	8	3000	223	194	35
TPS82698SIPT	uSIP	SIP	8	250	223	194	35

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS82692SIPR	ACTIVE	uSiP	SIP	8	3000	Green (RoHS & no Sb/Br)	SnAgCu	Level-2-260C-1 YEAR	-40 to 85	E9 TXI692	Samples
TPS82692SIPT	ACTIVE	uSiP	SIP	8	250	Green (RoHS & no Sb/Br)	SnAgCu	Level-2-260C-1 YEAR	-40 to 85	E9 TXI692	Samples
TPS82693SIPR	ACTIVE	uSiP	SIP	8	3000	Green (RoHS & no Sb/Br)	SnAgCu	Level-2-260C-1 YEAR	-40 to 85	W3 TXI693	Samples
TPS82693SIPT	ACTIVE	uSiP	SIP	8	250	Green (RoHS & no Sb/Br)	SnAgCu	Level-2-260C-1 YEAR	-40 to 85	W3 TXI693	Samples
TPS826951SIPR	ACTIVE	uSiP	SIP	8	3000	Green (RoHS & no Sb/Br)	SnAgCu	Level-2-260C-1 YEAR	-40 to 85	DO TXI695	Samples
TPS826951SIPT	ACTIVE	uSiP	SIP	8	250	Green (RoHS & no Sb/Br)	SnAgCu	Level-2-260C-1 YEAR	-40 to 85	DO TXI695	Samples
TPS82697SIPR	ACTIVE	uSiP	SIP	8	3000	Green (RoHS & no Sb/Br)	SnAgCu	Level-2-260C-1 YEAR	-40 to 85	C2 TXI697	Samples
TPS82697SIPT	ACTIVE	uSiP	SIP	8	250	Green (RoHS & no Sb/Br)	SnAgCu	Level-2-260C-1 YEAR	-40 to 85	C2 TXI697	Samples
TPS82698SIPR	ACTIVE	uSiP	SIP	8	3000	Green (RoHS & no Sb/Br)	SnAgCu	Level-2-260C-1 YEAR	-40 to 85	WN TXI698	Samples
TPS82698SIPT	ACTIVE	uSiP	SIP	8	250	Green (RoHS & no Sb/Br)	SnAgCu	Level-2-260C-1 YEAR	-40 to 85	WN TXI698	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

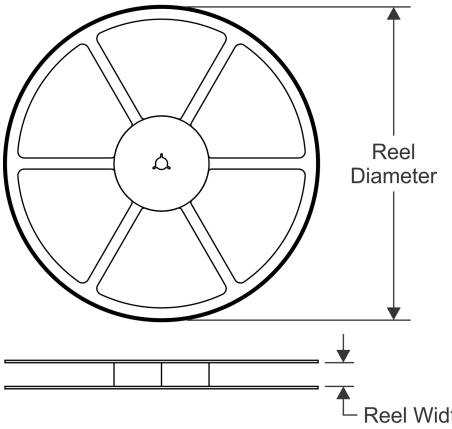
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

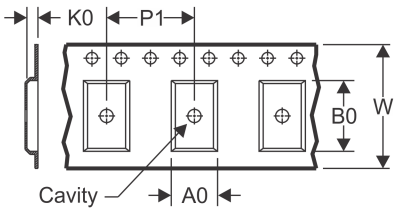
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

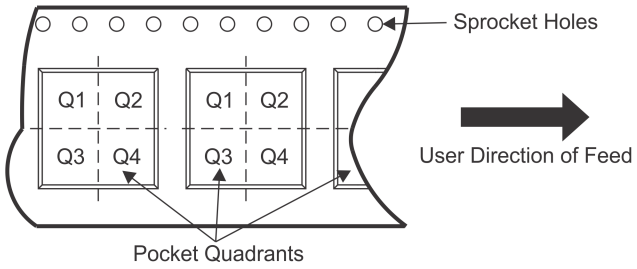


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

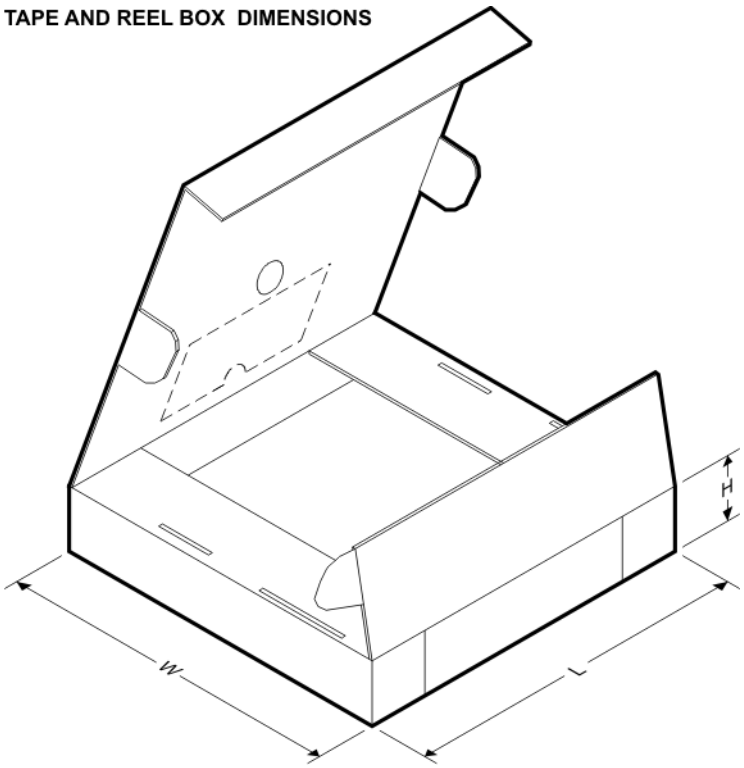
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS82692SIPR	uSiP	SIP	8	3000	180.0	8.4	1.04	1.41	0.21	2.0	8.0	Q1
TPS82692SIPT	uSiP	SIP	8	250	180.0	8.4	1.04	1.41	0.21	2.0	8.0	Q1
TPS82693SIPR	uSiP	SIP	8	3000	180.0	8.4	1.04	1.41	0.21	2.0	8.0	Q1
TPS82693SIPT	uSiP	SIP	8	250	180.0	8.4	1.04	1.41	0.21	2.0	8.0	Q1
TPS826951SIPR	uSiP	SIP	8	3000	180.0	8.4	1.04	1.41	0.21	2.0	8.0	Q1
TPS826951SIPT	uSiP	SIP	8	250	180.0	8.4	1.04	1.41	0.21	2.0	8.0	Q1
TPS82697SIPR	uSiP	SIP	8	3000	180.0	8.4	1.04	1.41	0.21	2.0	8.0	Q1
TPS82697SIPT	uSiP	SIP	8	250	180.0	8.4	1.04	1.41	0.21	2.0	8.0	Q1
TPS82698SIPR	uSiP	SIP	8	3000	180.0	8.4	1.04	1.41	0.21	2.0	8.0	Q1
TPS82698SIPT	uSiP	SIP	8	250	180.0	8.4	1.04	1.41	0.21	2.0	8.0	Q1

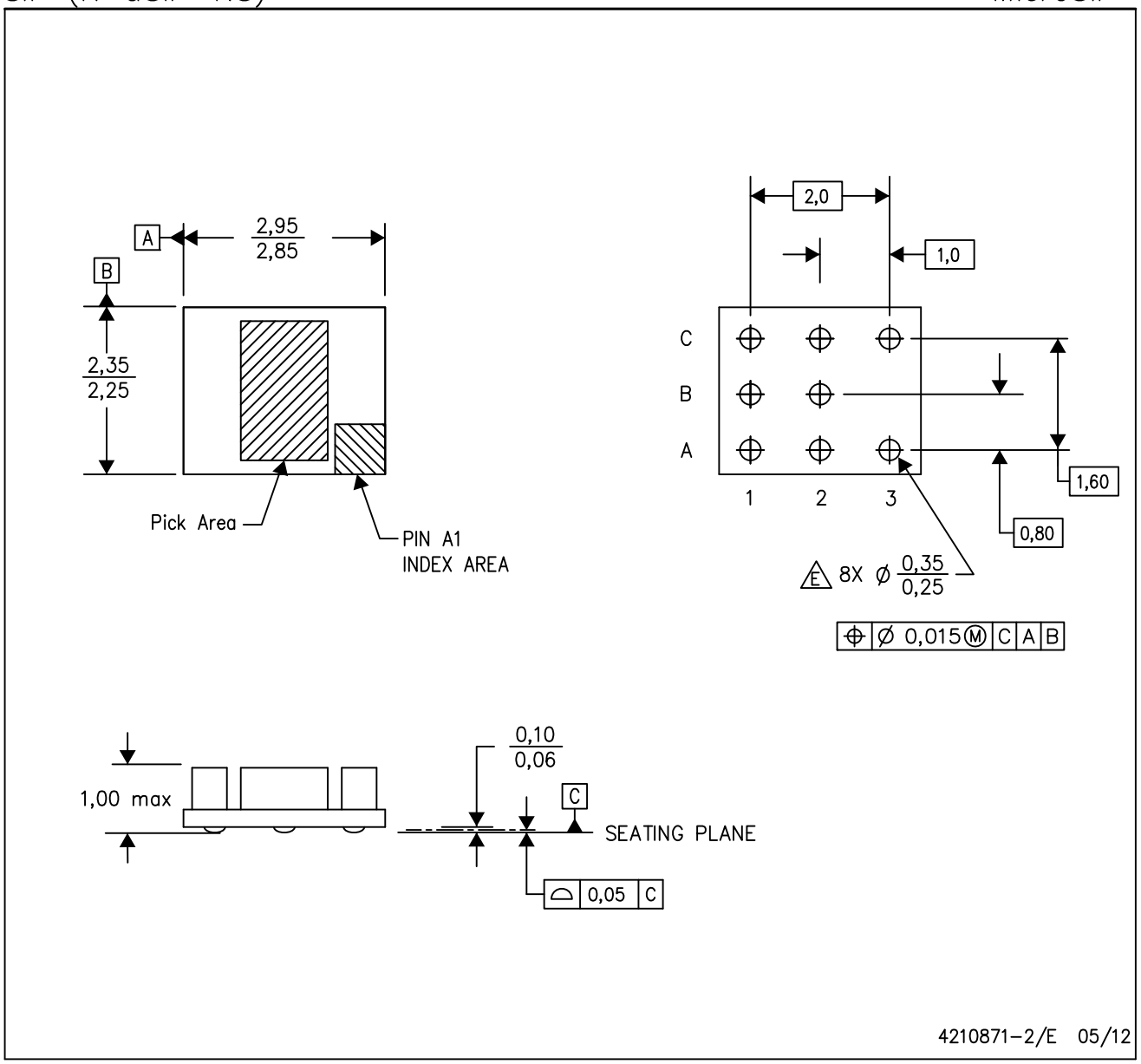
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS82692SIPR	uSiP	SIP	8	3000	182.0	182.0	20.0
TPS82692SIPT	uSiP	SIP	8	250	182.0	182.0	20.0
TPS82693SIPR	uSiP	SIP	8	3000	210.0	185.0	35.0
TPS82693SIPT	uSiP	SIP	8	250	210.0	185.0	35.0
TPS826951SIPR	uSiP	SIP	8	3000	182.0	182.0	20.0
TPS826951SIPT	uSiP	SIP	8	250	182.0	182.0	20.0
TPS82697SIPR	uSiP	SIP	8	3000	210.0	185.0	35.0
TPS82697SIPT	uSiP	SIP	8	250	210.0	185.0	35.0
TPS82698SIPR	uSiP	SIP	8	3000	210.0	185.0	35.0
TPS82698SIPT	uSiP	SIP	8	250	210.0	185.0	35.0

SIP (R–uSiP–N8) MicroSiP™



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. MicroSiP™ package configuration – Micro System in Package.
D. Reference Product Data Sheet for array population. 3 x 3 matrix pattern is shown for illustration only.
E. This package contains Pb–free balls.

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