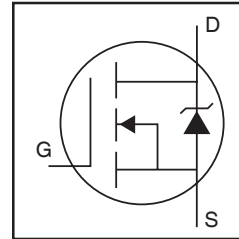


IRFR1018EPbF IRFU1018EPbF

HEXFET® Power MOSFET

Applications

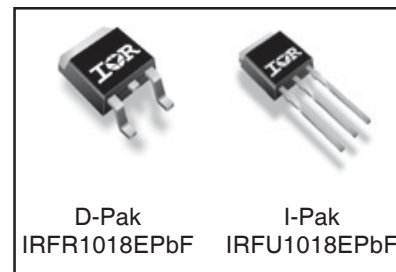
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



| | | |
|-------------------------|------|--------------|
| V_{DSS} | | 60V |
| $R_{DS(on)}$ | typ. | 7.1mΩ |
| | max. | 8.4mΩ |
| I_D (Silicon Limited) | | 79A ① |
| I_D (Package Limited) | | 56A |

Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability



| | | |
|----------|----------|----------|
| G | D | S |
| Gate | Drain | Source |

Absolute Maximum Ratings

| Symbol | Parameter | Max. | Units |
|-----------------------------------|--|--------------|-------|
| I_D @ $T_C = 25^\circ\text{C}$ | Continuous Drain Current, V_{GS} @ 10V (Silicon Limited) | 79① | A |
| I_D @ $T_C = 100^\circ\text{C}$ | Continuous Drain Current, V_{GS} @ 10V (Silicon Limited) | 56① | |
| I_D @ $T_C = 25^\circ\text{C}$ | Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited) | 56 | |
| I_{DM} | Pulsed Drain Current ② | 315 | |
| P_D @ $T_C = 25^\circ\text{C}$ | Maximum Power Dissipation | 110 | W |
| | Linear Derating Factor | 0.76 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| dv/dt | Peak Diode Recovery ④ | 21 | V/ns |
| T_J T_{STG} | Operating Junction and Storage Temperature Range | -55 to + 175 | °C |
| | Soldering Temperature, for 10 seconds (1.6mm from case) | 300 | |

Avalanche Characteristics

| | | | |
|------------------------------|---------------------------------|----|----|
| E_{AS} (Thermally limited) | Single Pulse Avalanche Energy ③ | 88 | mJ |
| I_{AR} | Avalanche Current ② | 47 | A |
| E_{AR} | Repetitive Avalanche Energy ⑤ | 11 | mJ |

Thermal Resistance

| Symbol | Parameter | Typ. | Max. | Units |
|-----------------|------------------------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case ⑥ | — | 1.32 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mount) ⑥⑦ | — | 50 | |
| $R_{\theta JA}$ | Junction-to-Ambient ⑥ | — | 110 | |

Notes ① through ⑦ are on page 2

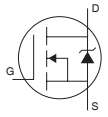
Static @ T_J = 25°C (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|--------------------------------------|--------------------------------------|------|-------|------|-------|---|
| V _{(BR)DSS} | Drain-to-Source Breakdown Voltage | 60 | — | — | V | V _{GS} = 0V, I _D = 250μA |
| ΔV _{(BR)DSS/ΔT_J} | Breakdown Voltage Temp. Coefficient | — | 0.073 | — | V/°C | Reference to 25°C, I _D = 5mA ^② |
| R _{DS(on)} | Static Drain-to-Source On-Resistance | — | 7.1 | 8.4 | mΩ | V _{GS} = 10V, I _D = 47A ^③ |
| V _{GS(th)} | Gate Threshold Voltage | 2.0 | — | 4.0 | V | V _{DS} = V _{GS} , I _D = 100μA |
| I _{DSS} | Drain-to-Source Leakage Current | — | — | 20 | μA | V _{DS} = 60V, V _{GS} = 0V |
| | | — | — | 250 | | V _{DS} = 48V, V _{GS} = 0V, T _J = 125°C |
| I _{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | V _{GS} = 20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | V _{GS} = -20V |

Dynamic @ T_J = 25°C (unless otherwise specified)

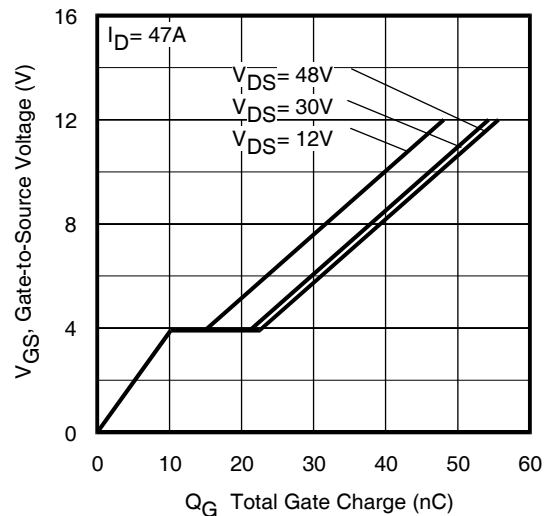
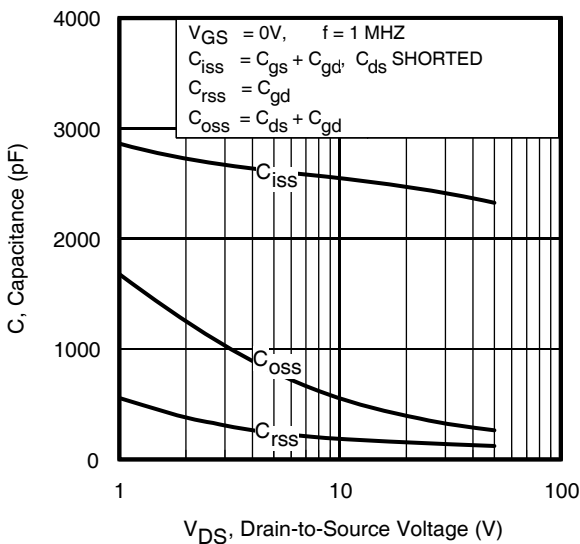
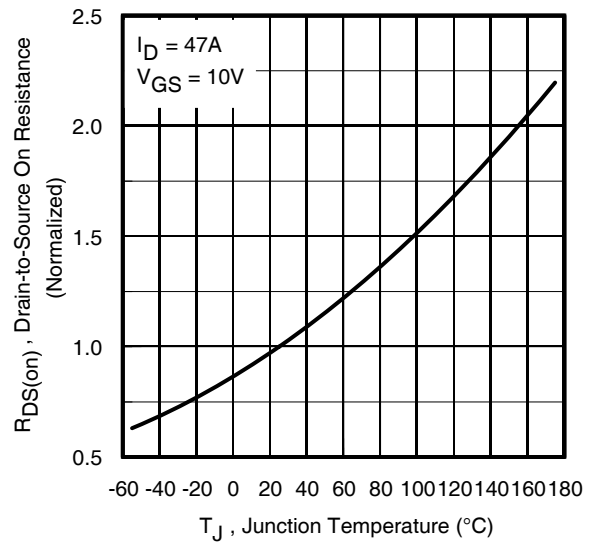
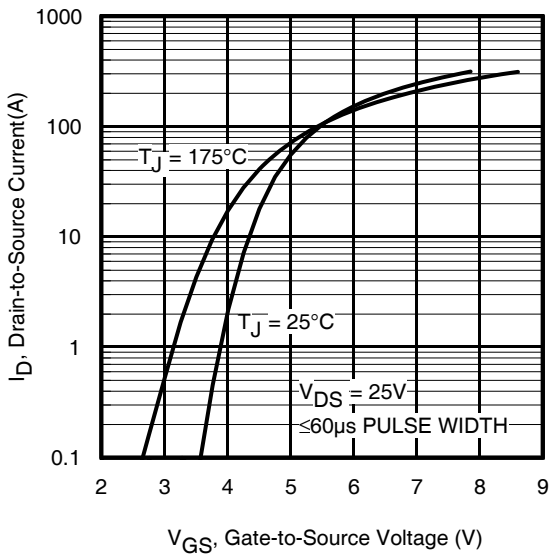
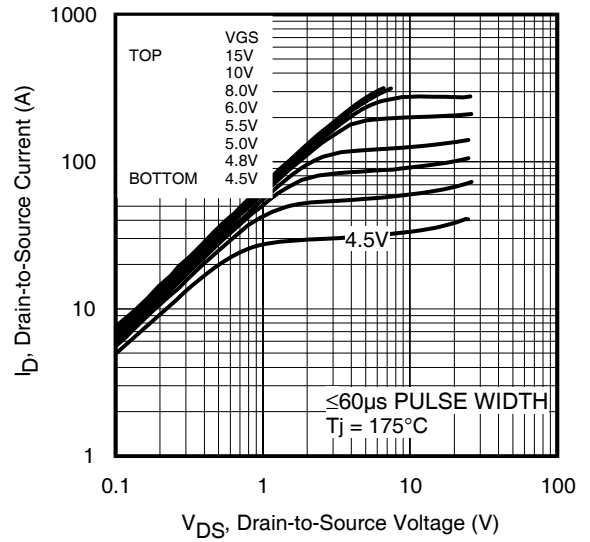
| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------------------------|---|------|------|------|-------|---|
| g _{fs} | Forward Transconductance | 110 | — | — | S | V _{DS} = 50V, I _D = 47A |
| Q _g | Total Gate Charge | — | 46 | 69 | nC | I _D = 47A |
| Q _{gs} | Gate-to-Source Charge | — | 10 | — | | V _{DS} = 30V |
| Q _{gd} | Gate-to-Drain ("Miller") Charge | — | 12 | — | | V _{GS} = 10V ^⑤ |
| Q _{sync} | Total Gate Charge Sync. (Q _g - Q _{gd}) | — | 34 | — | | I _D = 47A, V _{DS} = 0V, V _{GS} = 10V |
| R _{G(int)} | Internal Gate Resistance | — | 0.73 | — | Ω | |
| t _{d(on)} | Turn-On Delay Time | — | 13 | — | ns | V _{DD} = 39V |
| t _r | Rise Time | — | 35 | — | | I _D = 47A |
| t _{d(off)} | Turn-Off Delay Time | — | 55 | — | | R _G = 10Ω |
| t _f | Fall Time | — | 46 | — | | V _{GS} = 10V ^⑤ |
| C _{iss} | Input Capacitance | — | 2290 | — | | V _{GS} = 0V |
| C _{oss} | Output Capacitance | — | 270 | — | | V _{DS} = 50V |
| C _{rfs} | Reverse Transfer Capacitance | — | 130 | — | pF | f = 1.0MHz |
| C _{oss eff. (ER)} | Effective Output Capacitance (Energy Related) ^④ | — | 390 | — | | V _{GS} = 0V, V _{DS} = 0V to 60V ^⑦ |
| C _{oss eff. (TR)} | Effective Output Capacitance (Time Related) ^⑤ | — | 630 | — | | V _{GS} = 0V, V _{DS} = 0V to 60V ^⑥ |

Diode Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|------------------|--|--|------|-----------------|-------|--|
| I _S | Continuous Source Current (Body Diode) | — | — | 79 ^① | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I _{SM} | Pulsed Source Current (Body Diode) ^② | — | — | 315 | | |
| V _{SD} | Diode Forward Voltage | — | — | 1.3 | V | T _J = 25°C, I _S = 47A, V _{GS} = 0V ^⑤ |
| t _{rr} | Reverse Recovery Time | — | 26 | 39 | ns | T _J = 25°C V _R = 51V, T _J = 125°C I _F = 47A |
| Q _{rr} | Reverse Recovery Charge | — | 24 | 36 | nC | T _J = 25°C T _J = 125°C |
| I _{RRM} | Reverse Recovery Current | — | 1.8 | — | A | T _J = 25°C |
| t _{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 56A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.08mH
R_G = 25Ω, I_{AS} = 47A, V_{GS} = 10V. Part not recommended for use above this value.
- ④ I_{SD} ≤ 47A, di/dt ≤ 1668A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.
- ⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑥ C_{oss eff. (TR)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑦ C_{oss eff. (ER)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R_θ is measured at T_J approximately 90°C.



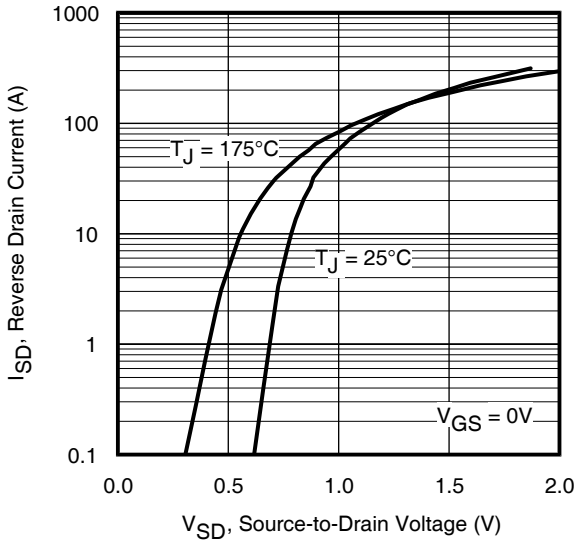


Fig 7. Typical Source-Drain Diode Forward Voltage

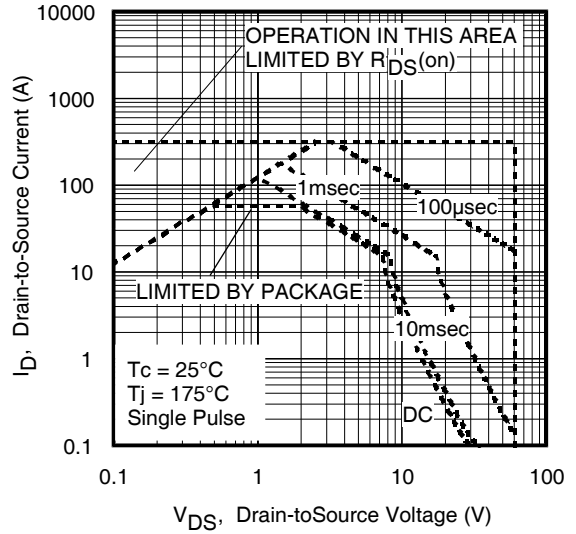


Fig 8. Maximum Safe Operating Area

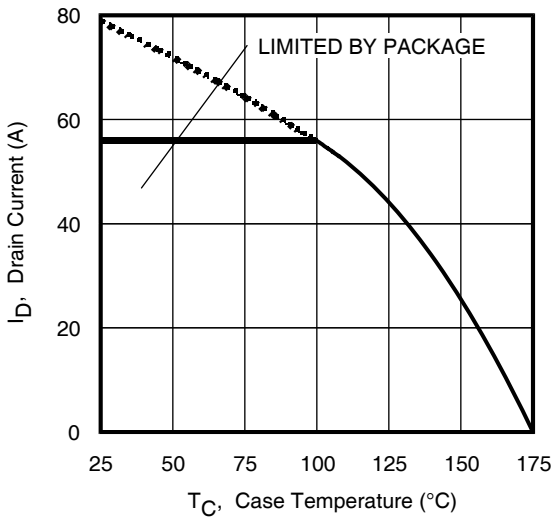


Fig 9. Maximum Drain Current vs. Case Temperature

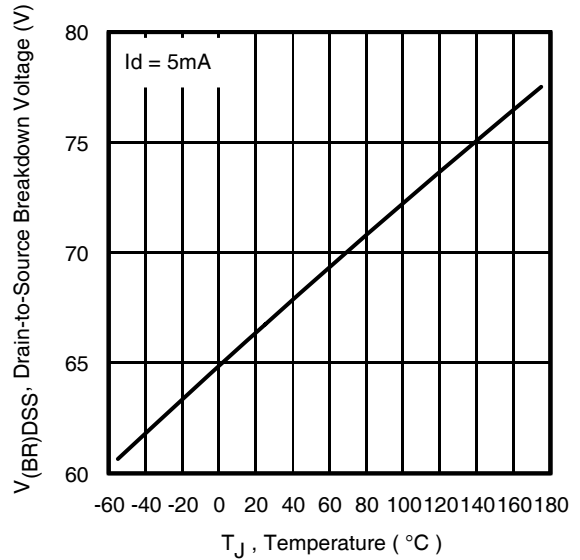


Fig 10. Drain-to-Source Breakdown Voltage

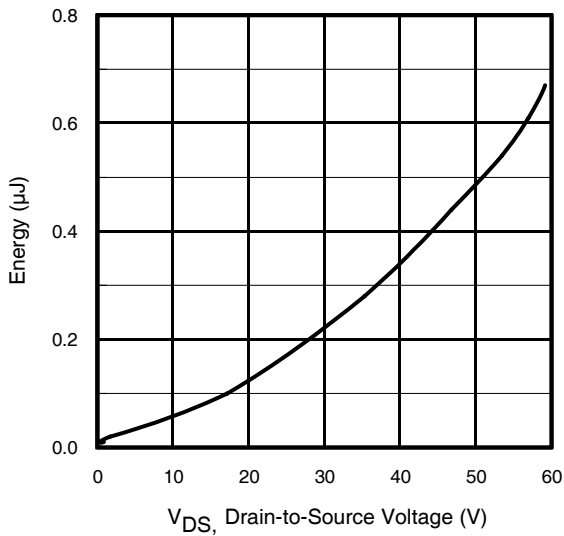


Fig 11. Typical C_{OSS} Stored Energy

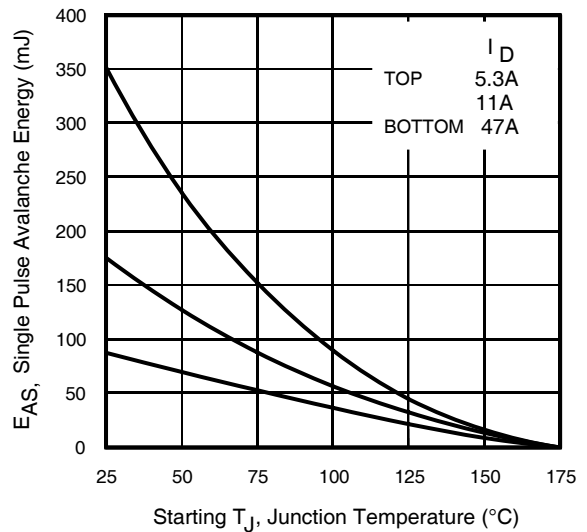


Fig 12. Maximum Avalanche Energy vs. Drain Current
www.irf.com

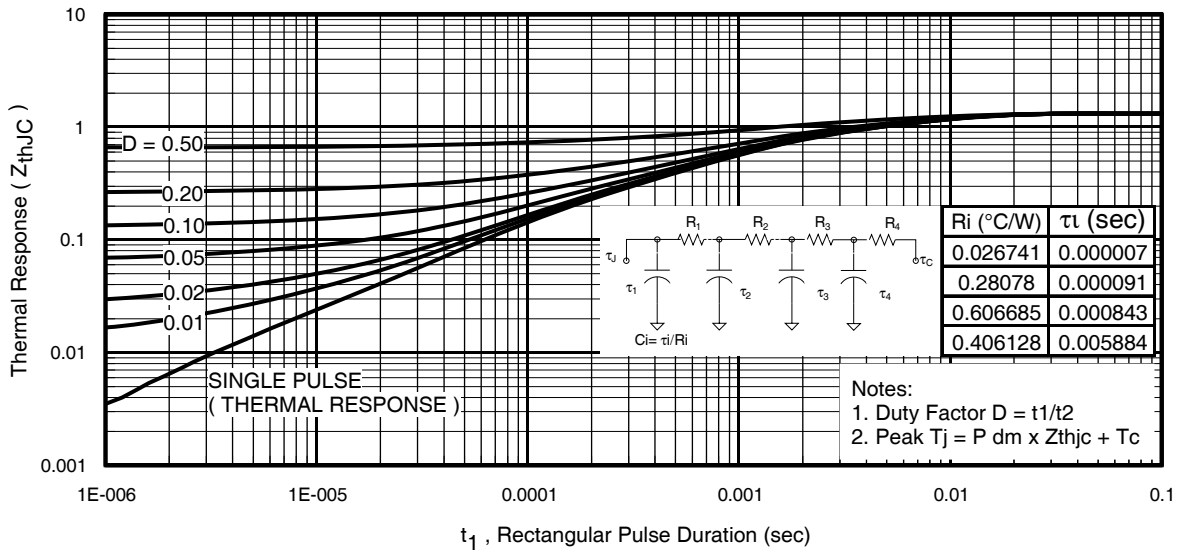


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

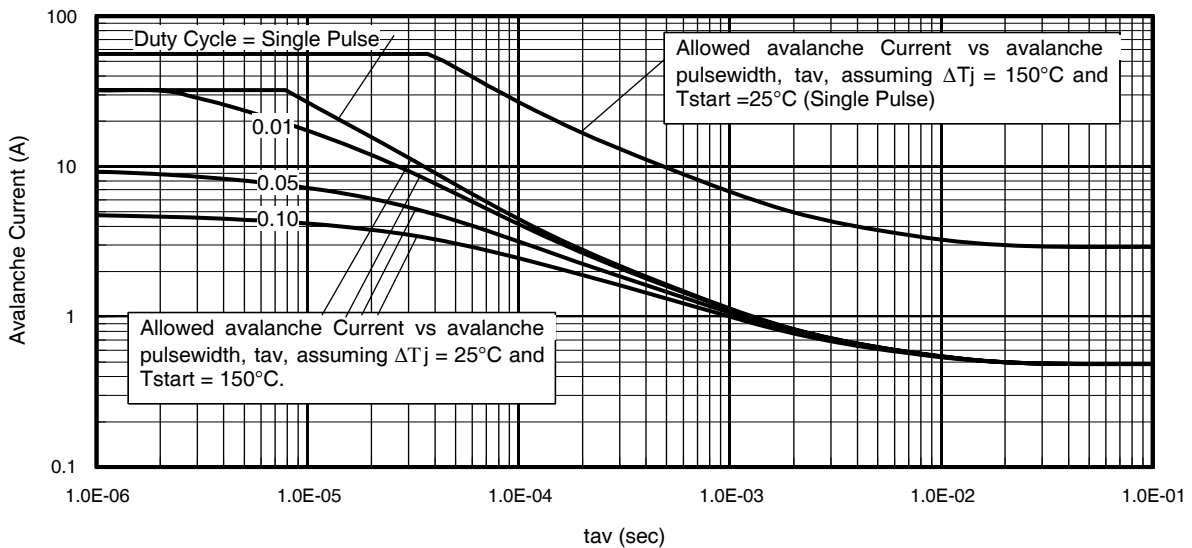
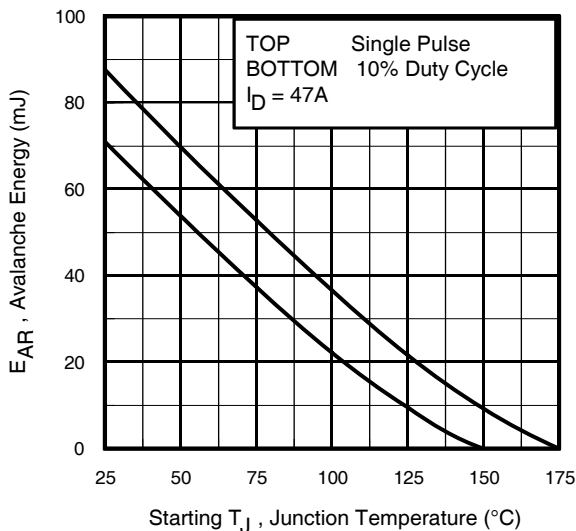


Fig 14. Typical Avalanche Current vs. Pulsewidth



Notes on Repetitive Avalanche Curves, Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

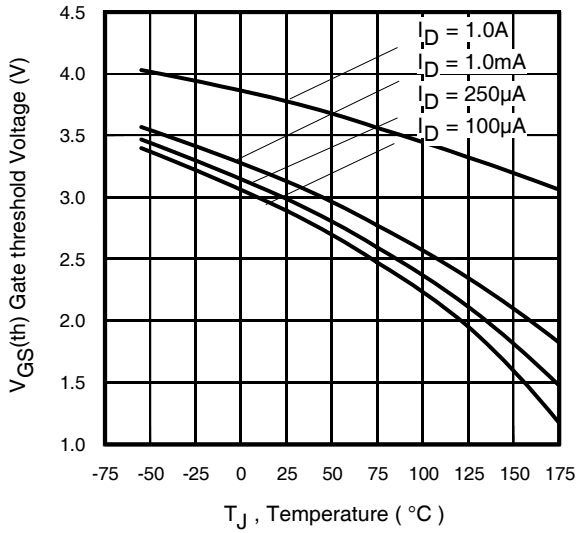


Fig 16. Threshold Voltage vs. Temperature

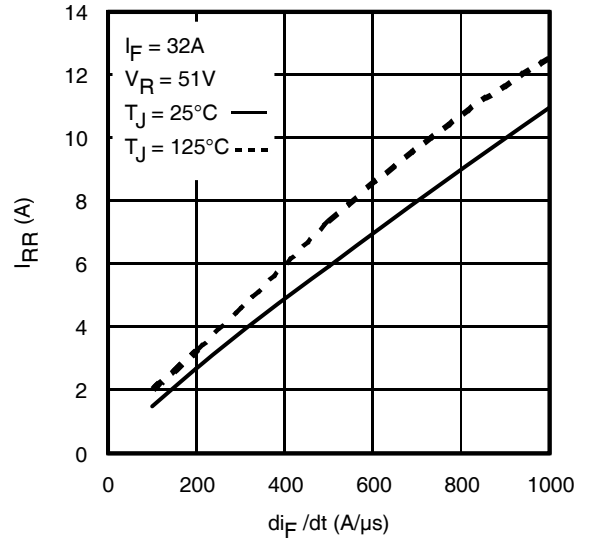


Fig. 17 - Typical Recovery Current vs. di/dt

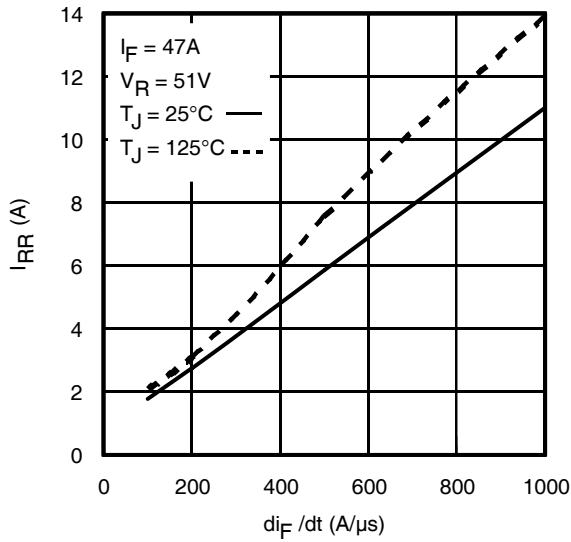


Fig. 18 - Typical Recovery Current vs. di/dt

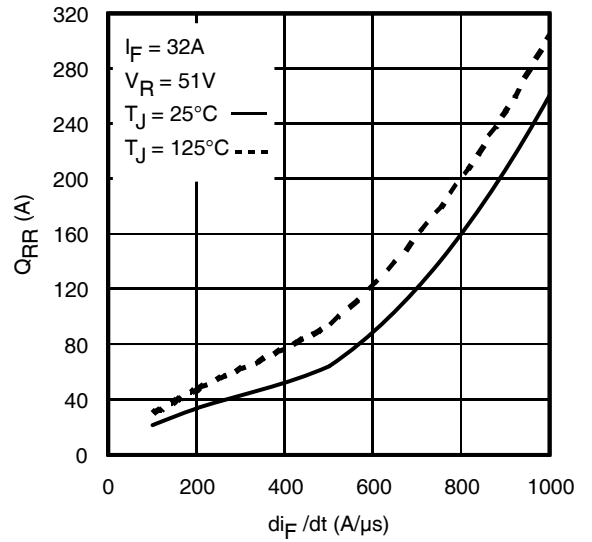


Fig. 19 - Typical Stored Charge vs. di/dt

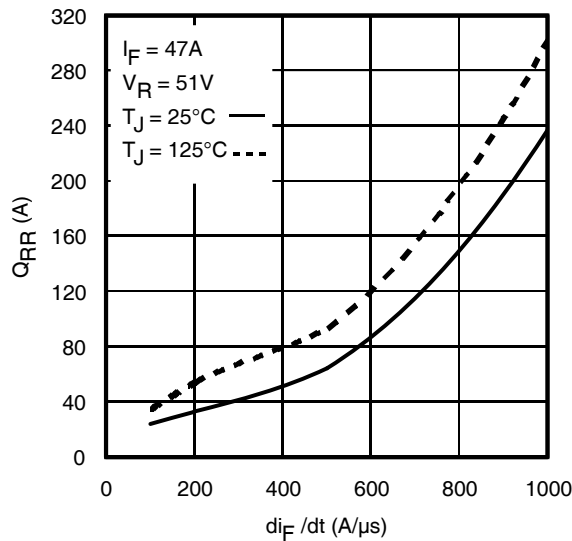


Fig. 20 - Typical Stored Charge vs. di/dt

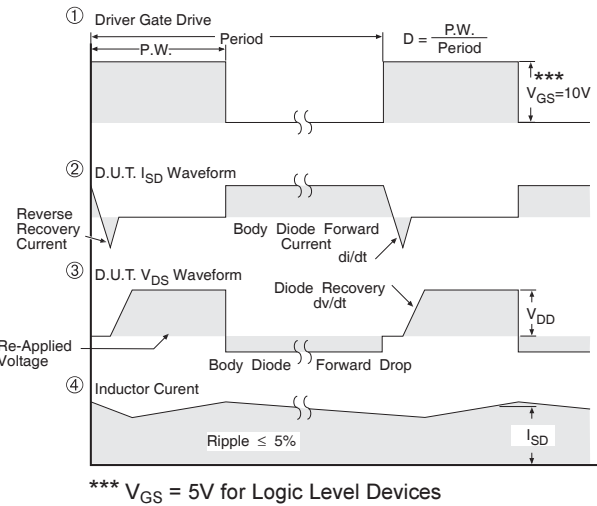


Fig 21. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs

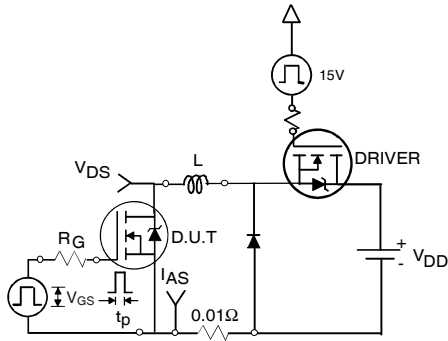


Fig 22a. Unclamped Inductive Test Circuit

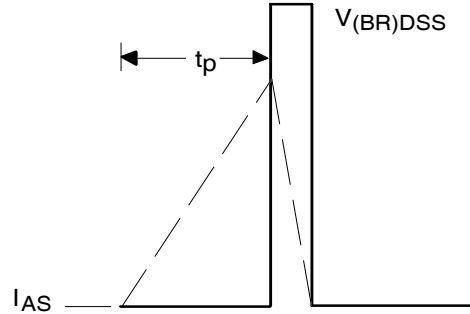


Fig 22b. Unclamped Inductive Waveforms

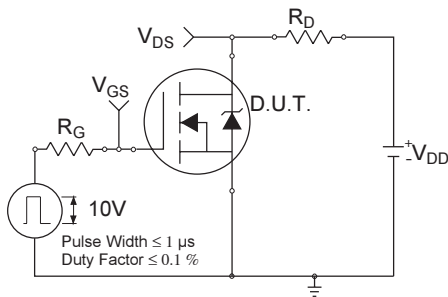


Fig 23a. Switching Time Test Circuit

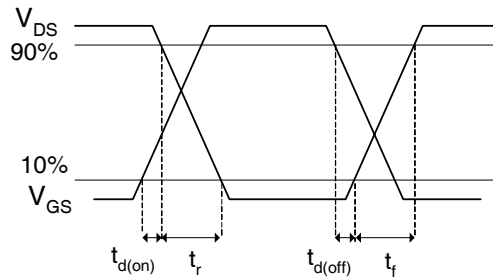


Fig 23b. Switching Time Waveforms

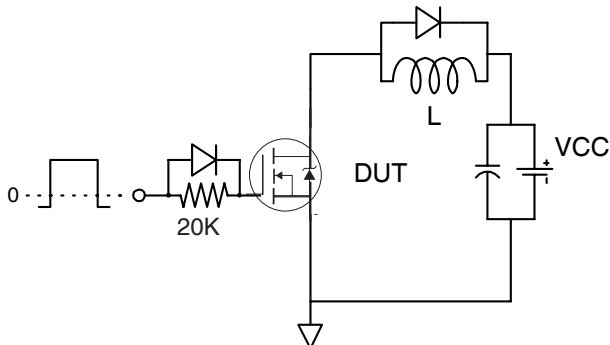


Fig 24a. Gate Charge Test Circuit

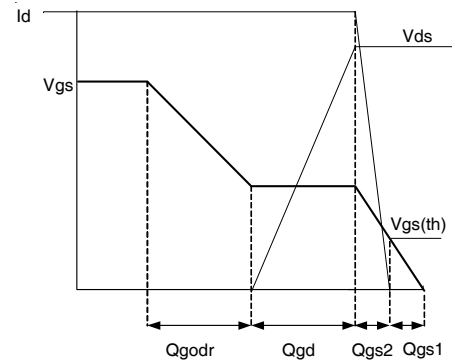
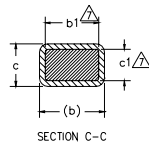
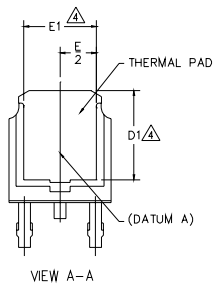
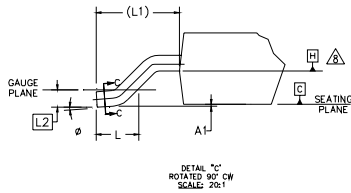
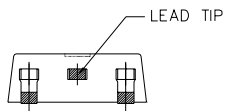
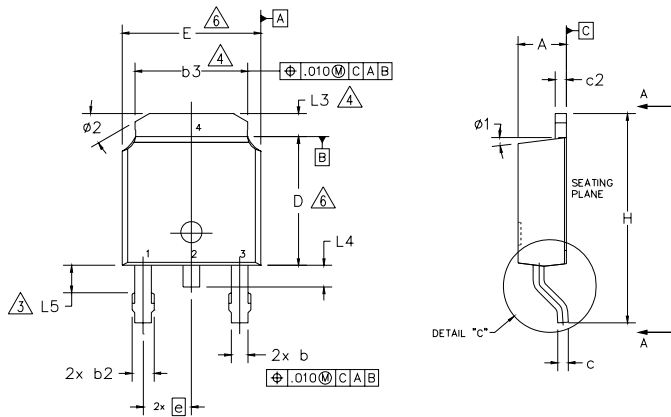


Fig 24b. Gate Charge Waveform

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|-------|-----------|------|------------------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.18 | 2.39 | .086 | .094 | 7 |
| A1 | - | 0.13 | - | .005 | |
| b | 0.64 | 0.89 | .025 | .035 | |
| b1 | 0.65 | 0.79 | .025 | .031 | |
| b2 | 0.76 | 1.14 | .030 | .045 | |
| b3 | 4.95 | 5.46 | .195 | .215 | |
| c | 0.46 | 0.61 | .018 | .024 | |
| c1 | 0.41 | 0.56 | .016 | .022 | |
| c2 | 0.46 | 0.89 | .018 | .035 | |
| D | 5.97 | 6.22 | .235 | .245 | |
| D1 | 5.21 | - | .205 | - | 4 |
| E | 6.35 | 6.73 | .250 | .265 | 6 |
| E1 | 4.32 | - | .170 | - | 4 |
| e | 2.29 BSC | | .090 BSC | | LEAD ASSIGNMENTS |
| H | 9.40 | 10.41 | .370 | .410 | |
| L | 1.40 | 1.78 | .055 | .070 | |
| L1 | 2.74 BSC | | .108 REF. | | |
| L2 | 0.51 BSC | | .020 BSC | | HEXFET |
| L3 | 0.89 | 1.27 | .035 | .050 | |
| L4 | - | 1.02 | - | .040 | |
| L5 | 1.14 | 1.52 | .045 | .060 | |
| ø | 0" | 10" | 0" | 10" | |
| ø1 | 0" | 15" | 0" | 15" | IGBT & CoPAK |
| ø2 | 25" | 35" | 25" | 35" | |

LEAD ASSIGNMENTS

- HEXFET**
- 1.- GATE
 - 2.- DRAIN
 - 3.- SOURCE
 - 4.- DRAIN

IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

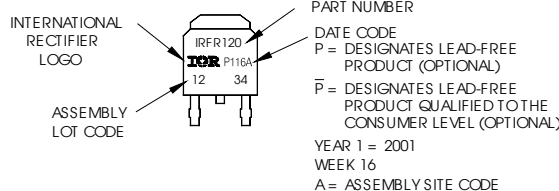
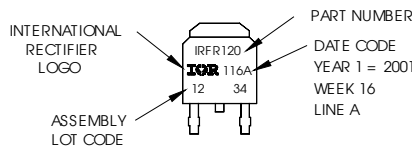
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120 WITH ASSEMBLY LOT CODE 1234 ASSEMBLED ON WW 16, 2001 IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"

"P̄" in assembly line position indicates "Lead-Free" qualification to the consumer-level

OR

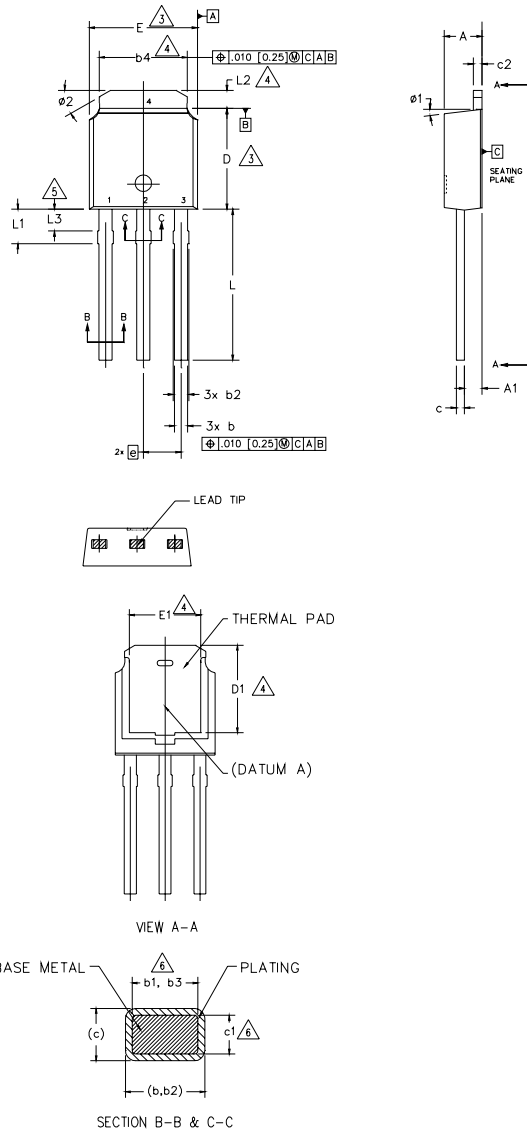


YEAR 1 = 2001
WEEK 16
A = ASSEMBLY SITE CODE

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 4.- THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5.- LEAD DIMENSION UNCONTROLLED IN L3.
- 6.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
- 8.- CONTROLLING DIMENSION : INCHES.

| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|------|----------|------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.18 | 2.39 | .086 | .094 | |
| A1 | 0.89 | 1.14 | .035 | .045 | |
| b | 0.64 | 0.89 | .025 | .035 | 6 |
| b1 | 0.65 | 0.79 | .025 | .031 | |
| b2 | 0.76 | 1.14 | .030 | .045 | 6 |
| b3 | 0.76 | 1.04 | .030 | .041 | |
| b4 | 4.95 | 5.46 | .195 | .215 | 4 |
| c | 0.46 | 0.61 | .018 | .024 | 6 |
| c1 | 0.41 | 0.56 | .016 | .022 | |
| c2 | 0.46 | 0.89 | .018 | .035 | 3 |
| D | 5.97 | 6.22 | .235 | .245 | |
| D1 | 5.21 | - | .205 | - | 4 |
| E | 6.35 | 6.73 | .250 | .265 | 3 |
| E1 | 4.32 | - | .170 | - | 4 |
| e | 2.29 BSC | | .090 BSC | | |
| L | 8.89 | 9.65 | .350 | .380 | 4 |
| L1 | 1.91 | 2.29 | .045 | .090 | |
| L2 | 0.89 | 1.27 | .035 | .050 | 5 |
| L3 | 1.14 | 1.52 | .045 | .060 | |
| phi1 | 0" | 15" | 0" | 15" | |
| phi2 | 25" | 35" | 25" | 35" | |

LEAD ASSIGNMENTS

HEXFET

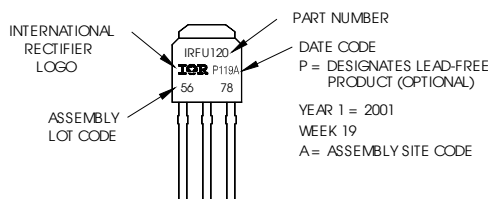
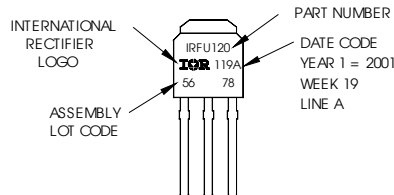
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120 WITH ASSEMBLY LOT CODE 5678 ASSEMBLED ON WW 19, 2001 IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates Lead-Free'

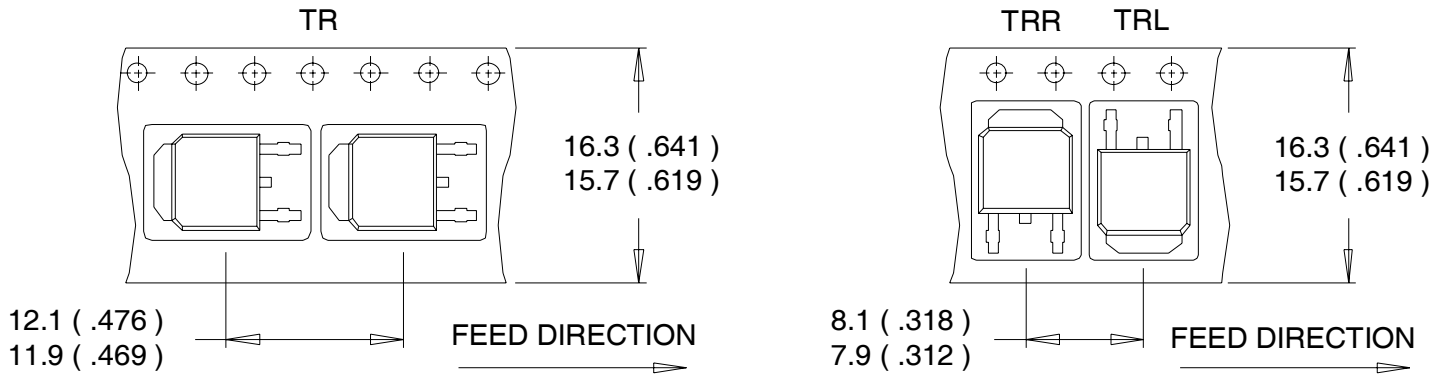
OR



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

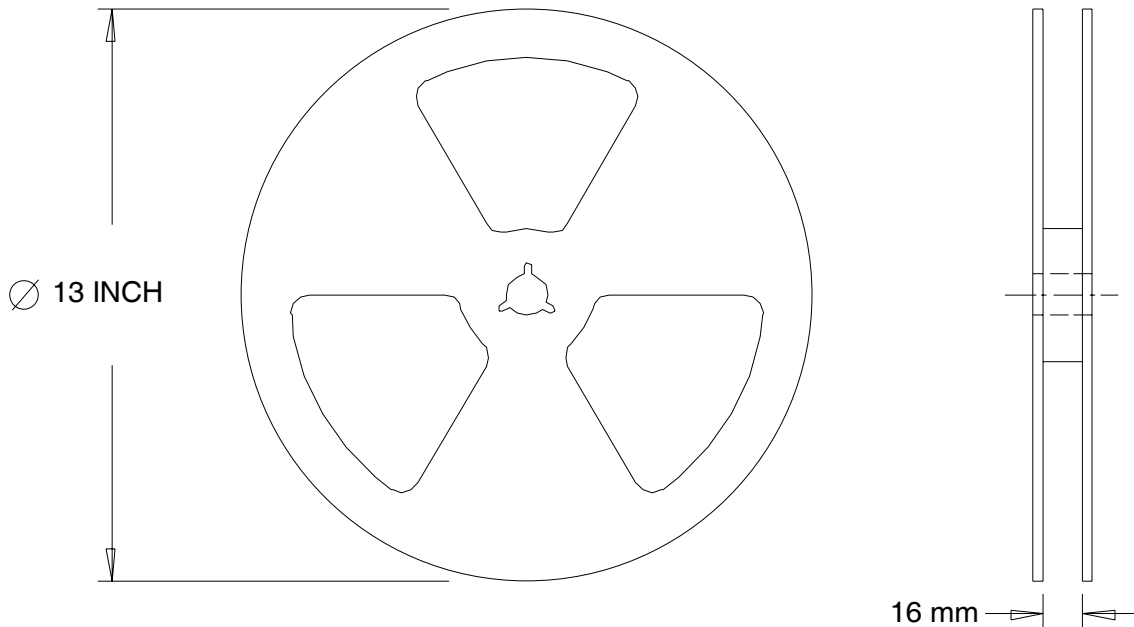
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.
This product has been designed for the industrial market.
Qualification Standards can be found on IR's Web site.

Mouser Electronics

Authorized Distributor

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