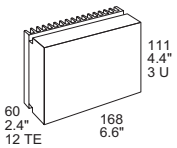


RoHS Compliant

Features

- RoHS lead-free-solder and lead-solder-exempted products are available.
- Class I equipment
- Power factor >0.93, harmonics IEC/EN 61000-3-2
- Immunity according to IEC/EN 61000-4-2, -3, -4, -5, -6, -8, -9
- Compliant with EN 50155, EN 50121-4, EN 45545.
- High efficiency
- Input over- and undervoltage lockout
- Adjustable output voltage with remote on/off
- 1 or 2 outputs: SELV, no load, overload, and short-circuit proof
- Rectangular current limiting characteristic
- PCBs protected by lacquer
- Very high reliability

Safety-approved according to IEC/EN 60950-1, UL/CSA 60950-1 2nd Ed.

Description

The LS 4000/5000 Series of AC-DC converters represents a flexible range of power supplies for use in advanced electronic systems. Features include full power factor correction, good hold-up time, high efficiency and reliability, low output voltage noise, and excellent dynamic response to load/line changes.

The converters are protected against surges and transients occurring at the source lines. Input over- and undervoltage lockout circuitry disables the outputs, when the input voltage is outside of the specified range. Input inrush current limitation is included for preventing circuit breakers and fuses from tripping at switch-on.

All outputs are overload, open- and short-circuit proof and protected by a built-in suppressor diode. The outputs can be inhibited by a logic signal applied to connector pin 18. If the inhibit function is not used, pin 18 must be connected with pin 14 to enable the outputs.

LED indicators display the status of the converter and allow visual monitoring of the system at any time.

Full input to output, input to case, output to case and output to output isolation is provided. The converters are designed and built according to the international safety standards IEC/EN 60950-1 2nd Ed. They have been approved by the safety agencies Nemko and CSA (for USA and Canada).

The case design allows operation at nominal load up to 71 °C in a free air ambient temperature. If forced cooling is provided, the ambient temperature may exceed 71 °C but the case temperature must remain below 95 °C under all conditions.

Table of Contents

An internal temperature sensor generates an inhibit signal, which disables the outputs, if the case temperature T_C exceeds the limit. The outputs automatically recover, when the temperature drops below the limit.

Various options including battery chargers are available to adapt the converters to individual applications.

The converters may either be plugged into 19" rack systems according to IEC 60297-3, or be chassis mounted.

Important:
These products are intended to replace the LS1000 and LS2000 models in order to comply with IEC/EN 61000-3-2. For applications with DC input or main frequencies other than 50/60 Hz, the LS1000 and LS2000 models are still available.

Model Selection

Non-standard input/output configurations or special customer adaptations are available on request.

Table 1: Model types LS

Output 1		Output 2		Oper. input voltage range	Efficiency [1]	Options
$V_{o\ nom}$ [VDC]	$I_{o\ nom}$ [A] [2]	$V_{o\ nom}$ [VDC]	$I_{o\ nom}$ [A]	$V_{i\ min} – V_{i\ max}$ 85 – 264 VAC	η_{min} [%]	
5.1	16			LS4001-9ER	77	-7, -7E, P, D [2], V [2], T, B, B1, B2 [4], G
12	8			LS4301-9ER	81	-7, -7E, P, D, T, B, B1, B2 [4], G
15	6.5			LS4501-9ER	83	
24	4.2			LS4601-9ER	83	
24	4			LS5320-9ER	81	
30	3.2			LS5540-9ER	81	
48	2			LS5660-9ER	81	
12	4	12 [3]	4	LS5320-9ER	81	
15	3.2	15 [3]	3.2	LS5540-9ER	81	
24	2	24 [3]	2	LS5660-9ER	81	

1 Min. efficiency at $V_{i\ nom}$, $I_{o\ nom}$ and $T_A = 25$ °C. Typical values are approximately 2% better.
2 Option V for LS4000 models with 5.1 V output; excludes option D
3 Second output semi-regulated
4 For customer-specific models with 220 mm case length

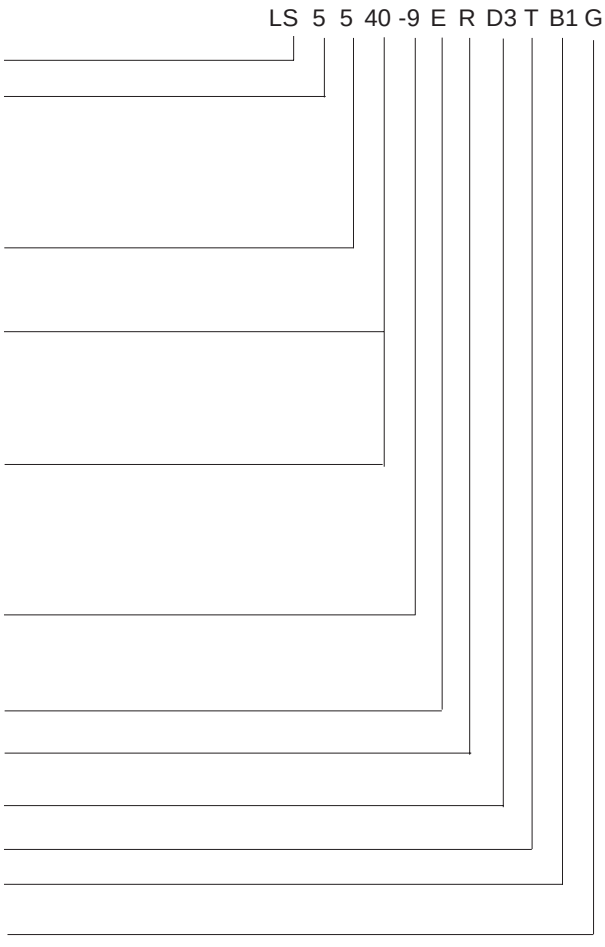
Table 2: Battery charger models

Nom. output values		Output range		Oper. input voltage range	Efficiency [1]	Options
$V_{o\ nom}$ [VDC]	$I_{o\ nom}$ [A]	$V_{o\ nom}$ [VDC]	$I_{o\ nom}$ [A]	$V_{i\ min} – V_{i\ max}$ 85 – 264 VAC	η_{min} [%]	
12.84	7	12.62 – 14.12		LS4740-9ER	81	-7, -7E, D, T, B, B1, G
25.68 [2]	3.4	25.25 – 28.25		LS5740-9ER	81	
51.36 [3]	1.7	50.5 – 56.5		LS5740-9ER	81	

1 Min. efficiency at $V_{i\ nom}$, $I_{o\ nom}$ and $T_A = 25$ °C. Typical values are approximately 2% better.
2 Both outputs connected in parallel
3 Both outputs connected in series

NFND: Not for new designs Preferred for new designs

Part Number Description



Operating input voltage V_i: 85 – 264 VAC ..... LS

Number of outputs 4, 5

Single output models:

Nominal voltage output 1 (main output), $V_{o1\ nom}$

- 5.1 V 0, 1, 2
- 12 V 3
- 15 V 4, 5
- 24 V 6
- Other voltages [1] 7, 8
- Other specifications (single output models)[1] ..... 01 – 99

Double output models:

Nominal voltage output 1 and 2

- 12 V, 12 V 20
- 15 V, 15 V 40
- 24 V, 24 V 60
- Other specifications or additional features [1] 21– 99

Operational ambient temperature range T_A:

- –25 to 71 °C ..... -7
- –40 to 71 °C ..... -9
- Other [1] ..... -0, -5, -6

Auxiliary functions and options:

- Inrush current limitation ..... E [2]
- Output voltage control input ..... R [3]
- Potentiometer (output voltage adjustment) ..... P [3]
- Undervoltage monitor (D0 – DD, to be specified) ..... D [4]
- ACFAIL signal (V2, V3, to be specified) ..... V [4]
- Current share ..... T
- Cooling plate standard case ..... B or B1
- Cooling plate for long case 220 mm [1] B2
- RoHS-compliant for all 6 substances ..... G

[1] Customer-specific models
[2] Option E mandatory for all -9 models
[3] Feature R excludes option P and vice versa.
[4] Option D excludes option V and vice versa; option V is available for 5.1 V models only.

Note: The sequence of options must follow the order above. This part number description is descriptive only; it is not inteded for creating part numbers.

NFND: Not for new designs

Preferred for new designs

Example: LS5540-9ERD3TB1G: Power factor corrected AC-DC converter, operating input voltage range 85 – 264 VAC, 2 electrically isolated outputs, each providing 15 V, 3.2 A, equipped with inrush current limiter, R-input to adjust the output voltages, undervoltage monitor D3, current share feature, a cooling plate B1, RoHS-compatibel.

Product Marking

Basic type designation, applicable approval marks, CE mark, warnings, pin designation, Power-One patents and company logo, identification of LEDs, test sockets, and potentiometer.

Specific type designation, input voltage range, nominal output voltages and currents, degree of protection, batch no., serial no., and data code including production site, modification status and date of production.

Functional Description

The input voltage is fed via an input fuse, an input filter, a rectifier, and an inrush current limiter to a boost converter. This step-up converter provides a sinusoidal input current (IEC/EN 61000-3-2, class D equipment) and charges the bulk capacitor C_i to approx. 370 VDC. This capacitor sources a single transistor forward converter and provides the power during the hold-up time.

Each output is powered by a separate secondary winding of the main transformer. The resultant voltages are rectified and their ripple smoothed by a power choke and an output filter. The control logic senses the main output voltage V_{o1} and generates, with respect to the maximum admissible output currents, the control signal for the switching transistor of the forward converter.

The second output of double output models is tracking to the main output, but has its own current limiting circuit. If the main output voltage drops due to current limitation, the second output voltage will fall as well and vice versa.

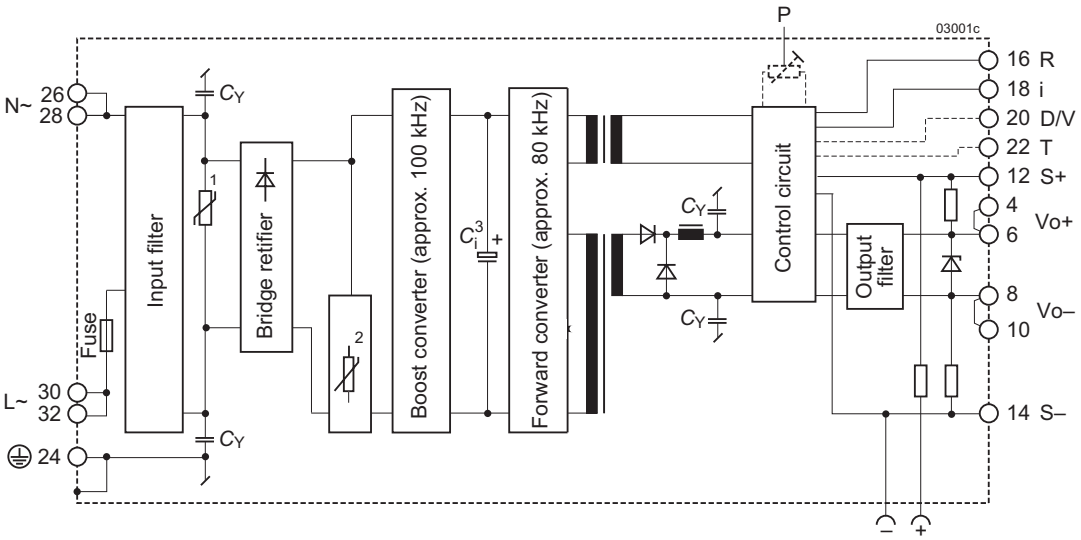


Fig. 1
Block diagram of single-output models

1 Transient suppressor (VDR)
2 Inrush current limiter (NTC, only models with $T_{A\,min}$ = –25 °C) or option E
3 Bulk capacitor C_b; bulk voltage approx. 370 V

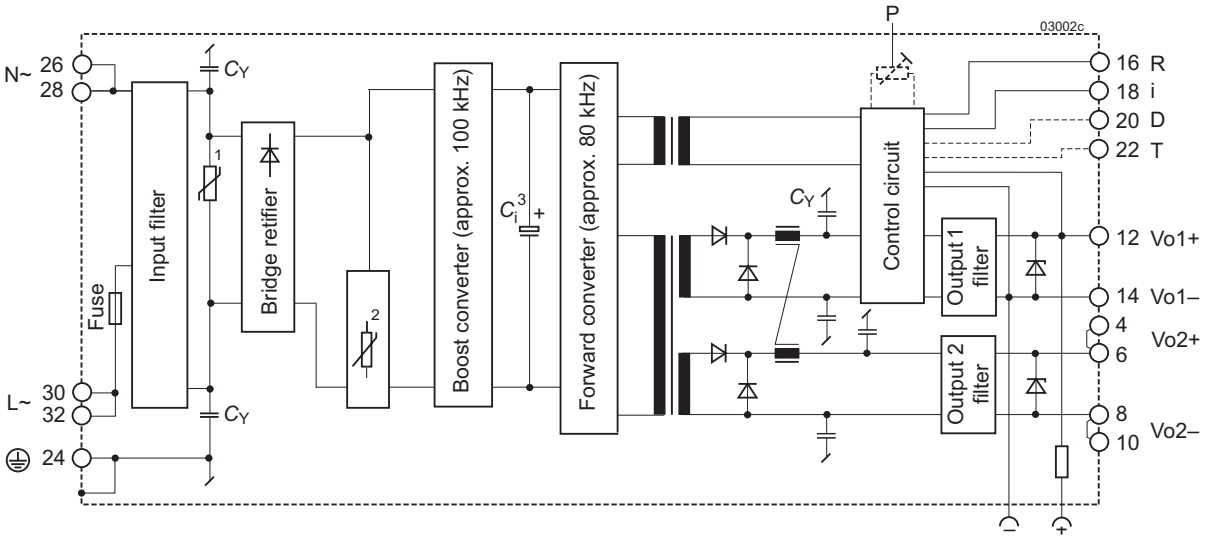


Fig. 2
Block diagram of double-output models

1 Transient suppressor (VDR)
2 Inrush current limiter (NTC, only models with $T_{A\,min}$ = –25 °C) or option E
3 Bulk capacitor C_b; bulk voltage approx. 370 V

Electrical Input Data

General Conditions
– T_A = 25 °C, unless T_C is specified.
– Pin 18 connected to pin 14, R input not connected, V_o adjusted to $V_{o\,nom}$ (option P)
– Sense line pins S+ and S– connected to Vo+ and Vo–, respectively.

Table 3: Input data

Input			LS			Unit
Characteristics		Conditions	min	typ	max	
V_i	Rated input voltage range	I_o = 0 – $I_{o\,nom}$ $T_{C\,min}$ – $T_{C\,max}$	100		240	VAC [1]
$V_{i\,op}$	Operating input voltage range		85		264	
$V_{i\,nom}$	Nominal input voltage	50 – 60 Hz		230		
I_i	Input current	$V_{i\,nom}$, $I_{o\,nom}$ [2]		0.55		A
P_{i0}	No-load input power	$V_{i\,min}$ – $V_{i\,max}$, I_o = 0		7.5	9	W
$P_{i\,inh}$	Idle input power	conv. inhibited		2	3	
R_i	Input resistance		480			mΩ
R_{NTC}	NTC resistance (see fig. 3) [3]	conv. not operating	3200	4000		
C_i	Input capacitance		80	100	120	µF
$V_{i\,RFI}$	Conducted input RFI	EN 55022 $V_{i\,nom}$, $I_{o\,nom}$		B		
	Radiated input RFI			B		
$V_{i\,abs}$	Input voltage limits without damage				283	VAC
			–400		400	VDC [4]

[1] Nominal frequency range: 50 – 60 Hz, operating frequency range 47 – 63 Hz
[2] With double-output models, both outputs loaded with $I_{o\,nom}$
[3] Valid for -7 versions without option E. This is the NTC resistance value at 25 °C and applies to cold converters. Subsequent switch-on/off cycles increase the inrush current peak value.
[4] Operation with DC input voltage is not specified and not recommended.

Input Transient Protection

A VDR together with the input fuse and a symmetrical input filter form an effective protection against high input transient voltages.

Input Fuse

A fuse mounted inside the converter in series to the phase line protects against severe defects. A second fuse in the neutral line may be necessary in certain applications; see *Installation Instructions.*

Fuse specification:

Slow-blow, 4 A, 250 V, 5 × 20 mm.

Input Under-/Overvoltage Lockout

If the input voltage remains below approx. 65 VAC or exceeds $V_{i\,abs}$, an internally generated inhibit signal disables the output(s). Do not check the overvoltage lockout function!

If V_i is below $V_{i\,min}$, but above the undervoltage lockout level, the output voltage may be below the value specified in the tables *Electrical Output Data.*

Inrush Current Limitation

The -7 models without option E incorporate an NTC resistor in the input circuitry, which at initial turn-on reduces the peak inrush current value by a factor of 5 to 10 to protect connectors and switching devices from damage. Subsequent switch-on cycles within short periods will cause an increase of the peak inrush current value due to the warming-up of the NTC resistor.

The inrush current peak value (initial switch-on cycle) can be determined by following calculation:

$$I_{inr\,p} = \frac{V_i \bullet \sqrt{2}}{(R_{s\,ext} + R_i + R_{NTC})}$$

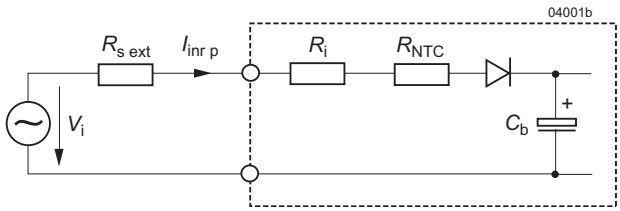


Fig. 3
Equivalent circuit diagram for input impedance.

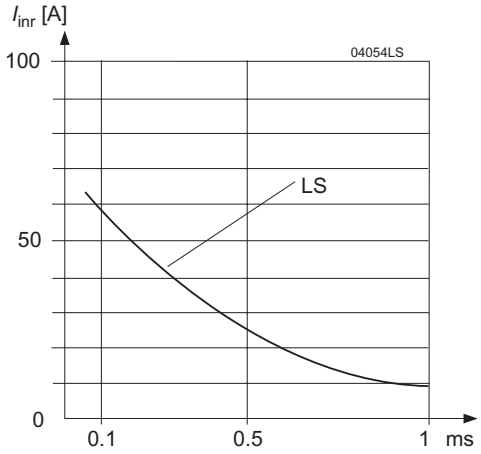


Fig. 4
Theoretical input inrush current versus time at V_i = 255 V and 115 V, R_{ext} = 0 for models without option E

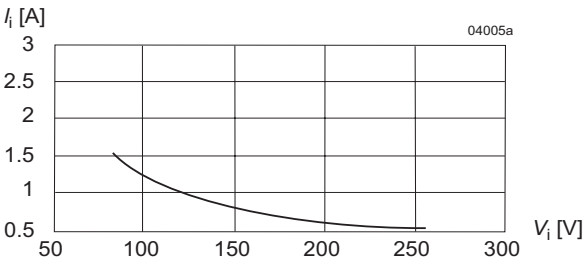


Fig. 5
Input current versus input voltage at $I_{o\ nom}$

Power Factor and Harmonics

Power factor correction is achieved by controlling the input current waveform synchronously with the input voltage waveform. The power factor control is active under all operating conditions.

The harmonic distortion is well below the limits specified in IEC/EN 61000-3-2, class D.

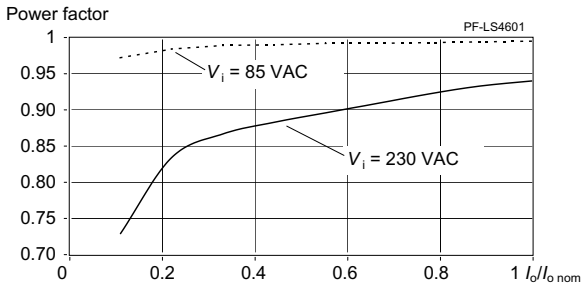


Fig. 6
Power factor versus output current (LS4601-7R)

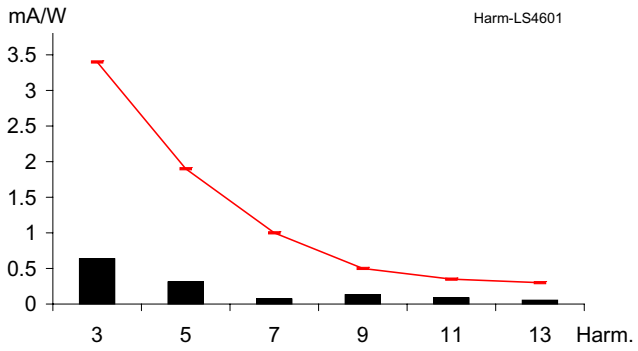


Fig. 7
Harmonic currents at the input (LS4601, V_i = 230 VAC, $I_o = I_{o\ nom}$).

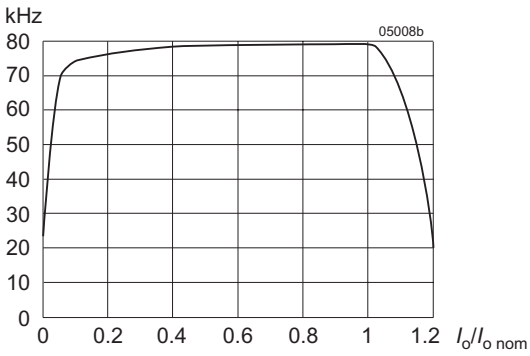


Fig. 8
Typ switching frequency versus load. The boost converter at the input stage operates with a constant switching frequency of 100 kHz.

Hold-up Time

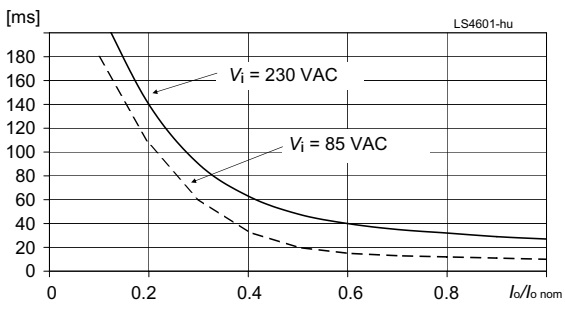


Fig. 9
Hold-up time versus output power (LS4601-7R)

Efficiency

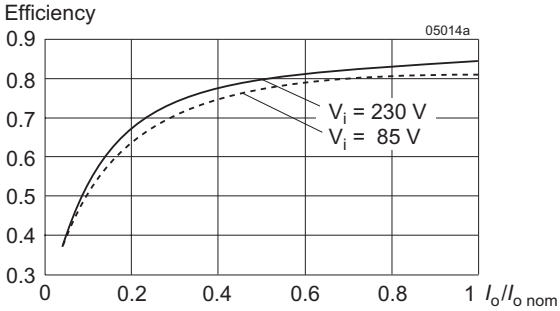


Fig. 10
Efficiency versus output power.

Electrical Output Data

General Conditions:
– T_A = 25 °C, unless T_C is specified.
– Pin 18 (i) connected to pin 14 (S– or Vo1–), R input not connected, V_o adjusted to $V_{o\,nom}$ (option P),
– Sense line pins 12 (S+) and 14 (S–) connected to pins 4 (Vo1+) and 8 (Vo1–), respectively.

Table 4a: Output data of single-output models

Output				LS4001 5.1 V			LS4301 / 4740[5] 12 V[5]			LS4501 15 V			LS4601 24 V			Unit
Characteristics			Conditions	min	typ	max	min	typ	max	min	typ	max	min	typ	max	
V_o	Output voltage		$V_{i\,nom}$, $I_{o\,nom}$	5.07		5.13	11.93[5]		12.07[5]	14.91		15.09	23.86		24.14	V
$V_{o\,BR}$	Overvoltage protection (supressor diode)[6]			7.6			15.2/17[5]			19.6			28.5			
$I_{o\,nom}$	Output current nom.[1]		$V_{i\,min}$ – $V_{i\,max}$ $T_{C\,min}$ – $T_{C\,max}$		16			8/7[5]			6.5			4.2		A
I_{oL}	Output current limit[1]		$V_{i\,min}$ – $V_{i\,max}$	16.2			8.2/8[5]			6.7			4.4			
v_o	Output noise[3]	Low frequency	$V_{i\,nom}$, $I_{o\,nom}$		2			2			2			2		mV_{pp}
		Switching frequ.	BW = 20 MHz		10			5			5			5		
		Total incl.spikes			50			40			40			40		
$\Delta V_{o\,u}$	Static line regulation with respect to $V_{i\,nom}$		$V_{i\,min}$ – $V_{i\,max}$ $I_{o\,nom}$			±5			±12			±15			±24	mV
$\Delta V_{o\,l}$	Static load regulation		$V_{i\,nom}$ (0.1 – 1) $I_{o\,nom}$			–20			–25			–30			–40	
$v_{o\,d}$	Dynamic load regulat.[2]	Voltage deviation[2]	$V_{i\,nom}$ $I_{o\,nom} \leftrightarrow {}^1/_2\, I_{o\,nom}$		±100			±100			±100			±100		
t_d		Recovery time[2]			0.3			0.4			0.4			0.3		ms
$\alpha_{v\,o}$	Temperature coefficient of output voltage[4]		$T_{C\,min}$ – T_{Cmax} $I_{o\,nom}$		±0.02			±0.02			±0.02			±0.02		%/K

[1] If the output voltages are increased above $V_{o\,nom}$ through R-input control, option P setting, remote sensing or option T, the output currents should be reduced accordingly so that $P_{o\,nom}$ is not exceeded.
[2] See *Dynamic load regulation (fig. 13)*
[3] Measured according to IEC/EN 61204 with a probe according to annex A
[4] For battery charger applications, a defined negative temperature coefficient can be provided by using a temperature sensor (see *Accessories)*, but we recommend choosing special battery charger models.
[5] Especially designed for battery charging using the temperature sensor (see *Accessories*). V_o is set to 12.84 V ±1% (R-input open).
[6] Breakdown voltage of the incorporated suppressor diode (1 mA; 10 mA for 5 V output). Exceeding $V_{o\,BR}$ is dangerous for the suppressor diode.

Table 4b: Output data of double-output models

Output				LS5320 2 × 12 V				LS5540 2 × 15 V				Unit
Characteristics			Conditions	Output 1			Output 2	Output 1			Output 2	
				min	typ	max	min typ max	min	typ	max	min typ max	
V_o	Output voltage		$V_{i\,nom}$, $I_{o\,nom}$ [1]	11.93		12.07	11.82 12.18	14.91		15.09	14.78 15.22	V
$V_{o\,P}$	Overvoltage protection (supressor diode) [8]			15.2			15.2	19.6			19.6	
$I_{o\,nom}$	Output current nom [2]		$V_{i\,min} - V_{i\,max}$ $T_{C\,min} - T_{C\,max}$	4			4	3.2			3.2	A
I_{oL}	Output current limit [6]		$V_{i\,min} - V_{i\,max}$	4.2			4.2	3.4			3.4	
uv_o	Output noise [3]	Low frequency	$V_{i\,nom}$, $I_{o\,nom}$	3			3	3			3	mV_{pp}
		Switching frequ.	BW = 20 MHz	12			12	10			10	
		Total incl.spikes		40			40	50			50	
$\Delta V_{o\,u}$	Static line regulation with respect to $V_{i\,nom}$		$V_{i\,min} - V_{i\,max}$ $I_{o\,nom}$			±12	[6]			±15	[6]	mV
$\Delta V_{o\,l}$	Static load regulation		$V_{i\,nom}$ (0.1 – 1) $I_{o\,nom}$			–40	[6]			–50	[6]	
$v_{o\,d}$	Dynamic load regulat.[3]	Voltage deviation [4]	$V_{i\,nom}$ $I_{o1\,nom} \leftrightarrow ½\, I_{o1\,nom}$	±100			±150	±100			±150	
t_d		Recovery time[4]	$½\, I_{o2\,nom}$	0.3				0.4				ms
$\alpha_{v\,o}$	Temperature coefficient of output voltage [5]		$T_{C\,min} - T_{C\,max}$ $I_{o\,nom}$	±0.02				±0.02				%/K

Table 4c: Output data of double-output models

Output				LS5660 / 5740[7] 2 × 24 V / 25.68 V[7]				Unit
Characteristics			Conditions	Output 1			Output 2	
				min	typ	max	min typ max	
V_o	Output voltage		$V_{i\,nom}$, $I_{o\,nom}$ [1]	23.86 [7]		24.14[7]	23.64 [7] 24.36[7]	V
$V_{o\,P}$	Overvoltage protection (supressor diode)			28.5/34[7]			28.5/34[7]	
$I_{o\,nom}$	Output current nom [2]		$V_{i\,min} - V_{i\,max}$ $T_{C\,min} - T_{C\,max}$	2/1.7[7]			2/1.7[7]	A
I_{oL}	Output current limit [6]		$V_{i\,min} - V_{i\,max}$	2.1/2[7]			2.1/2[7]	
uv_o	Output noise [3]	Low frequency	$V_{i\,nom}$, $I_{o\,nom}$	3			3	mV_{pp}
		Switching frequ.	BW = 20 MHz	5			5	
		Total incl.spikes		40			40	
$\Delta V_{o\,u}$	Static line regulation with respect to $V_{i\,nom}$ [3]		$V_{i\,min} - V_{i\,max}$ $I_{o\,nom}$			±30	[6]	mV
$\Delta V_{o\,l}$	Static load regulation		$V_{i\,nom}$ (0.1 – 1) $I_{o\,nom}$			–40	[6]	
$v_{o\,d}$	Dynamic load regulat.[3]	Voltage deviation [4]	$V_{i\,nom}$ $I_{o1\,nom} \leftrightarrow ½\, I_{o1\,nom}$	±100			±150	
t_d		Recovery time[4]	$½\, I_{o2\,nom}$	0.3				ms
$\alpha_{v\,o}$	Temperature coefficient of output voltage [5]		$T_{C\,min} - T_{C\,max}$ $I_{o\,nom}$	±0.02				%/K

1 Same conditions for both outputs
2 If the output voltages are increased above $V_{o\,nom}$ via R-input control, option P setting, remote sensing or option T, the output currents should be reduced accordingly so that $P_{o\,nom}$ is not exceeded.
3 Measured according to IEC/EN 61204 with a probe annex A
4 See *Dynamic load regulation (fig. 13)*
5 For battery charger applications a defined negative temperature coefficient can be provided by using a temperature sensor, see *Accessories.*
6 See *Output Voltage Regulation of Double-Output Models*
7 Especially designed for battery charging using the battery temperature sensor (see *Accessories*). V_{o1} is set to 25.68 V ±1% (R-input open).
8 Breakdown voltage of the incorporated suppressor diodes (1 mA). Exceeding $V_{o\,BR}$ is dangerous for the suppressor diodes.

Thermal Considerations

If a converter is located in free, quasi-stationary air (convection cooling) at the indicated maximum ambient temperature $T_{A\,max}$ (see table *Temperature specifications)* and is operated at its nominal input voltage and output power, the temperature measured at the *Measuring point of case temperature* T_C (see *Mechanical Data*) will approach the indicated value $T_{C\,max}$ after the warm-up phase. However, the relationship between T_A and T_C depends heavily on the conditions of operation and integration into a system. The thermal conditions are influenced by input voltage, output current, airflow, and temperature of surrounding components and surfaces. $T_{A\,max}$ is therefore, contrary to $T_{C\,max}$, an indicative value only.

Caution: The installer must ensure that under all operating conditions T_C remains within the limits stated in the table*Temperature specifications.*

Notes: Sufficient forced cooling or an additional heat sink allows T_A to be higher than 71 °C (e.g. 85 °C), if $T_{C\,max}$ is not exceeded.

For -7 or -9 models at an ambient temperature T_A of 85 °C with only convection cooling, the maximum permissible current for each output is approx. 40% of its nominal value as per the figure below.

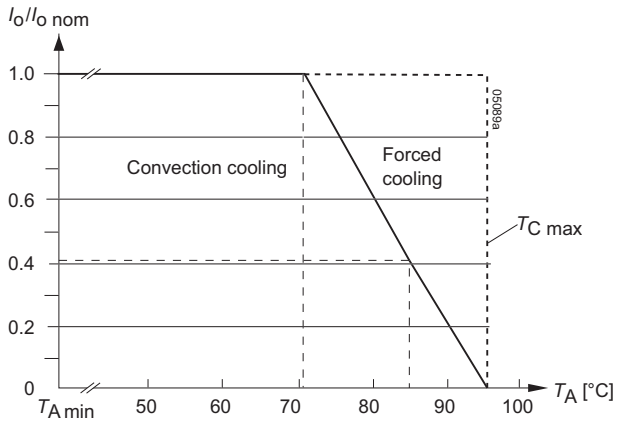


Fig. 11
Output current derating versus temperature for -7 and -9 models.

Thermal Protection

A temperature sensor generates an internal inhibit signal, which disables the outputs if the case temperature exceeds $T_{C\,max}$. The outputs are automatically re-enabled, when the temperature drops below this limit.

It is recommended that continuous operation under simultaneous extreme worst-case conditions of the following three parameters be avoided: Minimum input voltage, maximum output power, and maximum temperature.

Output Protection

Each output is protected by a suppressor diode against overvoltage, which could occur due to a failure of the control circuit. In such a case, the suppressor diode becomes a short circuit. The suppressor diodes may smooth short overvoltages resulting from dynamic laod changes, but they are not designed to withstand externally applied overvoltages.

A short circuit at any of the two outputs will cause a shut-down of the other output. A red LED indicates an overload condition.

Note: $V_{o\,BR}$ is specified in *Electrical Output Data*. If this voltage is exceeded, the suppressor diode generates losses and may become a short circuit.

Parallel or Series Connection of Converters

Single or double-output models with equal output voltage can be connected in parallel using option T (current sharing). If the T pins are interconnected, all converters share the output current equally.

Single-output models and/or main and second outputs of double-output models can be connected in series with any other (similar) output.

Notes:

- Parallel connection of double-output models should always include both, main and second output to maintain good regulation.
- Not more than 5 converters should be connected in parallel.
- Series connection of second outputs without involving their main outputs should be avoided, as regulation may be poor.
- The maximum output current is limited by the output with the lowest current limitation, if several outputs are connected in series.

Output Voltage Regulation

The following figures apply to single-output or double-output models with parallel-connected outputs.

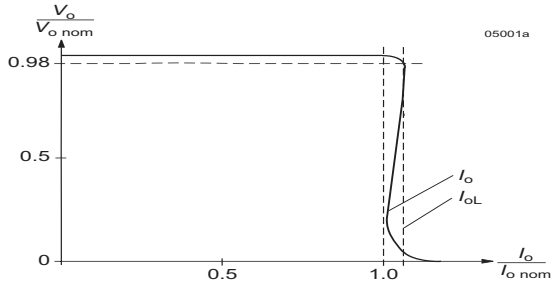


Fig. 12
Typ output characteristic V_{o1} versus I_{o1}.

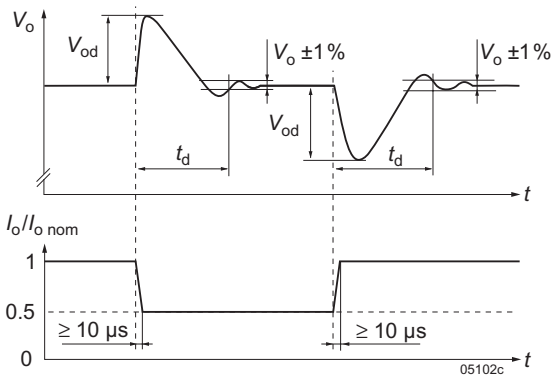


Fig. 13
Typical dynamic load regulation of V_o.

Output Regulation of Double-Output Models

Output 1 is under normal conditions regulated to $V_{o\,nom}$, independent of the output currents.

V_{o2} depends upon the load distribution. If both outputs are loaded with more than 10% of $I_{o\,nom}$, the deviation of V_{o2} remains within ±5% of the value of V_{o1}. The following 3 figures show the regulation with varying load distribution.

Two outputs of an LS5000 model connected in parallel will behave like the output of an LS4000 model.

Note: If output 2 is not used, we recommend connecting it in parallel with output 1. This ensures good regulation and efficiency.

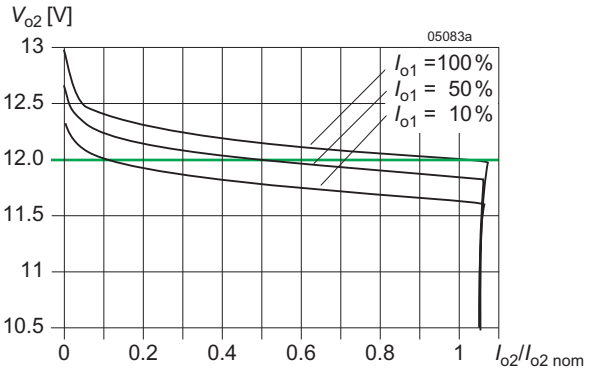


Fig. 14
LS5320: ΔV_{o2} versus I_{o2} with various I_{o1} (typ).

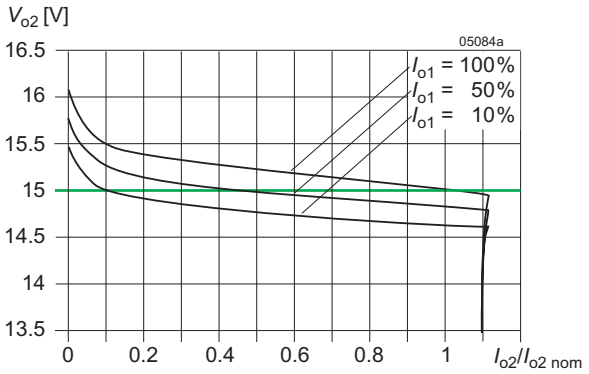


Fig. 15
LS5540: V_{o2} versus I_{o2} with various I_{o1} (typ).

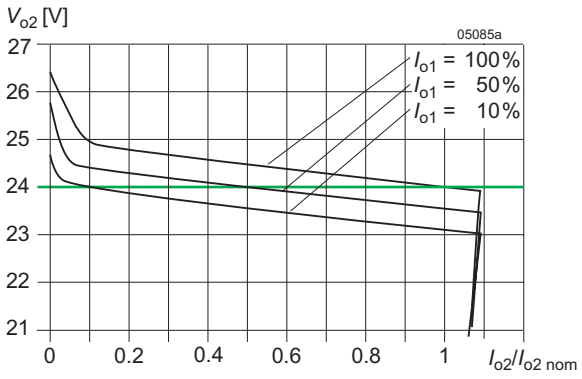


Fig. 16
LS5660: V_{o2} versus I_{o2} with various I_{o1} (typ).

Auxiliary Functions

Inhibit for Remote On and Off

The outputs may be enabled or disabled by means of a logic signal (TTL, CMOS, etc.) applied between the inhibit input i (pin 18) and pin 14 (S– or Vo1–). In systems with several converters, this feature can be used to control the activation sequence of the converters. If the inhibit function is not required, connect the inhibit pin 18 to pin 14.

Note: If pin 18 is not connected, the output is disabled.

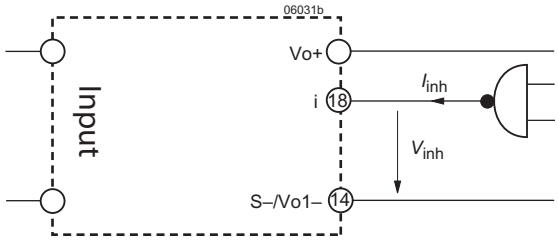


Fig. 17
Definition of V_{inh} and I_{inh}.

Table 5: Inhibit characteristics

Characteristic			Conditions	min	typ	max	Unit
V_{inh}	Inhibit voltage	V_o = on	$V_{i\,min} - V_{i\,max}$	–50		0.8	V
		V_o = off		2.4		50	
I_{inh}	Inhibit current		V_{inh} = 0			–400	µA
t_r	Rise time				30		ms
t_f	Fall time		depending on I_o				

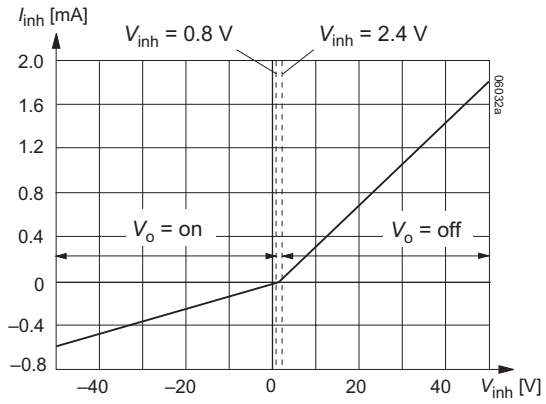


Fig. 18
Typical inhibit current I_{inh} versus inhibit voltage V_{inh}

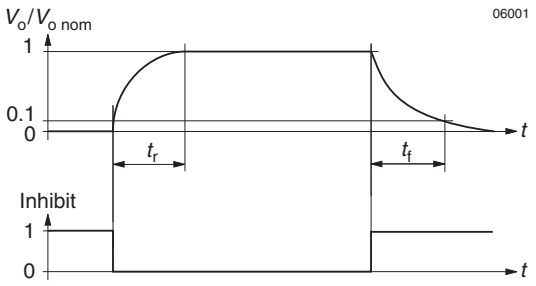


Fig. 19
Output response as a function of inhibit control

Sense Lines (Single-Output Models)

Important: Sense lines must always be connected! Incorrectly connected sense lines may activate the overvoltage protection resulting in a permanent short-circuit of the output.

This feature allows for compensation of voltage drops across the connector contacts and if necessary, across the load lines. We recommend connecting the sense lines directly at the female connector.

To ensure correct operation, both sense lines (S+, S–) should be connected to their respective power outputs (Vo+ and Vo–). The voltage difference between any sense line and its respective power output (as measured on the connector) should not exceed the following values:

Table 6: Maximum voltage compensation allowed using sense lines

Output voltage	Total voltage difference between sense lines and their respective outputs	Voltage difference between Vo– and S–
5.1 V	<0.5 V	<0.25 V
12 V, 15 V, 24 V	<1.0 V	<0.25 V

Note: If the output voltages are increased above $V_{o\,nom}$ via R-input control, option P setting, remote sensing, or option T, the output currents must be reduced accordingly, so that $P_{o\,nom}$ is not exceeded.

Programmable Output Voltage (R-Function)

As a standard feature, the converters offer an adjustable output voltage, identified by letter R in the type designation. The control input R (pin 16) accepts either a control voltage V_{ext} or a resistor R_{ext} to adjust the desired output voltage. When R is not connected, the output voltage is set to $V_{o\ nom}$.

a) Adjustment by means of an external control voltage V_{ext} between pin 16 (R) and pin 14:

The control voltage range is 0 – 2.75 V and allows an output voltage adjustment in the range of approximately 0 – 110% $V_{o\ nom}$.

$$V_{ext} \approx \frac{V_o}{V_{o\ nom}} \bullet 2.5\ V$$

b) Adjustment by means of an external resistor:

Depending upon the value of the required output voltage the resistor shall be connected

either: Between pin 16 and pin 14 ($V_o < V_{o\ nom}$) to achieve an output voltage adjustment range of approx. 0 – 100% $V_{o\ nom}$.

or: Between pin 16 and pin 12 ($V_o > V_{o\ nom}$) to achieve an output voltage adjustment range of approx. 100 – 110% $V_{o\ nom}$.

Warning:

- V_{ext} shall never exceed 2.75 V.
- The value of R'_{ext} shall never be less than the lowest value as indicated in table R'_{ext} (for $V_0 > V_{0\ nom}$) to prevent the converter from damage!

Notes:

- The R-Function excludes option P (output voltage adjustment by potentiometer).

  If the output voltages are increased above $V_{o\ nom}$ via R-input control, option P setting, remote sensing or option T, the output current(s) should be reduced accordingly so that $P_{o\ nom}$ is not exceeded.
- With double-output models the second output follows the value of the controlled main output.
- In case of parallel connection the output voltages should be individually set within a tolerance of 1 – 2%.

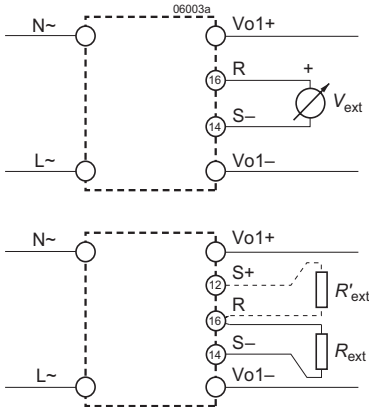


Fig. 20
Output voltage control for single-output models LS 4000

Table 7a: R_{ext} for $V_o < V_{o\ nom}$; approximate values ($V_{i\ nom}$, $I_{o\ nom}$, series E 96 resistors); R'_{ext} = not fitted

$V_{o\ nom}$ = 5.1 V		$V_{o\ nom}$ = 12 V			$V_{o\ nom}$ = 15 V			$V_{o\ nom}$ = 24 V		
V_o [V]	R_{ext} [kΩ]	V_o [V] [1]		R_{ext} [kΩ]	V_o [V] [1]		R_{ext} [kΩ]	V_o [V] [1]		R_{ext} [kΩ]
0.5	0.432	2	4	0.806	2	4	0.619	4	8	0.81
1.0	0.976	3	6	1.33	4	8	1.47	6	12	1.33
1.5	1.65	4	8	2	6	12	2.67	8	16	2
2.0	2.61	5	10	2.87	8	16	4.53	10	20	2.87
2.5	3.83	6	12	4.02	9	18	6.04	12	24	4.02
3.0	5.76	7	14	5.62	10	20	8.06	14	28	5.62
3.5	8.66	8	16	8.06	11	22	11	16	32	8.06
4.0	14.7	9	18	12.1	12	24	16.2	18	36	12.1
4.5	30.1	10	20	20	13	26	26.1	20	40	20
5.0	200	11	22	42.2	14	28	56.2	22	44	44.2

Table 7b: R'_{ext} for $V_o > V_{o\ nom}$; approximate values ($V_{i\ nom}$, $I_{o\ nom}$, series E 96 resistors); R_{ext} = not fitted

$V_{o\ nom}$ = 5.1 V		$V_{o\ nom}$ = 12 V			$V_{o\ nom}$ = 15 V			$V_{o\ nom}$ = 24 V		
V_o [V]	R'_{ext} [kΩ]	V_o [V] [1]		R'_{ext} [kΩ]	V_o[V][1]		R'_{ext} [kΩ]	V_o [V] [1]		R'_{ext} [kΩ]
5.15	432	12.1	24.2	1820	15.2	30.4	1500	24.25	48.5	3320
5.2	215	12.2	24.4	931	15.4	30.8	768	24.5	49.0	1690
5.25	147	12.3	24.6	619	15.6	31.2	523	24.75	49.5	1130
5.3	110	12.4	24.8	475	15.8	31.6	392	25.0	50.0	845
5.35	88.7	12.5	25.0	383	16.0	32.0	316	25.25	50.5	698
5.4	75	12.6	25.2	316	16.2	32.4	267	25.5	51.0	590
5.45	64.9	12.7	25.4	274	16.4	32.8	232	25.75	51.5	511
5.5	57.6	12.8	25.6	243	16.5	33.0	221	26.0	52.0	442
		13.0	26.0	196				26.25	52.5	402
		13.2	26.4	169				26.4	52.8	383

[1] First column: V_o or V_{o1}; second column: double-output models with outputs in series connection

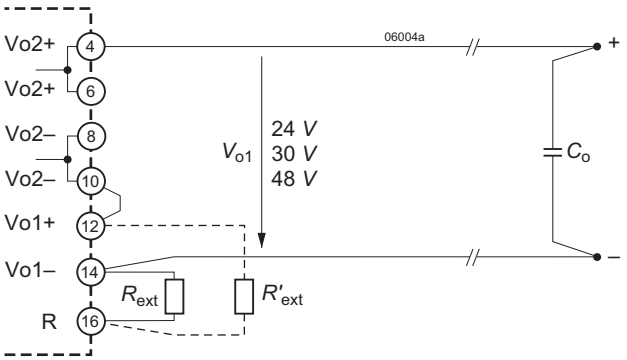


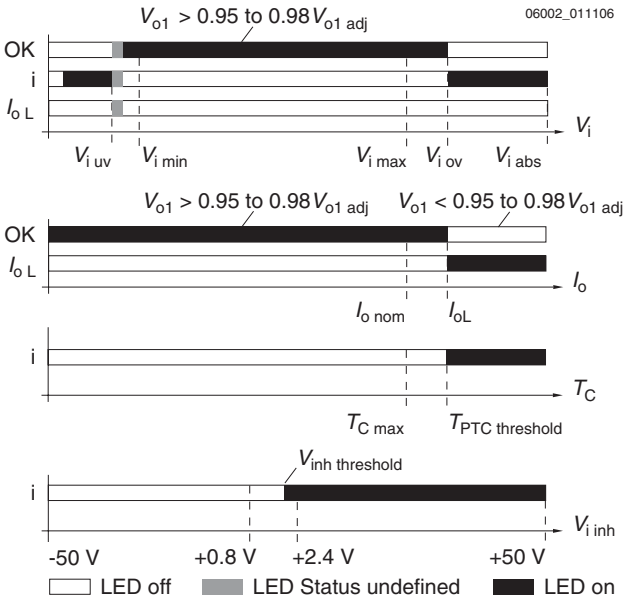
Fig. 21
Double-output models: R-input for output voltage control. Wiring for output voltage 24 V, 30 V ,or 48 V with both outputs connected in series. A ceramic capacitor (C_o) across the load reduces ripple and spikes.

Test Jacks

Test jacks (pin diameter 2 mm) for measuring the main output voltage V_o or V_{o1} are located at the front of the converter. The positive test jack is protected by a series resistor (see *Functional Description, block diagrams*).

The voltage measured at the test jacks is slightly lower than the value at the output terminals.

Display Status of LEDs



LEDs "OK", "i" and "$I_{o\ L}$" status versus input voltage
Conditions: $I_o \le I_{o\ nom}$, $T_C \le T_{C\ max}$, $V_{inh} \le 0.8$ V
$V_{i\ uv}$ = undervoltage lock-out, $V_{i\ ov}$ = overvoltage lockout

LEDs "OK" and "$I_{o\ L}$" status versus output current
Conditions: $V_{i\ min} - V_{i\ max}$, $T_C \le T_{C\ max}$, $V_{inh} \le 0.8$ V

LED "i" versus case temperature
Conditions: $V_{i\ min} - V_{i\ max}$, $I_o \le I_{o\ nom}$, $V_{inh} \le 0.8$ V

LED "i" versus V_{inh}
Conditions: $V_{i\ min} - V_{i\ max}$, $I_o \le I_{o\ nom}$, $T_C \le T_{C\ max}$

Fig. 22
LED indicators

Battery Charging/Temperature Sensor

The LS series converters are suitable for battery charger applications. For an optimum battery charging and life expectancy of the battery an external temperature sensor can be connected to the R-input. The sensor is mounted as close as possible to the battery pole and adjusts the output voltage according to the battery temperature.

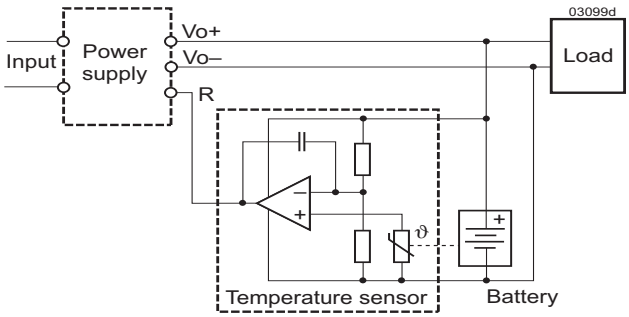


Fig. 23
Connection of a temperature sensor

Depending upon cell voltage and the temperature coefficient of the battery, different sensor types are available, see *Accessories*.

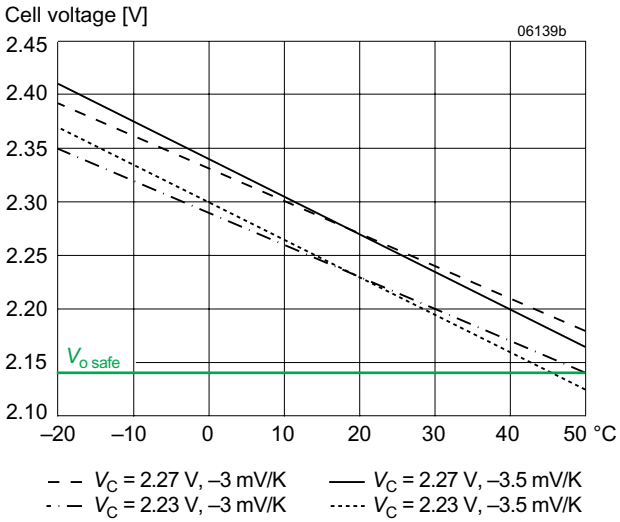


Fig. 24
Trickle charge voltage versus temperature for defined temperature coefficient.

Electromagnetic Compatibility (EMC)

A metal oxide VDR together with an input fuse and an input filter form an effective protection against high input transient voltages, which typically occur in most installations. The S Series has been successfully tested to the following specifications:

Immunity

Table 11: Electromagnetic immunity (type tests)

Phenomenon	Standard	Level	Coupling mode [1]	Value applied	Waveform	Source imped.	Test procedure	In oper.	Perf. crit. [2]
Electrostatic discharge (to case)	IEC / EN 61000-4-2	4	contact discharge	8000 V_p	1/50 ns	330 Ω 150 pF	10 positive and 10 negative discharges	yes	A
			air discharge	15000 V_p					
Electromagnetic field	IEC / EN 61000-4-3	3	antenna	10 V/m	AM 80% /1 kHz	n.a.	80 – 1000 MHz	yes	A
			antenna	20 V/m 10 V/m 5 V/m	AM 80% /1 kHz	n.a.	800 – 1000 MHz 1400 – 2100 MHz 2100 – 2500 MHz	yes	A
		3	antenna	10 V/m	50% duty cycle, 200 Hz rep. rate	n.a.	900 ±5 MHz pulse modul.	yes	A
Electrical fast transients/burst	IEC / EN 61000-4-4	3	capacitive, o/c	±2000 V_p	bursts of 5/50 ns 2.5/5 kHz over 15 ms; burst period: 300 ms	50 Ω	60 s positive 60 s negative transients per coupling mode	yes	A
			±i/c, +i/–i direct						
Surges	IEC / EN 61000-4-5	3	±i/c	±2000 V_p	1.2/50 µs	12 Ω	5 pos. and 5 neg. surges per coupling mode	yes	A
			+i/–i	±1000 V_p		2 Ω			
Conducted disturbances	IEC / EN 61000-4-6	3	i, o, signal wires	10 VAC (140 dBmV)	AM 80% 1 kHz	150 Ω	0.15 – 80 MHz sine wafe	yes	A
Power frequency magnetic field	IEC / EN 61000-4-8	3	--	100 A/m			60 s in all 3 axis	yes	A
Pulse magnetic field	IEC / EN 61000-4-9	-	--	±300 A/m			5 pulses per axis repetit. rate 10 s	yes	B

[1] i = input, o = output, c = case
[2] A = Normal operation, no deviation from specifications, B = Temporary loss of function or deviation from specs possible
[3] For converters with version V102 or higher. Older LKP models meet only B.
[4] Only LKP models have been tested.

Emissions

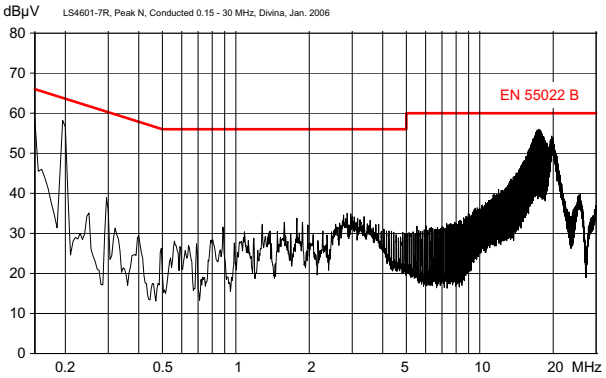


Fig. 25
Conducted emissions (peak) at the neutral input according to EN 55011/22, measured at $V_{i\ nom}$ and $I_{o\ nom}$ (LS4601-6R). The line input performs quite similar.

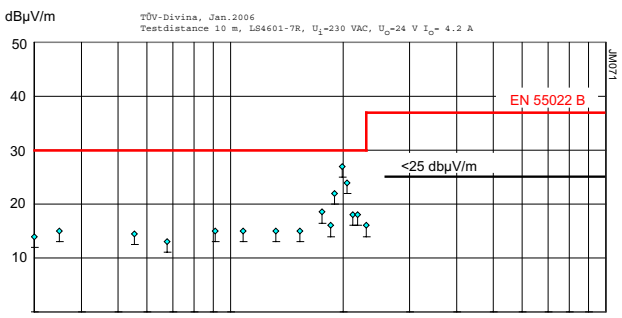


Fig. 26
Typ. radiated emissions accord. to EN 55011/22, antenna 10 m distance, measured at $V_{i\ nom}$ and $I_{o\ nom}$ (LS4601-7R).

Environmental Conditions

Table 9: Mechanical and climatic stress

Test Method		Standard	Test Conditions		Status
Cab	Damp heat steady state	IEC/EN 60068-2-78:2001 MIL-STD-810D sect. 507.2	Temperature: Relative humidity: Duration:	40 $^{\pm 2}$ °C 93 $^{+2/-3}$ % 56 days	Converter not operating
Ea	Shock (half-sinusoidal)	IEC/EN 60068-2-27:1987 MIL-STD-810D sect. 516.3	Acceleration amplitude: Bump duration: Number of bumps:	100 g_n = 981 m/s^2 6 ms 18 (3 each direction)	Converter operating
Eb	Bump (half-sinusoidal)	IEC/EN 60068-2-29:1987 MIL-STD-810D sect. 516.3	Acceleration amplitude: Bump duration: Number of bumps:	40 g_n = 392 m/s^2 6 ms 6000 (1000 each direction)	Converter operating
Fc	Vibration (sinusoidal)	IEC/EN 60068-2-6:1995 MIL-STD-810D sect. 514.3	Acceleration amplitude: Frequency (1 Oct/min): Test duration:	0.35 mm (10 – 60 Hz) 5 g_n = 49 m/s^2 (60 – 2000 Hz) 10 – 2000 Hz 7.5 h (2.5 h each axis)	Converter operating
Fh	Random vibration broad band (digital control)	IEC/EN 60068-2-64	Acceleration spectral density: Frequency band: Acceleration magnitude: Test duration:	0.05 g_n^2/Hz 8 – 500 Hz 4.9 $g_{n\ rms}$ 1.5 h (0.5 h each axis)	Converter operating
Kb	Salt mist, cyclic (sodium chloride NaCl solution)	IEC/EN 60068-2-52:1996	Concentration: Duration: Storage: Storage duration: Number of cycles:	5% (30 °C) 2 h per cycle 40 °C, 93% rel. humidity 22 h per cycle 3	Converter not operating

Temperatures

Table 10: Temperature specifications, values given are for an air pressure of 800 – 1200 hPa (800 – 1200 mbar)

Temperature			Option -7		Standard -9		Unit
Characteristics		Conditions	min	max	min	max	
T_A	Ambient temperature	Converter operating	–25	71	–40	71	°C
T_C	Case temperature [1]		–25	95	–40	95	
T_S	Storage temperature	Not operational	–40	100	–55	100	

[1] Overtemperature lockout at T_C > 95 °C

Reliability

Table 11: MTBF calculated according to MIL-Hdbk 217F

Values at specified case temperature	Model	Ground benign 40 °C	Ground fixed 40 °C	Ground fixed 70 °C	Ground mobile 50 °C	Unit
MTBF	LS 4000/5000	514 000	88 000	38 000	35 000	h

Mechanical Data

Dimensions in mm. The converters are designed to be inserted into a 19" rack, 160 mm long, according to IEC 60297-3.

European Projection

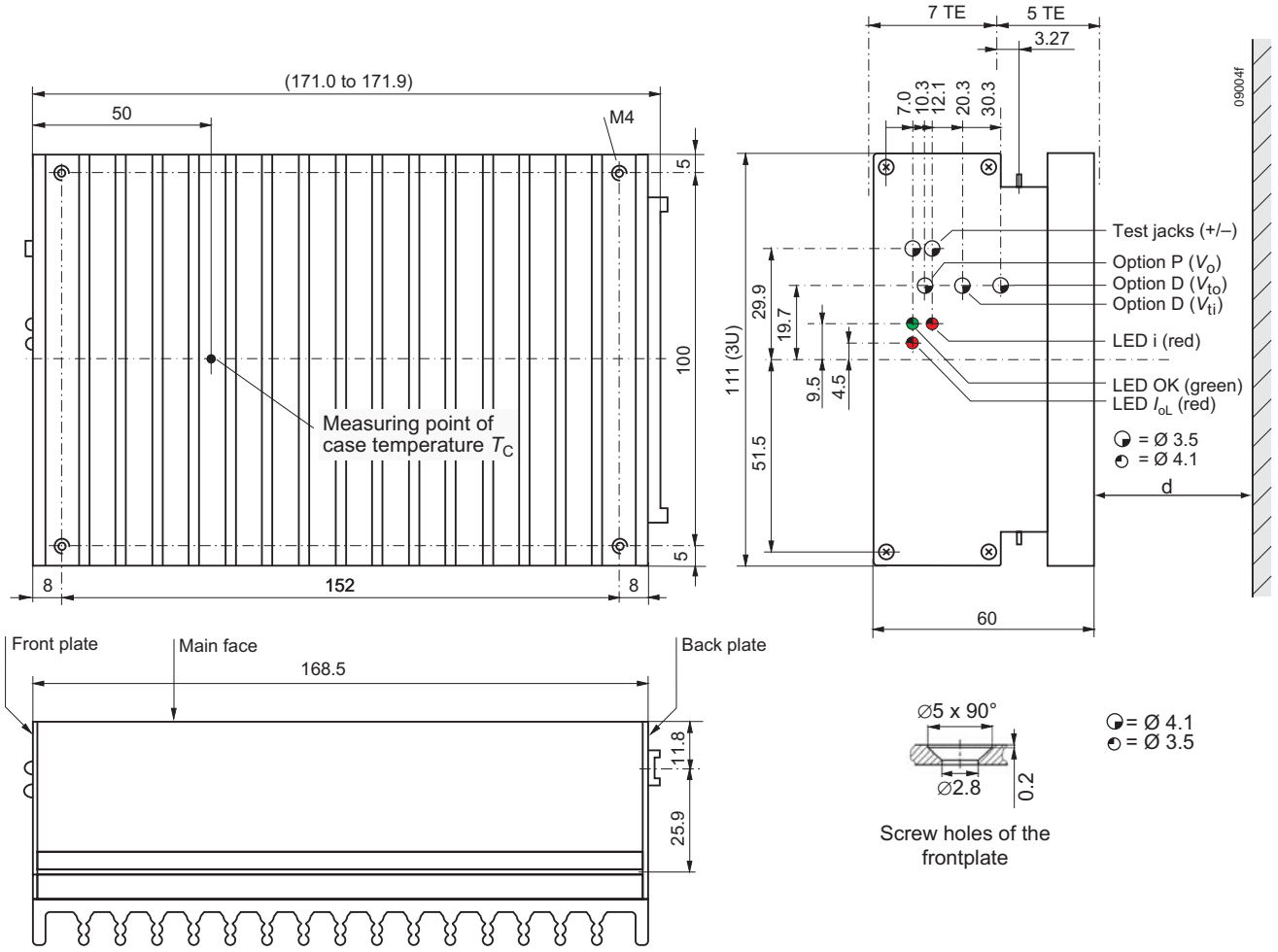


Fig. 27
Aluminum case S02 with heat sink; black finish (EP powder coated); weight approx. 1.25 kg

Notes:

- d ≥ 15 mm, recommended minimum distance to next part in order to ensure proper air circulation at full output power.
- free air location: the converter should be mounted with fins in a vertical position to achieve maximum airflow through the heat sink.

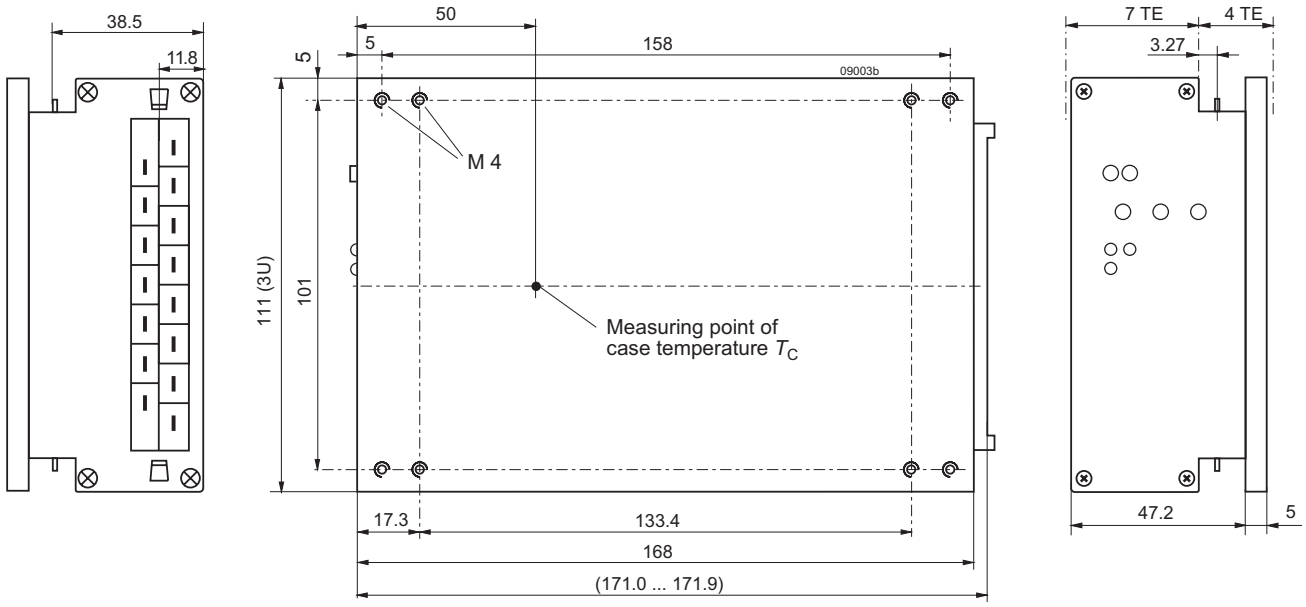


Fig. 28
Option B1: Aluminium case S02 with small cooling plate; black finish (EP powder coated).
Suitable for mounting with access from the backside.
Total weight approx. 1.2 kg.

European Projection

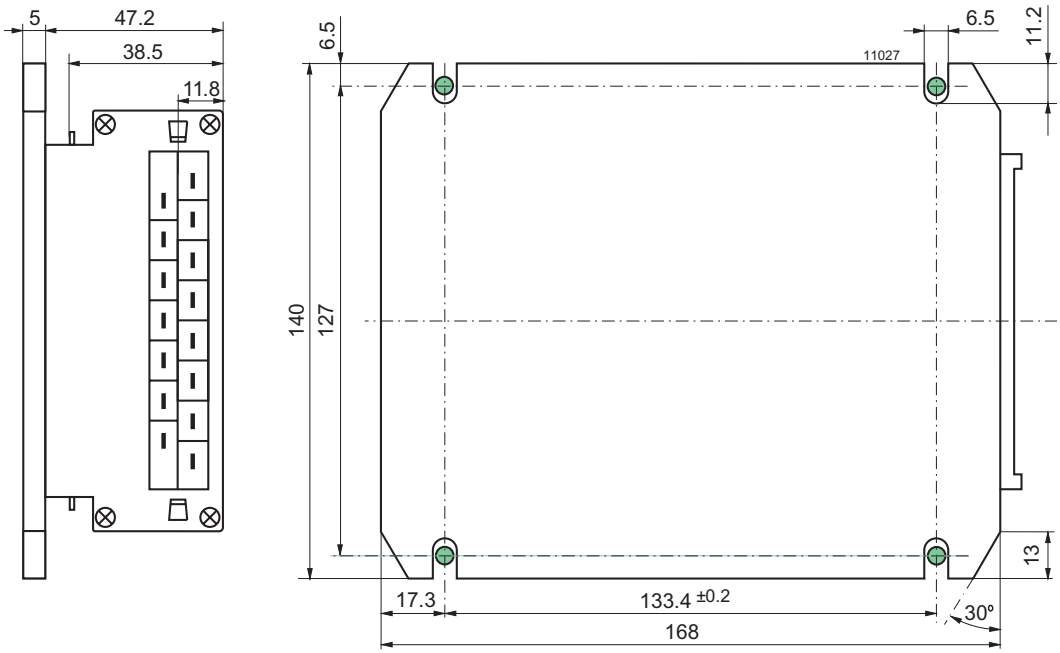


Fig. 29
Option B: Aluminium case S02 with large cooling plate; black finish (EP powder coated).
Suitable for front mounting.
Total weight approx. 1.3 kg

Note: Long case with option B2, elongated by 60 mm for 220 mm rack depth, is available on request. (No LEDs, no test jacks.)

Safety and Installation Instructions

Connector Pin Allocation

The connector pin allocation table defines the electrical potentials and the physical pin positions on the H15 connector. The protective earth is connected trough a leading pin (no. 24), ensuring that it makes contact with the female connector first.

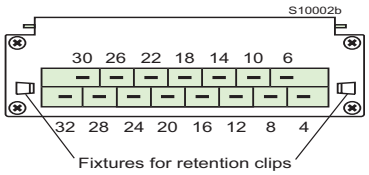


Fig. 30
View of converter's male connector, type H15

Table 12: Pin allocation

Pin no.	Connector type H15			
	LS4000		LS5000	
4	Vo1+	Positive output	Vo2+	Pos. output 2
6				
8	Vo1–	Negative output	Vo2–	Neg. output 2
10				
12	S+	Sense+	Vo1+	Output 1
14	S–	Sense–	Vo1–	Output 1
16	R [1]	Control of V_{o1}	R [1]	Control of V_{o1}
18	i	Inhibit	i	Inhibit
20	D [3]	Save data	D [3]	Save data
	V [3]	ACFAIL		
22	T [4]	Current share	T [4]	Current share
24 [2]		Protective earth	⏚	Protective earth
26	N~	Neutral line	N~	Neutral line
28				
30	L~	Phase line	L~	Phase line
32				

[1] Not connected, if option P is fitted
[2] Leading pin (pre-connecting)
[3] Option D excludes option V and vice versa. Pin is not connected, if neither option D or V is fitted.
[4] Not connected, unless option T is fitted.

Installation Instructions

Important: These products have a power factor correction (PFC) and are intended to replace the LS1000 and LS2000 series converters, in order to comply with IEC/EN 61000-3-2.

Switch off the system and check for hazardous voltages before altering any connection!

These converters are components, intended exclusively for inclusion within other equipment by an industrial assembly operation or by professional installers. The installation must strictly follow the national safety regulations in compliance with the enclosure, mounting, creepage, clearance, casualty, markings, and segregation requirements of the end-use application.

Connection to the system shall be made via the female connector H15 (see *Accessories*). Other installation methods may not meet the safety requirements.

Pin no. 24 (⏚) is reliably connected with the case. For safety reasons, it is essential to connect this pin reliably to protective earth. See *Safety of Operator-Accessible Output Circuits*.

The phase input 30/32 (L~) is connected via a built-in fuse (see *Input Fuse*), which is designed to protect in the case of a converter failure. An additional external fuse, suitable for the application, might be necessary in the wiring to the other line input 26/28 (N~) if:

- Local requirements demand an individual fuse in each source line
- Neutral and earth impedance is high or undefined
- Phase and neutral of the mains are not defined or cannot be assigned to the corresponding terminals (L~ to phase and N~ to neutral).

Notes:

– If the inhibit function is not used, pin no. 18 (i) should be connected to pin no. 14 (S–/Vo1–) to enable the output(s).

– Do not open the converters, or warranty will be invalidated.

– Due to high current values, the converters provide two internally parallel contacts for certain paths (pins 4/6, 8/10, 26/28 and 30/32). It is recommended to connect load and supply to both female connector pins of each path in order to keep the voltage drop low and to not overstress the connector contacts with high currents.

– If the second output of double-output models is not used, connect it parallel with the main output.

Make sure that there is sufficient airflow available for convection cooling. This should be verified by measuring the case temperature, when the converter is installed and operated in the end-use application. See *Thermal Considerations.*

Ensure that a converter failure (e.g., by an internal short-circuit) does not result in a hazardous condition. See also *Safety of Operator-Accessible Output Circuit.*

Standards and Approvals

The converters are safety-approved to EN/IEC 60950-1, and UL/CSA 60950-1 2nd Ed. (version 106 or greater).

The converters correspond to Class I equipment and have been evaluated for:

- Building-in
- Basic insulation between input and case based on 250 VAC, and double or reinforced insulation between input and output(s).
- Functional insulation between outputs.
- Overvoltage category II

Table 13: Isolation

Characteristic		Input to case and output(s)	Output(s) to case	Output 1 to output 2	Unit
Electric strength test	Factory test >1 s	2.8 [1]	1.4	0.15	kVDC
	AC test voltage equivalent to factory test	2.0	1.0	0.1	kVAC
Insulation resistance at 500 VDC		>300	>300	>100 [2]	MΩ
Creapage distances		≥ 3.2 [3]	--	--	mm

[1] According to IEC/EN 60950, subassemblies connecting input to output are pre-tested with 5.6 kVDC or 4 kVAC.
[2] Tested at 150 VDC
[3] Input to outputs: 6.4 mm

- Pollution degree 2 environment
- Max. altitude: 2000 m.
- The converters fulfill the requirements of a fire enclosure.

All boards of the converters are coated with a protective lacquer.

The converters are subject to manufacturing surveillance in accordance with the above mentioned UL standards and ISO 9001:2008. CB-scheme is available.

Protection Degree and Cleaning Liquids

Condition: Female connector fitted to the converter.

- IP 30: All models except those with option P, and except those with option D or V including a potentiometer.
- IP 20: All models fitted with option P, or with option D or V with potentiometer.

In order to avoid possible damage, any penetration of cleaning fluids is to be prevented.

Isolation and Leakage Currents

The electric strength test is performed in the factory as routine test in accordance with EN 50514 and IEC/EN 60950. The company will not honor warranty claims resulting from incorrectly performed electric strength field tests.

Leakage currents flow due to internal leakage capacitances and Y-capacitors. The current values are proportional to the supply voltage and are specified in the table below.

Table 14: Leakage currents

Characteristic		Class I	Unit
Maximum earth leakage current	Permissible according to IEC/EN 60950	3.5	mA
	Typ. value at 254 V, 50 Hz (LS models)	0.8	

Railway Applications and Fire Protection

The converters have been designed by observing the railway standards EN 50155 and EN 50121-4. All boards are coated with a protective lacquer.

The converters with version V108 (or later) comply with NF-F16 (I2/F1). They also accord to EN 45545-1, EN 45545-2 (2013), if installed in a technical compartment or cabinet.

Safety of Operator-Accessible Output Circuit

If the output circuit of an converter is operator-accessible, it shall be an SELV circuit according to IEC/EN 60950 .

The table below shows a possible installation configuration, compliance with which causes the output circuit of an S Series AC-DC converter to be an SELV circuit according to IEC/EN 60950 up to a configured output voltage of 36 V (sum of nominal output voltages connected in series) .

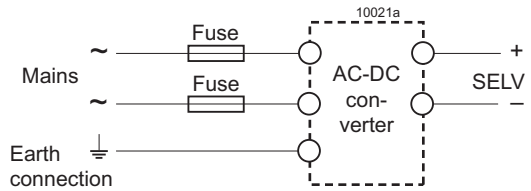


Fig. 31
Schematic safety concept.

Table 15: Safety concept leading to an SELV output circuit

Conditions	AC-DC converter	Installation	Result
Nominal voltage	Grade of insulation between input and output provided by the AC-DC converter	Measures to achieve the resulting safety status of the output circuit	Safety status of the AC-DC converter output circuit
Mains ≤ 250 VAC	Double or reinforced	Earthed case[1] and installation according to the applicable standards	SELV circuit

[1] The earth connection has to be provided by the installer according to the relevant safety standards, e.g. IEC/EN 60950.

Description of Options

Table 16: Survey of options

Option	Function of option	Characteristic
-7, -7E	Extended operational ambient temperature range	T_A = –25 to 71 °C
E	Electronic inrush current limitation circuitry	Active inrush current limitation, standard feature for T_A = –40 °C
P [2]	Potentiometer for fine adjustment of output voltage	Adjustment range +10/–60% of $V_{o\ nom}$, excludes R input
D[1]	Input and/or output undervoltage monitoring circuitry	Safe data signal output (D0 – DD)
V[1]	Input and/or output undervoltage monitoring circuitry	ACFAIL signal according to VME specifications (V0, V2, V3)
T	Current sharing	Interconnect T-pins if paralleling outputs (max 5 converters)
B, B1, B2	Cooling plate (160 or 220 mm long)	Replaces standard heat sink, allowing direct chassis-mounting
G	RoHS-compliant for all six substances	G is always the last character in the type designation

[1] Option D excludes option V and vice versa; option V only for 5.1 V outputs.
[2] Option P is not available for battery charger models.

--7 Restricted Temperature Range

Option -7 and -7E stand for a restricted operational ambient temperature range of –25 to 71 °C rather than –40 to 71 °C.

E Inrush Current Limitation

The converters exhibit an electronic circuit replacing the standard built-in NTC, in order to achieve an enhanced inrush current limiting function (standard feature).

Note: Subsequent switch-on cycles at start-up are limited to max. 10 cycles during the first 20 seconds (cold converter) and then to max. 1 cycle every 8 s.

Table 17: Inrush current characteristics with option E

Characteristics V_i = 230 VAC		LS typ	LS max	Unit
$I_{inr\ p}$	Peak inrush current	–	25.3	A
t_{inr}	Inrush current duration	35	50	ms

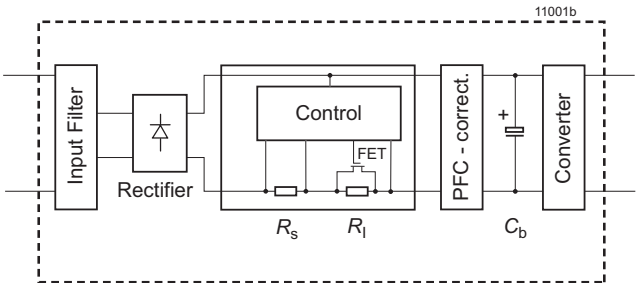


Fig. 32
Option E block diagram

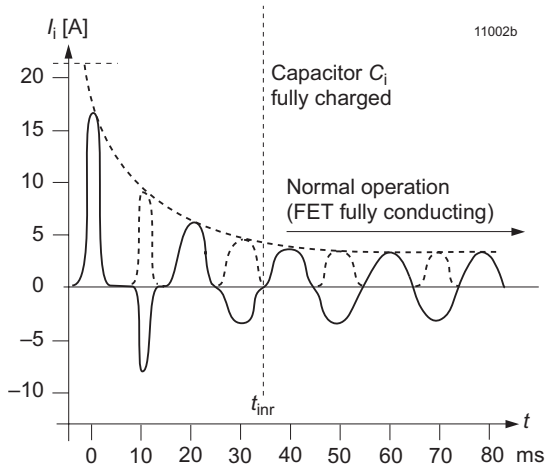


Fig. 33
Inrush current with option E
V_i = 230 VAC, f_i = 50 Hz, P_o = $P_{o\ nom}$

P Potentiometer

A potentiometer provides an output voltage adjustment range of +10/–60% of $V_{o\ nom}$. It is accessible through a hole in the front cover. Option P is not available for battery charger models and is not recommended for converters connected in parallel.

Option P excludes the R-function. With double-output models,both outputs are influenced by the potentiometer setting (doubling the voltage, if the outputs are in series).

If the output voltages are increased above $V_{o\ nom}$ via R input control, option P setting, remote sensing or option T, the output current(s) should be reduced accordingly, so that $P_{o\ nom}$ is not exceeded.

T Current Sharing

This option ensures that the output currents are approximately shared between all parallel-connected converters, hence increasing system reliability. To use this facility, simply interconnect the T pins of all converters and make sure that the reference for the T signal, pin 14 (S– or the Vo1–), are also connected together. The load lines should have equal length and cross section to ensure equal voltage drops.

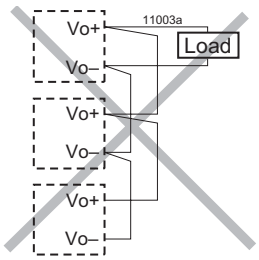
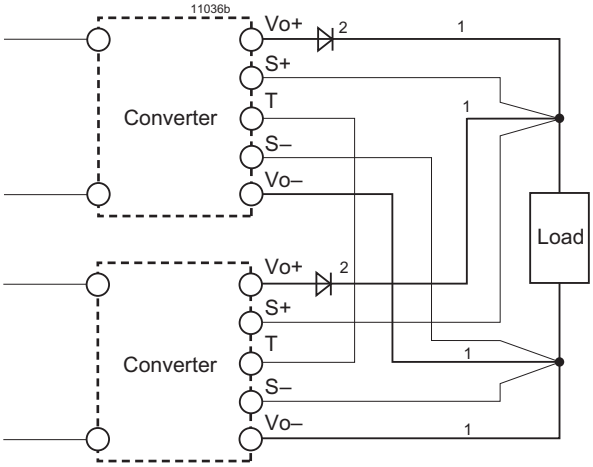


Fig. 34
An example of poor wiring for connection in parallel

Not more than 5 converters should be connected in parallel. The R pins should be left open-circuit. If not, the output voltages must be individually adjusted prior to paralleling within 1 to 2% or the R pins should be connected together.

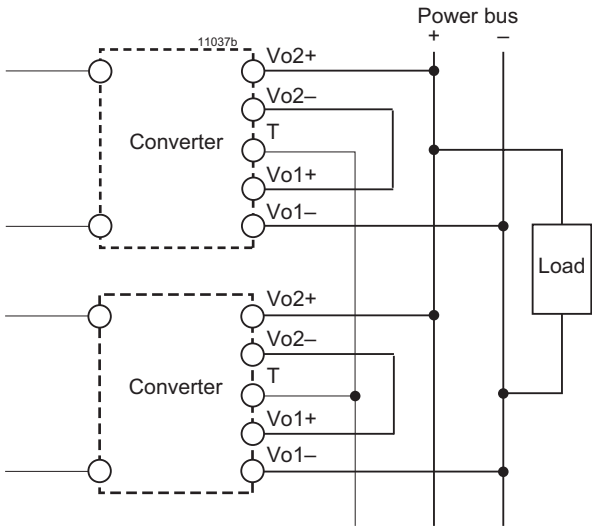
Parallel connection of converters with option P is not recommended.



Max. 5 converters in parallel connection

[1] Lead lines should have equal length and cross section, and should run in the same cable loom.
[2] Diodes recommended in redundant operation only

Fig. 35
Paralleling of single-output models using option T with the sense lines connected at the load



Max. 5 converters in parallel connection

Fig. 36
Paralleling of double-output models with the outputs connected in series, and using option T with power bus. Note that the signal at the T pins is referenced to Vo1–.

Table 18: Undervoltage monitoring functions

Output type JFET	Output type NPN	Monitoring V_b [4]	Monitoring V_o/V_{o1}	Minimum adjustment range of threshold level V_t V_{tb} [4]	Minimum adjustment range of threshold level V_t V_{to}	Typical hysteresis V_{ho} [% of V_t] for $V_{t\,min} - V_{t\,max}$ V_{ho}
D1	D5	no	yes	-	3.5 – V_{BR} [1]	2.5 – 0.6 V
D2	D6	yes	no	355 VDC	-	-
D3	D7	yes	yes	355 VDC	(0.95 – 0.985 V_{o1}) [2]	"0"
D4	D8	no	yes	-	(0.95 – 0.985 V_{o1}) [2]	"0"
D0	D9	no	yes	-	3.5 – V_{BR} [3]	2.5 – 0.6 V
		yes	yes	355 VDC	3.5 – V_{BR} [3]	2.5 – 0.6 V
	DD	yes	yes	355 VDC	3.5 – V_{BR} [1]	2.5 – 0.6 V

[1] Threshold level adjustable by potentiometer. See *Output Data* for V_{BR}.
[2] Fixed value. Tracking if V_{o1} is adjusted via R-input, option P, or sense lines.
[3] The threshold level permanently adjusted according to customer specification ±2% at 25 °C. Any value within the specified range is basically possible, but causes a special type designation in addition to the standard option designations (D0/D9).
[4] V_b is the voltage generated by the boost regulator. When V_b drops below 355 V, the D signal triggers, and the output(s) will remain powered during nearly the full hold-up time t_h.

D Undervoltage Monitor

The input and/or output undervoltage monitoring circuit operates independently of the built-in input undervoltage lockout circuit. A logic "low" (self conducting JFET) or "high" signal (NPN output) is generated at the D output (pin 20), when one of the monitored voltages drops below the preselected threshold level V_t. This signal is referenced to S–/Vo1–. The D output recovers, when the monitored voltages exceed $V_t + V_h$. The threshold level V_{bi} is adjusted in the factory. The threshold level V_{to} is either adjusted by a potentiometer accessible through a hole in the front cover, or adjusted in the factory to a fixed value specified by the customer.

Option D exists in various versions D0 – DD, as shown in the table below.

JFET output (D0 – D4):

Pin D is internally connected via the drain-source path of a JFET (self-conducting type) to the negative potential of output 1. $V_D \leq 0.4$ V (logic low) corresponds to a monitored voltage level (V_i and/or V_{o1}) $< V_t$. The current I_D through the JFET should not exceed 2.5 mA. The JFET is protected by a 0.5 W Zener diode of 8.2 V against external overvoltages.

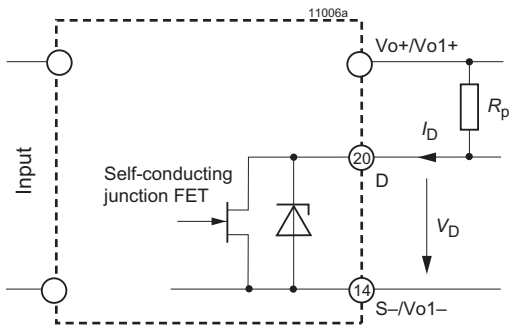


Fig. 37
Option D0 – D4: JFET output, $I_D \leq 2.5$ mA

Table 19: JFET output (D0 – D4)

V_b, V_{o1} status	D output, V_D
V_b or $V_{o1} < V_t$	low, L, $V_D \leq 0.4$ V at $I_D = 2.5$ mA
V_b and $V_{o1} > V_t + V_h$	high, H, $I_D \leq 25$ µA at $V_D = 5.25$ V

NPN output (D5 – DD):

Pin D is internally connected via the collector-emitter path of a NPN transistor to the negative potential of output 1. $V_D < 0.4$ V (logic low) corresponds to a monitored voltage level (V_i and/or V_{o1}) $> V_t + V_h$. The current I_D through the open collector should not exceed 20 mA. The NPN output is not protected against external overvoltages. V_D should not exceed 40 V.

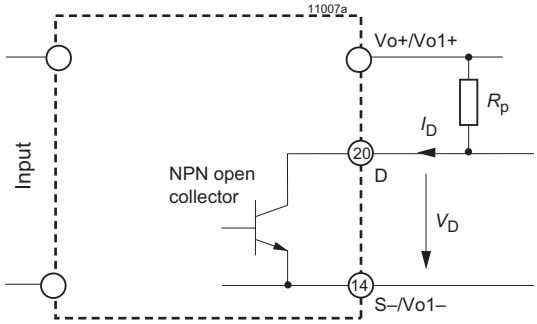


Fig. 38
Option D5 – DD: NPN output, $V_{o1} \leq 40$ V, $I_D \leq 20$ mA

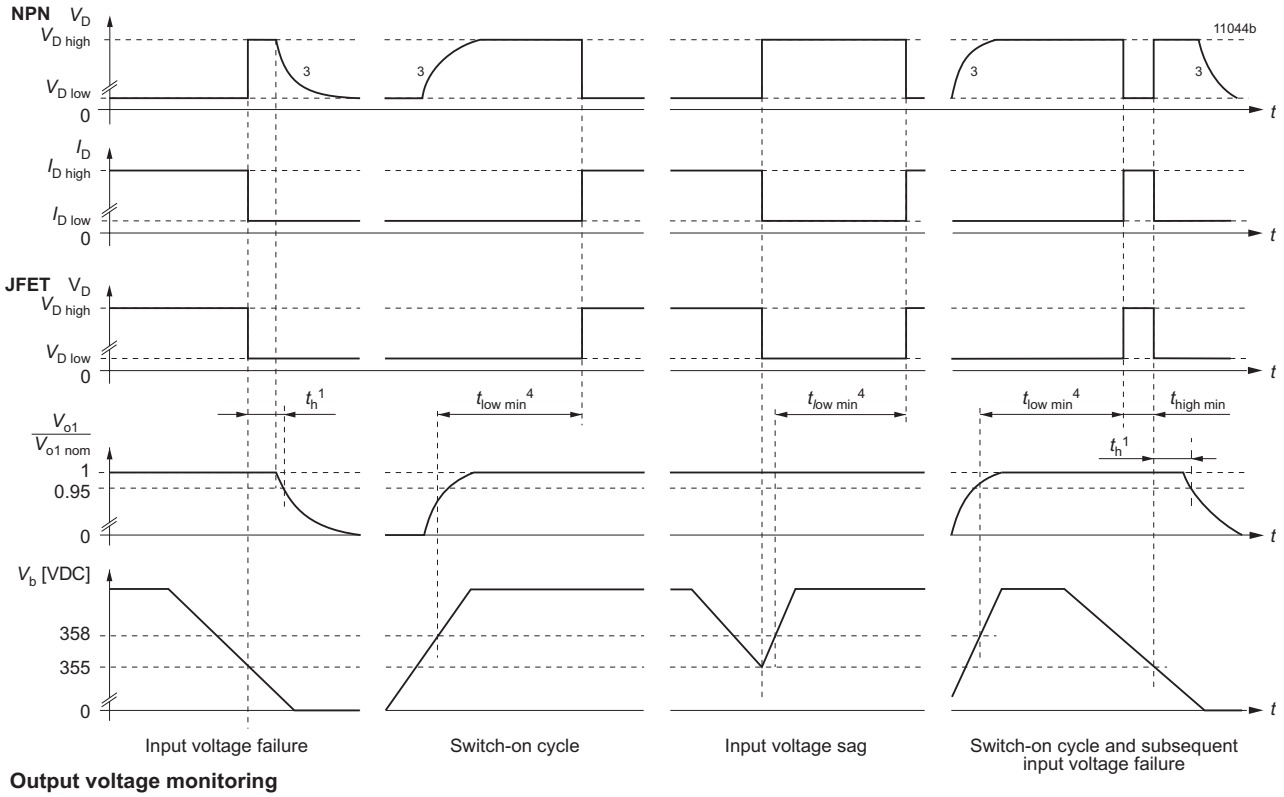
Table 20: JFET output (D5 – DD)

V_b, V_{o1} status	D output, V_D
V_b or $V_{o1} < V_t$	high, H, $I_D \leq 25$ µA at $V_D = 40$ V
V_b and $V_{o1} > V_t + V_h$	low, L, $V_D \leq 0.4$ V at $I_D = 20$ mA

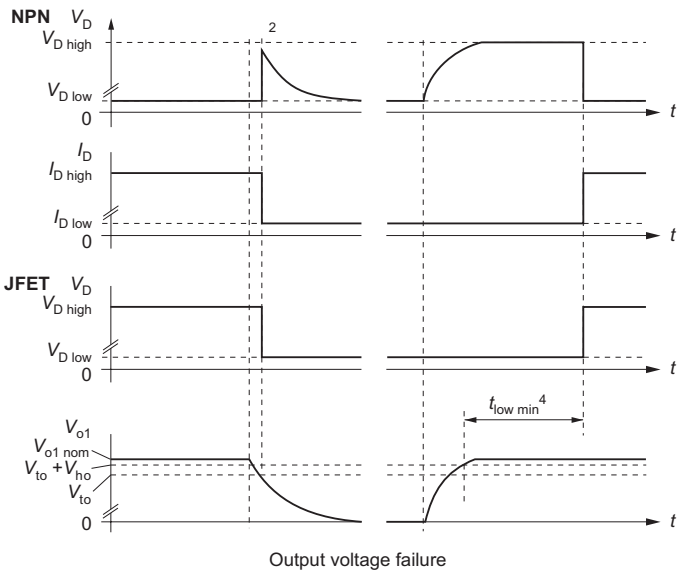
Table 21: D-output logic signals

Version of D	$V_b < V_t$ resp. $V_o < V_t$	$V_b > V_t + V_h$ resp. $V_o > V_t$	Configuration
D1, D2, D3, D4, D0	low	high	JFET
D5, D6, D7, D8, D9, DD	high	low	NPN

Input voltage monitoring



Output voltage monitoring



1 Hold-up time see: *Electrical Input Data.*
2 With output voltage monitoring, hold-up time $t_h = 0$.
3 The signal remains high, if the D output is connected to an external source.
4 $t_{low\,min}$ = 100 – 170 ms, typically 130 ms.

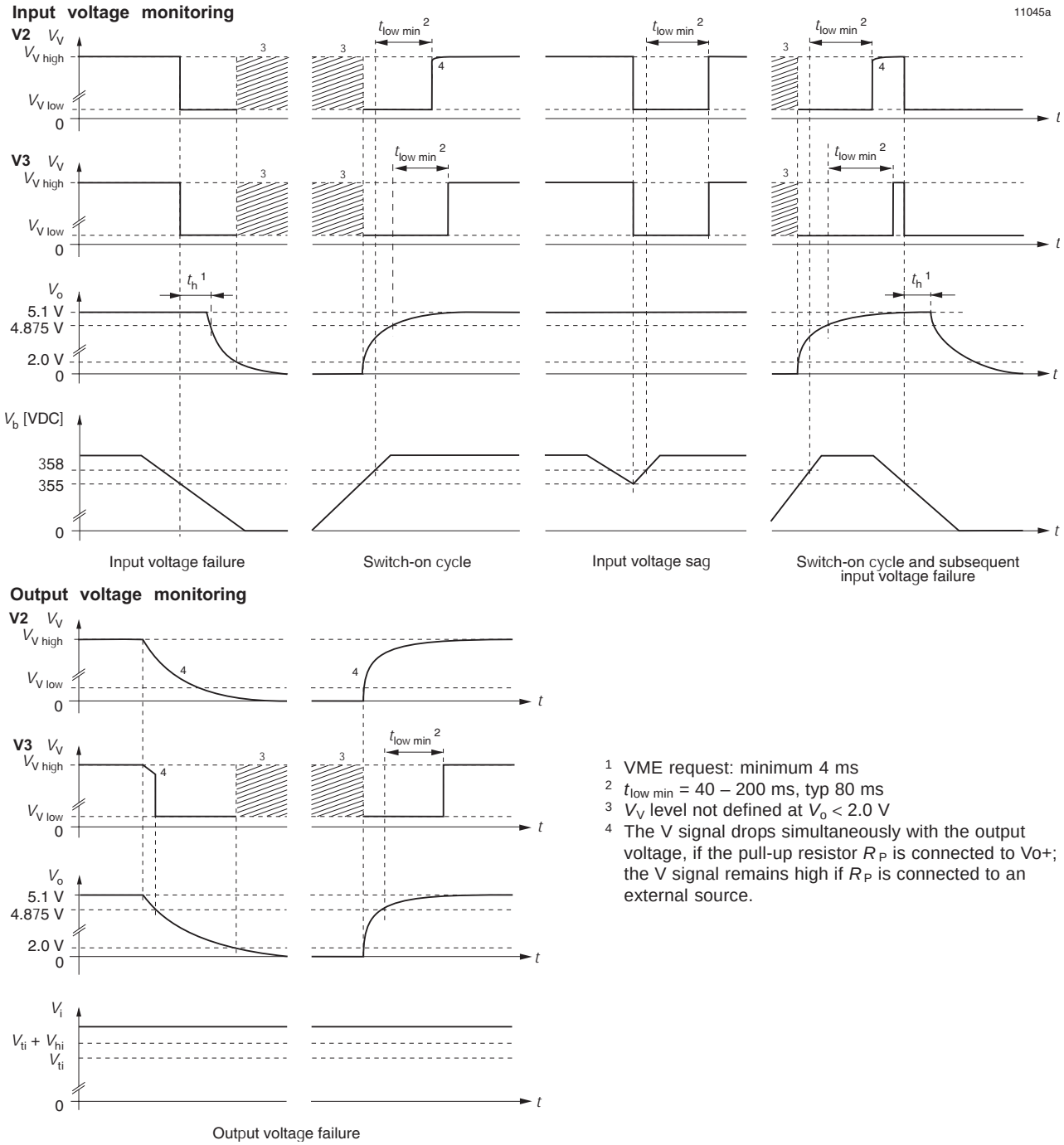
Fig. 39
Relationship between V_b, V_{o1}, V_D, $V_{o1}/V_{o1\,nom}$ versus time

V ACFAIL Signal (VME)

Available only for models with V_o = 5.1 V.

This option defines an undervoltage monitoring circuit for the input and main output voltage. It generates the ACFAIL signal (V signal) according to the VME standard.

The low state level of the ACFAIL signal is specified at a sink current of $I_V \leq 48$ mA to $V_V \leq 0.6$ V (open-collector output of an NPN transistor). The pull-up resistor feeding the open-collector output should be placed on the VME backplane.



1 VME request: minimum 4 ms
2 $t_{low\,min}$ = 40 – 200 ms, typ 80 ms
3 V_V level not defined at V_o < 2.0 V
4 The V signal drops simultaneously with the output voltage, if the pull-up resistor R_P is connected to Vo+; the V signal remains high if R_P is connected to an external source.

Fig. 40
V_{cb}, V_o, V_V, I_V, $V_o/V_{o\,nom}$ versus time.

After the ACFAIL signal has gone low, the VME standard requires a hold-up time t_h of at least 4 ms before the 5.1 V output drops at full load to 4.875 V. This hold-up time t_h is provided by the capacitance supporting the boost voltage V_b. See *Hold-up Time.*

Table 22: Undervoltage monitor functions

V output (VME compatible)	Monitoring V_b	Monitoring V_{o1}	Minimum adjustment range of threshold level V_{tb}	Minimum adjustment range of threshold level V_{to}
V2	yes	no	355 VDC [1]	–
V3	yes	yes	355 VDC [1]	0.95 – 0.985 V_{o1} [2]

[1] Option V monitors V_b generated by the boost regulator. The trigger level is adjusted in the factory to 355 VDC.
[2] Fixed value between 95% and 98.5% of V_{o1}

Option V operates independently of the built-in input undervoltage lockout circuit. A logic "low" signal is generated at pin 20, as soon as one of the monitored voltages drops below the preselected threshold level V_t. The return for this signal is S– or Vo1–. The V output recovers, when the monitored voltage(s) exceed(s) $V_t + V_h$. The threshold level V_{to} is adjusted in the factory to a customer-specified value.

V-output (V2, V3):

Connector pin V is internally connected with the open collector of an NPN transistor. The emitter is connected with S– or Vo1–. $V_V \leq 0.6$ V (logic low) corresponds to a monitored voltage level (V_i and/or V_o) $< V_t$. The current I_V through the open collector should not exceed 50 mA. The NPN output is not protected against external overvoltages. V_V should not exceed 60 V.

Table 23: Status of V output

V_b, V_o status	V output, V_V
V_b or $V_o < V_t$	low, L, $V_V \leq 0.6$ V at $I_V = 50$ mA
V_b and $V_{o1} > V_t + V_h$	high, H, $I_V \leq 25$ µA at $V_V = 5.1$ V

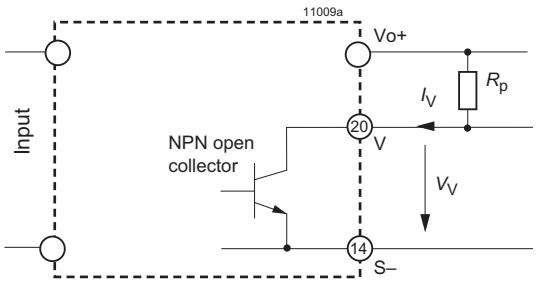


Fig. 41
Output configuration of options V2 and V3

B, B1, B2 Cooling Plate

Where a cooling surface is available, we recommend the use of a cooling plate instead of the standard heat sink. The mounting system should ensure sufficient cooling capacity to guarantee that the maximum case temperature $T_{C\,max}$ is not exceeded. The cooling capacity is calculated by:

$$P_{Loss} = \frac{(100\% - \eta)}{\eta} \bullet V_o \bullet I_o$$

Efficiency η see *Model Selection*

For the dimensions of the cooling plates, see *Mechnical Data*. Option B2 is for customer-specific models with elongated case (for 220 mm DIN-rack depth).

G RoHS

Models with G as last character of the type designation are RoHS-compliant for all six substances.

Accessories

A variety of electrical and mechanical accessories are available including:

– Front panels for 19" DIN-rack: Schroff or Intermas, 12 TE /3U; see fig. 42.
– Mating H15 connectors with screw, solder, faston, or press-fit terminals, code key system and coding wedges HZZ00202-G; see fig. 43.
– Pair of connector retention clips HZZ01209-G; see fig. 44
– Connector retention brackets HZZ01216-G; see fig. 45.
– Cage clamp adapter HZZ00144-G; see fig. 46
– Different cable hoods for H15 connectors (fig. 47):
  - HZZ00141-G, screw version
  - HZZ00142-G, use with retention brackets HZZ01218-G
  - HZZ00143-G, metallic version providing fire protection

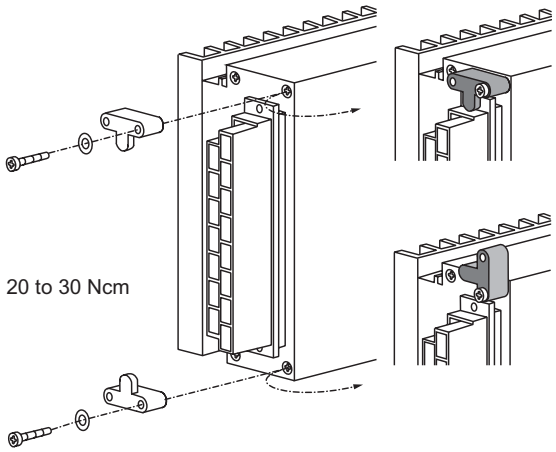


Fig. 45
Connector retention brackets HZZ01216-G (CRB-HKMS)

Fig. 42
Different front panels

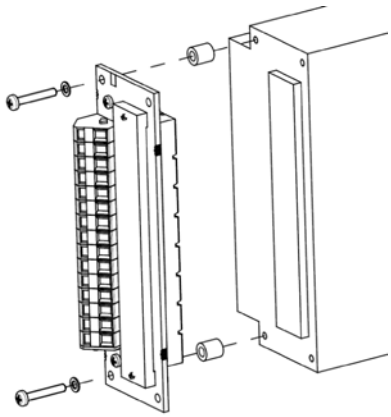


Fig. 46
Cage clamp adapter HZZ00144-G

Fig. 43
Different mating connectors

Fig. 47
Different cable hoods

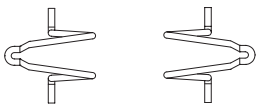


Fig. 44
Connector retention clips to fasten the H15 connector to the rear plate; see fig. 24. HZZ01209-G consists of 2 clips.

– Chassis or wall-mounting plate K02 (HZZ01213-G) for models with option B1. Mating connector (HZZ00107-G) with screw terminals; see fig. 48
– DIN-rail mounting assembly HZZ0615-G (DMB-K/S); see fig. 49
– Additional external input and output filters
– Different battery sensors S-KSMH... for using the converter as a battery charger. Different cell characteristics can be selected; see fig. 32, table 12, and *Battery Charging/Temperature Sensors.*

For additional accessory product information, see the accessory data sheets listed with each product series or individual model at our web site:

www.belpowersolutions.com/power

Fig. 48
Chassis- or wall-mounting plate HZZ01213-G (Mounting plate K02)

Fig. 49
DIN-rail mounting assembly HZZ00615-G (DMB-K/S)

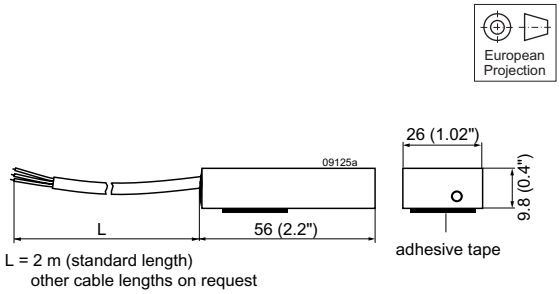


Fig. 50
Battery temperature sensor

Table 24: Battery temperature sensors

Battery voltage nom.[V]	Sensor type	Cell voltage [V]	Cell temp. coefficient [mV/K]	Cable length [m]
12	S-KSMH12-2.27-30-2	2.27	–3.0	2
12	S-KSMH12-2.27-35-2	2.27	–3.5	2
24	S-KSMH24-2.27-30-2	2.27	–3.0	2
24	S-KSMH24-2.27-35-2	2.27	–3.5	2
24	S-KSMH24-2.31-35-0	2.31	–3.5	4.5
24	S-KSMH24-2.31-35-2	2.31	–3.5	2
24	S-KSMH24-2.35-35-2	2.35	–3.5	2
48	S-KSMH48-2.27-30-2	2.27	–3.0	2
48	S-KSMH48-2-27-35-2	2.27	–3.5	2

Note: Other temperature coefficients and cable lengths are available on request.

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