

CLOCK SLICER USER CONFIGURABLE ZERO DELAY BUFFER
ICS527-01
Description

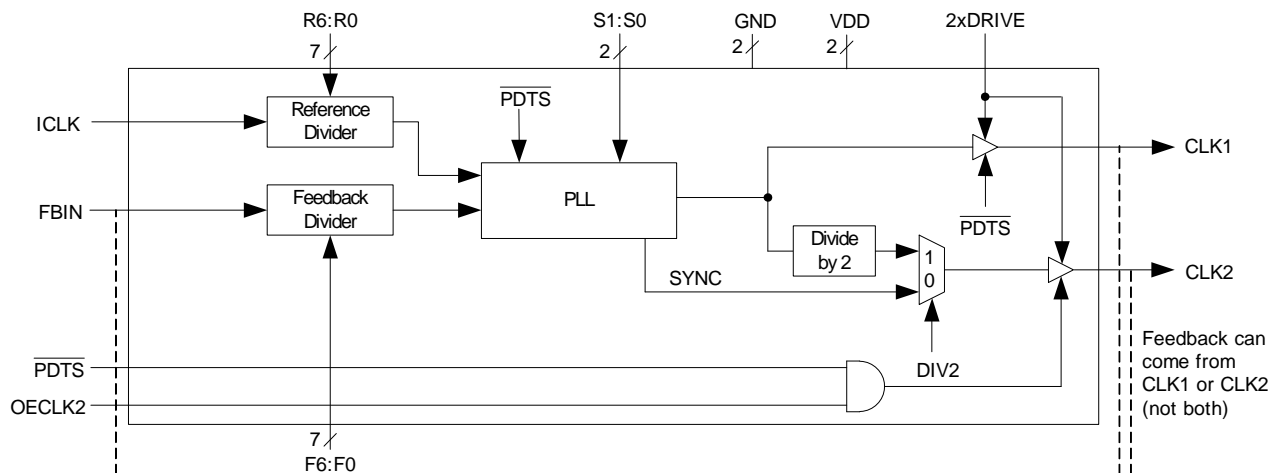
The ICS527-01 Clock Slicer is the most flexible way to generate an output clock from an input clock with zero skew. The user can easily configure the device to produce nearly any output clock that is multiplied or divided from the input clock. The part supports non-integer multiplications and divisions. A SYNC pulse indicates when the rising clock edges are aligned with zero skew. Using Phase-Locked Loop (PLL) techniques, the device accepts an input clock up to 200 MHz and produces an output clock up to 160 MHz.

The ICS527-01 aligns rising edges on ICLK and FBIN at a ratio determined by the reference and feedback dividers.

For configurable clocks that do not require zero delay, use the ICS525.

Features

- Packaged as 28-pin SSOP (150 mil body)
- Synchronizes fractional clocks rising edges
- Pin configurable multiplication/division ratio
- Slices frequency or period
- SYNC pulse output indicates aligned edges
- Input clock frequency of 600 kHz to 200 MHz
- Output clock frequencies up to 160 MHz
- Very low jitter
- Duty cycle of 45/55 up to 160 MHz
- Operating voltage of 3.3V
- Pin selectable drive strength
- Multiple outputs available when combined with fanout buffers
- Industrial temperature version available
- Pb (lead) free package

Block Diagram


Pin Assignment

| | | | |
|---------|----|----|---------------------------|
| R5 | 1 | 28 | R4 |
| R6 | 2 | 27 | R3 |
| DIV2 | 3 | 26 | R2 |
| S0 | 4 | 25 | R1 |
| S1 | 5 | 24 | R0 |
| VDD | 6 | 23 | VDD |
| ICLK | 7 | 22 | CLK1 |
| FBIN | 8 | 21 | CLK2 |
| GND | 9 | 20 | GND |
| OECLK2 | 10 | 19 | $\overline{\text{PDT S}}$ |
| 2XDRIVE | 11 | 18 | F6 |
| F0 | 12 | 17 | F5 |
| F1 | 13 | 16 | F4 |
| F2 | 14 | 15 | F3 |

28 pin 150 mil body SSOP

Frequency Range Table

| S1 | S0 | CLK1 Output Frequency (MHz) | |
|----|----|-----------------------------|--------------------------|
| | | Commercial (0 to 70°C) | Industrial (-40 to 85°C) |
| 0 | 0 | 37 - 75 | 35 - 70 |
| 0 | 1 | 18 - 37 | 16 - 35 |
| 1 | 0 | 4 - 10 | 4 - 8 |
| 1 | 1 | 75 - 160 | 70 - 140 |

To cover the range from 10 to 18 MHz (0 to 70°C) and 8 to 16 MHz (-40 to 85°C), select address 01 to generate 2x your desired output frequency, then configure CLK2 to generate CLK1/2.

CLK2 Operation Table

CLK Drive Select Table

| OECLK2 | DIV2 | CLK2 | 2XDRIVE | Output Drive |
|--------|------|--------|---------|--------------|
| 0 | X | Z | 0 | 12 mA |
| 1 | 0 | SYNC | 1 | 25 mA |
| 1 | 1 | CLK1/2 | | |

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|---------------------------|----------|---|
| 1,2, 24-28 | R5, R6, R0-R4 | Input | Reference divider word input pins determined by user. Forms a binary number from 0 to 127. Internal pull-up resistor. |
| 3 | DIV2 | Input | Selects CLK2 function to output a SYNC signal or a divide by 2 of CLK1 based on the table above. Internal pull-up resistor. |
| 4, 5 | S0, S1 | Input | Select pins for output divider determined by user. See table above. Internal pull-up resistor. |
| 6, 23 | VDD | Power | Connect to VDD. |
| 7 | ICLK | Input | Reference clock input. |
| 8 | FBIN | Input | Feedback clock input. |
| 9, 20 | GND | Power | Connect to ground. |
| 10 | OECLK2 | Input | CLK2 Output Enable. CLK2 tri-stated when low. Internal pull-up resistor. |
| 11 | 2XDRIVE | Input | Clock output drive strength doubled when high. Internal pull-up resistor. |
| 12-18 | F0-F6 | Input | Feedback divider word input pins determined by user. Forms a binary number from 0 to 127. Internal pull-up resistor. |
| 19 | $\overline{\text{PDT S}}$ | Input | Power Down. Active low. Turns off entire chip when low, both clock outputs are tri-stated. Internal pull-up resistor. |
| 21 | CLK2 | Output | Output clock 2. Can be SYNC output or a low skew divide by 2 of CLK1. |
| 22 | CLK1 | Output | Output clock 1. |

External Components

Decoupling Capacitors

As with any high performance mixed-signal IC, the ICS527-01 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of $0.01\mu\text{F}$ must be connected between each VDD and the PCB ground plane. The capacitor must be connected close to the device to minimize lead inductance.

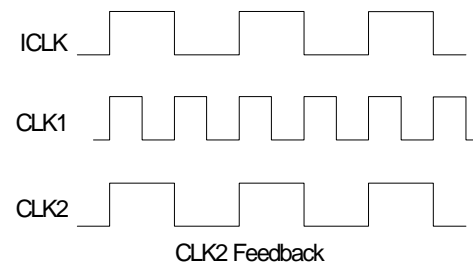
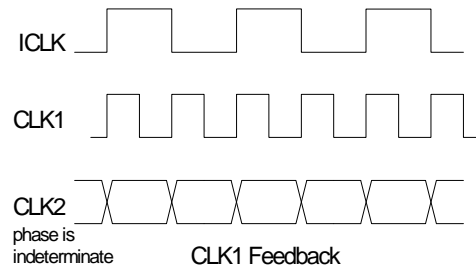
Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω .

Using the Clock Slicer

First use DIV2 to select the function of the CLK2 output. If DIV2 is high, a divide-by-2, low skew version of CLK1 is present on CLK2. If DIV2 is low, a SYNC pulse is generated on CLK2. The SYNC pulse goes high synchronously with the rising edges of ICLK and CLK1 that are de-skewed. The SYNC function operates at CLK1 frequencies up to 66 MHz. If neither CLK1/2 or a SYNC pulse are required, then CLK2 should be disabled by connecting OECLK2 to ground. This will also give the lowest jitter on CLK1.

Next, the feedback scheme should be chosen. If CLK2 is being used as a SYNC pulse, or is tri-stated, then CLK1 must be connected to FBIN. If CLK2 is selected to be CLK1/2 (DIV2=1, OECLK2=1) then either CLK1 or CLK2 must be connected to FBIN. The choice between CLK1 or CLK2 is illustrated by the following examples where the device has been configured to generate CLK1 that is twice the frequency on ICLK.



Using CLK1 as feedback will always result in synchronized rising edges between ICLK and CLK1 if CLK1 is used as feedback. CLK2 could be a falling edge compared to ICLK. Therefore, wherever possible, it is recommended to use CLK2 for feedback, which will synchronize the rising edges of all three clocks.

More complicated feedback schemes can be used, such as incorporating multiple output buffers in the feedback path. An example is given later in the datasheet. The fundamental property of the ICS527-01 is that it aligns rising edges on ICLK and FBIN at a ratio determined by the reference and feedback dividers.

The drive strength is selected by the 2XDRIVE pin. If high drive strength is required, we recommend tying this pin low.

Lastly, the divider settings should be selected. This is described in the following section.

Determining ICS527-01 Divider Settings

The user has full control in setting the desired output clock over the range shown in the table on page 2. The user should connect the divider select input pins directly to ground (or VDD, although this is not required

because of internal pull-ups) during Printed Circuit Board layout, so the ICS527-01 automatically produces the correct clock when all components are soldered. It is also possible to connect the inputs to parallel I/O ports in order to switch frequencies.

The output of the ICS527-01 can be determined by the following simple equation:

$$\text{FB Frequency} = \text{Input Frequency} \times \frac{\text{FDW} + 2}{\text{RDW} + 2}$$

Where:

Reference Divider Word (RDW) = 0 to 127
 Feedback Divider Word (FDW) = 0 to 127
 FB Frequency is the same as either CLK1 or CLK2 depending on feedback connection

Also, the following operating ranges should be observed:

$$300\text{kHz} < \frac{\text{Input Frequency}}{\text{RDW} + 2}$$

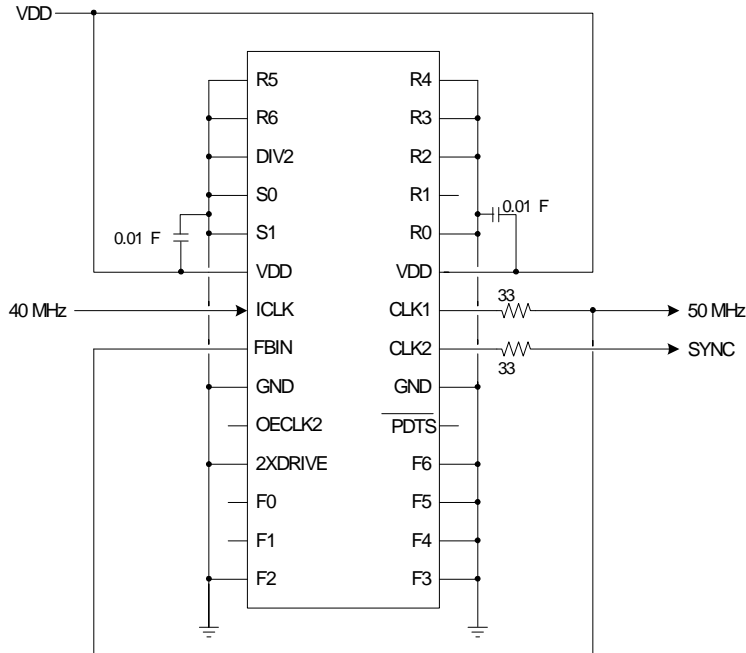
S1 and S0 should be set for the frequency of CLK1, according to the Frequency Range Table on page 2. The device can be operated below the lower limits stated in table 2, however, jitter and skew may be higher. Therefore, if your expected output frequency covers more than one frequency range, use the setting for the highest frequency expected.

The dividers are expressed as integers. For example, if a 50 MHz output on CLK1 is desired from a 40 MHz input, the reference divider word (RDW) should be 2 and the feedback divider word (FDW) should be 3 which gives the required 5/4 multiplication. Then R6:R0 is 0000010, F6:F0 is 0000011 and S1:S0 is 00. Also, this example assumes CLK1 is connected to FBIN. S1:S0 is set by referring to the Frequency Range Table. The setting for 50 MHz is 00.

For assistance with configuring the device, please send a description of your requirements using the "Technical Support" link at www.idt.com.

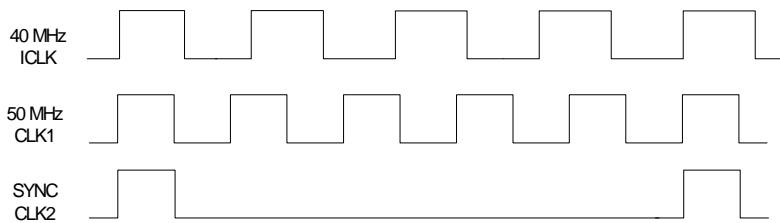
Typical Example

The following connection diagram shows the implementation of the example from the previous section. This will generate a 50 MHz clock synchronously with a 40 MHz input. A SYNC pulse is desired and the 1x output drive is selected.



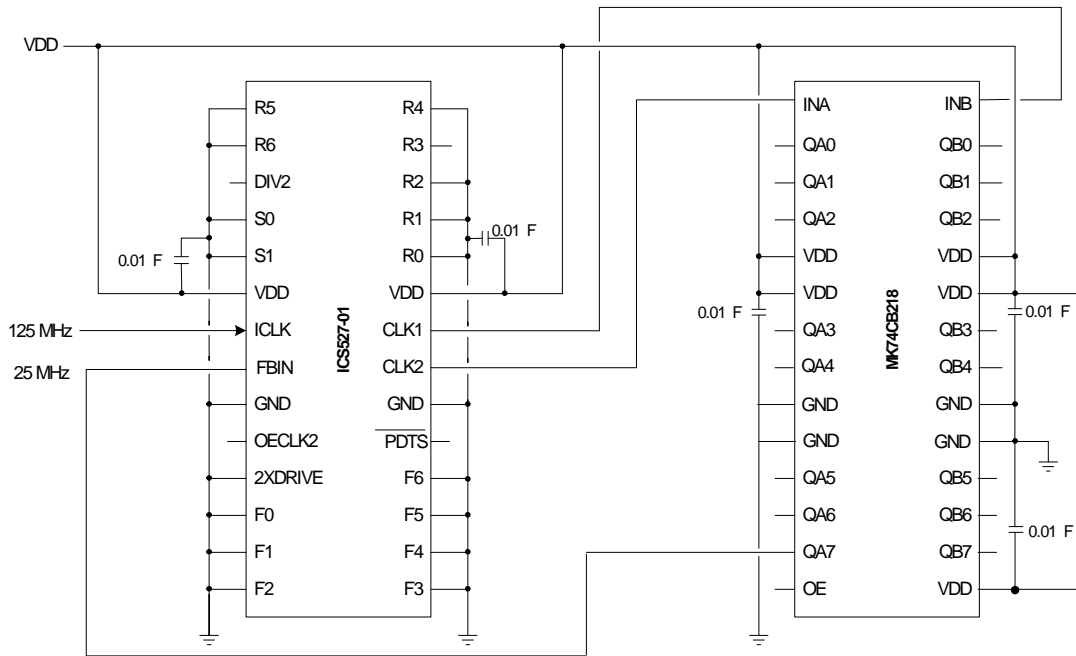
Note: The series termination resistor is located before the feedback trace.

This will give the following waveforms:



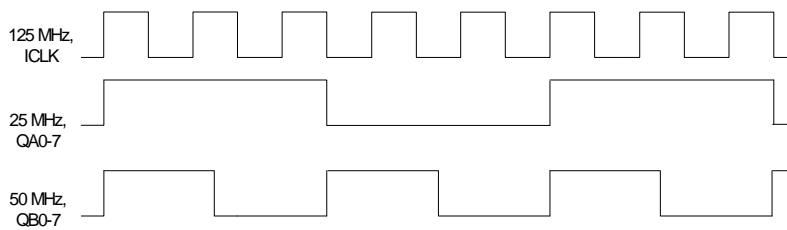
Multiple Output Example

In this example, an input clock of 125 MHz is used. Eight copies of 50 MHz are required as are eight copies of 25 MHz, de-skewed and aligned to the 125 MHz input clock. The following solution uses the MK74CB218 which has dual 1 to 8 buffers with low pin-to-pin skew.



The layout design above produces the waveforms shown below.

Note: Series terminating resistors are not shown.



Using the equation for selecting dividers gives:

$$25 \text{ MHz} = 125 \text{ MHz} \times \frac{(\text{FDW} + 2)}{(\text{RDW} + 2)}$$

If $\text{FDW} = 0$, then $\text{RDW} = 8$. This gives the required divide-by-5 function. Setting pin $\text{DIV2} = 1$ gives both a 25 MHz and a 50 MHz output from the ICS527-01. The FBIN pin is connected to the QA7 output of the MK74CB218. This aligns all the outputs of the MK74CB218 with the 25 MHz input since the ICS527-01 aligns rising edges on the ICLK and FBIN pins. The propagation delay of the buffer is compensated by the PLL.

In this example, series termination resistors have been omitted for clarity but should be used on all clock outputs.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

- 1) Each $0.01\mu\text{F}$ decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No via's should be used

between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) To minimize EMI the 33Ω series termination resistor, if needed, should be placed close to the clock outputs.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS527-01. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS527-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|--|---------------------|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature (Commercial) | 0 to +70° C |
| Ambient Operating Temperature (Industrial) | -40 to +85° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 260° C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|------|------|------|-------|
| Ambient Operating Temperature, ICS527R-01 | 0 | – | +70 | ° C |
| Ambient Operating Temperature, ICS527R-01I | -40 | – | +85 | ° C |
| Power Supply Voltage (measured in respect to GND) | 3 | 3.3 | 3.6 | V |

DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3 V ±10%, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|----------------------------|-----------------|-----------------------------------|------|------|------|-------|
| Operating Voltage | VDD | | 3 | 3.3 | 3.6 | V |
| Supply Current | IDD | 15 MHz in, 60MHz out, no load | | 8 | | mA |
| Supply Current, Power Down | IDDPD | $\overline{\text{PDT}}\text{S}=0$ | | 20 | | μA |
| Input High Voltage | V _{IH} | | 2 | | | V |

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------------|----------|-----------------------------------|--------------|-----------|--------------|-----------|
| Input Low Voltage | V_{IL} | | | | 0.8 | V |
| Input High Voltage, ICLK and FBIN | V_{IH} | Pins 7 and 8 | $V_{DD}/2+1$ | | | V |
| Input Low Voltage, ICLK and FBIN | V_{IL} | Pins 7 and 8 | | | $V_{DD}/2-1$ | V |
| Output High Voltage | V_{OH} | 2XDRIVE = 0, $I_{OH} = -12$ mA | 2.4 | | | V |
| Output Low Voltage | V_{OL} | 2XDRIVE = 0, $I_{OL} = 12$ mA | | | 0.4 | V |
| Output High Voltage | V_{OH} | 2XDRIVE = 1, $I_{OH} = -25$ mA | 2.4 | | | V |
| Output Low Voltage | V_{OL} | 2XDRIVE = 1, $I_{OL} = 25$ mA | | | 0.4 | V |
| Short Circuit Current | I_{OS} | 2XDRIVE = 0, CLK outputs | | ± 70 | | mA |
| Short Circuit Current | I_{OS} | 2XDRIVE = 1, CLK outputs | | ± 140 | | mA |
| On-chip Pull-up Resistor | R_{PU} | | | 270 | | $k\Omega$ |

AC Electrical Characteristics

Unless stated otherwise, $V_{DD} = 3.3\text{ V} \pm 10\%$, Ambient Temperature -40 to $+85^\circ\text{C}$

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|-----------|---|------|----------|------|-------|
| Input Frequency | F_{IN} | | 0.6 | | 200 | MHz |
| Output Frequency, CLK1 | F_{OUT} | 0 to $+70^\circ\text{C}$ | 4 | | 160 | MHz |
| | | -40 to $+85^\circ\text{C}$ | 4 | | 140 | MHz |
| CLK1 Frequency for Correct SYNC Operation | | | | | 66 | MHz |
| Output Rise Time | t_{OR} | 0.8 to 2.0 V | | 1 | | ns |
| Output Fall Time | t_{OF} | 2.0 to 0.8 V | | 1 | | ns |
| Output Clock Duty Cycle | t_{OD} | Measured at $V_{DD}/2$, $C_L=15\text{ pF}$ | 45 | 50 | 55 | % |
| Power Down Time, $\overline{PDT\overline{S}}$ low to clocks tri-stated | | | | | 50 | ns |
| Power Up Time, $\overline{PDT\overline{S}}$ high to clocks stable | | | | | 10 | ms |
| Absolute Clock Period Jitter | t_{ja} | Deviation from mean | | ± 90 | | ps |
| One sigma Clock Period Jitter | t_{js} | | | 40 | | ps |
| Skew of Output Clocks | t_{IO} | CLK1 to CLK2, Note 1 | -250 | | 250 | ps |
| Input Capacitance | C_{IN} | | | 4 | | pF |
| Input to Output Skew | t_{IO} | ICLK to FBIN, Note 1 | -250 | | 250 | ps |
| Device to Device Skew | t_{pi} | Common ICLK, at FBIN | | 0 | 500 | ps |

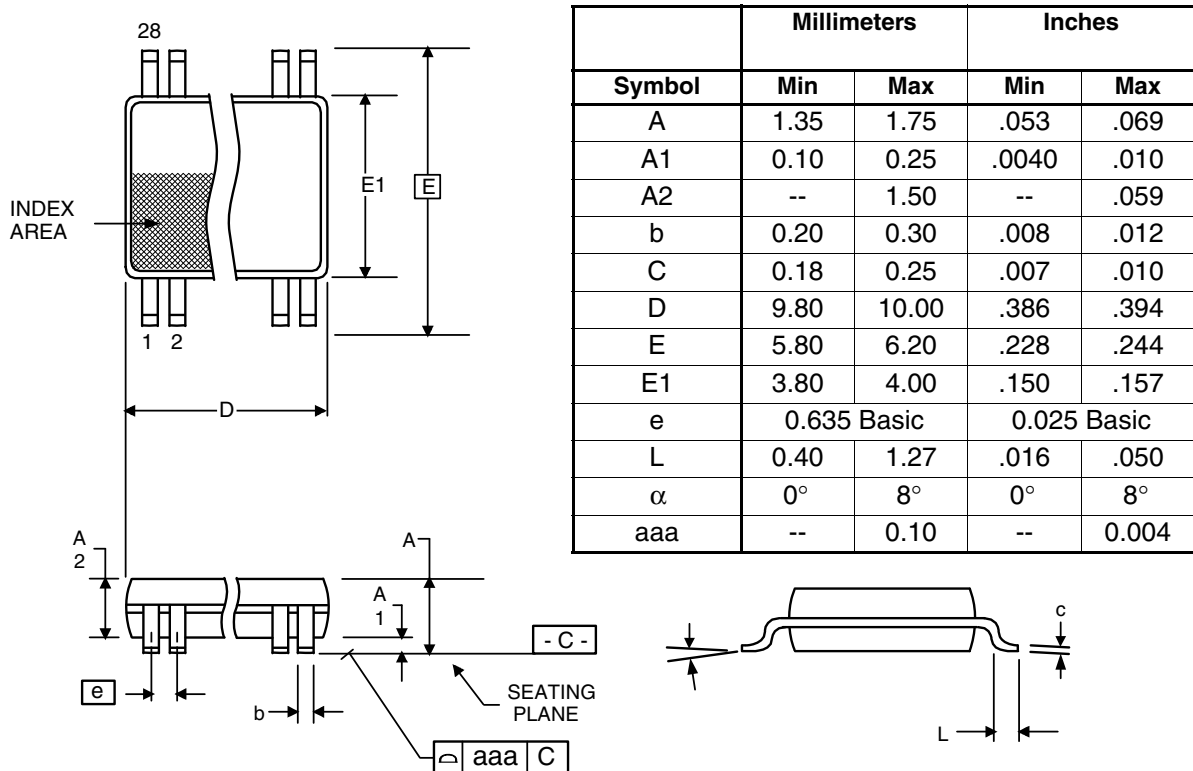
Note 1: Assumes clocks with same rise time, measured from rising edges at $V_{DD}/2$.

External Components

The ICS527-01 requires two $0.01\text{ }\mu\text{F}$ decoupling capacitors to be connected between V_{DD} and GND , one on each side of the chip. They must be connected close to the device to minimize lead inductance. No external power supply filtering is required for this device. A 33Ω series terminating resistor should be used on the CLK1 and CLK2 output pins.

Package Outline and Package Dimensions (28-pin SSOP, .150 mil Body, 0.025 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|---------------|--------------------|-------------|---------------|
| 527R-01LF | ICS527R-01LF | Tubes | 28-pin SSOP | 0 to +70° C |
| 527R-01LFT | ICS527R-01LF | Tape and Reel | 28-pin SSOP | 0 to +70° C |
| 527R-01ILF | ICS527R-01ILF | Tubes | 28-pin SSOP | -40 to +85° C |
| 527R-01ILFT | ICS527R-01ILF | Tape and Reel | 28-pin SSOP | -40 to +85° C |

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