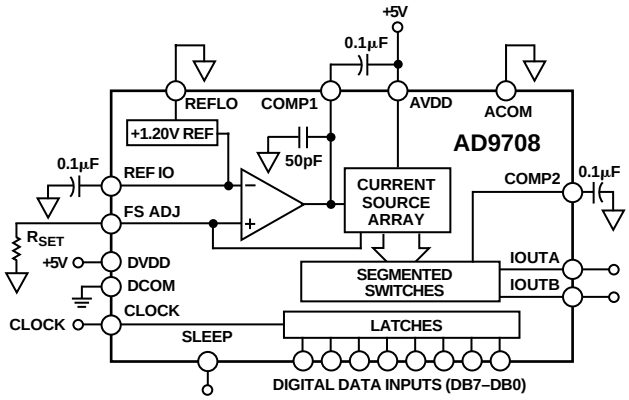
8-Bit, 100 MSPS+ TxDAC® D/A Converter

AD9708

FEATURES
Member of Pin-Compatible TxDAC Product Family
125 MSPS Update Rate
8-Bit Resolution
Linearity: 1/4 LSB DNL
1/4 LSB INL
Differential Current Outputs
SINAD @ 5 MHz Output: 50 dB
Power Dissipation: 175 mW @ 5 V to 45 mW @ 3 V
Power-Down Mode: 20 mW @ 5 V
On-Chip 1.20 V Reference
Single +5 V or +3 V Supply Operation
Packages: 28-Lead SOIC and 28-Lead TSSOP
Edge-Triggered Latches
Fast Settling: 35 ns Full-Scale Settling to 0.1%

APPLICATIONS
Communications
Signal Reconstruction
Instrumentation

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9708 is the 8-bit resolution member of the TxDAC series of high performance, low power CMOS digital-to-analog converters (DACs). The TxDAC family, which consists of pin compatible 8-, 10-, 12-, and 14-bit DACs, was specifically optimized for the transmit signal path of communication systems. All of the devices share the same interface options, small outline package and pinout, thus providing an upward or downward component selection path based on performance, resolution and cost. The AD9708 offers exceptional ac and dc performance while supporting update rates up to 125 MSPS.

The AD9708's flexible single-supply operating range of +2.7 V to +5.5 V and low power dissipation are well suited for portable and low power applications. Its power dissipation can be further reduced to 45 mW, without a significant degradation in performance, by lowering the full-scale current output. In addition, a power-down mode reduces the standby power dissipation to approximately 20 mW.

The AD9708 is manufactured on an advanced CMOS process. A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. Edge-triggered input latches and a temperature compensated bandgap reference have been integrated to provide a complete monolithic DAC solution. Flexible supply options support +3 V and +5 V CMOS logic families.

The AD9708 is a current-output DAC with a nominal full-scale output current of 20 mA and > 100 kΩ output impedance.

Differential current outputs are provided to support single-ended or differential applications. The current outputs may be directly tied to an output resistor to provide two complementary, single-ended voltage outputs. The output voltage compliance range is 1.25 V.

The AD9708 contains a 1.2 V on-chip reference and reference control amplifier, which allows the full-scale output current to be simply set by a single resistor. The AD9708 can be driven by a variety of external reference voltages. The AD9708's full-scale current can be adjusted over a 2 mA to 20 mA range without any degradation in dynamic performance. Thus, the AD9708 may operate at reduced power levels or be adjusted over a 20 dB range to provide additional gain ranging capabilities.

The AD9708 is available in 28-lead SOIC and 28-lead TSSOP packages. It is specified for operation over the industrial temperature range.

PRODUCT HIGHLIGHTS

1. The AD9708 is a member of the TxDAC product family, which provides an upward or downward component selection path based on resolution (8 to 14 bits), performance and cost.
2. Manufactured on a CMOS process, the AD9708 uses a proprietary switching technique that enhances dynamic performance well beyond 8- and 10-bit video DACs.
3. On-chip, edge-triggered input CMOS latches readily interface to +3 V and +5 V CMOS logic families. The AD9708 can support update rates up to 125 MSPS.
4. A flexible single-supply operating range of +2.7 V to +5.5 V and a wide full-scale current adjustment span of 2 mA to 20 mA allows the AD9708 to operate at reduced power levels (i.e., 45 mW) without any degradation in dynamic performance.
5. A temperature compensated, 1.20 V bandgap reference is included on-chip providing a complete DAC solution. An external reference may be used.
6. The current output(s) of the AD9708 can easily be configured for various single-ended or differential applications.

REV. B

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AD9708–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	8			Bits
MONOTONICITY	GUARANTEED OVER SPECIFIED TEMPERATURE RANGE			
DC ACCURACY[1]				
Integral Linearity Error (INL)	–1/2	±1/4	+1/2	LSB
Differential Nonlinearity (DNL)	–1/2	±1/4	+1/2	LSB
ANALOG OUTPUT				
Offset Error	–0.025		+0.025	% of FSR
Gain Error (Without Internal Reference)	–10	±2	+10	% of FSR
Gain Error (With Internal Reference)	–10	±1	+10	% of FSR
Full-Scale Output Current[2]	2.0		20.0	mA
Output Compliance Range	–1.0		1.25	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.08	1.20	1.32	V
Reference Output Current[3]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance		1		MΩ
Small Signal Bandwidth (w/o C_{COMP1})[4]		1.4		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD[5]	2.7	5.0	5.5	V
DVDD	2.7	5.0	5.5	V
Analog Supply Current (I_{AVDD})		25	30	mA
Digital Supply Current (I_{DVDD})[6]		3	6	mA
Supply Current Sleep Mode (I_{AVDD})			8.5	mA
Power Dissipation[6] (5 V, I_{OUTFS} = 20 mA)		140	175	mW
Power Dissipation[7] (5 V, I_{OUTFS} = 20 mA)		190		mW
Power Dissipation[7] (3 V, I_{OUTFS} = 2 mA)		45		mW
Power Supply Rejection Ratio—AVDD	–0.4		+0.4	% of FSR/V
Power Supply Rejection Ratio—DVDD	–0.025		+0.025	% of FSR/V
OPERATING RANGE	–40		+85	°C

NOTES

[1]Measured at IOUTA, driving a virtual ground.

[2]Nominal full-scale current, I_{OUTFS}, is 32 × the I_{REF} current.

[3]Use an external buffer amplifier to drive any external load.

[4]Reference bandwidth is a function of external cap at COMP1 pin.

[5]For operation below 3 V, it is recommended that the output current be reduced to 12 mA or less to maintain optimum performance.

[6]Measured at f_{CLOCK} = 50 MSPS and f_{OUT} = 1.0 MHz.

[7]Measured as unbuffered voltage output into 50 Ω R_{LOAD} at IOUTA and IOUTB, f_{CLOCK} = 100 MSPS and f_{OUT} = 40 MHz.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, Single-Ended Output, IOUTA, 50 Ω Doubly Terminated, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{CLOCK})	100	125		MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		35		ns
Output Propagation Delay (t_{PD})		1		ns
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (10% to 90%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)		50		pA/√Hz
Output Noise (I_{OUTFS} = 2 mA)		30		pA/√Hz
AC LINEARITY TO NYQUIST				
Signal-to-Noise and Distortion Ratio				
f_{CLOCK} = 10 MSPS; f_{OUT} = 1.00 MHz		50		dB
f_{CLOCK} = 50 MSPS; f_{OUT} = 1.00 MHz		50		dB
f_{CLOCK} = 50 MSPS; f_{OUT} = 12.51 MHz		48		dB
f_{CLOCK} = 100 MSPS; f_{OUT} = 5.01 MHz		50		dB
f_{CLOCK} = 100 MSPS; f_{OUT} = 25.01 MHz		45		dB
Total Harmonic Distortion				
f_{CLOCK} = 10 MSPS; f_{OUT} = 1.00 MHz		–67		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 1.00 MHz		–67	–62	dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 12.51 MHz		–59		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 5.01 MHz		–64		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 25.01 MHz		–48		dBc
Spurious-Free Dynamic Range to Nyquist				
f_{CLOCK} = 10 MSPS; f_{OUT} = 1.00 MHz		68		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 1.00 MHz	62	68		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 12.51 MHz		63		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 5.01 MHz		67		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 25.01 MHz		50		dBc

NOTES
[1]Measured single ended into 50 Ω load.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA unless otherwise noted)

Parameter	Min	Typ	Max	Units
DIGITAL INPUTS				
Logic "1" Voltage @ DVDD = +5 V	3.5	5		V
Logic "1" Voltage @ DVDD = +3 V	2.1	3		V
Logic "0" Voltage @ DVDD = +5 V		0	1.3	V
Logic "0" Voltage @ DVDD = +3 V		0	0.9	V
Logic "1" Current	–10		+10	µA
Logic "0" Current	–10		+10	µA
Input Capacitance		5		pF
Input Setup Time (t_S)	2.0			ns
Input Hold Time (t_H)	1.5			ns
Latch Pulsewidth (t_{LPW})	3.5			ns

Specifications subject to change without notice.

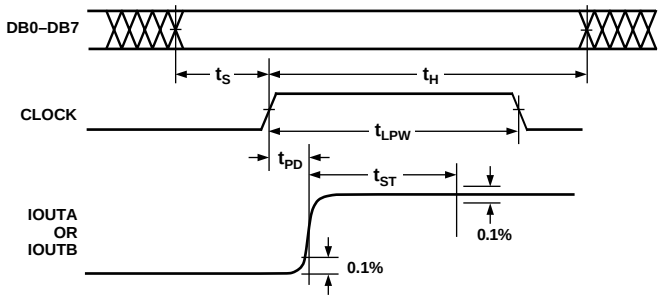


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	ACOM	–0.3	+6.5	V
DVDD	DCOM	–0.3	+6.5	V
ACOM	DCOM	–0.3	+0.3	V
AVDD	DVDD	–6.5	+6.5	V
CLOCK, SLEEP	DCOM	–0.3	DVDD + 0.3	V
Digital Inputs	DCOM	–0.3	DVDD + 0.3	V
IOUTA, IOUTB	ACOM	–1.0	AVDD + 0.3	V
COMP1, COMP2	ACOM	–0.3	AVDD + 0.3	V
REFIO, FSADJ	ACOM	–0.3	AVDD + 0.3	V
REFLO	ACOM	–0.3	+0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance

28-Lead 300 mil SOIC

θ_{JA} = 71.4°C/W

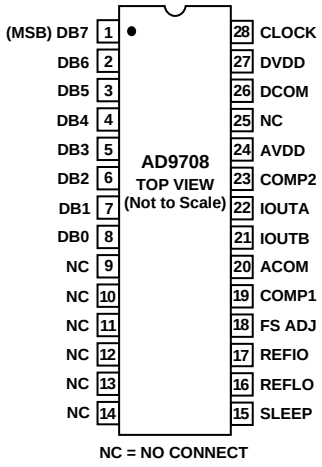
θ_{JC} = 23°C/W

28-Lead TSSOP

θ_{JA} = 97.9°C/W

θ_{JC} = 14.0°C/W

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
1	DB7	Most Significant Data Bit (MSB).
2–7	DB6–DB1	Data Bits 1–6.
8	DB0	Least Significant Data Bit (LSB).
9–14, 25	NC	No Internal Connection.
15	SLEEP	Power-Down Control Input. Active High. Contains active pull-down circuit, thus may be left unterminated if not used.
16	REFLO	Reference Ground when Internal 1.2 V Reference Used. Connect to AVDD to disable internal reference.
17	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled (i.e., Tie REFLO to AVDD). Serves as 1.2 V reference output when internal reference activated (i.e., Tie REFLO to ACOM). Requires 0.1 µF capacitor to ACOM when internal reference activated.
18	FS ADJ	Full-Scale Current Output Adjust.
19	COMP1	Bandwidth/Noise Reduction Node. Add 0.1 µF to AVDD for optimum performance.
20	ACOM	Analog Common.
21	IOUTB	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
22	IOUTA	DAC Current Output. Full-scale current when all data bits are 1s.
23	COMP2	Internal Bias Node for Switch Driver Circuitry. Decouple to ACOM with 0.1 µF capacitor.
24	AVDD	Analog Supply Voltage (+2.7 V to +5.5 V).
26	DCOM	Digital Common.
27	DVDD	Digital Supply Voltage (+2.7 V to +5.5 V).
28	CLOCK	Clock Input. Data latched on positive edge of clock.

ORDERING GUIDE

Model	Temperature Range	Package Descriptions	Package Options*
AD9708AR	–40°C to +85°C	28-Lead 300 Mil SOIC	R-28
AD9708ARU	–40°C to +85°C	28-Lead TSSOP	RU-28
AD9708-EB	Evaluation Board		

*R = Small Outline IC; RU = Thin Small Outline IC.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9708 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DEFINITIONS OF SPECIFICATIONS

Linearity Error (Also Called Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For IOUTA, 0 mA output is expected when the inputs are all 0s. For IOUTB, 0 mA output is expected when all inputs are set to 1s.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (+25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree C. For reference drift, the drift is reported in ppm per degree C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Signal-to-Noise and Distortion (S/N+D, SINAD) Ratio
S/N+D is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

Total Harmonic Distortion
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured output signal. It is expressed as a percentage or in decibels (dB).

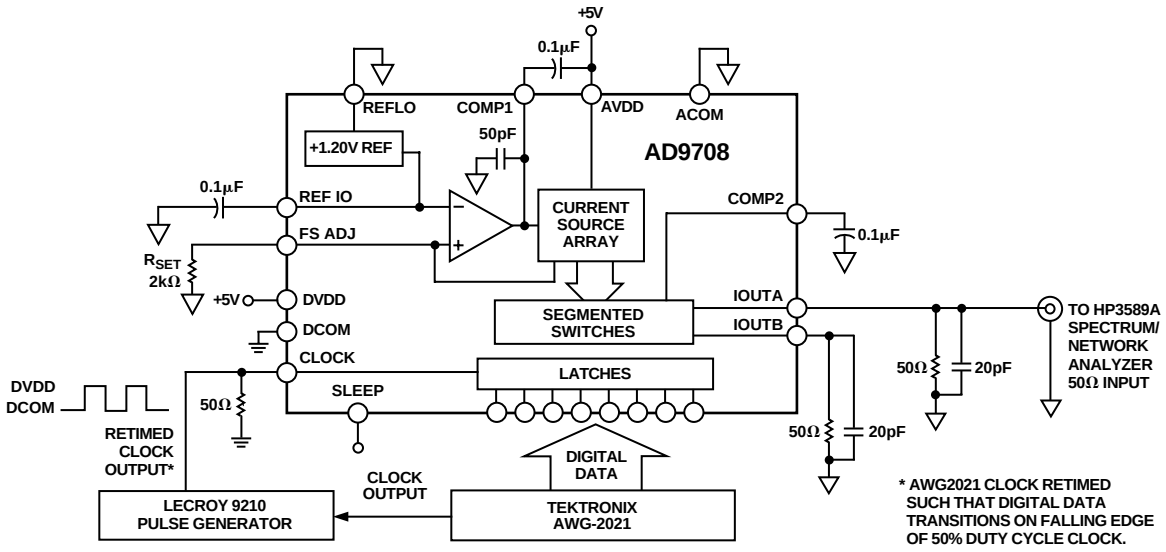


Figure 2. Basic AC Characterization Test Setup

Typical AC Characterization Curves (AVDD = +5 V or +3 V, DVDD = +5 V or +3 V, 50 Ω Doubly Terminated Load, Single-Ended Output, I_{OUTA}, I_{OUTFS} = 20 mA, T_A = +25°C, unless otherwise noted)

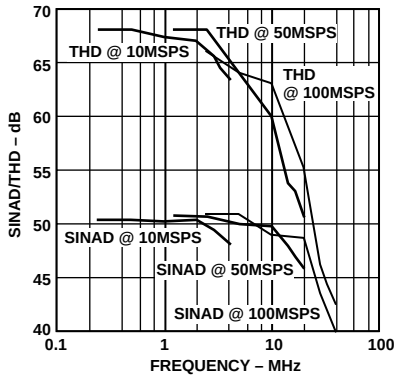


Figure 3. SINAD/THD vs. f_{OUT} (AVDD and DVDD = 5.0 V)

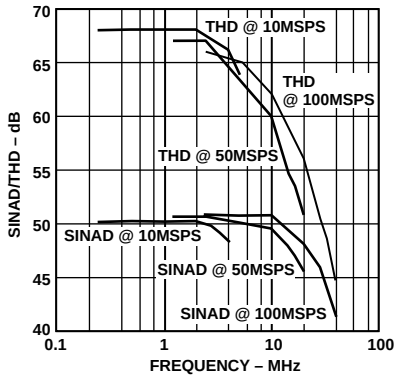


Figure 4. SINAD/THD vs. f_{OUT} (Differential Output, AVDD and DVDD = 5.0 V)

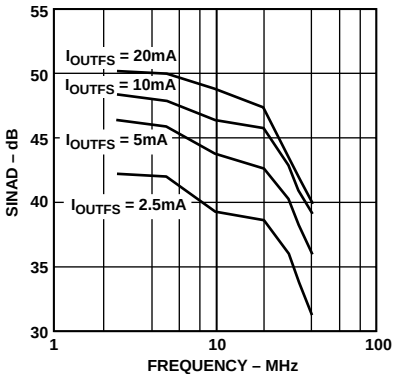


Figure 5. SINAD vs. I_{OUTFS} @ 100 MSPS

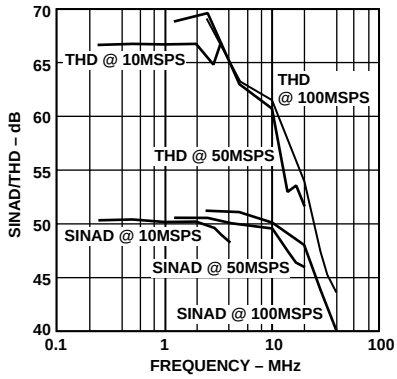


Figure 6. SINAD/THD vs. f_{OUT} (AVDD and DVDD = 3.0 V)

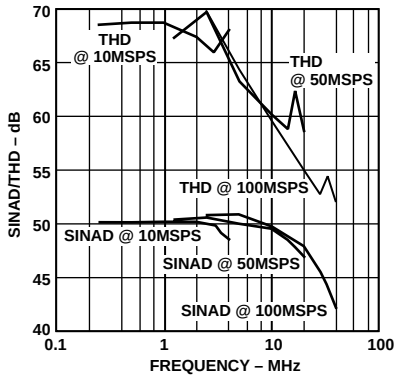


Figure 7. SINAD/THD vs. f_{OUT} (Differential Output, AVDD and DVDD = 3.0 V)

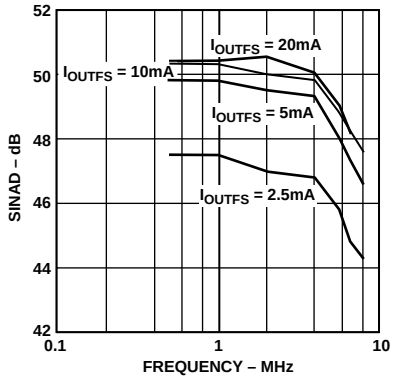


Figure 8. SINAD vs. I_{OUTFS} @ 20 MSPS

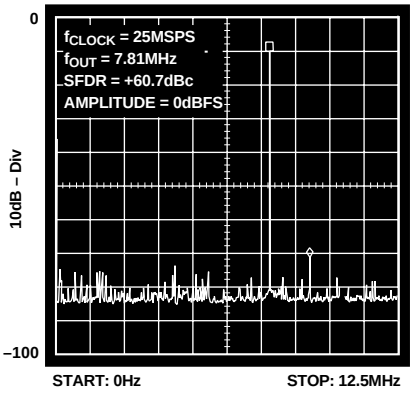


Figure 9. Single-Tone Spectral Plot @ 25 MSPS

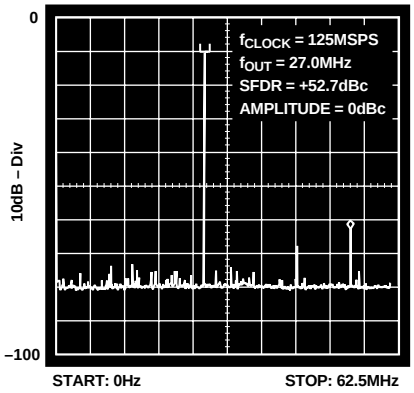


Figure 10. Single-Tone Spectral Plot @ 125 MSPS

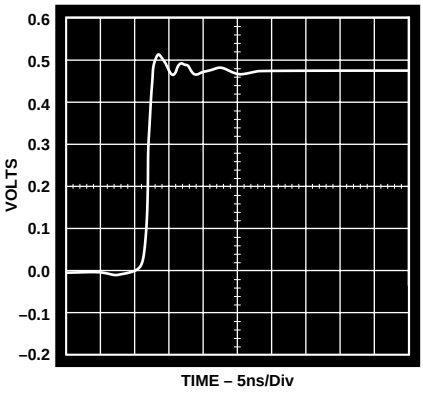


Figure 11. Step Response

FUNCTIONAL DESCRIPTION

Figure 12 shows a simplified block diagram of the AD9708. The AD9708 consists of a large PMOS current source array capable of providing up to 20 mA of total current. The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The remaining 3 LSBs are also implemented with equally weighted current sources whose sum total equals 7/8th of an MSB current source. Implementing the upper and lower bits with current sources helps maintain the DAC's high output impedance (i.e. > 100 kΩ). All of these current sources are switched to one or the other of the two output nodes (i.e., IOUTA or IOUTB) via PMOS differential current switches. The switches are based on a new architecture that drastically improves distortion performance.

The analog and digital sections of the AD9708 have separate power supply inputs (i.e., AVDD and DVDD) that can operate independently over a 2.7 volt to 5.5 volt range. The digital section, which is capable of operating up to a 125 MSPS clock rate, consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.20 V bandgap voltage reference and a reference control amplifier.

The full-scale output current is regulated by the reference control amplifier and can be set from 2 mA to 20 mA via an external resistor, R_{SET}. The external resistor, in combination with both the reference control amplifier and voltage reference V_{REFIO}, sets the reference current I_{REF}, which is mirrored over to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is thirty-two times the value of I_{REF}.

DAC TRANSFER FUNCTION

The AD9708 provides complementary current outputs, IOUTA and IOUTB. IOUTA will provide a near full-scale current output, I_{OUTFS}, when all bits are high (i.e., DAC CODE = 255), while IOUTB, the complementary output, provides no current. The current output appearing at IOUTA and IOUTB are a function of both the input code and I_{OUTFS} and can be expressed as:

$$I_{OUTA} = (DAC\ CODE/256) \times I_{OUTFS} \quad (1)$$

$$I_{OUTB} = (255 - DAC\ CODE)/256 \times I_{OUTFS} \quad (2)$$

where *DAC CODE* = 0 to 255 (i.e., Decimal Representation).

As previously mentioned, I_{OUTFS} is a function of the reference current I_{REF}, which is nominally set by a reference voltage V_{REFIO} and external resistor R_{SET}. It can be expressed as:

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where

$$I_{REF} = V_{REFIO}/R_{SET} \quad (4)$$

The two current outputs will typically drive a resistive load directly. If dc coupling is required, IOUTA and IOUTB should be directly connected to matching resistive loads, R_{LOAD}, which are tied to analog common, ACOM. Note, R_{LOAD} may represent the equivalent load resistance seen by IOUTA or IOUTB as would be the case in a doubly terminated 50 Ω or 75 Ω cable. The single-ended voltage output appearing at the IOUTA and IOUTB nodes is simply:

$$V_{OUTA} = I_{OUTA} \times R_{LOAD} \quad (5)$$

$$V_{OUTB} = I_{OUTB} \times R_{LOAD} \quad (6)$$

Note the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

The differential voltage, V_{DIFF}, appearing across IOUTA and IOUTB is:

$$V_{DIFF} = (I_{OUTA} - I_{OUTB}) \times R_{LOAD} \quad (7)$$

Substituting the values of I_{OUTA}, I_{OUTB}, and I_{REF}; V_{DIFF} can be expressed as:

$$V_{DIFF} = \{(2\ DAC\ CODE - 255)/256\}/ \times (32\ R_{LOAD}/R_{SET}) \times V_{REFIO} \quad (8)$$

VOLTAGE REFERENCE AND CONTROL AMPLIFIER

The AD9708 contains an internal 1.20 V bandgap reference that can be easily disabled and overridden by an external reference. REFIO serves as either an *input* or *output* depending on whether the internal or an external reference is selected. If REFLO is tied to ACOM, as shown in Figure 13, the internal reference is activated and REFIO provides a 1.20 V output. In this case, the internal reference *must* be compensated externally with a ceramic chip capacitor of 0.1 μF or greater from REFIO to REFLO. Note that REFIO is not designed to drive any external load. It should be buffered with an external amplifier having an input bias current less than 100 nA if any additional loading is required.

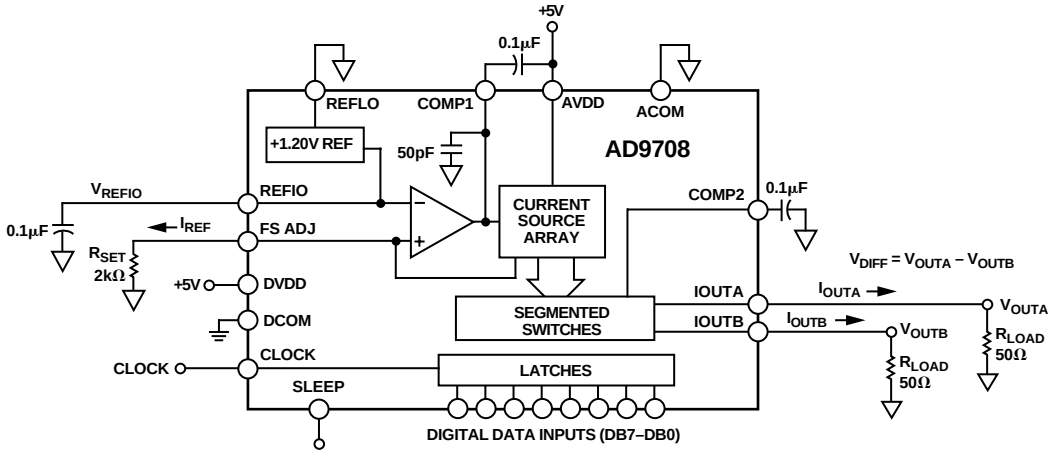


Figure 12. Functional Block Diagram

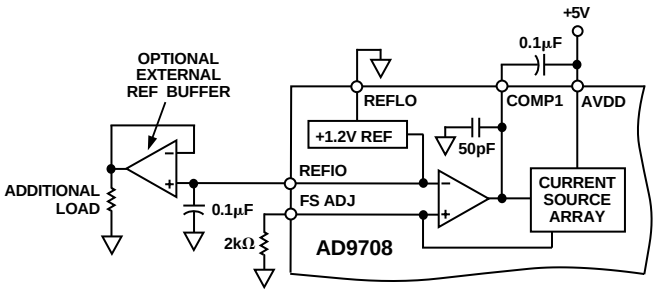


Figure 13. Internal Reference Configuration

The internal reference can be disabled by connecting REFLO to AVDD. In this case, an external reference may then be applied to REFIO as shown in Figure 14. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1 µF compensation capacitor is not required since the internal reference is disabled, and the high input impedance (i.e., 1 MΩ) of REFIO minimizes any loading of the external reference.

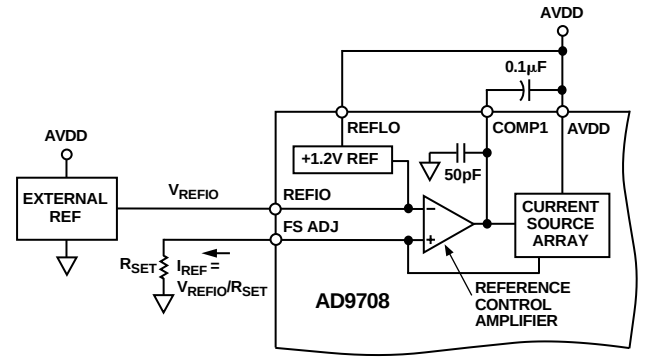


Figure 14. External Reference Configuration

The AD9708 also contains an internal control amplifier that is used to regulate the DAC's full-scale output current, I_{OUTFS}. The control amplifier is configured as a V-I converter, as shown in Figure 14, such that its current output, I_{REF}, is determined by the ratio of the V_{REFIO} and an external resistor, R_{SET}, as stated in Equation 4. The control amplifier allows a wide (10:1) adjustment span of I_{OUTFS} over a 2 mA to 20 mA range by setting I_{REF} between 62.5 µA and 625 µA. The wide adjustment span of I_{OUTFS} provides several application benefits. The first benefit relates directly to the power dissipation of the AD9708, which is proportional to I_{OUTFS} (refer to the POWER DISSIPATION section). The second benefit relates to the 20 dB adjustment, which is useful for system gain control purposes.

The small signal bandwidth of the reference control amplifier is approximately 1.8 MHz and can be reduced by connecting an external capacitor between COMP1 and AVDD. The output of the control amplifier, COMP1, is internally compensated via a 50 pF capacitor that limits the control amplifier small-signal bandwidth and reduces its output impedance. Any additional external capacitance further limits the bandwidth and acts as a filter to reduce the noise contribution from the reference amplifier. If I_{REF} is fixed for an application, a 0.1 µF ceramic chip capacitor is recommended.

I_{REF} can be varied for a fixed R_{SET} by disabling the internal reference and varying the common-mode voltage over its compliance range of 1.25 V to 0.10 V. REFIO can be driven by a single-supply amplifier or DAC, thus allowing I_{REF} to be varied for a fixed R_{SET}. Since the input impedance of REFIO is approximately 1 MΩ, a simple R-2R ladder DAC configured in the voltage mode topology may be used to control the gain. This circuit is shown in Figure 15 using the AD7524 and an external 1.2 V reference, the AD1580. Note another AD9708 could also be used as the gain control DAC since it can also provide a programmable unipolar output up to 1.2 V.

ANALOG OUTPUTS AND OUTPUT CONFIGURATIONS

The AD9708 produces two complementary current outputs, I_{OUTA} and I_{OUTB}, which may be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor, R_{LOAD}, as described in the DAC TRANSFER FUNCTION section. Figure 16 shows the AD9708 configured to provide a positive unipolar output range of approximately 0 V to +0.5 V for a double terminated 50 Ω cable for a nominal full-scale current, I_{OUTFS}, of 20 mA. In this case, R_{LOAD} represents the equivalent load resistance seen by IOUTA or IOUTB and is equal to 25 Ω. The unused output (IOUTA or IOUTB) can be connected to ACOM directly or via a matching R_{LOAD}. Different values of I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to.

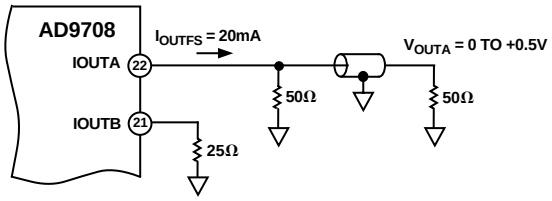


Figure 16. 0 V to +0.5 V Unbuffered Voltage Output

Alternatively, an amplifier could be configured as an I-V converter thus converting IOUTA or IOUTB into a negative unipolar

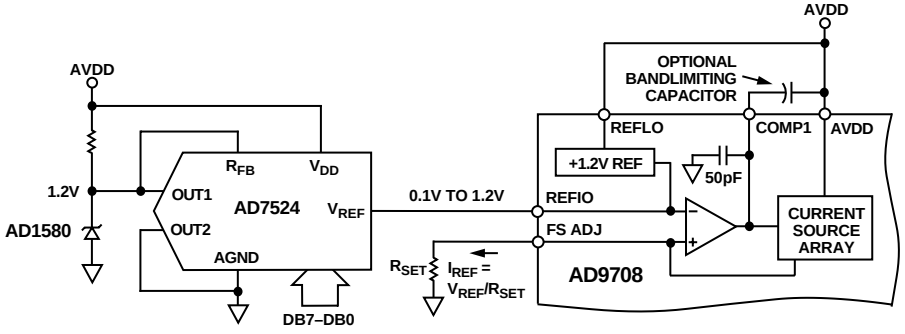


Figure 15. Single-Supply Gain Control Circuit

voltage. Figure 17 shows a buffered singled-ended output configuration in which the op amp, U1, performs an I-V conversion on the AD9708 output current. U1 provides a negative unipolar output voltage and its full-scale output voltage is simply the product of R_{FB} and I_{OUTFS}. The full-scale output should be set within U1's voltage output swing capabilities by scaling I_{OUTFS} and/or R_{FB}. An improvement in ac distortion performance may result with a reduced I_{OUTFS}, since the signal current U1 will be required to sink and will be subsequently reduced. Note, the ac distortion performance of this circuit at higher DAC update rates may be limited by U1's slewing capabilities.

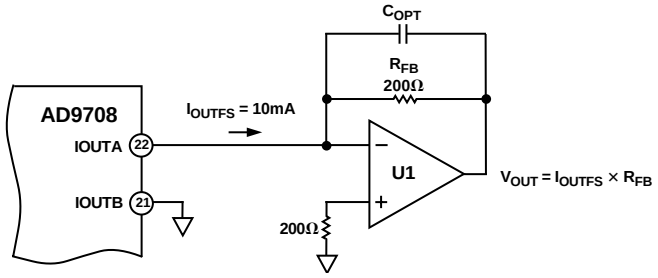


Figure 17. Unipolar Buffered Voltage Output

IOUTA and IOUTB also have a negative and positive voltage compliance range that must be adhered to in order to achieve optimum performance. The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS}. It degrades slightly from its nominal 1.25 V for an I_{OUTFS} = 20 mA to 1.00 V for an I_{OUTFS} = 2 mA. Applications requiring the AD9708's output (i.e., V_{OUTA} and/or V_{OUTB}) to extend up to its output compliance range should size R_{LOAD} accordingly. Operation beyond this compliance range will adversely affect the AD9708's linearity.

The differential voltage, V_{DIFF}, existing between V_{OUTA} and V_{OUTB} may also be converted to a single-ended voltage via a transformer or differential amplifier configuration. Refer to the DIFFERENTIAL OUTPUT CONFIGURATION section for more information.

DIGITAL INPUTS

The AD9708's digital input consists of eight data input pins and a clock input pin. The 8-bit parallel data inputs follow standard positive binary coding where DB7 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). The digital interface is implemented using an edge-triggered master slave latch. The DAC output is updated following the rising edge of the clock as shown in Figure 1 and is designed to support a clock rate as high as 125 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulsewidth. The setup-and-hold times can also be varied within the clock cycle as long as the specified minimum times are met; although the location of these transition edges may affect digital feedthrough and distortion performance.

The digital inputs are CMOS compatible with logic thresholds, $V_{THRESHOLD}$ set to approximately half the digital positive supply (DVDD) or

$$V_{THRESHOLD} = DVDD/2\ (\pm 20\%)$$

Figure 18 shows the equivalent digital input circuit for the data and clock inputs. The sleep mode input is similar, except that it contains an active pull-down circuit, thus ensuring that the AD9708 remains enabled if this input is left disconnected. The internal digital circuitry of the AD9708 is capable of operating over a digital supply range of 2.7 V to 5.5 V. As a result, the digital inputs can also accommodate TTL levels when DVDD is set to accommodate the maximum high level voltage, $V_{OH(MAX)}$, of the TTL drivers. A DVDD of 3 V to 3.3 V will typically ensure upper compatibility of most TTL logic families.

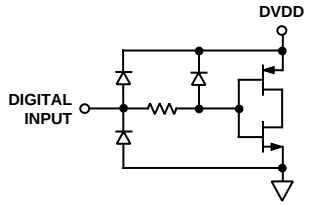


Figure 18. Equivalent Digital Input

Since the AD9708 is capable of being updated up to 125 MSPS, the quality of the clock and data input signals are important in achieving the optimum performance. The drivers of the digital data interface circuitry should be specified to meet the minimum setup-and-hold times of the AD9708 as well as its required min/max input logic level thresholds. Typically, the selection of the slowest logic family that satisfies the above conditions will result in the lowest data feedthrough and noise.

Digital signal paths should be kept short and run lengths matched to avoid propagation delay mismatch. The insertion of a low value resistor network (i.e., 20 Ω to 100 Ω) between the AD9708 digital inputs and driver outputs may be helpful in reducing any overshooting and ringing at the digital inputs that contribute to data feedthrough. For longer run lengths and high data update rates, strip line techniques with proper termination resistors should be considered to maintain "clean" digital inputs. Also, operating the AD9708 with reduced logic swings and a corresponding digital supply (DVDD) will also reduce data feedthrough.

The external clock driver circuitry should provide the AD9708 with a low jitter clock input meeting the min/max logic levels while providing fast edges. Fast clock edges will help minimize any jitter that will manifest itself as phase noise on a reconstructed waveform. However, the clock input could also be driven by via a sine wave, which is centered around the digital threshold (i.e., DVDD/2), and meets the min/max logic threshold. This may result in a slight degradation in the phase noise, which becomes more noticeable at higher sampling rates and output frequencies. Note, at higher sampling rates the 20% tolerance of the digital logic threshold should be considered since it will affect the effective clock duty cycle and subsequently cut into the required data setup-and-hold times.

SLEEP MODE OPERATION

The AD9708 has a power-down function that turns off the output current and reduces the supply current to less than 8.5 mA over the specified supply range of 2.7 V to 5.5 V and temperature range. This mode can be activated by applying a logic level "1" to the SLEEP pin. This digital input also contains an active pull-down circuit that ensures the AD9708 remains enabled if this input is left disconnected. The SLEEP input with active pull-down requires <40 μA of drive current.

The power-up and power-down characteristics of the AD9708 are dependent on the value of the compensation capacitor connected to COMP2 (Pin 23). With a nominal value of 0.1 μF, the AD9708 takes less than 5 μs to power down and approximately 3.25 ms to power back up.

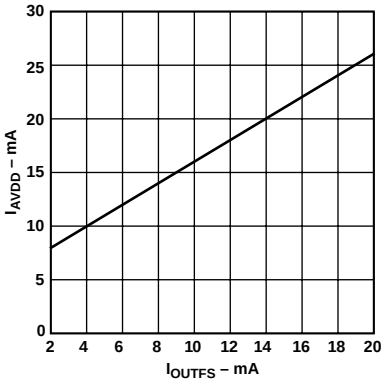


Figure 19. I_{AVDD} vs. I_{OUTFS}

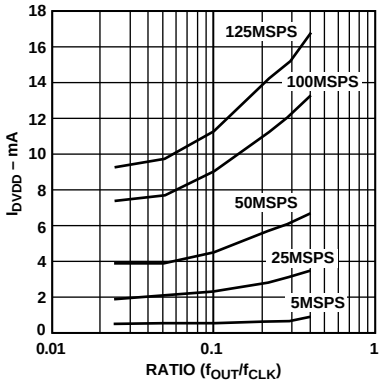


Figure 20. I_{DVDD} vs. Ratio @ DVDD = 5 V

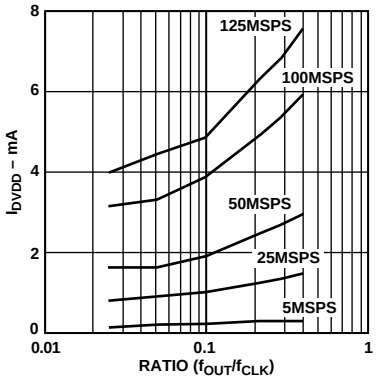


Figure 21. I_{DVDD} vs. Ratio @ DVDD = 3 V

POWER DISSIPATION

The power dissipation, P_D, of the AD9708 is dependent on several factors, including: (1) AVDD and DVDD, the power supply voltages; (2) I_{OUTFS}, the full-scale current output; (3) f_{CLOCK}, the update rate; (4) and the reconstructed digital input waveform. The power dissipation is directly proportional to the analog supply current, I_{AVDD}, and the digital supply current, I_{DVDD}. I_{AVDD} is directly proportional to I_{OUTFS}, as shown in Figure 19, and is insensitive to f_{CLOCK}.

Conversely, I_{DVDD} is dependent on both the digital input waveform, f_{CLOCK}, and digital supply DVDD. Figures 20 and 21 show I_{DVDD} as a function of full-scale sine wave output ratios (f_{OUT}/f_{CLOCK}) for various update rates with DVDD = 5 V and DVDD = 3 V, respectively. Note, how I_{DVDD} is reduced by more than a factor of 2 when DVDD is reduced from 5 V to 3 V.

APPLYING THE AD9708

Power and Grounding Considerations

In systems seeking to simultaneously achieve high speed and high performance, the implementation and construction of the printed circuit board design is often as important as the circuit design. Proper RF techniques must be used in device selection placement and routing and supply bypassing and grounding. The evaluation board for the AD9708, which uses a four layer PC board, serves as a good example for the above mentioned considerations. The evaluation board provides an illustration of the recommended printed circuit board ground, power and signal plane layouts.

Proper grounding and decoupling should be a primary objective in any high speed system. The AD9708 features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, AVDD, the analog supply, should be decoupled to ACOM, the analog common, as close to the chip as physically possible. Similarly, DVDD, the digital supply, should be decoupled to DCOM as close as physically as possible.

For those applications requiring a single +5 V or +3 V supply for both the analog and digital supply, a clean analog supply may be generated using the circuit shown in Figure 22. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained using low ESR type electrolytic and tantalum capacitors.

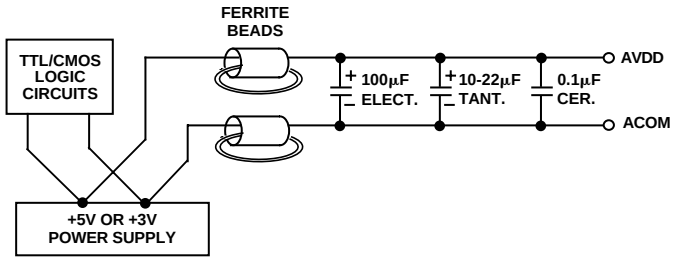


Figure 22. Differential LC Filter for Single +5 V or +3 V Applications

Maintaining low noise on power supplies and ground is critical to obtaining optimum results from the AD9708. If properly implemented, ground planes can perform a host of functions on high speed circuit boards: bypassing, shielding, current transport, etc. In mixed signal design, the analog and digital portions of the board should be distinct from each other, with the analog ground plane confined to the areas covering the analog signal traces, and the digital ground plane confined to areas covering the digital interconnects.

All analog ground pins of the DAC, reference and other analog components, should be tied directly to the analog ground plane. The two ground planes should be connected by a path 1/8 to 1/4 inch wide underneath or within 1/2 inch of the DAC to maintain optimum performance. Care should be taken to ensure that the ground plane is uninterrupted over crucial signal paths. On the digital side, this includes the digital input lines running to the DAC as well as any clock signals. On the analog side, this includes the DAC output signal, reference signal and the supply feeders.

The use of wide runs or planes in the routing of power lines is also recommended. This serves the dual role of providing a low series impedance power supply to the part, as well as providing some “free” capacitive decoupling to the appropriate ground plane. It is essential that care be taken in the layout of signal and power ground interconnects to avoid inducing extraneous voltage drops in the signal ground paths. It is recommended that all connections be short, direct and as physically close to the package as possible in order to minimize the sharing of conduction paths between different currents. When runs exceed an inch in length, strip line techniques with proper termination resistor

should be considered. The necessity and value of this resistor will be dependent upon the logic family used.

For a more detailed discussion of the implementation and construction of high speed, mixed signal printed circuit boards, refer to Analog Devices' application notes AN-280 and AN-333.

DIFFERENTIAL OUTPUT CONFIGURATIONS

For applications requiring the optimum dynamic performance and/or a bipolar output swing, a differential output configuration is suggested. A differential output configuration may consists of either an RF transformer or a differential op amp configuration. The transformer configuration is well suited for ac coupling applications. It provides the optimum high frequency performance due to its excellent rejection of common-mode distortion (i.e., even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load (i.e., assuming no source termination). The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain, and/or level shifting.

Figure 23 shows the AD9708 in a typical transformer coupled output configuration. The center-tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both IOUTA and IOUTB. The complementary voltages appearing at IOUTA and IOUTB (i.e., V_{OUTA} and V_{OUTB}) swing symmetrically around ACOM and should be maintained within the specified output compliance range of the AD9708. A differential resistor, R_{DIFF}, may be inserted in applications in which the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination. Note that approximately half the signal power will be dissipated across R_{DIFF}.

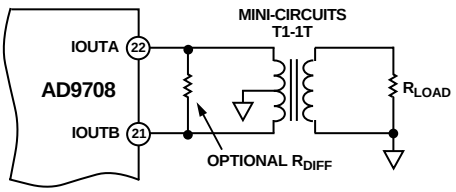


Figure 23. Differential Output Using a Transformer

An op amp can also be used to perform a differential to single-ended conversion as shown in Figure 24. The AD9708 is configured with two equal load resistors, R_{LOAD}, of 25 Ω. The differential voltage developed across IOUTA and IOUTB is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across IOUTA and IOUTB forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amps distortion performance by preventing the DACs high slewing output from overloading the op amp's input.

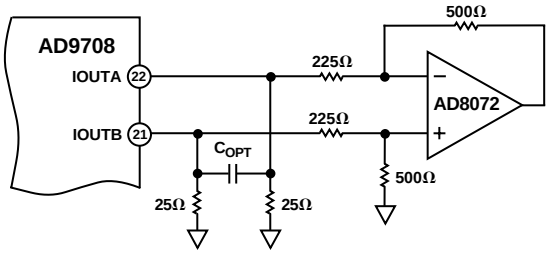


Figure 24. DC Differential Coupling Using an Op Amp

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit is configured to provide some additional signal gain. The op amp must operate off a dual supply since its output is approximately ±1.0 V. A high speed amplifier capable of preserving the differential performance of the AD9708 while meeting other system level objectives (i.e., cost, power) should be selected. The op amps differential gain, its gain setting resistor values and full-scale output swing capabilities should all be considered when optimizing this circuit.

The differential circuit shown in Figure 25 provides the necessary level-shifting required in a single supply system. In this case, AVDD, which is the positive analog supply for both the AD9708 and the op amp, is also used to level-shift the differential output of the AD9762 to midsupply (i.e., AVDD/2).

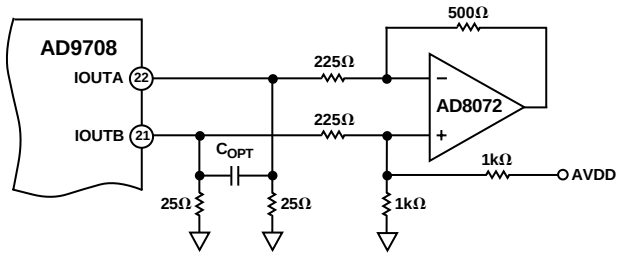


Figure 25. Single-Supply DC Differential Coupled Circuit

AD9708 EVALUATION BOARD

General Description

The AD9708-EB is an evaluation board for the AD9708 8-bit D/A converter. Careful attention to layout and circuit design, combined with a prototyping area, allows the user to easily and effectively evaluate the AD9708 in any application where high resolution, high speed conversion is required.

This board allows the user the flexibility to operate the AD9708 in various configurations. Possible output configurations include transformer coupled, resistor terminated, inverting/noninverting and differential amplifier outputs. The digital inputs are designed to be driven directly from various word generators, with the on-board option to add a resistor network for proper load termination. Provisions are also made to operate the AD9708 with either the internal or external reference, or to exercise the power-down feature.

Refer to the application note AN-420 "Using the AD9760/AD9762/AD9764-EB Evaluation Board" for a thorough description and operating instructions for the AD9708 evaluation board.

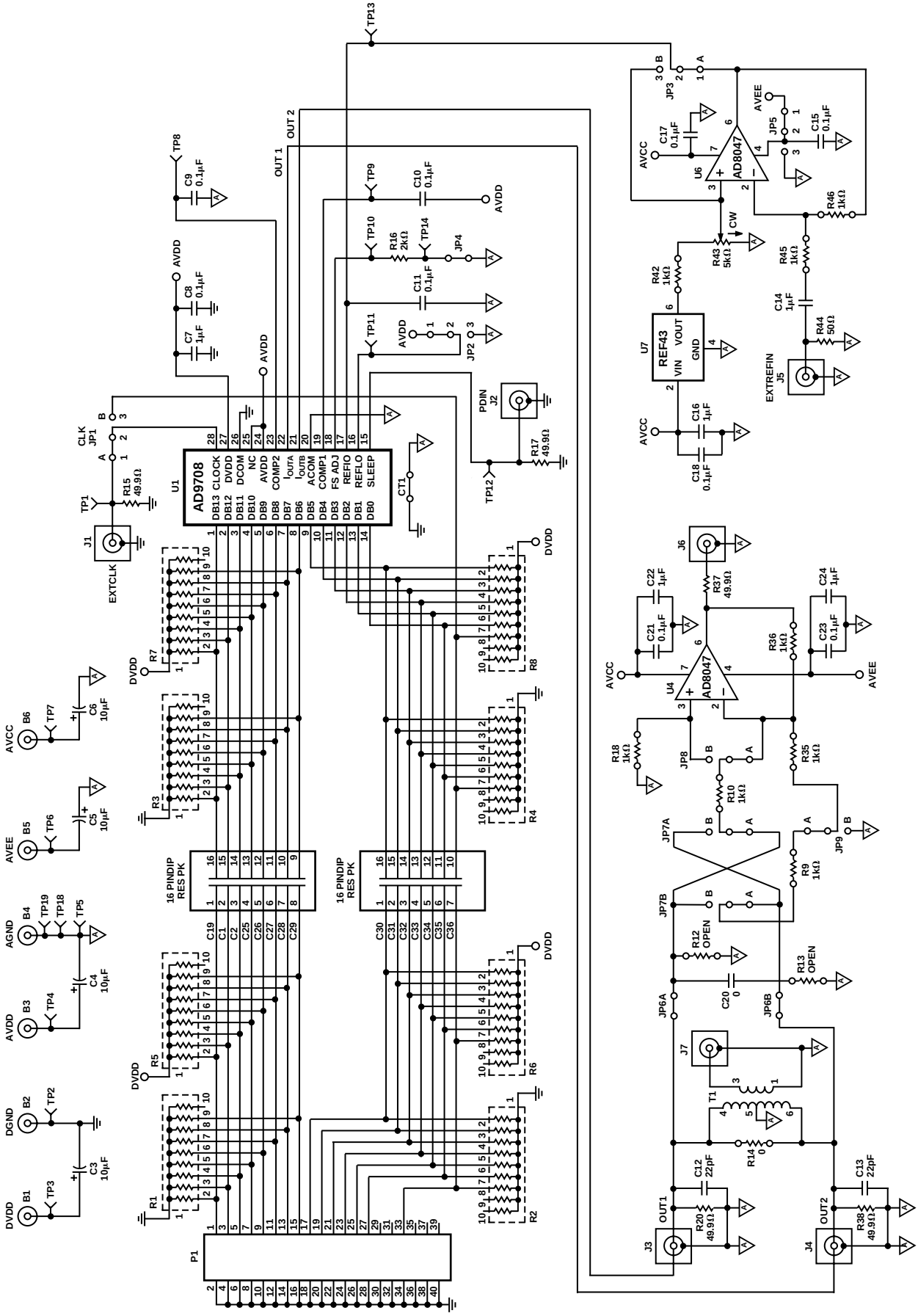


Figure 26. Evaluation Board Schematic

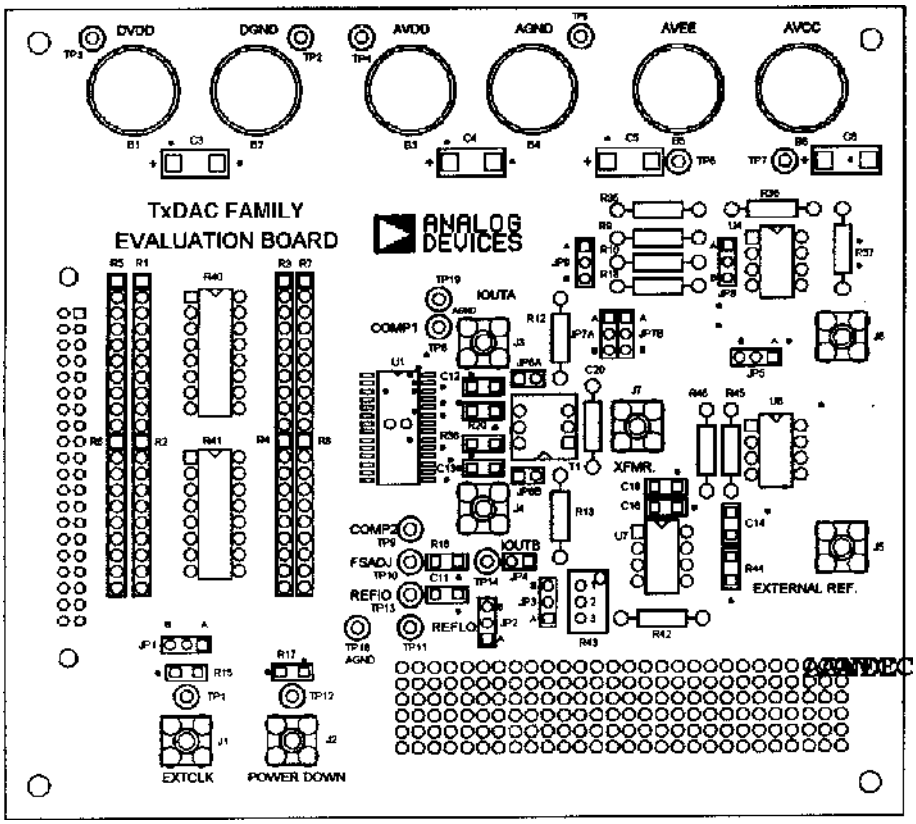


Figure 27. Silkscreen Layer—Top

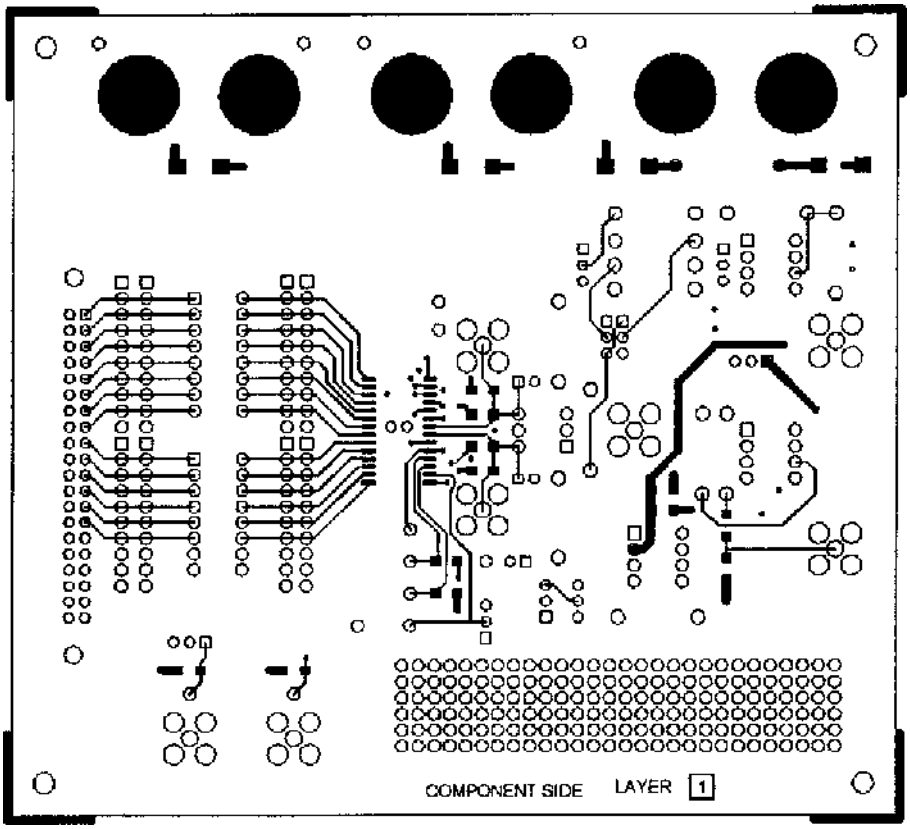


Figure 28. Component Side PCB Layout (Layer 1)

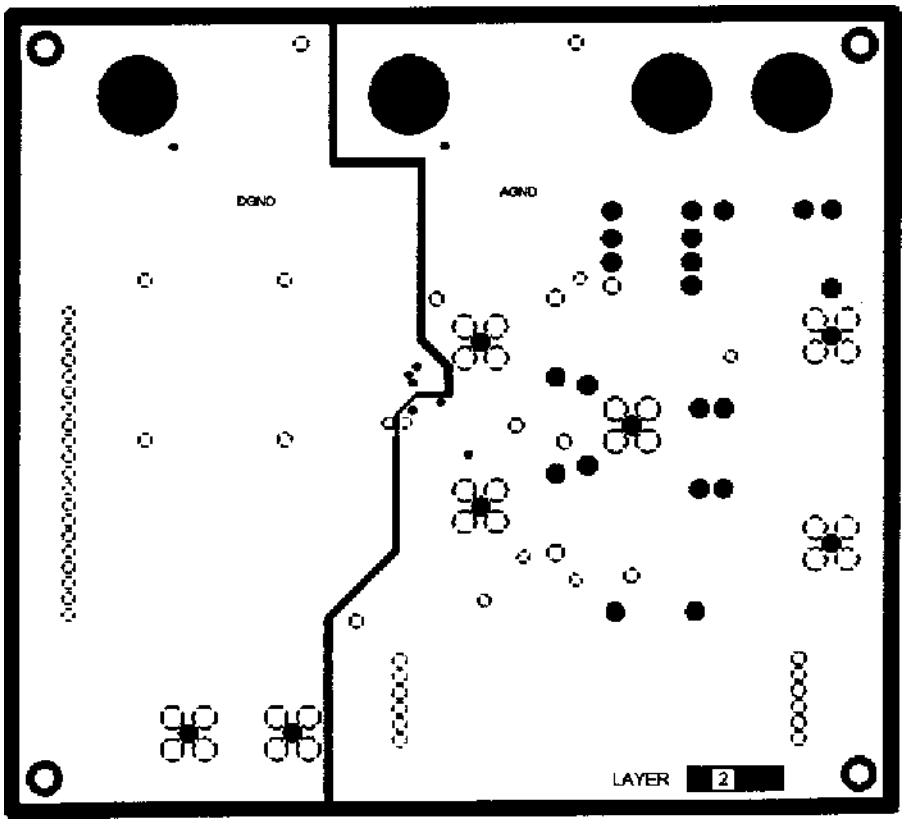


Figure 29. Ground Plane PCB Layout (Layer 2)

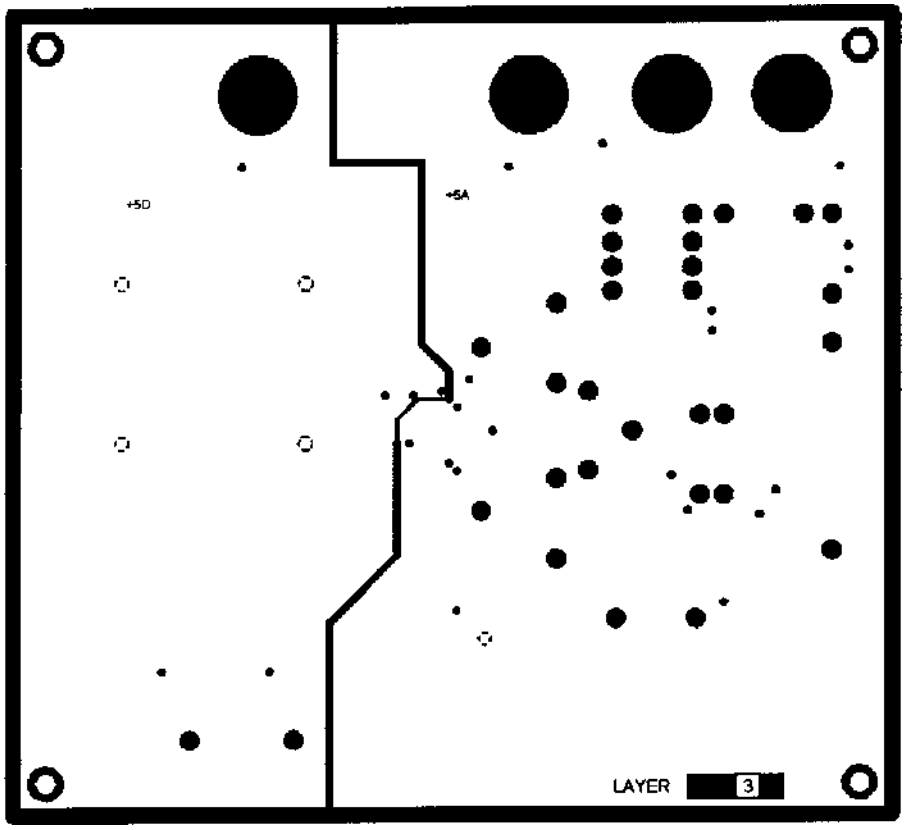


Figure 30. Power Plane PCB Layout (Layer 3)

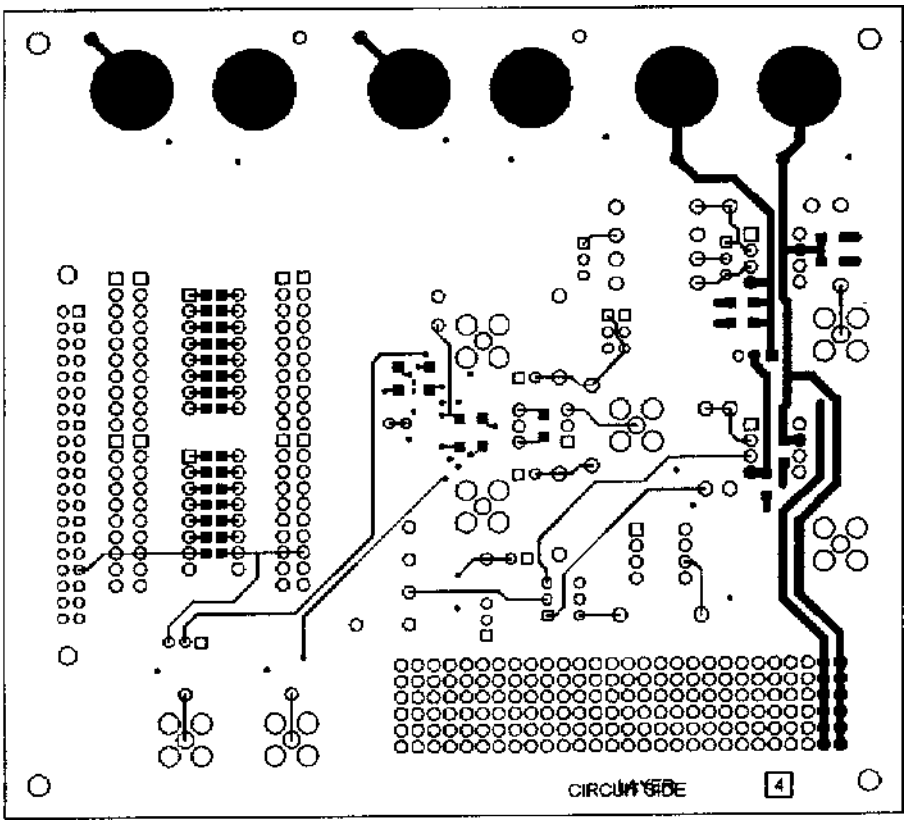


Figure 31. Solder Side PCB Layout (Layer 4)

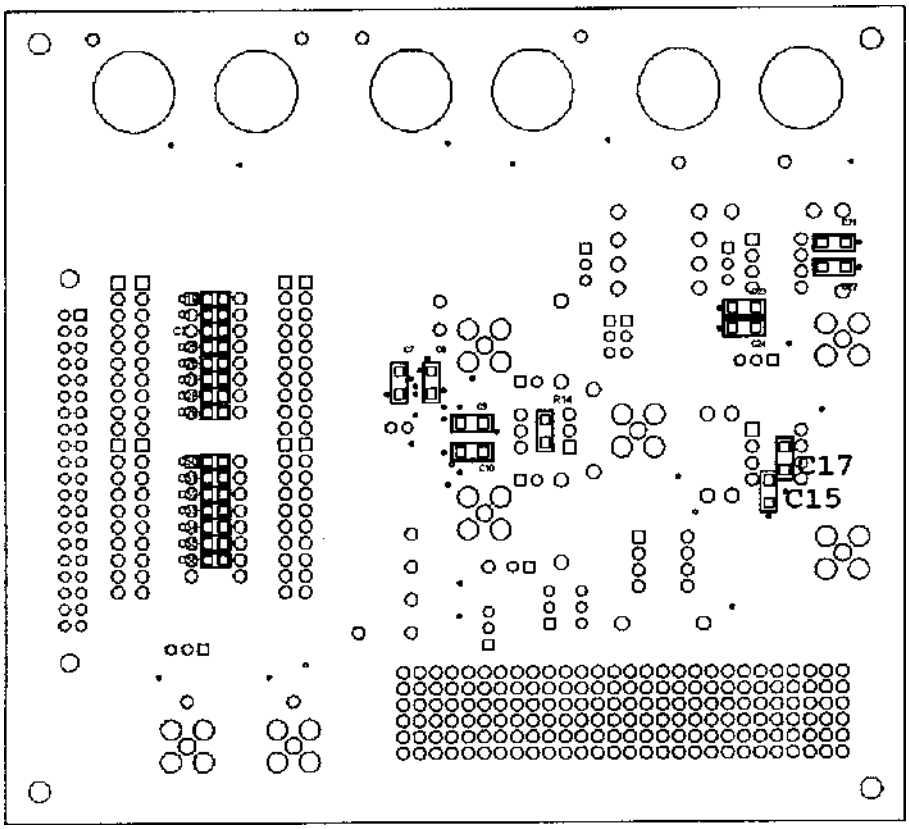
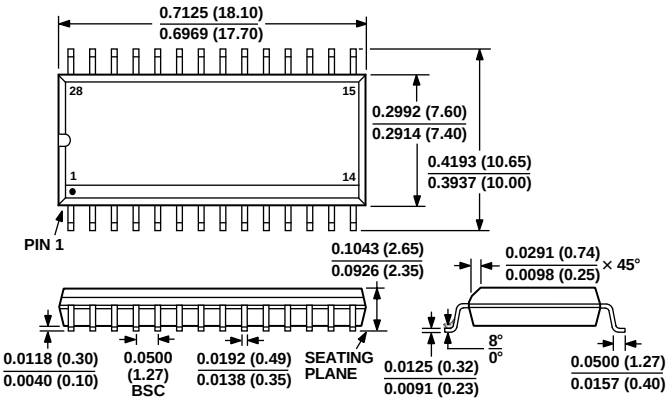


Figure 32. Silkscreen Layer—Bottom

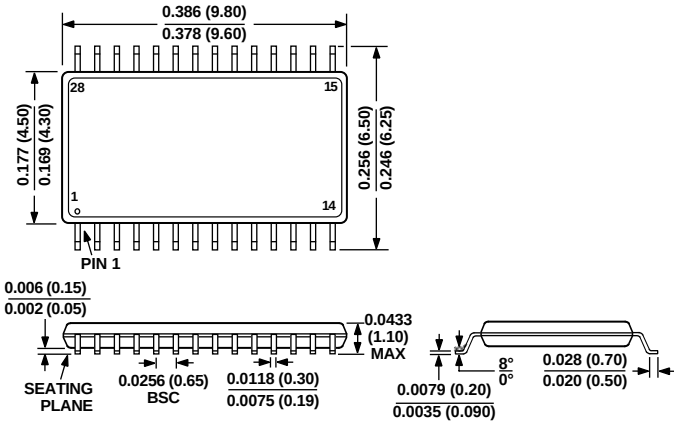
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead, 300 Mil SOIC
(R-28)



28-Lead TSSOP
(RU-28)



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