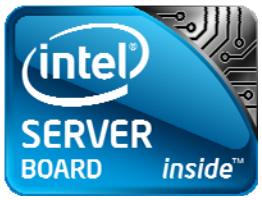
Intel® Server Board S5000VSA

Technical Product Specification

Intel order number: D36978-010



Revision 1.8

June 2010

Enterprise Platforms and Services Division – Marketing

Revision History

Date	Revision Number	Modifications
April 2006	1.0	Initial external release.
September 2006	1.1	Document updates.
November 2006	1.2	Document updates.
December 2006	1.3	Document updates, revised memory configuration guideline and clarified support for memory mirroring on the Intel® Server Board S5000VSA.
August 2007	1.4	Updated processor support and product codes.
March 2009	1.5	Updated the Memory capability from 16 G to 32 G.
June 2009	1.6	Updated section 5.3.
May 2010	1.7	Removed CCC and CNCA.
June 2010	1.8	Updated Sections 4.3.1 and 4.5.1.

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1. Introduction

This Technical Product Specification (TPS) provides board specific information detailing features, functionality, and high-level architecture of the Intel® Server Board S5000VSA. For more in-depth detail of various board sub-systems including chipset, BIOS, and system management, you can also reference the Intel® 5000 Series Chipset Server Board Family Datasheet.

In addition, you can obtain design-level information for specific sub-systems by ordering the External Product Specifications (EPS) or External Design Specifications (EDS) for a given sub-system. EPS and EDS documents are not publicly available and must be ordered through your local Intel representative.

1.1 Chapter Outline

This document is divided into the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – Intel® Server Board S5000VSA Overview
- Chapter 3 – Functional Architecture
- Chapter 4 – Platform Management
- Chapter 5 – Connector/Header Location and Pin-out
- Chapter 6 – Jumper Block Settings
- Chapter 7 – Intel® Light-Guided Diagnostics
- Chapter 8 – Power and Environmental Specifications
- Chapter 9 – Regulatory and Certification Information
- Appendix A – Integration and Usage Tips
- Appendix B – Sensor Tables
- Appendix C – POST Error Messages and Handling
- Glossary

1.2 Server Board Use Disclaimer

Intel® Server Boards support add-in peripherals and contain high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

2. Product Overview

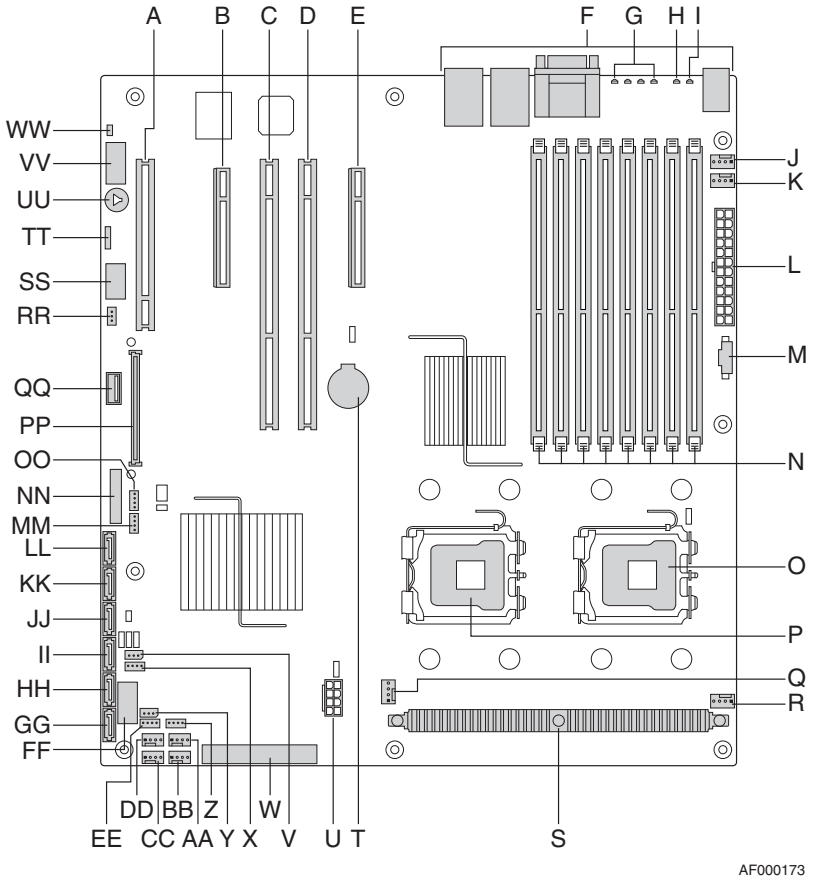
The Intel® Server Board S5000VSA is a monolithic printed circuit board (PCB) with features designed to support the pedestal server markets.

2.1 Feature Set

Table 1. Feature Set

Feature	Description
Processors	771-pin LGA sockets supporting the following processors: ▪ One or two Dual-Core Intel® Xeon® processors 5000 or 5100 sequence with a ▪ 677-, 1066-, or 1333-MHz front side bus with frequencies starting at 2.67 GHz. ▪ Up to two Quad-Core Intel® Xeon® processors 5300 sequence with a 1066- or ▪ 1333-MHz front side bus. ▪ Up to two 45 nm 2P Dual-Core Intel® Xeon® processors. Product codes S5000VSASATAR, S5000VSASASR, S5000VSASCSIR, and S5000VSA4DIMMR only. ▪ Up to two 45 nm next generation Quad-Core Intel® Xeon® processors. Product codes S5000VSASATAR, S5000VSASASR, S5000VSASCSIR, and S5000VSA4DIMMR only.
Memory	Maximum support for 32 GB. Four or eight (based on board SKU type) DIMM slots supporting fully buffered DIMM technology (FBDIMM) memory. 240-pin DDR2-533 and DDR2-667 FBDIMMs may be used. **Note:** Full DIMM heat spreaders are required.
Chipset	Intel® S5000V chipset, including: ▪ Intel® S5000V MCH ▪ Intel® ESB2-E
I/O Control	External connections: ▪ Stacked PS/2* ports for keyboard and mouse ▪ DB9 Serial port ▪ Two RJ-45 NIC connectors for 10/100/1000 Mb connections ▪ Seven USB 2.0 ports (4 rear, 2 front, and 1 floppy) Internal Connections: o One RS-232 Serial o One P-ATA133 o Six SATA (300MB) connectors with integrated RAID 0/1/5/10 support ▪ SSI-compliant front panel header ▪ SSI-compliant 24-pin main power connector, supporting the ATX-12V standard on the first 20 pins.
Video	On-board ATI* ES1000 video controller with 16MB DDR SDRAM external video memory
Hard Drives	Support for six SATA-300 hard drives
LAN	Intel® 82563EB dual port controller for 10/100/1000 Mbit/sec Ethernet LAN connectivity
Fans	Support for two processor fans, five system fans, and one memory fan
System Management	Support for Intel® System Management Software

2.2 Server Board Layout



A. PCI 32/33 Slot 1	B. PCI Express* x4 Slot 3	C. PCI-X* 64/133 Slot 4
D. PCI-X* 64/100 Slot 5	E. PCI Express* x4 Slot 6	F. Back Panel I/O Ports
G. Diagnostic LEDs	H. System ID LED	I. System Status LED
J. System Fan 6	K. System Fan 5	L. Main Power Connector
M. Auxiliary Signal Connector	N. DIMM Sockets	O. Processor 1 Socket
P. Processor 2 Socket	Q. Processor Fan 2 Header	R. Processor Fan 1 Header
S. Processor Voltage Regulator	T. Battery	U. Processor Power Connector
V. IPMB Header	W. SAS RAID5 Key	X. IDE Connector
Y. LCP Header	Z. SAS_SES2	AA. SAS SGPIO
BB. System Fan 3	CC. System Fan 4	DD. System Fan 2
EE. System Fan 1	FF. SATA SGPIO	GG. USB 4-5
HH. SATA 0 Connector	II. SATA 1 Connector	JJ. SATA 2/SAS 0 Connector
KK. SATA 3/SAS 1 Connector	LL. SATA 4/SAS 2 Connector	MM. SATA 5/SAS 3 Connector
NN. Backplane Connector B	OO. Front Panel Header	PP. Backplane Connector A
QQ. USB 6(J1E2)	RR. SATA RAID5 Key	SS. Speaker
TT. Serial B EMP Connector	UU. Chassis Intrusion	

Note: The USB 6 (J1E2) port (Q), the diagnostic LEDs (G), the system ID LED (H), and the system status LED (I) are not included on the Intel® Server Board S5000VSA4DIMM/S5000VSA4DIMMR boards.

Figure 1. Intel® Server Board S5000VSA picture

2.2.1 Server Board Mechanical Drawing

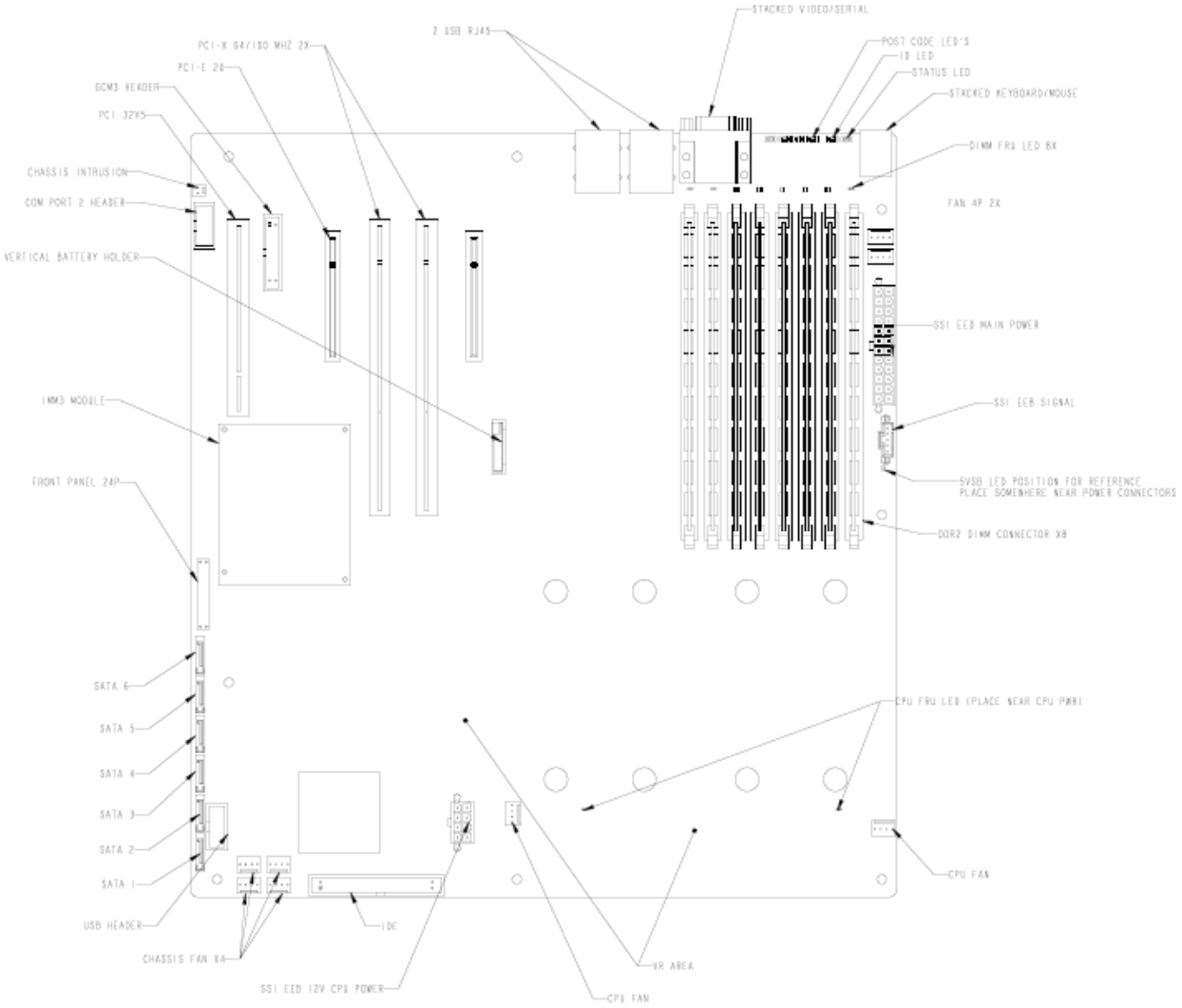


Figure 2. Intel® Server Board S5000VSA – Key Connectors and LED Indicators

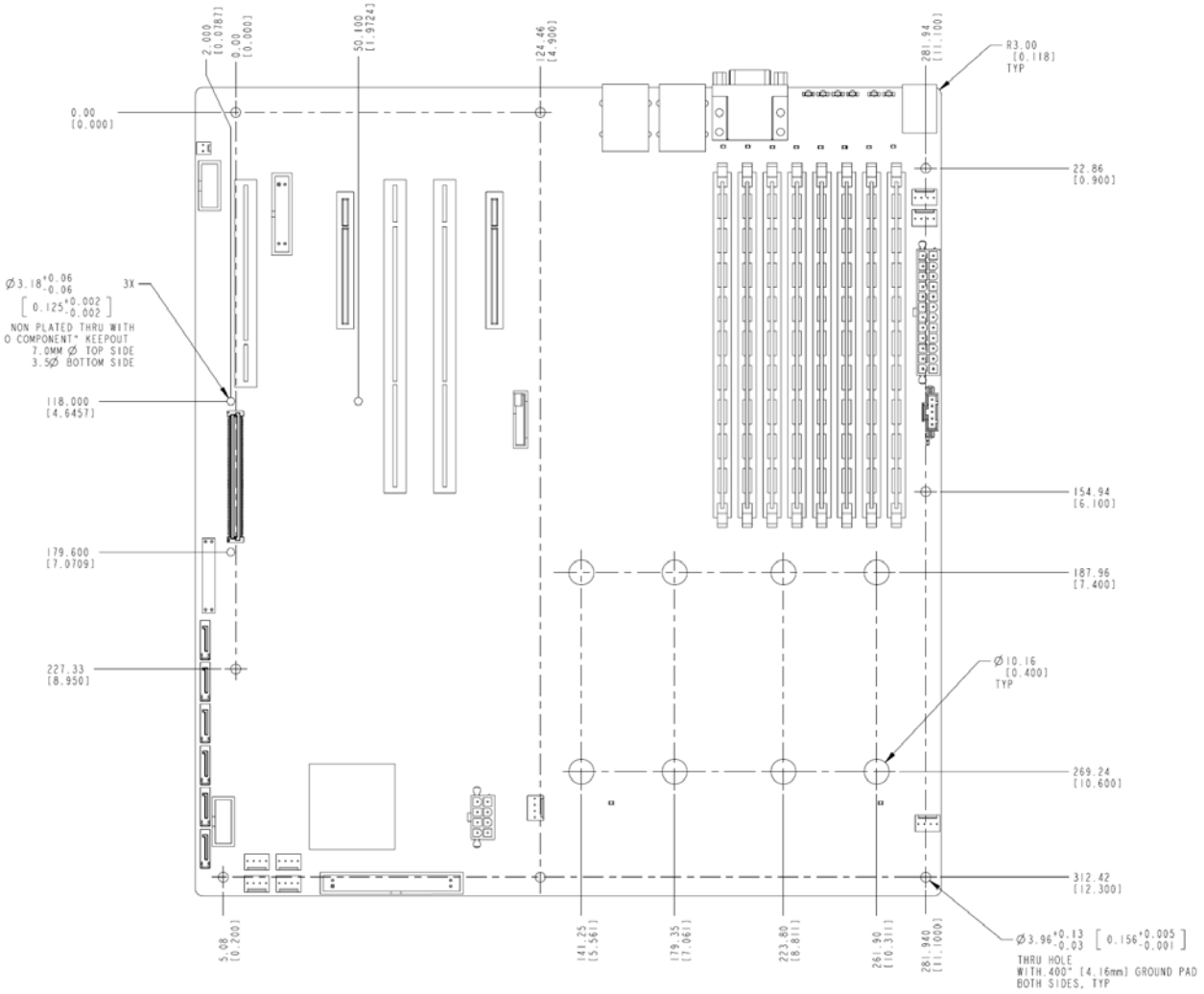


Figure 3. Intel® Server Board S5000VSA – Mounting Hole Locations

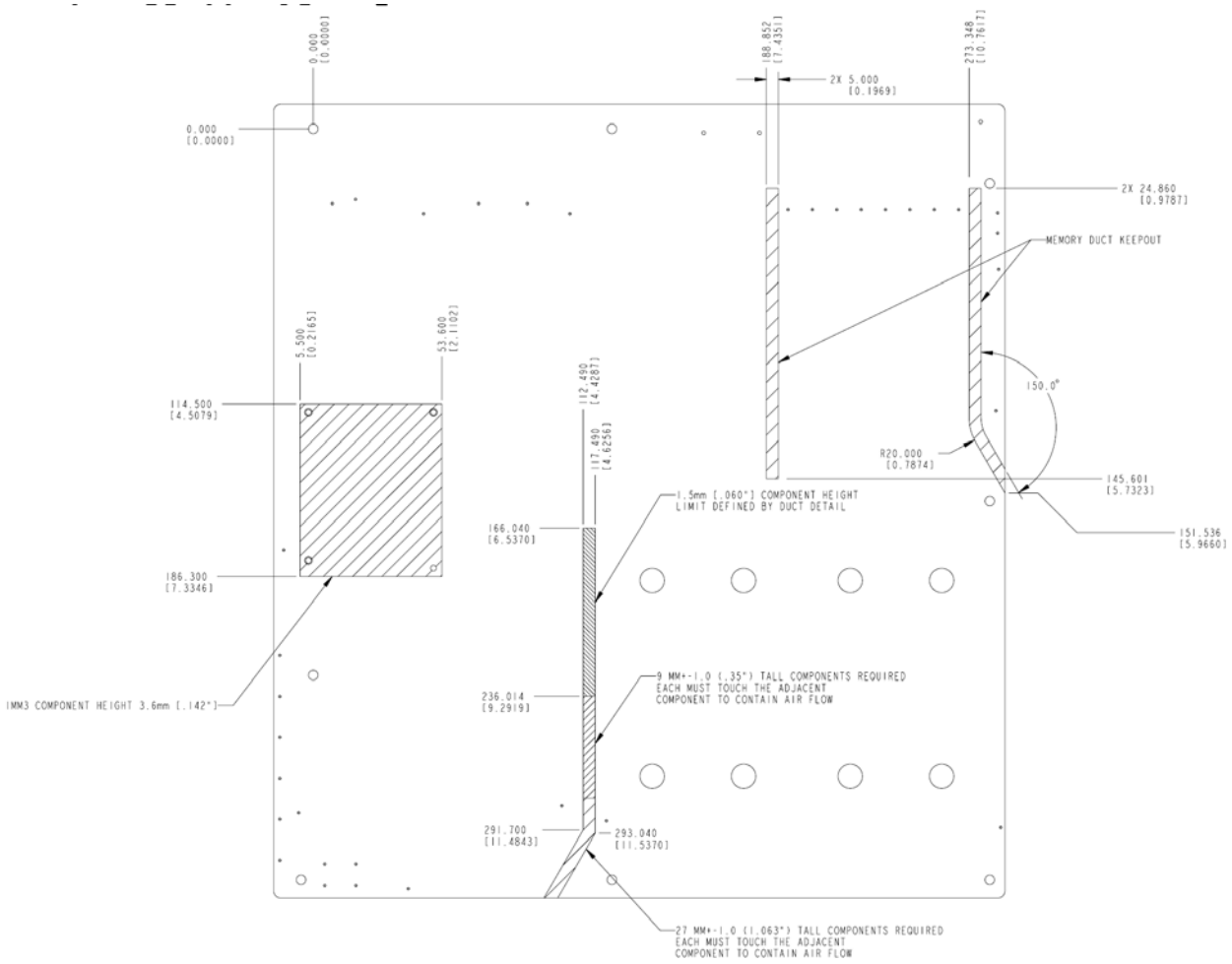


Figure 4. Intel® Server Board S5000VSA – Duct Keep Out Detail

2.3 Feature Set

The following figure shows the layout of the rear I/O components for the server board.

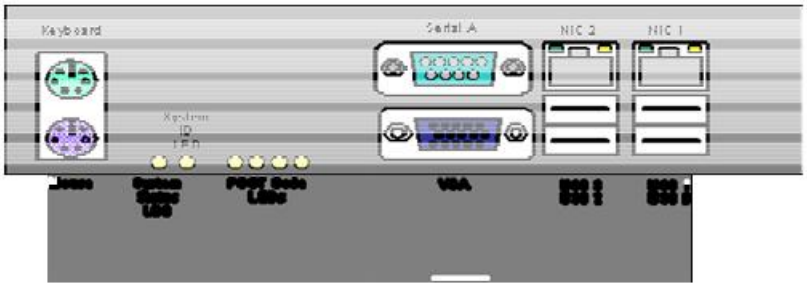


Figure 5. Intel® Server Board S5000VSA ATX I/O Layout

3. Functional Architecture

The architecture and design of the Intel® Server Board S5000VSA is based on the Intel® 5000V Chipset. The chipset is designed for systems based on the Intel® Xeon® processor 5000 or 5100 sequence and supports Front Side Bus (FSB) frequencies of 1066 MTS/1333 MTS. The chipset contains two main components: the Memory Controller Hub (MCH) for the host bridge, and the I/O controller hub for the I/O sub-system.

The Intel® 5000V chipset uses the Enterprise South Bridge (ESB2-E) for the I/O controller hub. This chapter provides a high-level description of the functionality associated with each chipset component and the architectural blocks that make up the Intel® Server Board S5000VSA. For more detailed descriptions for each of the functional architecture blocks, refer to the Intel® 5000 Series Chipset Server Board Family Datasheet.

3.1 Intel® 5000V Controller Hub (MCH)

The Intel® 5000V Memory Controller Hub (MCH) chip is packaged in a 1432 pin FCBGA package. It supports the Intel® Xeon® processor 5000 sequence (1067 MTS/1333 MTS) package. This package uses the matching LGA771 socket.

3.1.1 Processor Sub-system

The MCH supports a FSB frequency of 267MHz/333MHz (1067 MTS/1333 MTS) using a point-to-point, dual inline bus (DIB) processor system bus interface. Each processor FSB supports a peak address generation rates of 133 million addresses per second. Both FSB data buses are quad-pumped 64-bits, which allow peak bandwidths of 8.5GB/s (1067MT/s) or 10.7GB/s (1333MT/s) depending on the processor used.

The support circuitry for the processor sub-system consists of the following:

- Dual LGA771 zero insertion force (ZIF) processor sockets
- Processor host bus AGTL+ support circuitry
- Reset configuration logic
- Processor module presence detection logic
- BSEL detection capabilities
- CPU signal level translation
- Common Enabling Kit Direct Chassis Attach (CEK DCA) CPU retention support

For detailed information about the functional architecture provided by the chipset, refer to the Intel® 5000 Series Chipset Server Board Family Datasheet.

3.1.1.1 Processor Support

The server board supports the following processors:

- One or two Intel® Xeon® processors 5000 or 5100 sequence with a 677-, 1066-, or 1333-MHz front side bus (FSB) with frequencies starting at 2.67 GHz.
- Up to two Intel® Xeon® processors 5300 sequence with a 1066- or 1333-MHz front side bus.
- Up to two 45 nm 2P Intel® Xeon® processors. Product codes S5000VSASATAR, S5000VSASASR, S5000VSASCSIR, and S5000VSA4DIMMR only.
- Up to two 45 nm next generation Intel® Xeon® processors. Product codes S5000VSASATAR, S5000VSASASR, S5000VSASCSIR, and S5000VSA4DIMMR only.

This server board does not support previous generations of the Intel® Xeon® processor. Refer to the following table for a detailed list of supported, multi-core Intel® Xeon® processors 5000 sequence. For a complete updated list of supported processors, refer to: http://support.intel.com/support/motherboards/server/s5000vsa/.

Table 2. Processor Support Matrix

CPU Number	sSpec Number	Core Speed	Bus Speed	L2 Cache Size	Core Stepping	Notes (See Below)
Intel® Xeon® Processor 5300 series:						
X5355	SLAC4	2.66 GHz	1333 MHz	8 MB	B3	4,5
X5355	SL9YM	2.66 GHz	1333 MHz	8 MB	B3	4,5
E5345	SLAC5	2.33 GHz	1333 MHz	8 MB	B3	4,5
E5345	SL9YL	2.33 GHz	1333 MHz	8 MB	B3	4,5
E5335	SLAC7	2.00 GHz	1333 MHz	8 MB	B3	4,5
E5335	SL9YK	2.00 GHz	1333 MHz	8 MB	B3	4,5
E5320	SLAC8	1.86 GHz	1066 MHz	8 MB	B3	4,5
E5320	SL9MV	1.86 GHz	1066 MHz	8 MB	B3	4,5
L5320	SLAC9	1.86 GHz	1066 MHz	8 MB	B3	4,5,6
L5320	SLA4Q	1.86 GHz	1066 MHz	8 MB	B3	4,5,6
E5310	SLACB	1.60 GHz	1066 MHz	8 MB	B3	4,5
E5310	SL9XR	1.60 GHz	1066 MHz	8 MB	B3	4,5
L5310	SLACA	1.60 GHz	1066 MHz	8 MB	B3	4,5,6
L5310	SLAEQ	1.60 GHz	1066 MHz	8 MB	B3	4,5,6
L5310	SL9MT	1.60 GHz	1066 MHz	8 MB	B3	4,5,6
Intel® Xeon® Processor 5100 series:						
5160	SLABS	3.00 GHz	1333 MHz	4 MB	B2	2
5160	SL9RT	3.00 GHz	1333 MHz	4 MB	B2	2
5150	SLABM	2.66 GHz	1333 MHz	4 MB	B2	2
5150	SL9RU	2.66 GHz	1333 MHz	4 MB	B2	2
5148	SLABH	2.33 GHz	1333 MHz	4 MB	B2	2,3, 7
5148	SL9RR	2.33 GHz	1333 MHz	4 MB	B2	2,7
5140	SLABN	2.33 GHz	1333 MHz	4 MB	B2	2
5140	SL9RW	2.33 GHz	1333 MHz	4 MB	B2	2
5138	SL9RN	2.13 GHz	1066 MHz	4 MB	B2	8
5130	SLABP	2.00 GHz	1333 MHz	4 MB	B2	2
5130	SL9RX	2.00 GHz	1333 MHz	4 MB	B2	2
5120	SLABQ	1.86 GHz	1066 MHz	4 MB	B2	2

CPU Number	sSpec Number	Core Speed	Bus Speed	L2 Cache Size	Core Stepping	Notes (See Below)
5120	SL9RY	1.86 GHz	1066 MHz	4 MB	B2	2
5110	SLABR	1.60 GHz	1066 MHz	4 MB	B2	2
5110	SL9RZ	1.60 GHz	1066 MHz	4 MB	B2	2
Dual-Core Intel® Xeon® Processor 5000 series:						
5030	SL96E	2.67 GHz	667 MHz	2x2MB	C1	
5050	SL96C	3.00 GHz	667 MHz	2x2MB	C1	
5060	SL96A	3.20 GHz	1066 MHz	2x2MB	C1	
5063	SL96B	3.20 GHz	1066 MHz	2x2MB	C1	1
5080	SL968	3.73 GHz	1066 MHz	2x2MB	C1	

Notes:

1. Intel® Xeon® processor 5063 is a medium voltage SKU with lower wattage consumption—ideal for rack servers.
2. Your Intel® Server Board requires BIOS version 54 or later to support this processor.
3. Intel® Xeon® processor LV 5148 is a low voltage SKU with lower wattage consumption—ideal for rack servers.
4. Intel® Xeon® processor 5300 series employs Intel® Advanced Smart Cache (Shared Cache). Features 4 MB Smart Cache per core pair.
5. Important Information on: http://www.intel.com/support/motherboards/server/sb/CS-023585.htm of the Intel® Xeon® processor 5300 series.
6. These processors have a Thermal Design Power (TDP) of 50 W.
7. These processors have a TDP of 40 W.

3.1.2 Thermal Design Power of 35 W (Processor Population Rules)

When two processors are installed, both must be of identical revision, core voltage, and bus/core speed. When only one processor is installed, it must be in the socket labeled CPU1. The other socket must be empty.

You must populate the processors in sequential order. Therefore, you must populate processor socket 1 (CPU1) *before* processor socket 2 (CPU2).

The board is designed to provide up to 130 A of current per processor. This server board does not support processors with higher current requirements.

No terminator is required in the second processor socket when using a single processor configuration.

3.1.3 Common Enabling Kit (CEK) Design Support

The server board complies with Intel's Common Enabling Kit (CEK) processor mounting and heatsink retention solution. The server board ships with a CEK spring snapped onto the underside of the server board, beneath each processor socket. The heatsink attaches to the CEK over the top of the processor and the thermal interface material (TIM). Refer to the

following figure for the stacking order of the chassis, CEK spring, server board, TIM, and heatsink.

The CEK spring is removable, allowing the use of non-Intel heatsink retention solutions.

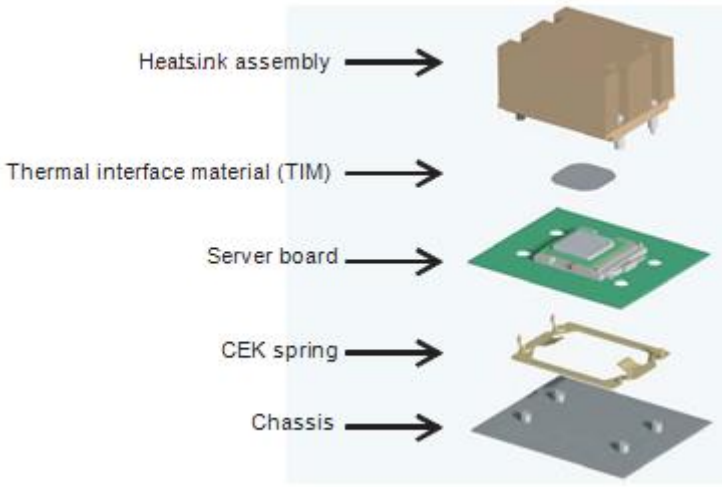


Figure 6. CEK Processor Mounting

3.1.4 Memory Sub-system

The MCH provides two channels of fully buffered DIMM (FB-DIMM) memory. Each channel can support up to 4 DIMMs. FB-DIMM memory channels are organized in to a single branch. The MCH can support up to 8 DIMM or a maximum memory size of 32 GB. The read bandwidth for each FB-DIMM channel is 4.25 GB/s for DDR533 FB-DIMM memory, which gives a total read bandwidth of 8.5 GB/s for two FB-DIMM channels. The read bandwidth for each FB-DIMM channel is 5.35 GB/s for DDR667 FB-DIMM memory which gives a total read bandwidth of 10.7GB/s for two FB-DIMM channels. Therefore, this provides 2.65 GB/s of write memory bandwidth for two FB-DIMM channels. This bandwidth is based on read bandwidth; therefore, the total bandwidth is 8.5 GB/s for 533 FB-DIMM and 10.7 GB/s for 667 FB-DIMM.

To boot the system, the system BIOS on the server board uses a dedicated I^2C bus to retrieve DIMM information needed to program the MCH memory registers. The following table provides the I^2C addresses for each DIMM slot:

Table 3. I^2C Addresses for Memory Module SMB

Device	Address
DIMM A1	0xA0
DIMM A2	0xA2
DIMM A3	0xA4
DIMM A4	0xA6
DIMM B1	0xA0
DIMM B2	0xA2
DIMM B3	0xA4
DIMM B4	0xA6

3.1.5 Supported Memory

The server board supports up to eight (four for the 4-DIMM SKU) DDR2-533 or DDR2-667 Fully Buffered DIMM memory (FBDIMM memory). This board does NOT support non-fully buffered DDR2 DIMMs. The following tables show the maximum memory configurations supported using specified memory technology.

Table 4. Maximum 8 DIMM System Memory Configuration – x8 (Width) Single Rank = 1 Load

DRAM Technology x8 Single Rank (64M8=64M x 8b=16M x 8b x 4 banks)	Maximum Capacity
512 Mb (Density)	2 GB

Table 5. Maximum 8 DIMM System Memory Configuration – x4 (Width) Dual Rank = 2 Loads

DRAM Technology x4 Dual Rank(128M4=128M x4b=32M x 4b x 4 banks)	Maximum Capacity
512 Mb (Density)	4 GB

3.1.6 DIMM Population Rules

DIMM population rules depend on the operating mode of the memory controller. On the server board, you must populate DIMMs in the following order: A1 and B1, A2 and B2, and so forth. The server board will support the population of DIMMs with different speed ratings; however, this is not recommended. The overall system memory speed is determined by the slowest DIMM populated.

3.1.6.1.1 Minimum Configuration

The following diagram shows a minimum two DIMM memory configuration for the server board. Populated DIMM slots are shown in Gray.

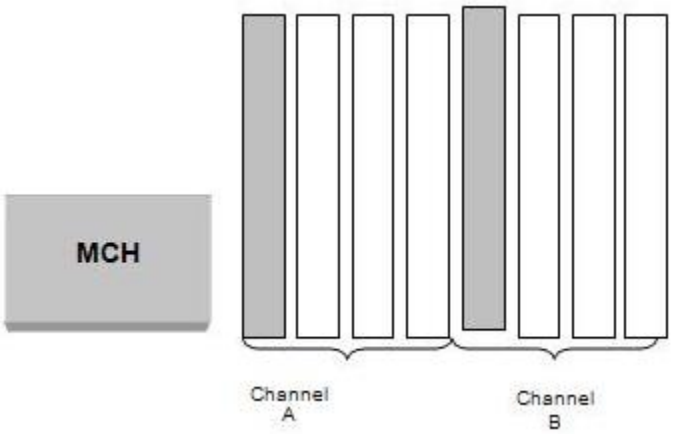


Figure 7. Minimum Two DIMM Memory Configuration

Note: The server board BIOS supports single DIMM mode operation, although this is generally not recommended for “performance” applications. This configuration is only supported with a 512MB FBDIMM installed in DIMM slot A1.

The Intel® Server Board S5000VSA (all SKUs) does not support the memory mirroring feature; this is a chipset limitation.

3.1.7 Memory Mirroring

The Intel® 5000P MCH and Intel® 5000X MCH components provide the ability to configure the available set of FBDIMMs in the mirrored configuration. Server boards with only one memory branch do not support memory mirroring.

Memory RAS Limitation:
The Intel® Server Board S5000VSA uses the Intel® 5000V MCH chipset. The Intel® 5000V has only one memory branch. Consequently, memory mirroring is not supported and memory is limited to a maximum of 32 GB.

3.1.7.1.1 Memory Upgrades

The minimum memory upgrade increment is two DIMMs. The DIMMs must cover the same slot number on both channels. DIMMs that cover a slot number must be identical with respect to size, speed, and organization. DIMMs that cover adjacent slot positions do need to be identical.

When adding two DIMMs to the configuration shown in the following figure, you should populate the DIMMs in DIMM slots A2 and B2 as shown. Populated DIMM slots are shown in Gray.

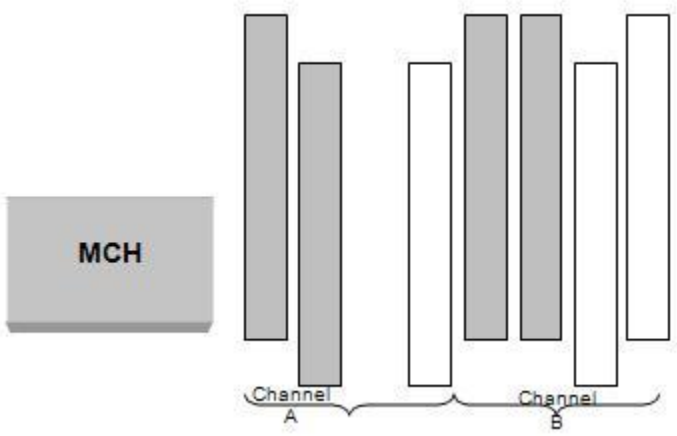


Figure 8. Minimum Two DIMM Memory Configuration

3.2 Enterprise South Bridge (ESB2-E)

The ESB2-E is a multi-function device that merges four distinct functions: an ICH6-like controller; a PCI-X* Bridge, a Gigabit Ethernet controller, and a BMC. Each function within the ESB2-E has its own set of configuration registers. Once configured, each appears to the system as a distinct hardware controller.

A primary role of the ESB2-E is to provide the gateway to all PC-compatible I/O devices and features. The baseboard uses the following ESB2-E features:

- PCI-X* bus interface
- Six Channel SATA interface w/SATA Busy LED Control
- Dual Gbe MAC
- Baseboard Management Controller (BMC)
- Single ATA interface with Ultra DMA 100 capability
- Universal Serial Bus 2.0 (USB) interface
- LPC bus interface
- PC-compatible timer/counter and DMA controllers
- APIC and 8259 interrupt controller
- Power management
- System RTC
- General purpose I/O

This section describes the function of each I/O interface and how they operate on the server board.

3.2.1 PCI Sub-system

3.2.2 PCI Express* Overview

The MCH supports three x4 PCI Express* ports. PCI Express is a high-speed, frame-based, serial I/O interface that can achieve peak theoretical bandwidths of 2 GB/s per x4 port (1 GB/s in each direction). You can configure these ports in a number of different combinations thus enhancing the scalability and performance of the system. The following is the PCI Express* port configuration used by the server board.

Server Board Configuration:

Port 0 (x4): Otherwise known as the Enterprise Server Interface (ESI) port, Port [0] connects to the ESB2-E. Although the ESI port follows the standard PCI Express* protocol, it also executes proprietary commands only used between Intel chipsets.

Port 2 and Port 3 (2 x4 = x8): Otherwise known as the Direct Memory Access (DMA) port, x4 Ports [3:2] combine to create a x8 port which also connects to the ESB2-E. The DMA port follows the standard PCI Express* protocol, but allows direct access to memory for higher speed I/O transactions.

3.2.3 PCI Express* Hot-Plug

The server board does not support PCI Express* hot-plug.

3.2.4 SATA Support

The integrated Serial ATA (SATA) controller of the ESB2-E provides six SATA ports on the server board. You can enable/disable and/or configure the SATA ports by accessing the BIOS Setup Utility during POST.

The SATA function in the ESB2-E has dual modes of operation to support different operating system conditions. In the case of native IDE-enabled operating systems, the ESB2-E has separate PCI functions for serial and parallel ATA. To support legacy operating systems, there is only one PCI function for both the serial and parallel ATA ports. The MAP register provides the ability to share PCI functions. When sharing is enabled, all decode of I/O is done through the SATA registers. A software write to the Function Disable Register (D31, F0, offset F2h, bit 1) causes Device 31, Function 1 (IDE controller) to hidden, and its configuration registers are not used. The SATA Capability Pointer Register (offset 34h) will change to indicate that MSI is not supported in the combined mode.

The ESB2-E SATA controller features two sets of interface signals that can be independently enabled or disabled. Each interface is supported by an independent DMA controller. The ESB2-E SATA controller interacts with an attached mass storage device through a register interface that is equivalent to that presented by a traditional IDE host adapter. The host software follows existing standards and conventions when accessing the register interface and follows standard command protocol conventions.

SATA interface transfer rates are independent of UDMA mode settings. SATA interface transfer rates operate at the bus's maximum speed, regardless of the UDMA mode reported by the SATA device or the system BIOS.

3.2.5 SATA RAID

The Intel® Embedded RAID Technology II solution, available with the ESB2-E ICH6, offers data striping for higher performance (RAID Level 0), alleviating disk bottlenecks by taking advantage of the dual independent SATA controllers integrated in the ESB2-E ICH6. There is no loss of PCI resources (request/grant pair) or add-in card slot.

Intel® Embedded RAID Technology II functionality requires the following items:

- ESB2-E ICH6
- Intel® Embedded RAID Technology II Option ROM must be on the server board
- Intel® Application Accelerator RAID Edition drivers, most recent revision
- Two SATA hard disk drives

Intel® Embedded RAID Technology II is not available in the following configurations:

- The SATA controller in compatible mode.
- Intel® Embedded RAID Technology II is disabled.

3.2.6 Intel® Embedded RAID Technology II Option ROM

The Intel® Embedded RAID Technology II for SATA Option ROM provides a pre-operating system user interface for the Intel® Embedded RAID Technology II implementation and provides the ability for an Intel® Embedded RAID Technology II volume to be used as a boot disk and detect any faults in the Intel® Embedded RAID Technology II volume(s) attached to the Intel® RAID controller.

3.2.7 Parallel ATA (PATA) Support)

The integrated IDE controller of the ESB2-E ICH6 provides one IDE channel. This IDE channel is capable of supporting one optical drive. A standard high density 40-pin IDE connector interfaces with the primary IDE channel signals. You can configure and enable or disable the IDE channels by accessing the BIOS Setup Utility during POST.

The BIOS supports the ATA/ATAPI Specification, version 6 or later. It initializes the embedded IDE controller in the chipset south-bridge and the IDE devices connected to these devices. The BIOS scans the IDE devices and programs the controller and devices with their optimum timings. The IDE disk read/write services provided by the BIOS use PIO mode, but the BIOS programs the necessary Ultra DMA registers in the IDE controller so the operating system can use the Ultra DMA modes.

The BIOS initializes and supports ATAPI devices such as LS-120/240, CD-ROM, CD-RW, and DVD.

The BIOS initializes and supports SATA devices just like PATA devices. It initializes the embedded the IDE controllers in the chipset and any SATA devices connected to these controllers. From a software standpoint, SATA controllers present the same register interface as the PATA controllers. Hot-plugging SATA drives during the boot process is not supported by the BIOS and may result in undefined behavior.

3.2.8 Ultra ATA/133

The IDE interface of the ESB2-E ICH DMA protocol redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 133MB/s.

3.2.9 IDE Initialization

The BIOS supports the ATA/ATAPI Specification, version 6 or later. The BIOS initializes the embedded IDE controller in the chipset (ESB2-E ICH) and the IDE device connected to these devices. The BIOS scans the IDE device and programs the controller and the device with their optimum timings. The IDE disk read/write services provided by the BIOS use PIO mode, but the BIOS programs the necessary Ultra DMA registers in the IDE controller so the operating system can use the Ultra DMA Modes.

3.2.10 USB 2.0 Support

The USB controller functionality integrated into ESB2-E ICH6 provides the server board with the interface for up to seven USB 2.0 ports. Four external connectors are located on the back edge of the server board. One internal 1x10 header is provided, capable of supporting an additional two optional USB 2.0 ports. There is also a USB port intended for USB floppy support.

Considering board positioning, the Intel® Server Board 5000SVA SATA 4DIMM SKU will not have USB_6 (J1E2) built on the board.

3.3 Video Support

The server board provides an ATI* ES1000 PCI graphics accelerator, along with 16MB of video DDR SDRAM and support circuitry for an embedded SVGA video sub-system. The ATI* ES1000 chip contains an SVGA video controller, clock generator, 2D and 3D engine, and RAMDAC in a 272-pin PBGA. One 4 Mx16x4 bank DDR SDRAM chip provides 16 MB of video memory.

The SVGA sub-system supports a variety of modes, up to 1600 x 1200 resolution in 8/16/32 bpp modes under 2D, and up to 1024 x 768 resolution in 8/16/24/32 bpp modes under 3D.

It also supports both CRT and LCD monitors with up to 100 Hz vertical refresh rate.

Video is accessed using a standard 15-pin VGA connector found on the back edge of the server board.

You can disable on-board video using the BIOS Setup Utility or when an add-in video card is installed. The system BIOS also provides the option for dual video operation when an add-in video card is configured in the system.

3.3.1 Video Modes

The chip supports all standard IBM* VGA modes. The following table shows the 2D/3D modes supported for both CRT and LCD.

Table 6. Video Modes

2D Mode	Refresh Rate (Hz)	2D Video Mode Support			
		8 bpp	16 bpp	24 bpp	32 bpp
640x480	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
800x600	60, 70, 75, 90, 100	Supported	Supported	Supported	Supported

2D Mode	Refresh Rate (Hz)	2D Video Mode Support			
		8 bpp	16 bpp	24 bpp	32 bpp
1024x768	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
1280x1024	43, 60	Supported	Supported	Supported	Supported
1280x1024	70, 72	Supported	–	Supported	Supported
1600x1200	60, 66	Supported	Supported	Supported	Supported
1600x1200	76, 85	Supported	Supported	Supported	–

3.3.2 Video Memory Interface

The memory controller sub-system of the ES1000 passes requests from the direct memory interface, VGA graphics controller, drawing coprocessor, display controller, video scalar, and hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/coprocessor drawing performance.

The server board supports a 16 MB (4 MB x 16-bit x 4 banks) DDR SDRAM device for video memory. The following table shows the video memory interface signals:

Table 7. Video Memory Interface

Signal Name	I/O Type	Description
V_M_CAS_N	O	Column Address Select
V_M_CKE	O	Clock Enable for Memory
V_M_CS_N	O	Chip Select for Memory
V_M_DQM[1..0]	O	Memory Data Byte Mask
V_M_QS[1..0]	I/O	Memory Data Strobe
V_M_CLK	I	Memory Clock
V_M_CLK_N	I	Memory Clock Compliment
V_M_MA[15..0]	O	Memory Address Bus
V_M_MD[15..0]	I/O	Memory Data Bus
V_M_RAS_N	O	Row Address Select
V_M_WE_N	O	Write Enable

3.3.3 Dual Video

The BIOS supports single and dual video modes. The dual video mode is enabled by default.

In single mode (Dual Monitor Video=Disabled), the on-board video controller is disabled when an add-in video card is detected.

In dual mode (On-board Video=Enabled, Dual Monitor Video=Enabled), the on-board video controller is enabled and is the primary video device. The external video card is allocated resources and considered the secondary video device. The BIOS Setup provides user options to configure the feature as follows:

Video is routed to the rear video connector by default. When a monitor is plugged in to the front panel video connector, the video is routed to it and the rear connector is disabled. You can do this by “hot-plugging” the video connector.

Table 8. Dual Video

Video Type	Enabled/Disabled	Description
On-board Video	**Enabled** Disabled	
Dual Monitor Video	**Enabled** Disabled	Shaded if on-board video is set to "Disabled"

3.4 Network Interface Controller (NIC)

The Intel® 82563EB Gigabit Platform LAN Connect is a dual, compact Physical Layer.

Transceiver (PHY) component designed for 10/100/1000 Mbps operation.

The Intel® 82563EB device is based upon proven PHY technology integrated into Intel® Gigabit Ethernet Controllers. The physical layer circuitry provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). The 82563EB device is capable of transmitting and receiving data at rates of 1000 Mbps, 100 Mbps, or 10 Mbps.

Each Network Interface Controller (NIC) drives two LEDs located on each network interface connector. The link/activity LED (to the left of the connector) indicates a network connection when on, and Transmit/Receive activity when blinking. The speed LED (to the right of the connector) indicates 1000-Mbps operation when amber; 100-Mbps operation when green; and 10-Mbps when off. The following table provides an overview of the LEDs.

Table 9. NIC Status LED

LED Color	LED State	NIC State
Green/Amber (Left)	Off	10 Mbps
	Green	100 Mbps
	Amber	1000 Mbps
Green (Right)	On	Active Connection
	Blinking	Transmit/Receive activity

3.5 Super I/O

Legacy I/O support is provided by using a National Semiconductor* PC87427 Super I/O device. This chip contains all of the necessary circuitry to control two serial ports, one parallel port, floppy disk, and PS/2-compatible keyboard and mouse. Of these, the server board supports the following:

- GPIOs
- Two serial ports
- Removable media drives

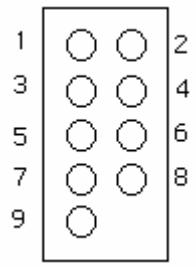
- Floppy controller
- Keyboard and mouse support
- Wake-up control
- System health support

3.5.1 Serial Ports

The server board provides two serial ports: an external DBb-9 serial port and an internal DH10 serial header.

Serial B is an optional port, accessed through a 9-pin internal DH-10 header. You can use a standard DH10 to DB9 cable to direct serial B to the rear of a chassis. The serial B interface follows the standard RS232 pin-out as defined in the following table.

Table 10. Serial A Header Pin-out

Pin	Signal Name	Serial A Header Pin-out
1	DCD	
2	DSR	
3	RX	
4	RTS	
5	TX	
6	CTS	
7	DTR	
8	RI	
9	GND	

The rear DB-9 serial A port is a fully functional serial port that can support any standard serial device.

3.5.2 Removable Media Drives

The BIOS supports removable media devices, including 1.44 MB floppy removable media devices and optical devices, such as a CD-ROM or a read-only DVD-ROM drive. The BIOS supports booting from USB mass storage devices connected to the chassis USB port, such as a USB key device.

The BIOS supports USB 2.0 media storage devices that are backward-compatible to the USB 1.1 specification.

3.5.3 Floppy Disk Controller (FDC)

The server board does not support a floppy disk controller (FDC) interface. However, the system BIOS does recognize USB floppy devices.

3.5.4 Keyboard and Mouse Support

Dual-stacked PS/2 ports, located on the back edge of the server board, are provided for keyboard and mouse support. Either port can support a mouse or keyboard but both ports do not support hot plugging.

3.5.5 Wake-Up Control

The super I/O contains functionality that allows various events to control the power-on and power-off the system.

4. Platform Management

The platform management sub-system on the server board is based on the integrated Baseboard Management Controller (BMC) features of the ESB2-E. In addition, the on-board platform management sub-system consists of communication buses, sensors, system BIOS, and system management firmware.

For additional information, see the Intel® 5000 Series Chipset Server Board Family Datasheet.

Platform management involves:

- ACPI implementation specific details
- System monitoring, control and response to thermal, voltage, and intrusion events
- BIOS security

4.1 Power Button

The system power button is connected to the ESB2-E component. When the button is pressed, the ESB2-E receives the signal and transitions the system to the proper sleep-state as determined by the operating system and software. If the power button is pressed and held for four seconds, the system powers off (S5 state). This feature is called “power button override” and is helpful in the case of system hang and locking up the system. The server board is fully ACPI 1.0a compliant.

4.2 Sleep States Supported

The ESB2-E controls the system sleep states. States S0, S1, S4 and S5 are supported. Either the BIOS or an operating system invokes the sleep states. This is done in response to a power button being pressed or an inactivity timer countdown. Normally, the operating system determines which sleep state to transition into. However a 4-second power button override event places the system immediately into S5. When transitioning into a software-invoked sleep state, the ESB2-E attempts to put the system to sleep by first going into the CPU C2 state.

4.2.1 S0 State

This is the normal operating state, even though there are some power savings modes in this state using CPU Halt and Stop Clock (CPU C1and C2 states). S0 affords the fastest wake-up response time of any sleep state because the system remains fully-powered and memory is intact.

4.2.2 S1 State

This state is entered via a CPU sleep signal from the ESB2-E (CPU C3 state). The system remains fully powered and memory contents intact but the CPUs enter their lowest power state. The operating system uses ACPI drivers to disable bus masters for uni-processor configurations, while the operating system flushes and invalidates caches before entering this

state in multi-processor configurations. Wake-up latency is slightly longer in this state than S0; however, power savings are quite improved from S0.

4.2.3 S4 State

This state is called Suspend to Disk. From a hardware perspective, it is equivalent to an S5 (Soft Off) state; however, S4 has the distinction of avoiding a full boot sequence. The operating system is responsible for saving the system context in a special partition on the hard drive. Although the system must power up and fully boot, boot time to an application is reduced because the computer is returned to the same system state as when the preceding power-off occurred.

4.2.4 S5 State

This state is the normal off state whether entered through the power button or soft off. All power is shut off except for the logic required to restart. This state supports several ”wake up events”. The system only remains in the S5 state while the power supply is plugged into the wall. If the power supply is unplugged from the wall, this is considered a mechanical OFF or G3.

4.3 Wakeup Events

The types of wake events and wake-up latencies are related to the actual power rails available to the system in a particular sleep state and to the location in which the system context is stored. Regardless of the sleep state, wake on the power button is always supported except in a “mechanical off” situation. When in a sleep state, the server board complies with the PCI 2.2 Specification by supplying the optional 3.3V standby voltage to each PCI slot as well as the PME signal. This enables any compliant PCI card to wake the system up from any sleep state except mechanical off.

4.3.1 Wakeup from S1 Sleep State

Advanced management features are enabled by the BMC only when it detects the presence of the Intel® Remote Management Module 2 (Intel® RMM2) card. Without the Intel® RMM2, the advanced features are dormant.

4.3.2 Wakeup from S3 Sleep State (BFAD Workstation Only)

During S1, the system is fully-powered, permitting support for wake on USB, wake on PS/2 keyboard/Mouse, wake on RTC alarm, and wake on PCI PME. Wake on USB, wake on PS/2 Keyboard/Mouse and wake on RTC alarm are not supported by the server board POE BIOS.

4.3.3 Wakeup from S4 and S5 States

In S4 or S5, wake from power button and LAN are supported.

4.4 AC Power Failuar Recovery

The design supports two modes of operation with regard to AC power recovery. The user can select (via a BIOS Setup Screen) whether the system should power back up or remain off after AC is restored. The ESB2-E does not rely on BIOS to boot and check system status in the case

of AC failure. The ESB2-E contains a register variable named “afterG3” which BIOS can set based on user configuration input. The ESB2-E internally examines after it detects an AC recovery.

4.5 PCI PM Support

The PCI Power Management Specification calls out three areas to be compliant: the system reset signal must be held low when in a sleep state, system must support the PCI PME signal, and the system should provide 3.3v standby to the PCI slots. The server board design complies with the PCI PM Specification and the PCI 2.2

Specification for optional 3.3V standby voltage to be supplied to each PCI, PCI-X*, and PCI Express* slots. This support allows any compliant PCI, PCI-X*, or PCI Express* adapter card to wake the system up from any sleep state except mechanical off.

Because of the limited amount of power available on 3.3V standby, the user and the operating system must configure the system carefully following the PCI Power Management Specification.

4.5.1 Reset# Control

The ESB2-E always drives the Platform Reset signal (LOW or HIGH), even when the system is in a sleep state. This is required for PCI power management. Any device that may be active is able to sample this signal to know the system is in a reset condition.

4.5.2 PCI Vaux

All standard PCI, PCI-X*, and PCI Express* slots are provided with 3.3 V aux power to support wake events from all sleep states. The MIC2169 power supply will deliver 4 A of 5 VSB, which in turn is regulated to 3.3 VSB when the system is in the S4 or S5 sleep state. Standby 3.3-V power will not be connected to x1 PCI Express debug slots and these debug slots will not wake events.

4.6 System Management

The LM94 monitors the majority of the system voltages. The LM94 also monitors the VID signals from the Intel® Xeon® processor 5000 sequence. All voltage levels can be read from the LM94 via the SMBus.

4.6.1 CPU Thermal Management

Each CPU monitors its own core temperature and thermally manages itself when it reaches a certain temperature. The system also uses the internal CPU diode(s) to monitor the die temperature. The diode pins are routed to the diode input pins in the LM94. For valid thermal diode configurations for dual-core processors, refer to the thermal diode options table. You can program the LM94 to force the CPU fans to full-speed operation when it senses the CPU core temperature exceeding a specific value. In addition, the LM94 itself has an on-chip thermal monitor. The placement of the LM94 allows it to monitor the incoming ambient temperature blown in by the chassis input fan in front of the processors.

4.7 System Fan Operation

The server board uses both the LM94 and super I/O to monitor and control the fans in the system. Both devices use pulse width modulated (PWM) outputs that can modulate the voltage across the fans, providing a variable duty-cycle to affect a reduced DC voltage from nominal 12 VDC. The fan drive circuit and headers are the new 4-pin type. The 4-pin fans now have a dedicated PWM input for speed control, in addition to the standard ground, +12V, and tachometer pins.

Both the LM94 and super I/O have fan tachometer inputs that you can use to monitor and control fan speeds. You can extract all fan tachometer data from the controllers via the SMBus. The fan speed control circuit does not control the power supply fan. To support limited controller and/or firmware functionality during power on and debug activities, each PWM output has a bypass jumper that causes all fans to run at full-speed and ignore the PWM control.

Each CPU fan has its own dedicated PWM input and tachometer output, so they can be controlled and monitored independently. The LM94 is dedicated to processor fan speed control and monitor, and the SIO will drive and monitor the remaining fans in the system: the chassis and memory fans.

Refer to the fan manual override jumpers table for identification of fan speed override jumpers. Refer to the National Semiconductor* PC87427 and LM94 (National Semiconductor* LM93) specifications regarding fan monitor and control capabilities and programming requirements.

4.8 Light-Guided Diagnostics – System Status and FRU LEDs

The standard system status LEDs for PWR/SLP, HDD, and other LEDs as specified in SSI EEB are supported on the front panel header.

For 10/100/1000 LAN, status LEDs are supported through the back panel 10/100/1000 RJ-45 jack and the front panel per the SSI-EEB specification. The dual-color LED indicates the LAN speed at 10Mbit/s (off), 100Mbit/s (green), or 1000 Mbit/s (yellow). The green link LED represents both link integrity (on/off) and LAN activity (blinking).

Table 11. Summary of LEDs on the Intel® Server Board S5000VSA

Name	Color	Condition	What it describes
Power/Sleep (S1/S3)	Green	ON	Power On
	Green	BLINK	Sleep (S1/S3)
	-	OFF	Power Off (also S4)
Status Front-Panel & Baseboard	Green	ON	System READY
	Green	BLINK	System Degraded (memory, CPU failure)
	Amber	ON	BW/BIOS: Fatal Alarm. Post error/NMI event FW Only: CPU/Terminator Missing, Fan, Temperature, Voltage, visible if fatal error causes a power down
	Amber	BLINK	FAN Alarm. Temperature or Voltage Non-Critical Alarm, Drive Fault

Name	Color	Condition	What it describes
	-	OFF	
FANS	-	OFF	
	Amber	ON	BIOS/FW: In redundant fan system, if one or more fans are missing during POST, BIOS should turn on
CPU	-	OFF	
	Amber	ON	Fatal Alarm.CPU/Terminator Missing/CPU
DIMM	-	OFF	
	Amber	ON	Memory failure - fatal
Progress Code			See Flash tab for details of the code
GEM424 (SATA/SAS) GEM359 (SCSI)	Green	BLINK	Hard Disk Drive Access **NOTE:** Only some SATA drive support this feature
	Amber	ON	Disk drive fault
Vitesse (SATA/SAS) **NOTE:** Amber ON, and GREEN OFF indicates its OK to remove HDD	Green	OFF	HDD in Standby/Stopped. HDD may be removed. LED normally OFF
	Green	BLINK 1s	Spin-up/Spin-down LED on 0.5s, OFF 0.5s, 50% duty cycle of 1s
	Green	ON	Active/Idle power
	Green	BLINK 2s	Formatting LED ON for 1s, OFF for 1s, 50% duty-cycle of 2s
	Amber	ON	Fault
	Amber	BLINK	Flashing - On 1s, OFF 1s, 50% duty-cycle of 2s Indicates Rebuild
Power Supply			
HDD ACTIVITY	Green	BLINK	Hard Disk Drive Access
	-	OFF	No Access
LAN#1-Link/Act	Green	ON	Link
	Green	BLINK	LAN Access (off when there is traffic)
	-	OFF	Disconnect
LAN#1-Speed	Green	ON	Green, link speed is 100Mbits/sec
	Amber	ON	Amber, link speed is 1000Mbits/sec
	-	OFF	OFF, link speed is 10Mbits/sec
LAN#2-Link/Act	Green	ON	Link
	Green	BLINK	LAN Access (off when there is traffic)
	-	OFF	Disconnect
LAN#2-Speed	Green	ON	Green, link speed is 100Mbits/sec
	Amber	ON	Amber, link speed is 1000Mbits/sec
	-	OFF	OFF, link speed is 10Mbits/sec
Identification	Blue	ON	Unit selected for identification
	Blue	BLINK	blink under software control
	-	OFF	No Identification

5. Connector/Header Locations and Pin-outs

5.1 Board Connectors

Table 12. Board Connector Matrix

Connector	Quantity	Reference Designators	Connector Type	Pin Count
Power supply	3	J4K1 J9C1 J9D1	CPU Power Main Power P/S Aux	8 24 5
CPU	2	J1000, J2000	CPU Sockets	771
Main Memory	8	U7B1, U7B2, U7B3, U8B1, U8B2, U8B3, U9B1, U9B2	DIMM Sockets	240
RAID Key	1	J1D1	Key Holder	3
IDE	1	J2K3	Shrouded Header	44
System Fans	4	J1K4, J1K5, J2K2, J2K5	Header	4
Memory Fans	2	J9B1, J9B2	Header	4
CPU Fans	2	J5K1, J9K1	Header	4
Battery	1	BT4E1	Battery Holder	3
Keyboard/Mouse	1	J9A1	PS2, stacked	12
Rear 2xUSB/LAN connector	2	JA6A1, JA6A2	External	16
Serial Port B	1	J1B1	Header	9
Serial Port A Video Connector	1 1	J7A1	External, RJ45 External, D-Sub	10 15
Front panel, main	1	J1F1	Header	24
Front panel, USB	1	J1J8	Header	10
Intrusion detect	1	J1A1	Header	2
Serial ATA	2	J1K3, J1J7	Header	7
SATA/SAS	4	J1J4, J1H3, J1H1, J1G6	Header	7
IPMB/LCP	1	J1J5	Header	4
IPMB	1	J1J6	Header	3
Configuration Jumpers	3	J1J1, J1J2, J1J3	Jumper	3

5.2 Power Connectors

The main power supply connection is obtained using an SSI compliant 2x12 pin connector (J9C1). In addition, there are two additional power related connectors; one SSI compliant 2x4 pin power connector (J4K1) providing support for additional 12 V, and one SSI compliant 1x5 pin connector (J9D1) providing I^2C monitoring of the power supply. The following tables define their pin-outs.

Table 13. Power Connector Pin-Out (J9C1)

Pin	Signal	Color	Pin	Signal	Color
1	+3.3Vdc	Orange	13	+3.3Vdc	Orange
2	+3.3Vdc	Orange	14	-12Vdc	Blue
3	GND	Black	15	GND	Black
4	+5Vdc	Red	16	PS_ON	Green
5	GND	Black	17	GND	Black
6	+5Vdc	Red	18	GND	Black
7	GND	Black	19	GND	Black
8	PWR_GND	Gray	20	NC	White
9	5VSB	Purple	21	+5Vdc	Red
10	+12Vdc	Yellow	22	+5Vdc	Red
11	+12Vdc	Yellow	23	+5Vdc	Red
12	+3.3Vdc	Orange	24	GND	Black

Table 14. 12-V Power Connector Pin-Out (J4K1)

Pin	Signal	Color
1	GND	Black
2	GND	Black
3	GND	Black
4	GND	Black
5	+12Vdc	Yellow/Black
6	+12Vdc	Yellow/Black
7	+12Vdc	Yellow/Black
8	+12Vdc	Yellow/Black

Table 15. Power Supply Signal Connector Pin-Out (J1K1)

Pin	Signal	Color
1	SMB_CLK_ESB_FP_PWR_R	Orange
2	SMB_DAT_ESB_FP_PWR_R	Black
3	SMB_ALRT_3_ESB_R	Red
4	3.3V SENSE-	Yellow
5	3.3V SENSE+	Green

5.3 Control Panel Connector

The server board provides an optional 24-pin SSI control panel connector (J1F1) for use with reference chassis. The following tables provide the pin-out for this connector.

Table 16. 24-pin SSI control panel connector (J1F1)

Pin	Signal Name	Front Panel Pin-out		Pin	Signal Name
1	P5V	Power		2	P5V_STBY
3	Key	LED	Cool Fault	4	P5V_STBY
5	FP_PWR_LED_L	HDD	System	6	FP_COOL_FLT_LED_R
7	P5V	LED	Fault	8	P5V_STBY
9	HDD_LED_ACT_R	Power	LAN A	10	FP_STATUS_LED2_R
11	FP_PWR_BTN_L	Button	Link/Act	12	LAN_ACT_A_L
13	GND	Reset	SM Bus	14	LAN_LINKA_L
15	Reset Button	Sleep	Intruder	16	PS_I2C_5VSB_SDA
17	GND	Button	LAN B	18	PS_I2C_5VSB_SCL
19	FP_SLP_BTN_L	NMI	Link/Act	20	FP_CHASSIS_INTRU
21	GND	ID LED ID		22	LAN_ACT_B_L
23	FP_NMI_BTN_L			24	LAN_LINKB_L
25	Key			26	Key
27	P5V_STBY			28	P5V_STBY
29	FP_ID_LED_L			30	FP_STATUS_LED1_R
31	FP_ID_BTN_L			32	P5V
33	GND			34	FP_HDD_FLT_LED_R

5.4 I/O Connectors

5.4.1 VGA Connector

The following table shows the pin-out definition of the VGA connector (J7A1):

Table 17. VGA Connector Pin-out (J7A1)

Pin	Signal Name	Description
1	V_IO_R_CONN	Red (analog color signal R)
2	V_IO_G_CONN	Green (analog color signal G)
3	V_IO_B_CONN	Blue (analog color signal B)
4	TP_VID_CONN_B4	No connection
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	TP_VID_CONN_B9	No Connection
10	GND	Ground
11	TP_VID_CONN_B11	No connection
12	V_IO_DDCDAT	DDCDAT
13	V_IO_HSYNC_CONN	HSYNC (horizontal sync)
14	V_IO_VSYNC_CONN	VSYNC (vertical sync)
15	V_IO_DDCCLK	DDCCLK

5.4.2 NIC Connectors

The server board provides two RJ-45 NIC connectors located side by side on the back edge of the board (JA6A1, JA6A2). The pin-out for each connector is identical and defined in the following table.

Table 18. RJ-45 10/100/1000 NIC Connector Pin-Out (JA6A1, JA6A2)

Pin	Signal Name
1	GND
2	P1V8_NIC
3	NIC_A_MDI3P
4	NIC_A_MDI3N
5	NIC_A_MDI2P
6	NIC_A_MDI2N
7	NIC_A_MDI1P
8	NIC_A_MDI1N
9	NIC_A_MDI0P
10	NIC_A_MDI0N
11 (D1)	NIC_LINKA_1000_N (LED
12 (D2)	NIC_LINKA_100_N (LED)
13 (D3)	NIC_ACT_LED_N
14	NIC_LINK_LED_N
15	GND
16	GND

5.4.3 ATA-100 Connector

The server board provides one legacy ATA-100 44-pin connector (J2K3). The pin-out is defined in the following table:

Table 19. ATA-100 44-pin Connector Pin-Out (J2K3)

Pin	Signal Name	Pin	Signal Name
1	ESB_PLT_RST_IDE_N	2	GND
3	RIDE_DD_7	4	RIDE_DD_8
5	RIDE_DD_6	6	RIDE_DD_9
7	RIDE_DD_5	8	RIDE_DD_10
9	RIDE_DD_4	10	RIDE_DD_11
11	RIDE_DD_3	12	RIDE_DD_12
13	RIDE_DD_2	14	RIDE_DD_13
15	RIDE_DD_1	16	RIDE_DD_14
17	RIDE_DD_0	18	RIDE_DD_15
19	GND	20	KEY
21	RIDE_DDREQ	22	GND
23	RIDE_DIOW_N	24	GND
25	RIDE_DIOR_N	26	GND
27	RIDE_PIORDY	28	GND

Pin	Signal Name	Pin	Signal Name
29	RIDE_DDACK_N	30	GND
31	IRQ_IDE	32	TP_PIDE_32
33	RIDE_DA1	34	IDE_PRI_CBLSNS
35	RIDE_DA0	36	RIDE_DA2
37	RIDE_DCS1_N	38	RIDE_DCS3_N
39	LED_IDE_N	40	GND
41	P5V	42	P5V
43	GND	44	GND

5.4.4 SATA Connectors

The server board provides six SATA (Serial ATA) connectors:

- SATA-0 (J1K3)
- SATA-1 (J1J7)
- SATA-2 (J1J4)
- SATA-3 (J1H3)
- SATA-4 (J1H1)
- SATA-5 (J1G6)

The pin configuration for each connector is identical and is defined in the following table:

Table 20. SATA Connector Pin-Out (J1K3, J1J7, J1J4, J1H3, J1H1, J1G6)

Pin	Signal Name	Description
1	GND	GND1
2	SATA#_TX_P_C	Positive side of transmit differential pair
3	SATA#_TX_N_C	Negative side of transmit differential pair
4	GND	GND2
5	SATA#_RX_N_C	Negative side of Receive differential pair
6	SATA#_RX_P_C	Positive side of Receive differential pair
7	GND	GND3

5.4.5 Serial Port Connectors

The server board provides one external DB-9 serial A port (J7A1) and one internal 9-pin serial B header (J1B1). The following tables define the pin-outs for each.

Table 21. External RJ-45 Serial B Port Pin-Out (J9A2)

Pin	Signal Name	Description
1	SPA_DCD	Data Carrier Detect
2	SPA_RD	Receive Data
3	SPA_TD	Transmit data
4	SPA_DTR	Data Terminal Ready
5	GND	Ground
6	SPA_DSR	Data Set Ready
7	SPA_RTS	Request to Send
8	SPA_CTS	Clear to Send
9	SPA_RI	Ring Indicator

Table 22. Internal 9-pin Serial A Header Pin-Out (J1B1)

Pin	Signal Name	Description
1	SPB_DCD	DCD (carrier detect)
2	SPB_DSR	DSR (data set ready)
3	SPB_SIN_L	RXD (receive data)
4	SPB_RTS	RTS (request to send)
5	SPB_SOUT_N	TXD (Transmit data)
6	SPB_CTS	CTS (clear to send)
7	SPB_DTR	DTR (Data terminal ready)
8	SPB_RI	RI (Ring Indicate)
9	GND	Ground

5.4.6 Keyboard and Mouse Connector

Two stacked PS/2 ports (J9A1) are provided to support both a keyboard and a mouse. Either PS/2 port can support a mouse or keyboard. The following table defines the pin-out of the PS/2 connector:

Table 23. Stacked PS/2 Keyboard and Mouse Port Pin-Out (J9A1)

Pin	Signal Name	Description
1	KB_DATA_F	Keyboard Data
2	TP_PS2_2	Test point – keyboard
3	GND	Ground
4	P5V_KB_F	Keyboard/mouse power
5	KB_CLK_F	Keyboard Clock
6	TP_PS2_6	Test point – keyboard/mouse
7	MS_DAT_F	Mouse Data
8	TP_PS2_8	Test point – keyboard/mouse
9	GND	Ground
10	P5V_KB_F	Keyboard/mouse power

Pin	Signal Name	Description
11	MS_CLK_F	Mouse Clock
12	TP_PS2_12	Test point – keyboard/mouse
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground

5.4.7 USB Connector

The following table details the pin-out of the external USB connectors (JA6A1, JA6A2) found on the back edge of the server board:

Table 24. External USB Connector Pin-Out (JA6A1, JA6A2)

Pin	Signal Name	Description
1	USB_OC#_FB_1	USB_PWR
2	USB_P#N_FB_2	DATAL0 (Differential data line paired with DATAH0)
3	USB_P#N_FB_2	DATAH0 (Differential data line paired with DATAL0)
4	GND	Ground

One 2x5 connector on the server board (J1J8) provides an option to support an additional two USB ports. The following table details the pin-out of the connector.

Note: Considering board positioning, one board in the Intel® Server Board 5000VSA board families, the 5000VSA SATA 4DIMM will not have the J1J8 internal USB port built on the board.

Table 25. Internal USB Connector Pin-Out (J1J8)

Pin	Signal Name	Description
1	P5V_USB2_VBUS0	USB Power (Ports 0,1)
2	P5V_USB2_VBUS1	USB Power (Ports 0,1)
3	USB_ESB_P0N_CONN	USB Port 0 Negative Signal
4	USB_ESB_P1N_CONN	USB Port 0 Positive Signal
5	USB_ESB_P0P_CONN	USB Port 1 Negative Signal
6	USB_ESB_P1P_CONN	USB Port 1 Positive Signal
7	Ground	
8	Ground	
9	--	No Pin
10	TP_USB_ESB_NC	TEST POINT

5.5 Fan Headers

The server board provides eight SSI-compliant, 4-pin fan connectors. Two fans are designated as processor cooling fans, CPU1 Fan (J9K1) and CPU2 Fan (J5K1); six fans are designated as System Fan 1 (J1K4), System Fan 2 (J1K5), System Fan 3 (J2K2), System Fan 4 (J2K5), System Fan 5 (J9B1), and System Fan 6 (J9B2).

Table 26. SSI Fan Connector Pin-Out (J9K1, J5K1, J1K4, J1K5, J2K2, J2K5, J9B1, J9B2)

Pin	Signal Name	Type	Description
1	Ground	GND	GROUND is the power supply ground
2	12V	Power	Power supply 12V
3	Fan Tach	Out	FAN_TACH signal is connected to the BMC to monitor the fan speed
4	Fan PWM	In	FAN_PWM signal to control fan speed

6. Jumper Block Settings

The Intel® Server Board S5000VSA has several jumper blocks that you can use to configure, protect, or recover specific features of the server board. Pin 1 on each jumper block is denoted by "▼".

6.1 Recovery Jumper Blocks

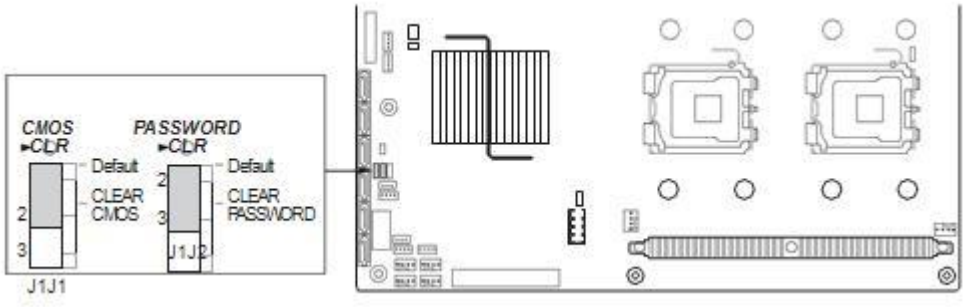


Figure 9. Recovery Jumper Blocks (J1J1, J1J2)

Table 27. Recovery Jumper Blocks (J1J1, J1J2)

Jumper Name	Pins	What happens at system reset...
J1J2: Password Clear	**1-2**	These pins should have a jumper in place for normal system operation. **(Default)**
	2-3	If these pins are jumpered, administrator and user passwords will be cleared on the next reset. These pins should **not** be jumpered for normal operation.
J1J1: CMOS Clear	**1-2**	These pins should have a jumper in place for normal system operation. **(Default)**
	2-3	If these pins are jumpered, the CMOS settings will be cleared on the next reset. These pins should **not** be jumpered for normal operation

6.2 BIOS Select Jumper

The jumper block at J1J3, located next the recovery jumper blocks, is used to select which BIOS image the system boots to. Pin 1 on the jumper is identified with a '▼'.

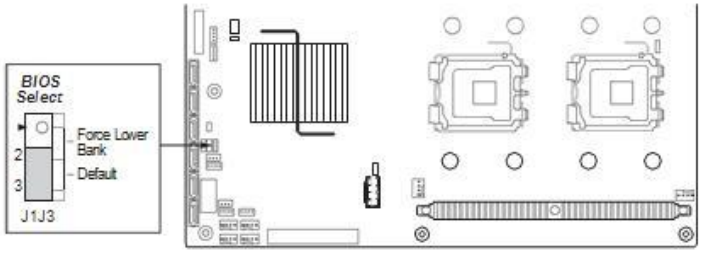


Figure 10. BIOS Select Jumper (J3H1)

Pins	What happens at system reset...
1-2	Force BIOS to bank 2
2-3	System is configured for normal operation (bank 1) (Default)

6.3 Other Configuration Jumpers

Table 28. Other Configuration Jumpers

Function	Pins	Operation
BMC Force Update	1-2	Normal Operation
	2-3	Force Update Mode
FRB3 Timer Disable	1-2	FRB3 Timer Enabled
	2-3	FRB3 Timer Disabled
FSB Speed Select	1-2	533 MHz
	2-3	Default Position. 1066 MHz
XDP CPU1 Isolation Jumper	1-2	Isolate CPU2 from scan chain
	2-3	Include CPU2 in scan chain
Processor Select	Installed	Nocona-T/Dempsey-T
	Removed	Dempsey-J

7. Intel® Light-Guided Diagnostics

The server board has several on-board diagnostic LEDs to assist in troubleshooting board-level issues. This section provides a description of where each LED is located on the board and their function. For a more detailed description of what drives the diagnostic LED operation, refer to the Intel® 5000 Series Chipset Server Board Family Datasheet.

7.1 5-Volt Standby LED

This LED is illuminated when AC is applied to the platform and 5-V standby voltage is supplied to the server board by the power supply.

7.2 Fan Fault LEDs

Fan fault LEDs are present for all eight cooling fan headers. Each LED is located adjacent to its corresponding header.

7.3 System ID LED, System Status LED, and POST Diagnostic LEDs

The server board provides LEDs for both system ID and system status. POST code diagnostic LEDs are located on the back edge of the server board. For a complete description of how these LEDs are read and for a list of all supported POST codes, refer to Appendix C.

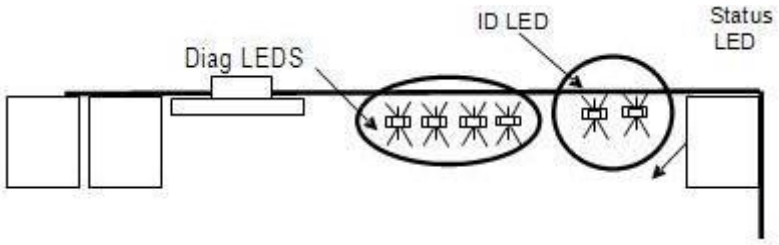


Figure 11. System ID LED and System Status LED Locations

7.4 DIMM Fault LEDs

The server board provides a memory fault LED for each DIMM slot.

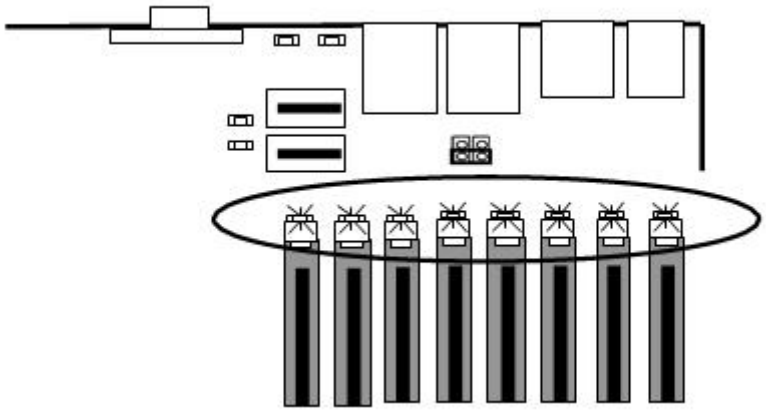


Figure 12. DIMM Fault LED Locations

7.5 Processor Fault LEDs

The server board provides a fault LED for each processor socket.

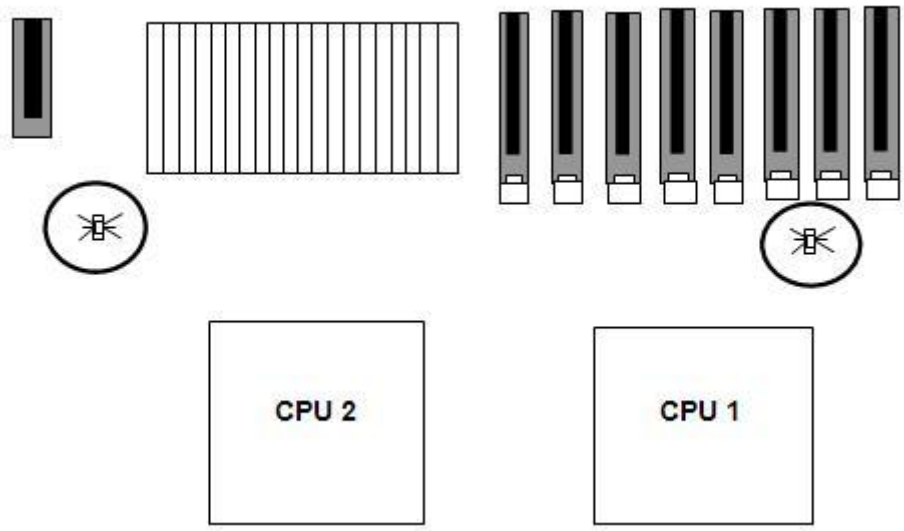


Figure 13. Processor Fault LED Locations

8. Power and Environmental Specifications

8.1 Intel® Server Board S5000VSA Design Specifications

Operating the server board at conditions beyond the specifications outlined in the following table may cause permanent damage to the system. Exposure to maximum conditions for extended periods may impact system reliability.

Table 29. Server Board Design Specifications

Parameter	Limit
Operating Temperature	5º C to 50º C [1] (32º F to 131º F)
Non-Operating Temperature	-40º C to 70º C (-40º F to 158º F)
DC Voltage	± 5% of all nominal voltages
Shock (unpackaged)	Trapezoidal, 50 g, 170 inches/sec
Shock (packaged): ≥ 40 lbs to < 80 lbs	24 inches
Vibration (unpackaged)	5 Hz to 500 Hz 3.13 g RMS random

Note: Chassis design must provide proper airflow to avoid exceeding the Intel® Xeon® processor 5000 sequence maximum case temperature.

Disclaimer Note: Intel Corporation server boards contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for the specific application and environmental conditions. Intel Corporation cannot be held responsible, if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

8.2 Processor Power Support

The server board supports the Thermal Design Point (TDP) guideline for Intel® Xeon® processors 5000 sequence. The Flexible Motherboard Guidelines (FMB) were also followed to help determine the suggested thermal and current design values for anticipating future processor needs. The following table provides maximum values for Icc, TDP power, and TCASE for the Intel® Xeon® processor 5000 sequence family.

Table 30. Intel® Xeon® Processor 5000 Sequence DP TDP Guidelines

TDP Power	Max TCASE	Icc MAX
130 W	70º C	150 A

Note: These values are for reference only. The processor EMTS contains the actual specifications for the processor. If the values found in the EMTS are different then those published here, the EMTS values will supersede these, and should be used.

8.3 Power Supply Specifications

This section provides power supply design guidelines for a system using the Intel® Server Board S5000VSA, including voltage and current specifications, and power supply on/off sequencing characteristics.

8.3.1 Output Power/Currents

The following table defines power and current ratings for the 550-W power supply. The combined output power of all outputs does not exceed the rated output power. The power supply meets both static and dynamic voltage regulation requirements for the minimum loading conditions.

Table 31. Load Ratings

Output Voltage	Load Range		Peak
	Min.	Max.	
+3V3	1.0A	24A	
+5V	2A	20A	
+12V1	0.5A	24A	48A
+12V2	0.5A	17A	22A (500msec)
–12V	0A	0.5A	
+5VSB	0A	2A	

Notes:

1. Maximum continuous total output power will not exceed 550 W.
2. The maximum continuous total output power capability increases at lower ambient temperatures at a rate of 3.3W/ ºC up to 600 W with a 30º C ambient temperature.
3. Maximum continuous load on the combined 12-V output will not exceed 40 A at 45º C, ramping up to 44 A at 30 C.
4. Peak load on the combined 12-V output will not exceed 48 A.
5. Peak total DC output power will not exceed 600 W.
6. Peak power and current loading is supported for a minimum of 12 seconds.
7. Combined 3.3 V and 5 V power should not exceed 160 W.

8.3.2 Grounding

The ground of the pins of the power supply output connector provides the power return path. The output connector ground pins are connected to the safety ground (power supply enclosure).

The power supply must be provided with a reliable protective earth ground. All secondary circuits are connected to protective earth ground. Resistance of the ground returns to chassis does not exceed 1.0 m. This path may be used to carry DC current.

8.3.3 Standby Outputs

The 5 VSB output is present when an AC input greater than the power supply turn on voltage is applied.

8.3.4 Remote Sense

The power supply has remote sense return (ReturnS) to regulate out ground drops for all output voltages; +3.3 V, +5 V, +12 V1, +12 V2, -12 V, and 5 VSB. The power supply uses remote sense to regulate out drops in the system for the +3.3 V, +5 V, and 12 V1 outputs. The remote sense input impedance to the power supply is greater than 200 □ on 3.3 VS, 5 VS. This is the value of the resistor connecting the remote sense to the output voltage internal to the power supply.

Remote sense is able to regulate out a minimum of 200 mV drop on the +3.3 V output. The remote sense return (ReturnS) is able to regulate out a minimum of 200 mV drop in the power ground return. The current in any remote sense line is less than 5 mA to prevent voltage sensing errors. The power supply operates within specification over the full range of voltage drops from the power supply's output connector to the remote sense points.

8.3.5 Voltage Regulation

The power supply output voltages are within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise.

All outputs are measured with reference to the return remote sense signal (ReturnS). The 5 V, 12 V1, 12 V2, –12 V, and 5 VSB outputs are measured at the power supply connectors referenced to ReturnS. The +3.3 V is measured at the remote sense signal (3.3 VS) located at the signal connector.

Table 32. Voltage Regulation Limits

Parameter	Tolerance	MIN	NOM	MAX	Units
+ 3.3V	- 5%/+5%	+3.14	+3.30	+3.46	V_{rms}
+ 5V	- 5%/+5%	+4.75	+5.00	+5.25	V_{rms}
+ 12V1	- 5%/+5%	+11.40	+12.00	+12.60	V_{rms}
+ 12V2	- 5%/+5%	+11.40	+12.00	+12.60	V_{rms}
- 12V	- 5%/+9%	-11.40	-12.00	-13.08	V_{rms}
+ 5VSB	- 5%/+5%	+4.75	+5.00	+5.25	V_{rms}

8.3.6 Dynamic Loading

The output voltages are within limits specified for the step loading and capacitive loading specified in the following table. The step load may occur anywhere within the MIN load to the MAX load conditions.

Table 33. Transient Load Requirements

Output	Step Load Size (see note 2)	Load Slew Rate	Test Capacitive Load
+3.3 VDC	5.0 A	0.25 A/□sec	250 □F
+5 V	4.0 A	0.25 A/□sec	400 □F
+12 V1	25.0 A	0.25 A/□sec	2200 □F [1,2]
+12 V2	25.0 A	0.25 A/□sec	2200 □F [1,2]
+5 VSB	0.5 A	0.25 A/□sec	20 □F

Notes:

1. Step loads on each 12-V output may happen simultaneously.
2. The +12 V should be tested with 2200 □F evenly split between the two +12 V rails.

8.3.7 Capacitive Loading

The power supply is stable and meets all requirements with the following capacitive loading ranges.

Table 34. Capacitive Loading Conditions

Output	MIN	MAX	Units
+3.3V	250	6,800	□F
+5V	400	4,700	□F
+12V(1, 2)	500 each	11,000	□F
-12V	1	350	□F
+5VSB	20	350	□F

8.3.8 Closed Loop Stability

The power supply is unconditionally stable under all line/load/transient load conditions, including capacitive load ranges. A minimum of: 45° phase margin and -10dB-gain margin is required. Closed-loop stability is ensured at the maximum and minimum loads as applicable.

8.3.9 Common Mode Noise

The common mode noise on any output does not exceed 350 mV pk-pk over the frequency band of 10 Hz to 20 MHz.

1. The measurement shall be made across a 100 Ω resistor between each of DC outputs, including ground, at the DC power connector and chassis ground (power sub-system enclosure).

2. The test set-up shall use an FET probe such as Tektronix* model P6046 or equivalent.

8.3.10 Ripple/Noise

The maximum allowed ripple/noise output of the power supply is defined in the following table. This is measured over a bandwidth of 0 Hz to 20 MHz at the power supply output connectors.

Table 35. Ripple and Noise

+3.3V	+5V	+12V1/2	-12V	+5VSB
50mVp-p	50mVp-p	120mVp-p	120mVp-p	50mVp-p

8.3.11 Timing Requirements

The timing requirements for power supply operation are as follows. The output voltages must rise from 10% to within regulation limits (Tvout_rise) within 5 to 70 ms except for 5 VSB; it is allowed to rise from 1.0 to 25 ms. The +3.3 V, +5 V and +12 V output voltages should start to rise approximately at the same time. All outputs rise monotonically. The +5 V output needs to be greater than the +3.3 V output during any point of the voltage rise. The +5 V output must never be greater than the +3.3 V output by more than 2.25 V. Each output voltage shall reach regulation within 50 ms (Tvout_on) of each other during turn on of the power supply. Each output voltage shall fall out of regulation within 400 ms (Tvout_off) of each other during turn off. The following figure shows the timing requirements for the power supply being turned on and off through the AC input with PSON held low and the PSON signal with the AC input applied.

Table 36. Output Voltage Timing

Item	Description	Minimum	Maximum	Units
T_{vout_rise}	Output voltage rise time from each main output.	5.0 *	70 *	msec
T_{vout_on}	All main outputs must be within regulation of each other within this time.		50	msec
T_{vout_off}	All main outputs must leave regulation within this time.		400	msec

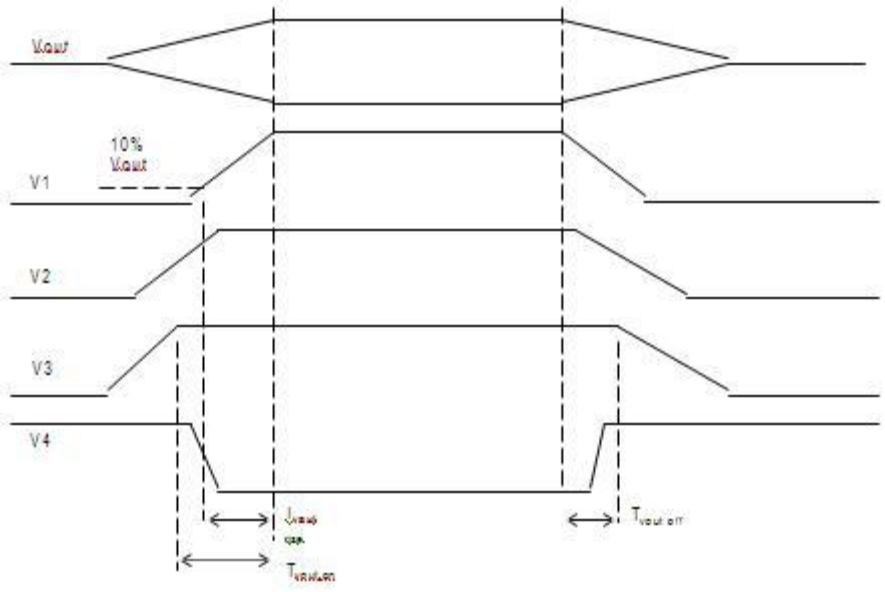


Figure 14. Output Voltage Timing

Table 37. Turn On/Off Timing

Item	Description	Minimum	Maximum	Units
$T_{sb\_on\_delay}$	Delay from AC being applied to 5VSB being within regulation.		1000	msec
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		2500	msec
T_{vout_holdup}	Time all output voltages stay within regulation after loss of AC.	21		msec
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK	20		msec
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	msec
T_{pson_pwok}	Delay from PSON# de-active to PWOK being de-asserted.		50	msec
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	1000	msec
T_{pwok_off}	Delay from PWOK de-asserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits.	1		msec
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		msec
T_{sb_vout}	Delay from 5VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	msec
T_{5VSB_holdup}	Time the 5VSB output voltage stays within regulation after loss of AC.	70		msec

8.3.12 Residual Voltage Immunity in Standby Mode

The power supply is immune to any residual voltage placed on its outputs (typically a leakage voltage through the system from standby output) up to 500 mV. There is neither additional heat generated nor stress of any internal components with this voltage applied to any individual output and all outputs simultaneously. It also does not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition does not exceed 100 mV when AC voltage is applied.

9. Regulatory and Certification Information

⚠ WARNING
To ensure regulatory compliance, you must adhere to the assembly instructions in this guide to ensure and maintain compliance with existing product certifications and approvals. Use only the described, regulated components specified in this guide. Use of other products/components will void the UL listing and other regulatory approvals of the product and will most likely result in noncompliance with product regulations in the region(s) in which the product is sold.

To help ensure EMC compliance with your local regional rules and regulations, before computer integration, make sure that the chassis, power supply, and other modules have passed EMC testing using a server board with a microprocessor from the same family (or higher) and operating at the same (or higher) speed as the microprocessor used on this server board. The final configuration of your end system product may require additional EMC compliance testing. For more information please contact your local Intel Representative.

This is an FCC Class A device. Integration of it into a Class B chassis does not result in a Class B device.

9.1 Product Regulatory Compliance

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, etc.), other than an ITE application, may require further evaluation. This is an FCC Class A device. Integration of it into a Class B chassis does not result in a Class B device.

Note: The use and/or integration of telecommunication devices such as modems and/or wireless devices have not been planned for with respect to these systems. If there is any change of plan to use such devices, then telecommunication type certifications will require additional planning. If NEBS compliance is required for system level products, additional certification planning and design will be required.

9.1.1 Product Safety Compliance

- UL60950 – CSA 60950 (USA/Canada)
- EN60950 (Europe)
- IEC60950 (International)
- CB Certificate & Report, IEC60950 (report to include all country national deviations)
- BSMI Declaration of Conformity (Taiwan)
- Belarus License – Listed on System License (Belarus)
- UL 60950 Recognition (USA)

9.1.2 Product EMC Compliance – Class A Compliance

Note: This product requires complying with Class A EMC requirements. However, Intel targets a 10 db margin to support customer enablement.

- CISPR 22 – Emissions (International)
- EN55022 - Emissions (Europe)
- EN55024 - Immunity (Europe)
- CE – EMC Directive 89/336/EEC (Europe)
- FCC – Part 15 Emissions (USA) Verification
- AS/NZS 3548 Emissions (Australia/New Zealand)
- BSMI CNS13438 Emissions (Taiwan)
- RRL MIC Notice No. 1997-41 (EMC) & 1997-42 (EMI) (Korea)

IMPORTANT NOTE:

The host system with the Server Board S5500BC requires the use of shielded LAN cable to comply with Immunity regulatory requirements. Use of non-shield cables may result in the product having insufficient protection against electromagnetic effects, which may cause improper operation of the product.

9.1.3 Certifications/Registrations/Declarations

- UL Certification (US/Canada)
- CE Declaration of Conformity (CENELEC Europe)
- FCC/ICES-003 Class A Attestation (USA/Canada)
- C-Tick Declaration of Conformity (Australia)
- MED Declaration of Conformity (New Zealand)
- BSMI Declaration (Taiwan)
- RRL Certification (Korea)
- GOST – Listed on one System License (Russia)
- Belarus – Listed on one System License (Belarus)
- Ecology Declaration (International)

9.1.4 Product Ecology Requirements

Intel restricts the use of banned substances in accordance with world wide product ecology regulatory requirements. Suppliers Declarations of Conformity to the banned substances must be obtained from all suppliers; and a Material Declaration Data Sheet (MDDS) must be produced to illustrate compliance. Due verification of random materials is required as a screening/audit to verify suppliers declarations.

The server board complies with the following ecology regulatory requirements:

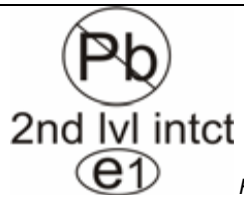
- All materials, parts, and subassemblies must not contain restricted materials as defined in Intel's Environmental Product Content Specification of Suppliers and Outsourced Manufacturers – http://supplier.intel.com/ehs/environmental.htm.

- Europe - European Directive 2002/95/EC - Restriction of Hazardous Substances (RoHS) Threshold limits and banned substances are noted below.
- Quantity limit of 0.1% by mass (1000 PPM) for Lead, Mercury, Hexavalent Chromium, Polybrominated Biphenyls Diphenyl Ethers (PBB/PBDE)
- Quantity limit of 0.01% by mass (100 PPM) for Cadmium
- China RoHS
- All plastic parts that weigh >25gm shall be marked with the ISO11469 requirements for recycling. Example >PC/ABS<
- EU Packaging Directive
- CA. Lithium Perchlorate insert Perchlorate Material – Special handling may apply. Refer to http://www.dtsc.ca.gov/hazardouswaste/perchlorate.
  This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product/part includes a battery which contains Perchlorate material.
- German Green Dot
- Japan Recycling

9.2 Product Regulatory Compliance Markings

The server board is provided with the following regulatory marks:

Regulatory Compliance	Region	Marking
UL Mark	USA/Canada	c UL us E139761
CE Mark	Europe	CE
EMC Marking (Class A)	Canada	CANADA ICES-003 CLASS A
BSMI Marking (Class A)	Taiwan	D33025 警告使用者： 這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策
C-tick Marking	Australia/New Zealand	N232
RRL MIC Mark	Korea	MIC 인증번호: CPU-Model Name (A)
Country of Origin	Exporting Requirements	MADE IN xxxxx (Provided by label, not silk screen)

Regulatory Compliance	Region	Marking
Model Designation	Regulatory Identification	Examples (Intel® Server Board S5500BC) for boxed type boards; or Board PB number for non-boxed boards (typically high-end boards)
PB Free Marking?	Environmental Requirements	 *Refer to the spec* http://prodregs.intel.com/ProductCertifications/Servers/GG-1035%20spec%20Rev%2002.pdf.
China RoHS Marking	China	
China Recycling Package Marking (Marked on packaging label)	China	
Other Recycling Package Marking (Marked on packaging label)	Other Recycling Package Marks	
Other Recycling Package Marking (Marked on packaging label)	CA. Lithium Perchlorate insert	Perchlorate Material – Special handling may apply. See www.dtsc.ca.gov/hazardouswaste/perchlorate This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product/part includes a battery which contains Perchlorate material.

9.3 Electromagnetic Compatibility Notices

9.3.1 FCC Verification Statement (USA)

This device complies with Part 15 of the FCC Rules. Operation is subject to two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124-6497
Phone: 1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of these measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.

All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals that are not shielded and grounded may result in interference to radio and TV reception.

9.3.2 ICES-003 (Canada)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe B prescrites dans la norme sur le matériel brouilleur: "Appareils Numériques", NMB-003 édictée par le Ministre Canadian des Communications.

English translation of the notice above:
This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled "Digital Apparatus," ICES-003 of the Canadian Department of Communications.

9.3.3 Europe (CE Declaration of Conformity)

This product has been tested in accordance too, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

9.3.4 VCCI (Japan)

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＢ情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。
取扱説明書に従って正しい取り扱いをして下さい。

English translation of the notice above:

This is a Class B product based on the standard of the Voluntary Control Council for Interference (VCCI) from Information Technology Equipment. If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

9.3.5 BSMI (Taiwan)

The BSMI Certification Marking and EMC warning is located on the outside rear area of the product.

警告使用者：
這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策

9.3.6 RRL (Korea)

Following is the RRL certification information for Korea.

1. 기기의 명칭(모델명) :
2. 인증번호 :
3. 인증받은 자의 상호 :
4. 제조년월일:
5. 제조자/제조국가 :

English translation of the notice above:

1. Type of Equipment (Model Name): On License and Product
2. Certification No.: On RRL certificate. Obtain certificate from local Intel representative
3. Name of Certification Recipient: Intel Corporation
4. Date of Manufacturer: Refer to date code on product
5. Manufacturer/Nation: Intel Corporation/Refer to country of origin marked on product

Appendix A: Integration and Usage Tips

- When adding or removing components or peripherals from the server board, you must remove AC power. With AC plugged in to the server board, 5-volt standby is still present even though the server board is powered off.
- You must install processors in order. CPU 1 is located near the edge of the server board and must be populated to operate the board.
- On the back edge of the server board are four diagnostic LEDs that display a sequence of red, green, or amber POST codes during the boot process. If your server board hangs during POST, the LEDs display the last POST event run before the hang.
- You must install memory DIMMs in pairs across branches in similarly numbered slots (for example, A2 and B2). Upgrade pairs must be identical with respect to size, speed, and organization.

Appendix B: Sensor Tables

This appendix lists the sensor identification numbers and information regarding the sensor type, name, supported thresholds, assertion and de-assertion information, and a brief description of the sensor purpose. See the *Intelligent Platform Management Interface Specification, Version 2.0*, for sensor and event/reading-type table information.

- **Sensor Type**

  The sensor type references the values in the sensor type codes table in the Intelligent Platform Management Interface Specification Second Generation v2.0. It provides the context to interpret the sensor.

- **Event/Reading Type**

  The event/reading type references values from the event/reading type code ranges and the generic event/reading type code tables in the Intelligent Platform Management Interface Specification Second Generation v2.0. Digital sensors are a specific type of discrete sensors that only have two states.

- **Event Thresholds/Triggers**

  The following event thresholds are supported for threshold type sensors.

[u,l][nr,c,nc]	upper non-recoverable, upper critical, upper non-critical, lower non-recoverable, lower critical, lower non-critical
uc, lc	upper critical, lower critical

  Event triggers are supported, event-generating offsets for discrete type sensors. You can find the offsets in the generic event/reading type code or sensor type code tables in the Intelligent Platform Management Interface Specification Second Generation v2.0, depending on whether the sensor event/reading type is generic or a sensor-specific response.

- **Assertion/De-assertion Enables**

  Assertion and de-assertion indicators reveal the type of events the sensor can generate:

  As: Assertions

  De: De-assertion

- **Readable Value/Offsets**

  Readable Value indicates the type of value returned for threshold and other non-discrete type sensors.

  Readable Offsets indicate the offsets for discrete sensors that are readable via the Get Sensor Reading command. Unless otherwise indicated, all event triggers are readable (for example, Readable Offsets consists of the reading type offsets that do not generate events).

- **Event Data**

  This is the data included in an event message generated by the associated sensor. For threshold-based sensors, these abbreviations are used:

  R: Reading value

  T: Threshold value

- **Rearm Sensors**

  The rearm is a request for the event status for a sensor to be rechecked and updated upon a transition between good and bad states. Rearming the sensors can be done manually or automatically. This column indicates the type supported by the sensor. The following abbreviations are used in the comment column to describe a sensor:

  A: Auto-rearm

  M: Manual rearm

  I: Rearm by init agent

- **Default Hysteresis**

  Hysteresis setting applies to all thresholds of the sensor. This column provides the count of hysteresis for the sensor, which can be 1 or 2 (positive or negative hysteresis).

- **Criticality**

  Criticality is a classification of the severity and nature of the condition. It also controls the behavior of the Control Panel Status LED.

- **Standby**

  Some sensors operate on standby power. These sensors may be accessed and/or generate events when the main (system) power is off, but AC power is present.

Table 38. Integrated BMC Core Sensors

Sensor Name	Sensor Number	System Applica -bility	Senso r Type	Event/Reading Type	Event Offset Triggers	Criticality	Assert/De-assert	Readable Value/Offsets	Event Data	Rearm	Stand -by
Power Unit Status	01h	All	Power Unit 09h	Sensor Specific 6Fh	Power down Power cycle A/C lost	OK	As	–	Trig Offset	A	X
					Soft power control failure Power unit failure	Crit					
					Predictive failure	Non-Crit					

Sensor Name	Sensor Number	System Applica -bility	Senso r Type	Event/Reading Type	Event Offset Triggers	Criticality	Assert/De-assert	Readable Value/Offsets	Event Data	Rearm	Stand -by
Power Unit Redund ancy	02h	Chassis - specific	Power Unit 09h	Generic 0Bh	Redundan cy regained Non-red: suff res from redund	OK	As	–	Trig Offset	A	X
					Redundan cy lost Redundan cy	Degraded					
					Non-red: suff from insuff	OK					
					Non-red: insufficient	Critical					
					Redun degrade from full Redun degrade from non-redundant	OK					
Watchdo g	03h	All	Watch dog 2 23h	Sensor Specific 6Fh	Timer expired, status only Hard reset Power down Power cycle Timer interrupt	OK	As	–	Trig Offset	A	X
Platform Security Violation	04h	All	Platform Security Violation Attempt 06h	Sensor Specific 6Fh	Secure mode violation attempt Out-of-band access password violation	OK	As	–	Trig Offset	A	X
Physical Security	05h	Chassis Intrusion is chassis - specific	Physic al Security 05h	Sensor Specific 6Fh	Chassis intrusion LAN leash lost 1	OK	As and De	–	Trig Offset	A	X

Appendix C: POST Code Diagnostic LEDs

All port 80 codes are displayed using the diagnostic LEDs found on the back edge of the baseboard. The diagnostic LED feature consists of a hardware decoder and four dual-color LEDs. During POST, the LEDs display all normal POST codes representing the progress of the BIOS POST. Each code is represented by a combination of colors from the four LEDs.

The LEDs are capable of displaying three colors: green, red, and amber. The POST codes are divided into two nibbles: an upper nibble and a lower nibble. Each bit in the upper nibble is represented by a red LED and each bit in the lower nibble is represented by a green LED. If both bits are set in the upper and lower nibbles then both red and green LEDs are lit, resulting in an amber color. If both bits are clear, then the LED is off.

In the following example, the BIOS sends a value of ACh to the diagnostic LED decoder. The LEDs are decoded as follows:

- Red bits = 1010b = Ah
- Green bits = 1100b = Ch

Since the red bits correspond to the upper nibble and the green bits correspond to the lower nibble, the two are concatenated to be ACh.

Table 39. POST Progress Code LED Example

LEDs	Red	Green	Red	Green	Red	Green	Red	Green
Ach	1	1	0	1	1	0	0	0
Result	Amber		Green		Red		Off	
	MSB						LSB	

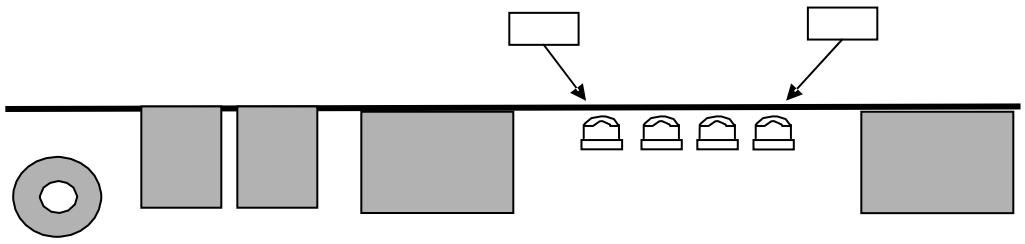


Figure 15. POST Code Diagnostic LEDs

Table 40. Diagnostic LED Post Code Decoder

	Upper Nibble LEDs				Lower Nibble LEDs			
	MSB							LSB
	LED #7	LED #6	LED #5	LED #4	LED #3	LED #2	LED #1	LED #0
	8h	4h	2h	1h	8h	4h	2h	1h
Status	ON	OFF	ON	OFF	ON	ON	OFF	OFF
	1	0	1	0	1	1	0	0
	Ah				Ch			

Upper nibble bits = 1010b = Ah; Lower nibble bits = 1100b = Ch; the two are concatenated as ACh.

Table 41. Diagnostic LED POST Code Decoder

Checkpoint	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	MSB			LSB	
Host Processor					
0x10h	OFF	OFF	OFF	R	Power-on initialization of the host processor (bootstrap processor)
0x11h	OFF	OFF	OFF	A	Host processor cache initialization (including AP)
0x12h	OFF	OFF	G	R	Starting application processor initialization
0x13h	OFF	OFF	G	A	SMM initialization
Chipset					
0x21h	OFF	OFF	R	G	Initializing a chipset component
Memory					
0x22h	OFF	OFF	A	OFF	Reading configuration data from memory (SPD on DIMM)
0x23h	OFF	OFF	A	G	Detecting presence of memory
0x24h	OFF	G	R	OFF	Programming timing parameters in the memory controller
0x25h	OFF	G	R	G	Configuring memory parameters in the memory controller
0x26h	OFF	G	A	OFF	Optimizing memory controller settings
0x27h	OFF	G	A	G	Initializing memory, such as ECC init
0x28h	G	OFF	R	OFF	Testing memory
PCI Bus					
0x50h	OFF	R	OFF	R	Enumerating PCI buses
0x51h	OFF	R	OFF	A	Allocating resources to PCI buses
0x52h	OFF	R	G	R	Hot Plug PCI controller initialization
0x53h	OFF	R	G	A	Reserved for PCI bus
0x54h	OFF	A	OFF	R	Reserved for PCI bus
0x55h	OFF	A	OFF	A	Reserved for PCI bus
0x56h	OFF	A	G	R	Reserved for PCI bus
0x57h	OFF	A	G	A	Reserved for PCI bus
USB					
0x58h	G	R	OFF	R	Resetting USB bus
0x59h	G	R	OFF	A	Reserved for USB devices

Checkpoint	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	MSB			LSB	
ATA/ATAPI/SATA					
0x5Ah	G	R	G	R	Resetting PATA/SATA bus and all devices
0x5Bh	G	R	G	A	Reserved for ATA
SMBUS					
0x5Ch	G	A	OFF	R	Resetting SMBUS
0x5Dh	G	A	OFF	A	Reserved for SMBUS
Local Console					
0x70h	OFF	R	R	R	Resetting the video controller (VGA)
0x71h	OFF	R	R	A	Disabling the video controller (VGA)
0x72h	OFF	R	A	R	Enabling the video controller (VGA)
Remote Console					
0x78h	G	R	R	R	Resetting the console controller
0x79h	G	R	R	A	Disabling the console controller
0x7Ah	G	R	A	R	Enabling the console controller
Keyboard (PS2 or USB)					
0x90h	R	OFF	OFF	R	Resetting the keyboard
0x91h	R	OFF	OFF	A	Disabling the keyboard
0x92h	R	OFF	G	R	Detecting the presence of the keyboard
0x93h	R	OFF	G	A	Enabling the keyboard
0x94h	R	G	OFF	R	Clearing keyboard input buffer
0x95h	R	G	OFF	A	Instructing keyboard controller to run Self Test (PS2 only)
Mouse (PS2 or USB)					
0x98h	A	OFF	OFF	R	Resetting the mouse
0x99h	A	OFF	OFF	A	Detecting the mouse
0x9Ah	A	OFF	G	R	Detecting the presence of mouse
0x9Bh	A	OFF	G	A	Enabling the mouse
Fixed Media					
0xB0h	R	OFF	R	R	Resetting fixed media device
0xB1h	R	OFF	R	A	Disabling fixed media device
0xB2h	R	OFF	A	R	Detecting presence of a fixed media device (IDE hard drive detection, etc.)
0xB3h	R	OFF	A	A	Enabling/configuring a fixed media device
Removable Media					
0xB8h	A	OFF	R	R	Resetting removable media device
0xB9h	A	OFF	R	A	Disabling removable media device
0xBAh	A	OFF	A	R	Detecting presence of a removable media device (IDE CDROM detection, etc.)
0xBCh	A	G	R	R	Enabling/configuring a removable media device
Boot Device Selection					
0xD0	R	R	OFF	R	Trying boot device selection
0xD1	R	R	OFF	A	Trying boot device selection
0xD2	R	R	G	R	Trying boot device selection
0xD3	R	R	G	A	Trying boot device selection

Checkpoint	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	MSB			LSB	
0xD4	R	A	OFF	R	Trying boot device selection
0xD5	R	A	OFF	A	Trying boot device selection
0xD6	R	A	G	R	Trying boot device selection
0xD7	R	A	G	A	Trying boot device selection
0xD8	A	R	OFF	R	Trying boot device selection
0xD9	A	R	OFF	A	Trying boot device selection
0XDA	A	R	G	R	Trying boot device selection
0xDB	A	R	G	A	Trying boot device selection
0xDC	A	A	OFF	R	Trying boot device selection
0xDE	A	A	G	R	Trying boot device selection
0xDF	A	A	G	A	Trying boot device selection
Pre-EFI Initialization (PEI) Core					
0xE0h	R	R	R	OFF	Started dispatching early initialization modules (PEIM)
0xE2h	R	R	A	OFF	Initial memory found, configured, and installed correctly
0xE1h	R	R	R	G	Reserved for initialization module use (PEIM)
0xE3h	R	R	A	G	Reserved for initialization module use (PEIM)
Driver Execution Environment (DXE) Core					
0xE4h	R	A	R	OFF	Entered EFI driver execution phase (DXE)
0xE5h	R	A	R	G	Started dispatching drivers
0xE6h	R	A	A	OFF	Started connecting drivers
DXE Drivers					
0xE7h	R	A	A	G	Waiting for user input
0xE8h	A	R	R	OFF	Checking password
0xE9h	A	R	R	G	Entering BIOS setup
0xEAh	A	R	A	OFF	Flash Update
0xEEh	A	A	A	OFF	Calling Int 19. One beep unless silent boot is enabled.
0xEFh	A	A	A	G	Unrecoverable boot failure/S3 resume failure
Runtime Phase/EFI Operating System Boot					
0xF4h	R	A	R	R	Entering Sleep state
0xF5h	R	A	R	A	Exiting Sleep state
0xF8h	A	R	R	R	Operating system has requested EFI to close boot services (ExitBootServices ( ) has been called)
0xF9h	A	R	R	A	Operating system has switched to virtual address mode (SetVirtualAddressMap ( ) has been called)
0xFAh	A	R	A	R	Operating system has requested the system to reset (ResetSystem () has been called)
Pre-EFI Initialization Module (PEIM)/Recovery					
0x30h	OFF	OFF	R	R	Crisis recovery has been initiated because of a user request
0x31h	OFF	OFF	R	A	Crisis recovery has been initiated by software (corrupt flash)
0x34h	OFF	G	R	R	Loading crisis recovery capsule
0x35h	OFF	G	R	A	Handing off control to the crisis recovery capsule
0x3Fh	G	G	A	A	Unable to complete crisis recovery.

Glossary

This appendix contains important terms used in the preceding chapters. For ease of use, numeric entries are listed first (for example, “82460GX”) with alpha entries following (for example, “AGP 4x”). Acronyms are then entered in their respective place, with non-acronyms following:

Term	Definition
ACPI	Advanced Configuration and Power Interface
AP	Application Processor
APIC	Advanced Programmable Interrupt Control
ASIC	Application Specific Integrated Circuit
BIOS	Basic Input/Output System
BIST	Built-In Self Test
BMC	Baseboard Management Controller
Bridge	Circuitry connecting one computer bus to another, allowing an agent on one to access the other
BSP	Bootstrap Processor
byte	8-bit quantity
CBC	Chassis Bridge Controller (A microcontroller connected to one or more other CBCs, together they bridge the IPMB buses of multiple chassis.)
CEK	Common Enabling Kit
CHAP	Challenge Handshake Authentication Protocol
CMOS	In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board
DPC	Direct Platform Control
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface
EMP	Emergency Management Port
EPS	External Product Specification
FMB	Flexible Mother Board
FMC	Flex Management Connector
FMM	Flex Management Module
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
FSB	Front Side Bus
GB	1024MB
GPIO	General Purpose I/O
GTL	Gunning Transceiver Logic
HSC	Hot-Swap Controller
Hz	Hertz (1 cycle/second)
I2C	Inter-Integrated Circuit Bus
IA	Intel® Architecture
IBF	Input Buffer
ICH	I/O Controller Hub
ICMB	Intelligent Chassis Management Bus
IERR	Internal Error

Term	Definition
IFB	I/O and Firmware Bridge
INTR	Interrupt
IP	Internet Protocol
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
IR	Infrared
ITP	In-Target Probe
KB	1024 bytes
KCS	Keyboard Controller Style
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LPC	Low Pin Count
LUN	Logical Unit Number
MAC	Media Access Control
MB	1024KB
mBMC	National Semiconductor© PC87431x mini BMC
MCH	Memory Controller Hub
MD2	Message Digest 2 – Hashing Algorithm
MD5	Message Digest 5 – Hashing Algorithm – Higher Security
ms	milliseconds
MTTR	Memory Type Range Register
Mux	Multiplexor
NIC	Network Interface Controller
NMI	Nonmaskable Interrupt
OBF	Output Buffer
OEM	Original Equipment Manufacturer
Ohm	Unit of electrical resistance
PEF	Platform Event Filtering
PEP	Platform Event Paging
PIA	Platform Information Area (This feature configures the firmware for the platform hardware.)
PLD	Programmable Logic Device
PMI	Platform Management Interrupt
POST	Power-On Self Test
PSMI	Power Supply Management Interface
PWM	Pulse-Width Modulation
RAM	Random Access Memory
RASUM	Reliability, Availability, Serviceability, Usability, and Manageability
RISC	Reduced Instruction Set Computing
ROM	Read Only Memory
RTC	Real-Time Clock (Component of ICH peripheral chip on the server board.)
SDR	Sensor Data Record
SECC	Single Edge Connector Cartridge
SEEPROM	Serial Electrically Erasable Programmable Read-Only Memory

Term	Definition
SEL	System Event Log
Term	Definition
SIO	Server Input/Output
SMI	System Management Interrupt (SMI is the highest priority nonmaskable interrupt.)
SMM	System Management Mode
SMS	System Management Software
SNMP	Simple Network Management Protocol
TBD	To Be Determined
TIM	Thermal Interface Material
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UHCI	Universal Host Controller Interface
UTC	Universal time coordinate
VID	Voltage Identification
VRD	Voltage Regulator Down
Word	16-bit quantity
ZIF	Zero Insertion Force

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