

# NHD-1.27-12896UGC3

## Graphic Color OLED Display Module

NHD-	Newhaven Display
1.27-	1.27" Diagonal Size
12896-	128 x 96 Pixels
UG-	Model
C-	Full Color
3-	+3V Power Supply

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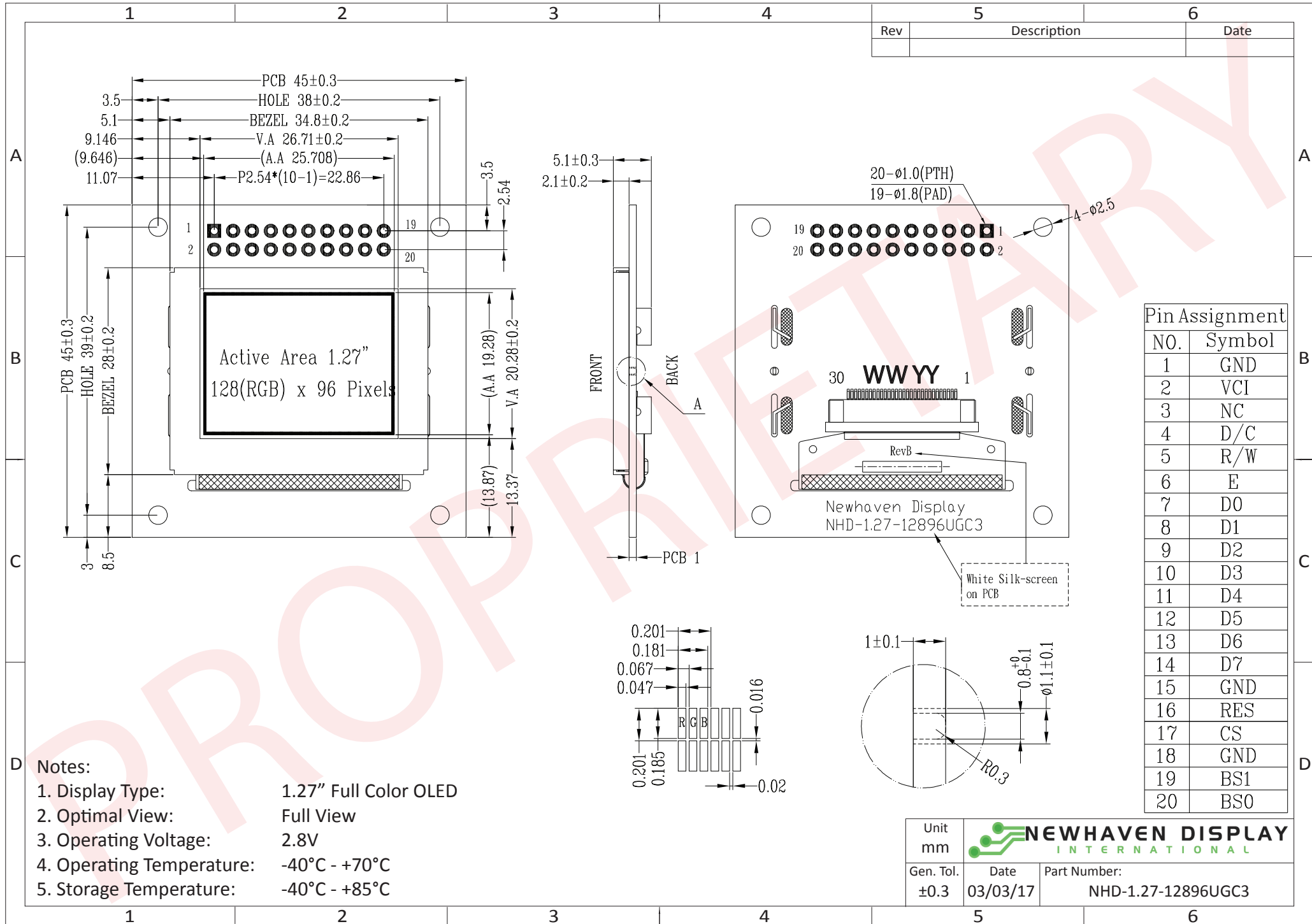
## Document Revision History

Revision	Date	Description	Changed by
0	3/23/14	Initial Release	AK
1	10/20/15	Bezel Alignment Holes Added	SB
2	3/3/17	Thru-Hole Diameter Increased, Temperature Range Updated	SB

## Functions and Features

- 128 x 96 pixel resolution
- Built-in SSD1351 controller
- Parallel or serial MPU interface
- Single, low voltage power supply
- RoHS compliant

# Mechanical Drawing



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# Interface Description

## Parallel Interface:

Pin No.	Symbol	External Connection	Function Description
1	GND	Power Supply	Ground
2	V <sub>DD</sub>	Power Supply	Supply Voltage for OLED and logic.
3	NC	-	No Connect
4	D/C	MPU	Register select signal. D/C=0: Command, D/C=1: Data
5	R/W or /WR	MPU	<b>6800-interface:</b> Read/Write select signal, R/W=1: Read R/W: =0: Write <b>8080-interface:</b> Active LOW Write signal.
6	E or /RD	MPU	<b>6800-interface:</b> Operation enable signal. Falling edge triggered. <b>8080-interface:</b> Active LOW Read signal.
7-14	DB0 – DB7	MPU	8-bit Bi-directional data bus lines.
15	GND	Power Supply	Ground
16	/RES	MPU	Active LOW Reset signal.
17	/CS	MPU	Active LOW Chip Select signal.
18	GND	Power Supply	Ground
19	BS1	MPU	MPU Interface Select signal.
20	BS0	MPU	MPU Interface Select signal.

## Serial Interface:

Pin No.	Symbol	External Connection	Function Description
1	GND	Power Supply	Ground
2	V <sub>DD</sub>	Power Supply	Supply Voltage for OLED and logic.
3	NC	-	No Connect
4	D/C	MPU	Register select signal. D/C=0: Command, D/C=1: Data Tie LOW for 3-wire Serial Interface.
5-6	V <sub>SS</sub>	Power Supply	Ground
7	SCLK	MPU	Serial Clock signal.
8	SDIN	MPU	Serial Data Input signal.
9	NC	-	No Connect
10-14	V <sub>SS</sub>	Power Supply	Ground
15	GND	Power Supply	Ground
16	/RES	MPU	Active LOW Reset signal.
17	/CS	MPU	Active LOW Chip Select signal.
18	GND	Power Supply	Ground
19	BS1	MPU	MPU Interface Select signal.
20	BS0	MPU	MPU Interface Select signal.

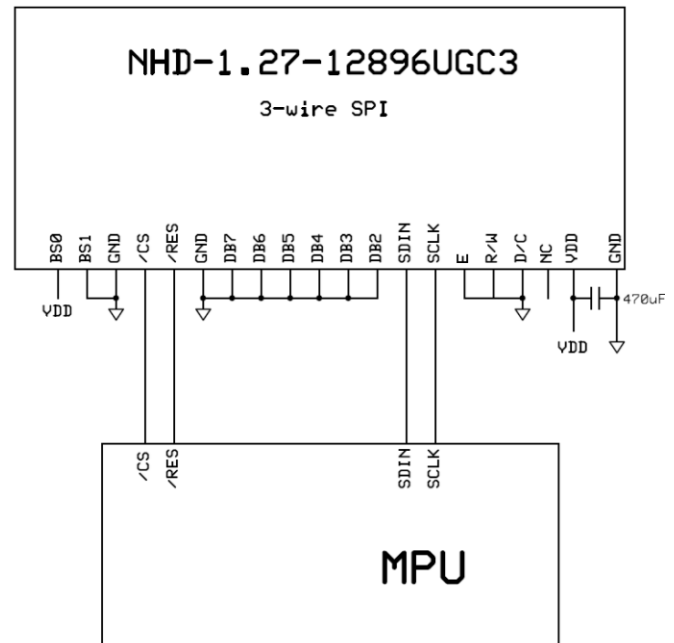
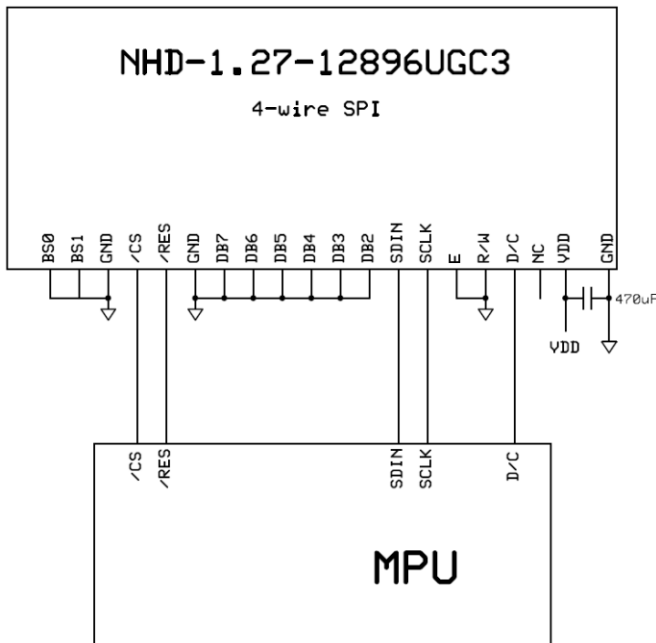
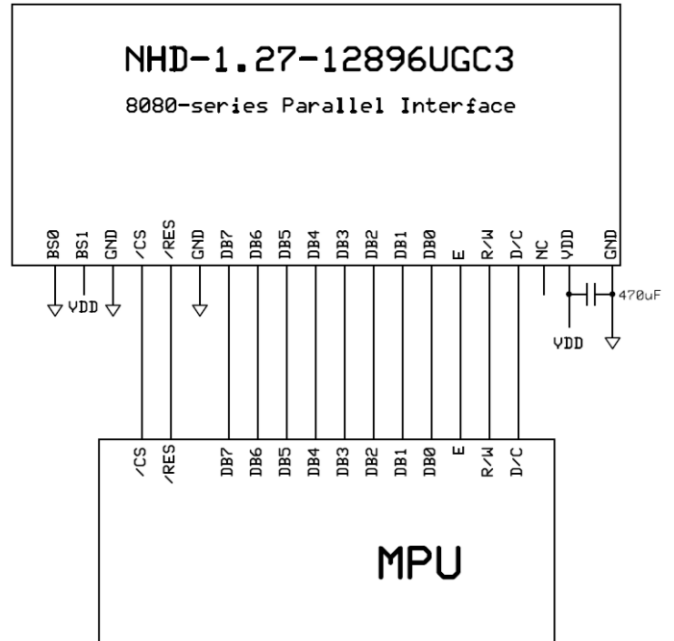
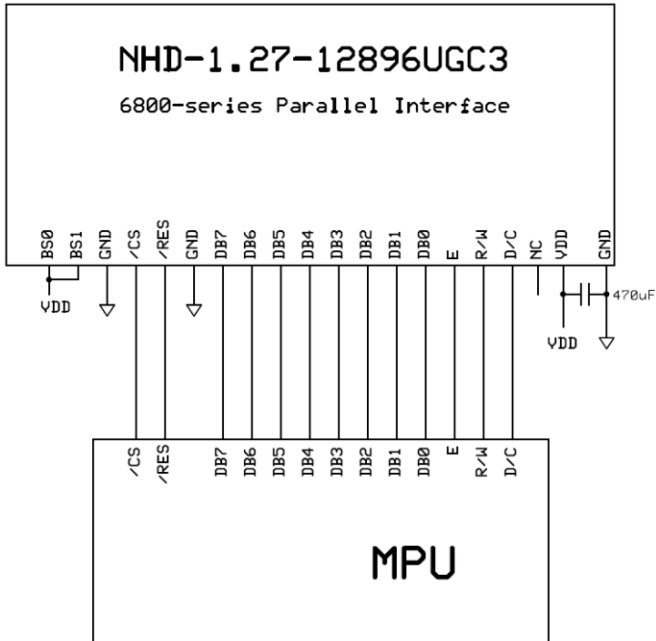
## MPU Interface Pin Selections

Pin Name	6800 Parallel 8-bit interface	8080 Parallel 8-bit interface	4-wire Serial Interface	3-wire Serial Interface
BS1	1	1	0	0
BS0	1	0	0	1

# MPU Interface Pin Assignment Summary

Bus Interface	Data/Command Interface							Control Signals						
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W	/CS	D/C	/RES	
8-bit 6800	D[7:0]							E	R/W	/CS	D/C	/RES		
8-bit 8080	D[7:0]							/RD	/WR	/CS	D/C	/RES		
4-wire SPI	Tie LOW				NC	SDIN	SCLK		Tie LOW	/CS	D/C	/RES		
3-wire SPI	Tie LOW				NC	SDIN	SCLK		Tie LOW	/CS	Tie LOW	/RES		

## Wiring Diagrams



## Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	$T_{OP}$	Absolute Max	-40	-	+70	°C
Storage Temperature Range	$T_{ST}$	Absolute Max	-40	-	+85	°C
Supply Voltage	$V_{DD}$		2.4	2.8	3.5	V
Supply Current (logic)	$I_{DD}$	$T_{OP}=25^{\circ}\text{C}$ , $V_{DD}=2.8\text{V}$	-	4	12	mA
Supply Current (display)	$I_{CC}$	$V_{DD}=2.8\text{V}$	-	140	310	mA
Sleep Mode Current	$I_{DD}+I_{CC_{SLEEP}}$	$V_{DD} = 2.8\text{V}$	-	2	10	mA
"H" Level input	$V_{IH}$	-	$0.8 * V_{DD}$	-	$V_{DD}$	V
"L" Level input	$V_{IL}$	-	$V_{SS}$	-	$0.2 * V_{DD}$	V
"H" Level output	$V_{OH}$	-	$0.9 * V_{DD}$	-	$V_{DD}$	V
"L" Level output	$V_{OL}$	-	0	-	$0.1 * V_{DD}$	V

## Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Optimal Viewing Angles	Top	-	80	-	-	°
	Bottom		80	-	-	°
	Left		80	-	-	°
	Right		80	-	-	°
Contrast Ratio	CR	-	10,000:1	-	-	-
Response Time	Rise	$T_R$	-	10	-	μs
	Fall	$T_F$	-	10	-	μs
Brightness	$L_V$	50% Checkerboard	80	100	-	cd/m <sup>2</sup>
Lifetime	-	100 cd/m <sup>2</sup> , $T_{OP}=25^{\circ}\text{C}$ , 50% Checkerboard	10,000	-	-	Hrs.

**Note:** Lifetime at typical temperature is based on accelerated high-temperature operation. Lifetime is tested at average 50% pixels on and is rated as Hours until **Half-Brightness**. The Display OFF command can be used to extend the lifetime of the display.

Luminance of active pixels will degrade faster than inactive pixels. Residual (burn-in) images may occur. To avoid this, every pixel should be illuminated uniformly.

## Controller information

Built-in SSD1351 controller.

Please download specification at [www.newhavendisplay.com/app\\_notes/SSD1351.pdf](http://www.newhavendisplay.com/app_notes/SSD1351.pdf)

## Table of Commands

(D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated

Single byte command (D/C# = 0), Multiple byte command (D/C# = 0 for first byte, D/C# = 1 for other bytes)

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	15	0	0	0	1	0	1	0	1	Set Column Address	A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
1	A[6:0]	*	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
1	B[6:0]	*	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		
0	75	0	1	1	1	0	1	0	1	Set Row Address	A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
1	A[6:0]	*	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
1	B[6:0]	*	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0	A0	1	0	1	0	0	0	0	0	Set Re-map / Color Depth (Display RAM to Panel)	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment
1	A[7:0]	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		<p>A[1]=0b, Column address 0 is mapped to SEG0 [reset] A[1]=1b, Column address 127 is mapped to SEG0</p> <p>A[2]=0b, Color sequence: A → B → C [reset] A[2]=1b, Color sequence is swapped: C → B → A</p> <p>A[3]=0b, Reserved A[3]=1b, Reserved</p> <p>A[4]=0b, Scan from COM0 to COM[N-1] [reset] A[4]=1b, Scan from COM[N-1] to COM0. Where N is the Multiplex ratio.</p> <p>A[5]=0b, Disable COM Split Odd Even A[5]=1b, Enable COM Split Odd Even [reset]</p> <p>A[7:6] Set Color Depth, 00b / 01b: 65k color [reset] 10b: 262k color 11b 262k color, 16-bit format 2</p> <p>Refer to Table 8-8 for details</p>

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1	A1 A[6:0]	1 *	0 A <sub>6</sub>	1 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Display Start Line	Set vertical scroll by RAM from 0~127. [reset=00h]
0 1	A2 A[6:0]	1 *	0 A <sub>6</sub>	1 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	1 A <sub>1</sub>	0 A <sub>0</sub>	Set Display Offset	Set vertical scroll by Row from 0-127. [reset=60h]  Note (1) This command is locked by Command FDh by default. To unlock it, please refer to Command FDh.
0	A4~A7	1	0	1	0	0	1	X <sub>1</sub>	X <sub>0</sub>	Set Display Mode	A4h: All OFF A5h: All ON (All pixels have GS63) A6h : Reset to normal display [reset] A7h: Inverse Display (GS0 -> GS63, GS1 -> GS62, ....)
0 1	AB A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	1 0	0 0	1 0	0 0	1 0	1 A <sub>0</sub>	Function Selection	A[0]=0b, Select external V <sub>DD</sub> A[0]=1b, Enable internal V <sub>DD</sub> regulator [reset]  A[7:6]=00b, Select 8-bit parallel interface [reset] A[7:6]=01b, Select 16-bit parallel interface A[7:6]=11b, Select 18-bit parallel interface
0	AD	1	0	1	0	1	1	0	1	NOP	Command for no operation.
0	AE~AF	1	0	1	0	1	1	1	X <sub>0</sub>	Set Sleep mode ON/OFF	AEh = Sleep mode On (Display OFF) AFh = Sleep mode OFF (Display ON)
0	B0	1	0	1	1	0	0	0	0	NOP	Command for no operation.
0 1	B1 A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	1 A <sub>5</sub>	1 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Reset (Phase 1) / Pre-charge (Phase 2) period	A[3:0] Phase 1 period of 5~31 DCLK(s) clocks [reset=0010b] A[3:0]: 0-1 invalid 2 = 5 DCLKs 3 = 7 DCLKs : 15 = 31DCLKs  A[7:4] Phase 2 period of 3~15 DCLK(s) clocks [reset=1000b] A[7:4]: 0-2 invalid 3 = 3 DCLKs 4 = 4 DCLKs : 15 = 15DCLKs  Note (1) 0 DCLK is invalid in phase 1 & phase 2 (2) This command is locked by Command FDh by default. To unlock it, please refer to Command FDh.



Fundamental Command Table																																					
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																										
0	B2	1	0	1	1	0	0	1	0	Display Enhancement	A[7:0] = 00h, B[7:0] = 00h, C[7:0] = 00h normal [reset] A[7:0] = A4h, B[7:0] = 00h, C[7:0] = 00h enhance display performance																										
1	A[7:0]	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>																												
1	B[7:0]	0	0	0	0	0	0	0	0																												
1	C[7:0]	0	0	0	0	0	0	0	0																												
0	B3	1	0	1	1	0	0	1	1	Front Clock Divider (DivSet)/ Oscillator Frequency	A[3:0] [reset=0001], divide by DIVSET where  <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>A[3:0]</th> <th>DIVSET</th> </tr> </thead> <tbody> <tr><td>0000</td><td>divide by 1</td></tr> <tr><td>0001</td><td>divide by 2</td></tr> <tr><td>0010</td><td>divide by 4</td></tr> <tr><td>0011</td><td>divide by 8</td></tr> <tr><td>0100</td><td>divide by 16</td></tr> <tr><td>0101</td><td>divide by 32</td></tr> <tr><td>0110</td><td>divide by 64</td></tr> <tr><td>0111</td><td>divide by 128</td></tr> <tr><td>1000</td><td>divide by 256</td></tr> <tr><td>1001</td><td>divide by 512</td></tr> <tr><td>1010</td><td>divide by 1024</td></tr> <tr><td>&gt;=1011</td><td>invalid</td></tr> </tbody> </table> A[7:4] Oscillator frequency, frequency increases as level increases [reset=1101b]  <b>Note</b> <sup>(1)</sup> This command is locked by Command FDh by default. To unlock it, please refer to Command FDh.	A[3:0]	DIVSET	0000	divide by 1	0001	divide by 2	0010	divide by 4	0011	divide by 8	0100	divide by 16	0101	divide by 32	0110	divide by 64	0111	divide by 128	1000	divide by 256	1001	divide by 512	1010	divide by 1024	>=1011	invalid
A[3:0]	DIVSET																																				
0000	divide by 1																																				
0001	divide by 2																																				
0010	divide by 4																																				
0011	divide by 8																																				
0100	divide by 16																																				
0101	divide by 32																																				
0110	divide by 64																																				
0111	divide by 128																																				
1000	divide by 256																																				
1001	divide by 512																																				
1010	divide by 1024																																				
>=1011	invalid																																				
1	A[7:0]	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>																												
0	B4	1	0	1	1	0	1	0	0	Set Segment Low Voltage (VSL)	A[1:0]=00 External VSL [reset] A[1:0]=01,10,11 are invalid <b>Note</b> <sup>(1)</sup> When external VSL is enabled, in order to avoid distortion in display pattern, an external circuit is needed to connect between VSL and V <sub>SS</sub> as shown in Figure 14-1.																										
1	A[7:0]	1	0	1	0	0	0	A <sub>1</sub>	A <sub>0</sub>																												
1	B[7:0]	1	0	1	1	0	1	0	1																												
1	C[7:0]	0	1	0	1	0	1	0	1																												
0	B5	1	0	1	1	0	1	0	1	Set GPIO	A[1:0] GPIO0: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH  A[3:2] GPIO1: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH																										
1	A[3:0]	*	*	*	*	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>																												
0	B6	1	0	1	1	0	1	0	0	Set Second Pre-charge Period	A[3:0] Set Second Pre-charge Period  0000b invalid 0001b 1 DCLKS 0010b 2 DCLKS .... 1000 8 DCLKS [reset] .... 1111 15 DCLKS																										
1	A[3:0]	*	*	*	*	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>																												

Fundamental Command Table																													
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																		
0	B8	1	0	1	1	1	0	0	0	Look Up Table for Gray Scale Pulse width	<p>The next 63 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d)</p> <p>A1[7:0]: Gamma Setting for GS1,  A2[7:0]: Gamma Setting for GS2,  :  A62[7:0]: Gamma Setting for GS62,  A63[7:0]: Gamma Setting for GS63</p> <p><b>Note</b>  <sup>(1)</sup> <math>0 \leq \text{Setting of GS1} &lt; \text{Setting of GS2} &lt; \text{Setting of GS3} \dots &lt; \text{Setting of GS62} &lt; \text{Setting of GS63}</math>  <sup>(2)</sup> GS0 has only pre-charge but no current drive stages.  <sup>(3)</sup> GS1 can be set as only pre-charge but no current drive stage by input gamma setting for GS1 equals 0.</p>																		
1	A1[7:0]	A17	A16	A15	A14	A13	A12	A11	A10																				
1	A2[7:0]	A27	A26	A25	A24	A23	A22	A21	A20																				
1	.	.	.	.	.	.	.	.	.																				
1	.	.	.	.	.	.	.	.	.																				
1	.	.	.	.	.	.	.	.	.																				
1	A62[7:0]	A627	A626	A625	A624	A623	A622	A621	A620																				
1	A63[7:0]	A637	A636	A635	A634	A633	A632	A631	A630																				
0	B9	1	0	1	1	1	0	0	1	Use Built-in Linear LUT [reset= linear]	Reset to default Look Up Table: GS1 = 0 DCLK GS2 = 2 DCLK GS3 = 4 DCLK GS4 = 6 DCLK ... GS62 = 122 DCLK GS63 = 124 DCLK																		
0	BB	1	0	1	1	1	0	1	1	Set Pre-charge voltage	Set pre-charge voltage level.[reset = 17h]																		
1	A[4:0]	0	0	0	A4	A3	A2	A1	A0																				
											<table border="1"> <thead> <tr> <th>A[4:0]</th> <th>Hex code</th> <th>pre-charge voltage</th> </tr> </thead> <tbody> <tr> <td>00000</td> <td>00h</td> <td><math>0.20 \times V_{CC}</math></td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>11111</td> <td>1Fh</td> <td><math>0.60 \times V_{CC}</math></td> </tr> </tbody> </table>	A[4:0]	Hex code	pre-charge voltage	00000	00h	$0.20 \times V_{CC}$	:	:	:	11111	1Fh	$0.60 \times V_{CC}$						
A[4:0]	Hex code	pre-charge voltage																											
00000	00h	$0.20 \times V_{CC}$																											
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											<p><b>Note</b>  <sup>(1)</sup>This command is locked by Command FDh by default. To unlock it, please refer to Command FDh.</p>																		
0	BE	1	0	1	1	1	1	1	0	Set $V_{COMH}$ Voltage	Set COM deselect voltage level [reset = 05h]																		
1	A[2:0]	0	0	0	0	0	A2	A1	A0																				
											<table border="1"> <thead> <tr> <th>A[2:0]</th> <th>Hex code</th> <th><math>V_{COMH}</math></th> </tr> </thead> <tbody> <tr> <td>000</td> <td>00h</td> <td><math>0.72 \times V_{CC}</math></td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>101</td> <td>05h</td> <td><math>0.82 \times V_{CC}</math> [reset]</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>111</td> <td>07h</td> <td><math>0.86 \times V_{CC}</math></td> </tr> </tbody> </table>	A[2:0]	Hex code	$V_{COMH}$	000	00h	$0.72 \times V_{CC}$	:	:	:	101	05h	$0.82 \times V_{CC}$ [reset]	:	:	:	111	07h	$0.86 \times V_{CC}$
A[2:0]	Hex code	$V_{COMH}$																											
000	00h	$0.72 \times V_{CC}$																											
:	:	:																											
101	05h	$0.82 \times V_{CC}$ [reset]																											
:	:	:																											
111	07h	$0.86 \times V_{CC}$																											
											<p><b>Note</b>  <sup>(1)</sup>This command is locked by Command FDh by default. To unlock it, please refer to Command FDh.</p>																		

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	C1	1	1	0	0	0	0	0	1	Set Contrast Current for Color A,B,C	A[7:0] Contrast Value Color A [reset=10001010b]
1	A[7:0]	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		B[7:0] Contrast Value Color B [reset=01010001b]
1	B[7:0]	B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		C[7:0] Contrast Value Color C [reset=10001010b]
1	C[7:0]	C <sub>7</sub>	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>		
0	C7	1	1	0	0	0	1	1	1	Master Contrast Current Control	A[3:0] :
1	A[3:0]	*	*	*	*	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		0000b reduce output currents for all colors to 1/16 0001b reduce output currents for all colors to 2/16 .... 1110b reduce output currents for all colors to 15/16 1111b no change [reset]
0	CA	1	1	0	0	1	0	1	0	Set MUX Ratio	A[6:0] MUX ratio 16MUX ~ 128MUX, [reset=127], (Range from 15 to 127)
1	A[6:0]	0	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	D1	1	0	1	0	1	1	0	1	NOP	Command for No Operation
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation
0	FD	1	1	1	1	1	1	0	1	Set Command Lock	A[7:0]: MCU protection status [reset = 12h] A[7:0] = 12b, Unlock OLED driver IC MCU interface from entering command [reset] A[7:0] = 16b, Lock OLED driver IC MCU interface from entering command
1	A[7:0]	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		A[7:0] = B0b, Command A2,B1,B3,BB,BE,C1 inaccessible in both lock and unlock state [reset] A[7:0] = B1b, Command A2,B1,B3,BB,BE,C1 accessible if in unlock state
											<b>Note</b> (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.

**Note**

(1) "\*" stands for "Don't care".

Set (GAC) (D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated

Single byte command (D/C# = 0), Multiple byte command (D/C# = 0 for first byte, D/C# = 1 for other bytes)

Graphic acceleration command										Command	Description
D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0		
0	96	1	0	0	1	0	1	1	0		A[7:0] = 00000000b No scrolling
1	A[7:0]	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		A[7:0] = 00000001b to 00111111b Scroll towards SEG127 with 1 column offset
1	B[6:0]	0	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		A[7:0] = 01000000b to 11111111b Scroll towards SEG0 with 1 column offset
1	C[7:0]	C <sub>7</sub>	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>		
1	D[6:0]	0	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		B[6:0] : start row address
1	E[1:0]	0	0	0	0	0	0	E <sub>1</sub>	E <sub>0</sub>		C[7:0] : number of rows to be H-scrolled B+C ≤ 128
										Horizontal Scroll	D[6:0] : Reserved (reset=00h)
											E[1:0] : scrolling time interval 00b test mode 01b normal 10b slow 11b slowest
											<b>Note</b> (1) Operates during display ON.
0	9E	1	0	0	1	1	1	1	0	Stop Moving	Stop horizontal scroll
											<b>Note</b> (1) After sending 9Eh command to stop the scrolling action, the ram data needs to be rewritten
0	9F	1	0	0	1	1	1	1	1	Start Moving	Start horizontal scroll

**Note**

(1) After executed the graphic command, waiting time is required for update GDDRAM content.

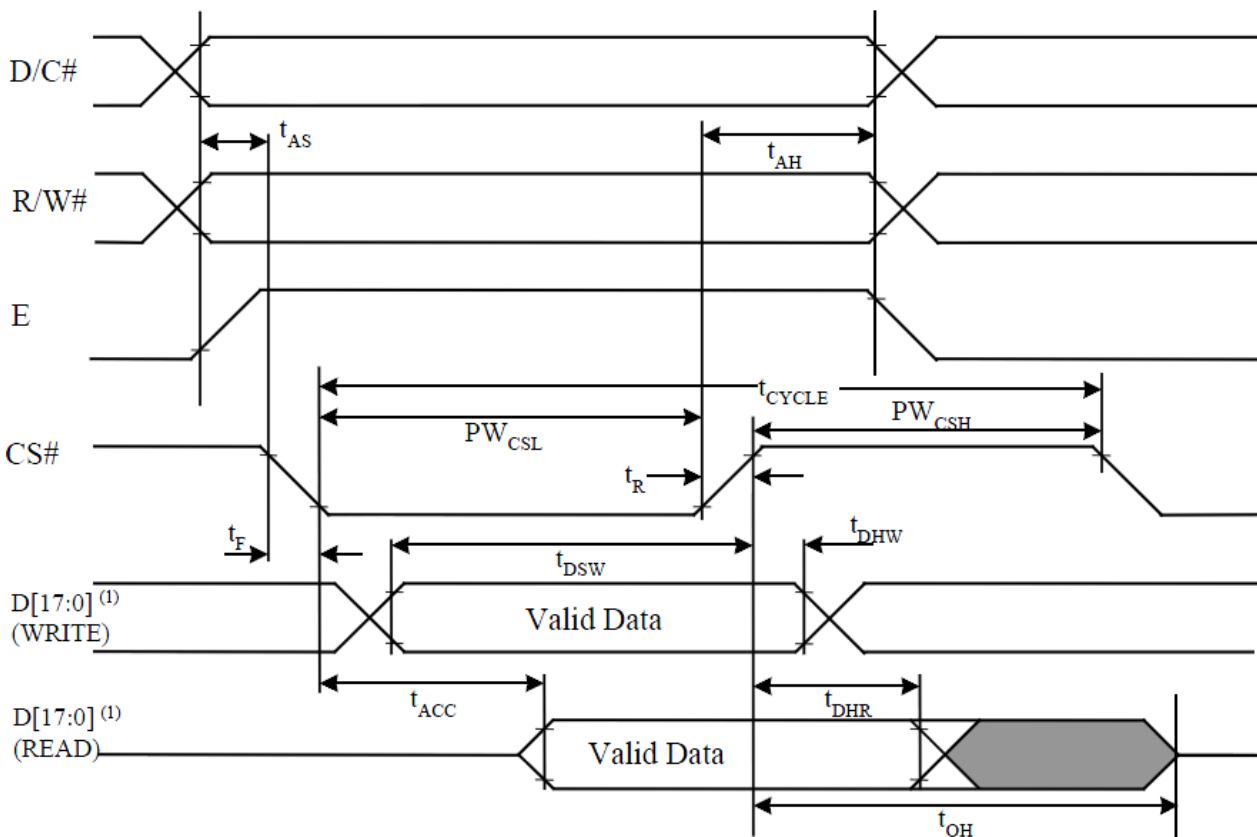
V<sub>CI</sub> = 2.4~3.5V, waiting time = 500ns/pixel.

(2) “\*” stands for “Don’t care”.

# Timing Characteristics

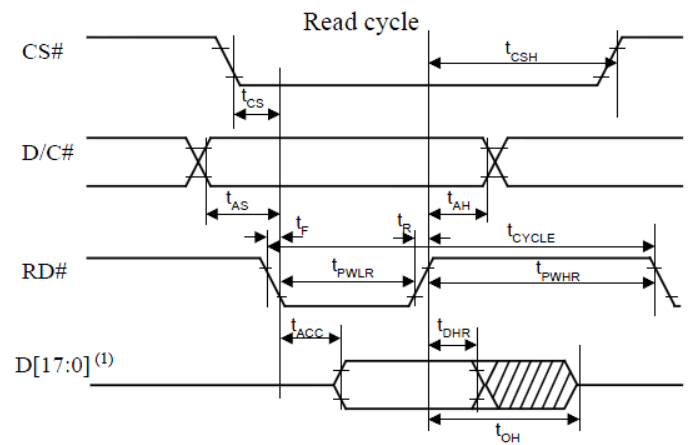
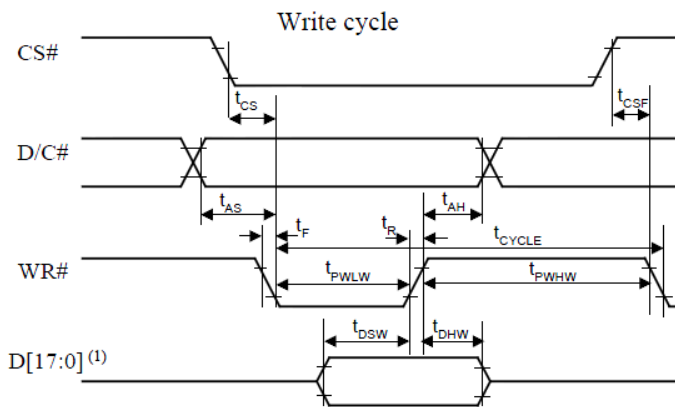
## 6800-Series MCU Parallel Interface:

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYCLE}$	Clock Cycle Time (read) Clock Cycle Time (write)	320 300	-	-	ns
$t_{AS}$	Address Setup Time	24	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	7	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$PW_{CSL}$	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
$PW_{CSH}$	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns



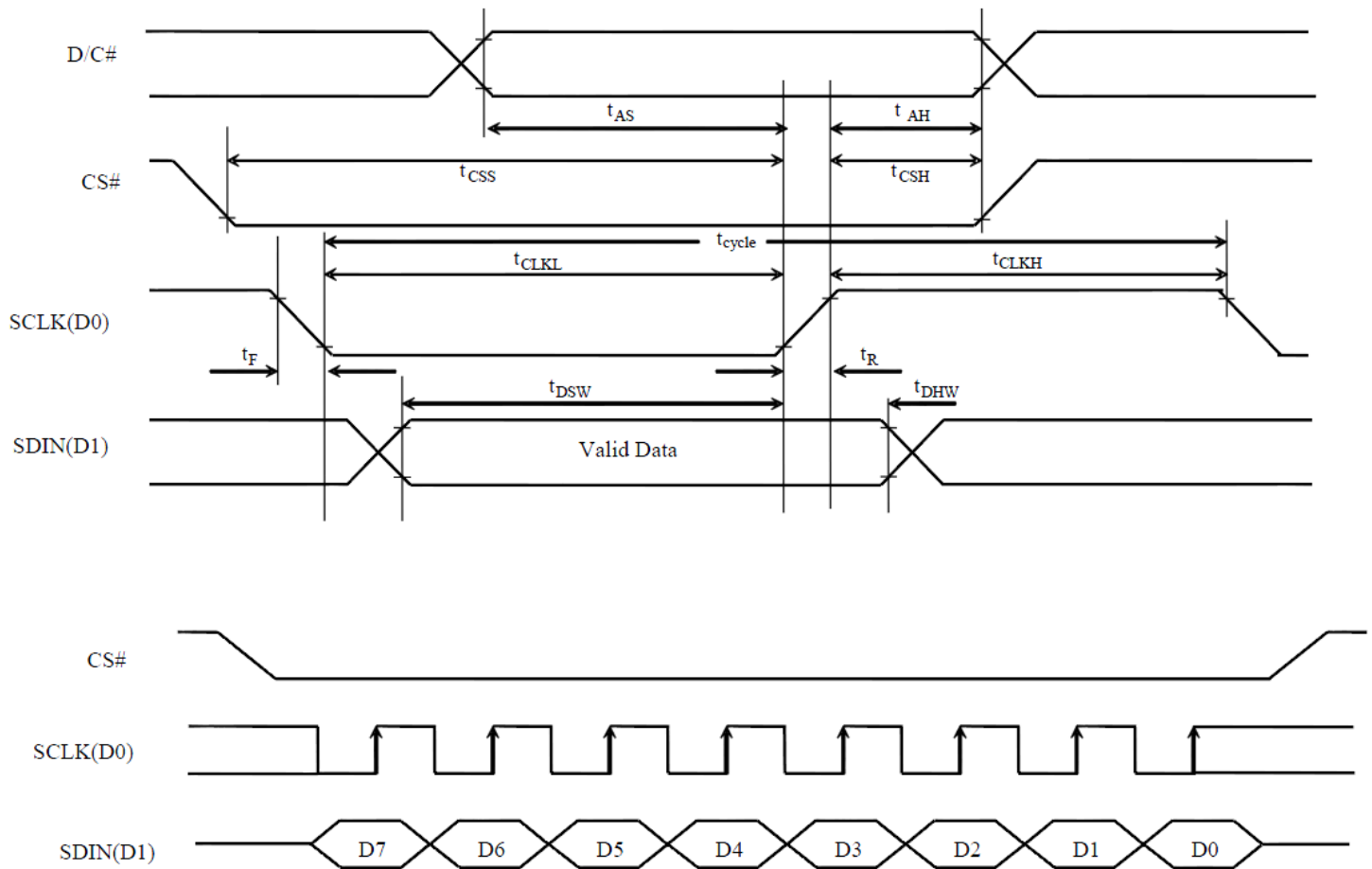
## 8080-Series MCU Parallel Interface:

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CYCLE}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	10	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	7	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	46	ns
$t_{ACC}$	Access Time	-	-	140	ns
$t_{PWLW}$	Read Low Time	150	-	-	ns
$t_{PWLW}$	Write Low Time	60	-	-	ns
$t_{PWHR}$	Read High Time	60	-	-	ns
$t_{PWHW}$	Write High Time	60	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns
$t_{CS}$	Chip select setup time	0	-	-	ns
$t_{CSH}$	Chip select hold time to read signal	0	-	-	ns
$t_{CSF}$	Chip select hold time	20	-	-	ns



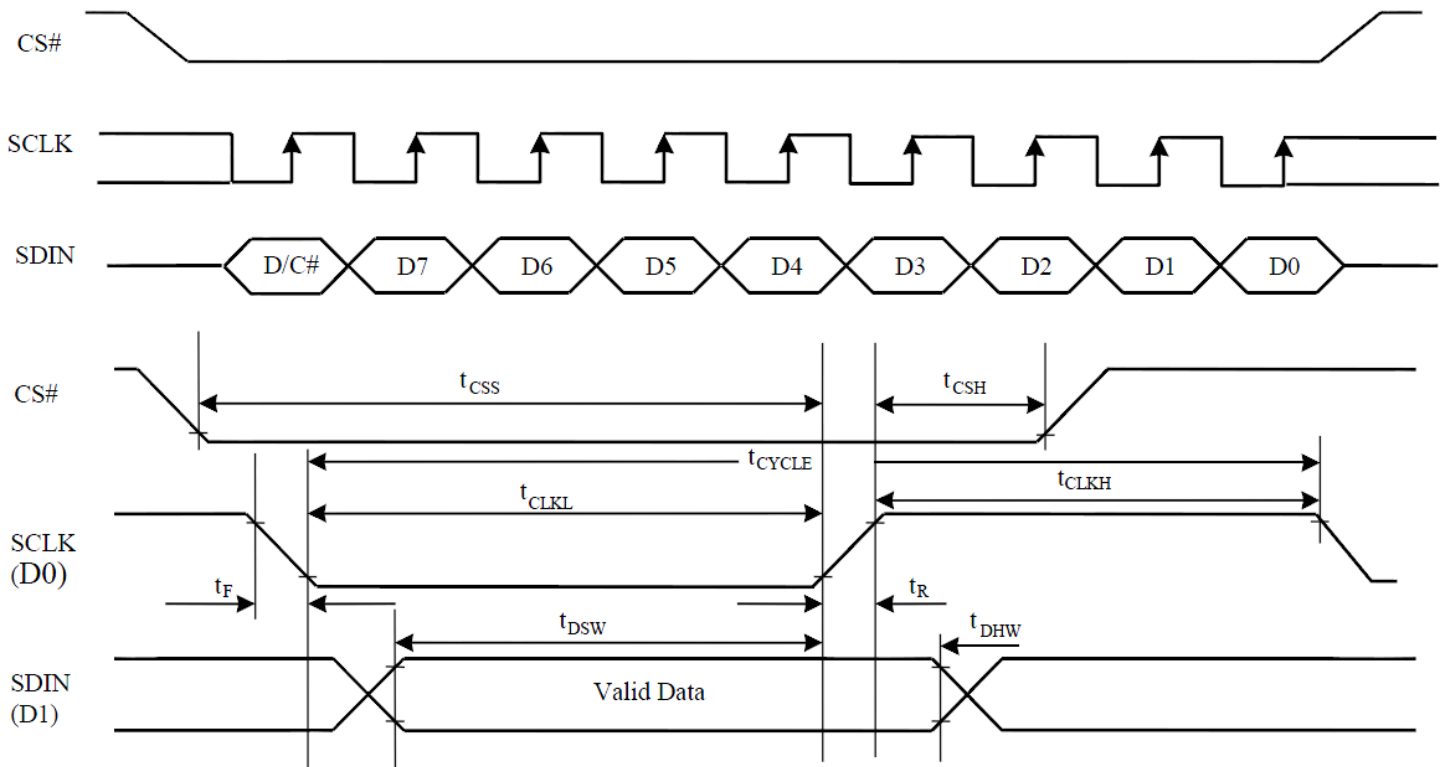
#### 4-wire SPI:

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{cycle}}$	Clock Cycle Time	220	-	-	ns
$t_{\text{AS}}$	Address Setup Time	15	-	-	ns
$t_{\text{AH}}$	Address Hold Time	42	-	-	ns
$t_{\text{CSS}}$	Chip Select Setup Time	20	-	-	ns
$t_{\text{CSH}}$	Chip Select Hold Time	10	-	-	ns
$t_{\text{DSW}}$	Write Data Setup Time	15	-	-	ns
$t_{\text{DHW}}$	Write Data Hold Time	20	-	-	ns
$t_{\text{CLKL}}$	Clock Low Time	20	-	-	ns
$t_{\text{CLKH}}$	Clock High Time	20	-	-	ns
$t_{\text{R}}$	Rise Time	-	-	15	ns
$t_{\text{F}}$	Fall Time	-	-	15	ns



### 3-wire SPI:

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{cycle}}$	Clock Cycle Time	220	-	-	ns
$t_{\text{CSS}}$	Chip Select Setup Time	20	-	-	ns
$t_{\text{CSH}}$	Chip Select Hold Time	44	-	-	ns
$t_{\text{DSW}}$	Write Data Setup Time	15	-	-	ns
$t_{\text{DHW}}$	Write Data Hold Time	20	-	-	ns
$t_{\text{CLKL}}$	Clock Low Time	20	-	-	ns
$t_{\text{CLKH}}$	Clock High Time	20	-	-	ns
$t_{\text{R}}$	Rise Time	-	-	15	ns
$t_{\text{F}}$	Fall Time	-	-	15	ns





## Example Initialization Sequence:

```
void oled_Data_12896RGB(unsigned char Data)
{
  GPIO_Write(GPIOB, Data);
  GPIO_SetBits(GPIOC, RS);
  GPIO_ResetBits(GPIOC, CS1);
  GPIO_ResetBits(GPIOC, RW);
  GPIO_SetBits(GPIOC, E1);
  GPIO_ResetBits(GPIOC, E1);
  GPIO_SetBits(GPIOC, RW);
  GPIO_SetBits(GPIOC, CS1);
}

void oled_Command_12896RGB(unsigned char Data)
{
  GPIO_Write(GPIOB, Data);
  GPIO_ResetBits(GPIOC, RS);
  GPIO_ResetBits(GPIOC, CS1);
  GPIO_ResetBits(GPIOC, RW);
  GPIO_SetBits(GPIOC, E1);
  GPIO_ResetBits(GPIOC, E1);
  GPIO_SetBits(GPIOC, RW);
  GPIO_SetBits(GPIOC, CS1);
}

void OLED_Init_12896RGB(void)
{
  int i,j;
  GPIO_ResetBits(GPIOC, RES);
  graphic_delay(500000);
  GPIO_SetBits(GPIOC, RES);
  graphic_delay(500000);

  oled_Command_12896RGB(0xFD); //Command lock setting
  oled_Data_12896RGB(0x12); //unlock
  oled_Command_12896RGB(0xFD); //Command lock setting
  oled_Data_12896RGB(0xB1); //unlock

  oled_Command_12896RGB(0xAE);

  oled_Command_12896RGB(0xB3); //clock & frequency
  oled_Data_12896RGB(0xF1); //clock=Diviser+1 frequency=fh

  oled_Command_12896RGB(0xCA); //Duty
  oled_Data_12896RGB(0x7F); //OLED_END+1

  oled_Command_12896RGB(0xA2); //Display offset
  oled_Data_12896RGB(0x00);

  oled_Command_12896RGB(0xA1); //Set display start line
```

```

oled_Data_12896RGB(0x00); //0x00 start line

oled_Command_12896RGB(0xA0); //Set Re-map, color depth
oled_Data_12896RGB(0xA0); //8-bit 262K

oled_Command_12896RGB(0xB5); //set GPIO
oled_Data_12896RGB(0x00); //disabled

oled_Command_12896RGB(0xAB); //Function Set
oled_Data_12896RGB(0x01); //8-bit interface, internal VDD regulator

oled_Command_12896RGB(0xB4); //set VSL
oled_Data_12896RGB(0xA0); //external VSL
oled_Data_12896RGB(0xB5);
oled_Data_12896RGB(0x55);

oled_Command_12896RGB(0xC1); //Set contrast current for A,B,C
oled_Data_12896RGB(0x8a); //Color A //8a
oled_Data_12896RGB(0x51); //Color B //51
oled_Data_12896RGB(0x8a); //Color C //8a

oled_Command_12896RGB(0xC7); //Set master contrast
oled_Data_12896RGB(0x0F); //

oled_Command_12896RGB(0xB9); //use linear grayscale LUT

oled_Command_12896RGB(0xB1); //Set pre & dis-charge
oled_Data_12896RGB(0x32); //pre=1h, dis=1h

oled_Command_12896RGB(0xBB); //Set precharge voltage of color A,B,C
oled_Data_12896RGB(0x07); //

oled_Command_12896RGB(0xB2); //display enhancement
oled_Data_12896RGB(0xa4);
oled_Data_12896RGB(0x00);
oled_Data_12896RGB(0x00);

oled_Command_12896RGB(0xB6); //precharge period
oled_Data_12896RGB(0x01);

oled_Command_12896RGB(0xBE); //Set VcomH
oled_Data_12896RGB(0x07);

oled_Command_12896RGB(0xA6); //Normal display

oled_Command_12896RGB(0x15); //set column start and end addresses
oled_Data_12896RGB(0x00); //
oled_Data_12896RGB(0x7F); //
oled_Command_12896RGB(0x75); //set row start and end addresses
oled_Data_12896RGB(0x00); //

```

```

oled_Data_12896RGB(0x5F);      //
oled_Command_12896RGB(0x5C);  //write to RAM command

    for(i=0;i<128;i++)
    {
        for(j=0;j<96;j++)
        {
            oled_Data_12896RGB(0x00);
            oled_Data_12896RGB(0x00);
            oled_Data_12896RGB(0x00);
        }
    }
oled_Command_12896RGB(0xAF);  //Display on
}

int oled_12896RGB(void)
{
column = 0x00;
byte1 = 0x00;
byte2 = 0x00;
oled_Command_12896RGB(0x15);  //set column start and end addresses
oled_Data_12896RGB(column);  //
oled_Data_12896RGB(0x7F);    //
oled_Command_12896RGB(0x75);  //set row start and end addresses
oled_Data_12896RGB(0x00);    //
oled_Data_12896RGB(0x5F);    //
oled_Command_12896RGB(0x5C);  //write to RAM command

for (i=0;i<12288;i++)  //for each 24-bit pixel...128*96=12288
{
    f_read(&File1, &red, 1, &blen);    //read the red 8-bits
    f_read(&File1, &green, 1, &blen);  //read the green 8-bits
    f_read(&File1, &blue, 1, &blen);  //read the blue 8-bits

    red = red >> 2;
    green = green >> 2;
    blue = blue >> 2;
    oled_Data_12896RGB(red);
    oled_Data_12896RGB(green);
    oled_Data_12896RGB(blue);
}
////////////////////////////////////

```

## Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Test the endurance of the display at high storage temperature.	+85°C , 240 Hrs.	2
Low Temperature storage	Test the endurance of the display at low storage temperature.	-40°C , 240 Hrs.	1,2
High Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature.	+70°C 240 Hrs.	2
Low Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at low temperature.	-40°C , 240 Hrs.	1,2
High Temperature / Humidity Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature with high humidity.	+60°C , 90% RH , 120 Hrs.	1,2
Thermal Shock resistance	Test the endurance of the display by applying electric stress (voltage & current) during a cycle of low and high temperatures.	-30°C,30min -> 25°C,5min -> 70°C,30min = 1 cycle 10 Cycles	
Vibration test	Test the endurance of the display by applying vibration to simulate transportation and use.	10-22Hz , 15mm amplitude. 22-500Hz, 1.5G 30min in each of 3 directions X,Y,Z	3
Atmospheric Pressure test	Test the endurance of the display by applying atmospheric pressure to simulate transportation by air.	115mbar, 40hrs	3
Static electricity test	Test the endurance of the display by applying electric static discharge.	V <sub>s</sub> =±800V, R <sub>s</sub> =330Ω, C <sub>s</sub> =150pF 10 Times	

**Note 1:** No condensation to be observed.

**Note 2:** Conducted after 2 hours of storage at 25°C, 0%RH.

**Note 3:** Test performed on product itself, not inside a container.

### Evaluation Criteria:

- 1: Display is fully functional during operational tests and after all tests, at room temperature.
- 2: No observable defects.
- 3: Luminance >50% of initial value.
- 4: Current consumption within 50% of initial value

## Precautions for using OLEDs/LCDs/LCMs

See Precautions at [www.newhavendisplay.com/specs/precautions.pdf](http://www.newhavendisplay.com/specs/precautions.pdf)

## Warranty Information and Terms & Conditions

[http://www.newhavendisplay.com/index.php?main\\_page=terms](http://www.newhavendisplay.com/index.php?main_page=terms)

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