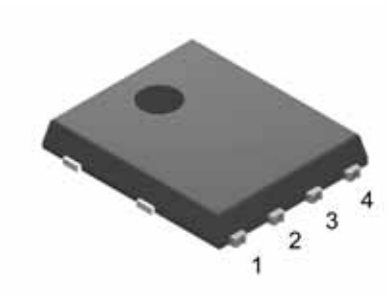
STL40DN3LLH5

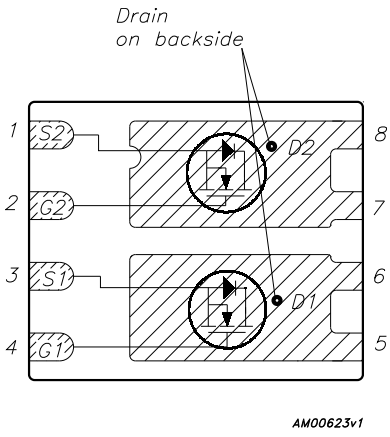
Automotive-grade dual N-channel 30 V, 0.016 Ω typ., 40 A STripFET™ H5 Power MOSFET in a PowerFLAT™ 5x6 DI package

Datasheet - production data



PowerFLAT™ 5x6
double island

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL40DN3LLH5	30 V	0.018 Ω	40 A

- AEC-Q101 qualified
- Low on-resistance
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™ H5 technology. The device has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Table 1. Device summary

Order code	Marking	Package	Packing
STL40DN3LLH5	40DN3LH5	PowerFLAT™ 5x6 double island	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 22	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	40	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	28	A
I_D (2)	Drain current (continuous) at T_{pcb} = 25 °C	11	A
I_D (2)	Drain current (continuous) at T_{pcb}=100°C	7	A
I_{DM} (2)(3)	Drain current (pulsed)	44	A
I_{DM} (1)(3)	Drain current (pulsed)	160	A
P_{TOT} (1)	Total dissipation at T_C = 25°C	50	W
P_{TOT} (2)	Total dissipation at T_{pcb} = 25°C	4.7	W
T_J	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

1. The value is rated according $R_{thj\text{-}c}$
2. The value is rated according $R_{thj\text{-}pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	3.0	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	32	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 s

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0 V	30			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V, V_{GS} = 0 V			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J =125 °C(1)			10	µA
I_{GSS}	Gate body leakage current	V_{GS} = ± 22 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.5		V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D= 5.5 A		0.016	0.018	Ω
		V_{GS} = 4.5 V, I_D= 5.5 A		0.02	0.025	Ω

1. Defined by design, not subject to production test

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	475	-	pF
C_{oss}	Output capacitance		-	97	-	pF
C_{rss}	Reverse transfer capacitance		-	19	-	pF
Q_g	Total gate charge	V_{DD}= 15 V, I_D = 11 A V_{GS} = 4.5 V *(see Figure 13)*	-	4.5	-	nC
Q_{gs}	Gate-source charge		-	1.7	-	nC
Q_{gd}	Gate-drain charge		-	1.9	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V, I_D = 11 A, R_G= 4.7 Ω, V_{GS} = 10 V *(see Figure 12)*	-	4	-	ns
t_r	Rise time		-	22	-	ns
$t_{d(off)}$	Turn-off delay time		-	13	-	ns
t_f	Fall time		-	2.8	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 11 A, V_{GS} = 0 V	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/µs, V_{DD} = 25 V, Tj =150 °C	-	16.2		ns
Q_{rr}	Reverse recovery charge		-	1		nC
I_{RRM}	Reverse recovery current		-	8.1		A

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

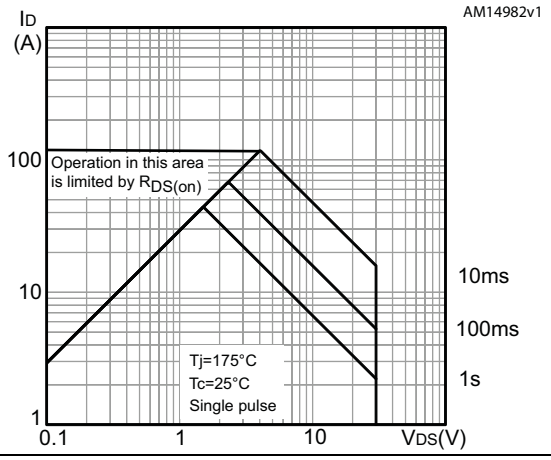


Figure 3. Thermal impedance

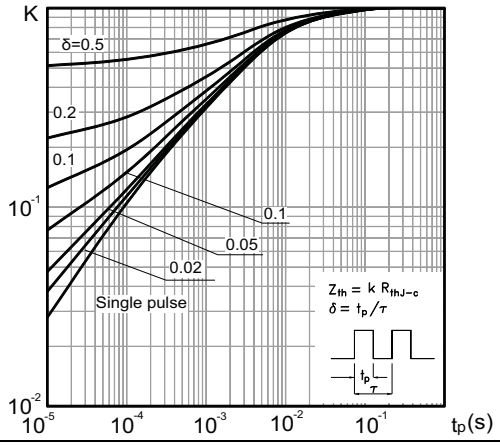


Figure 4. Output characteristics

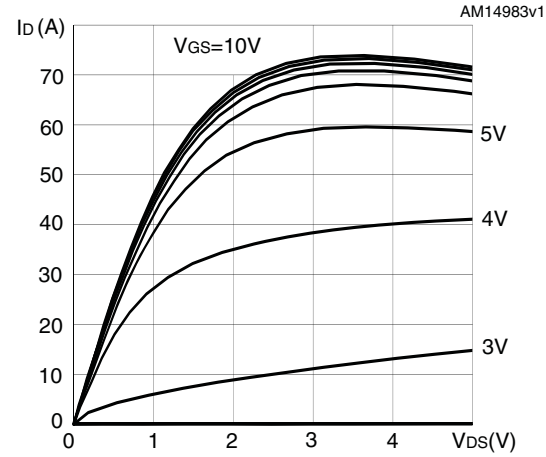


Figure 5. Transfer characteristics

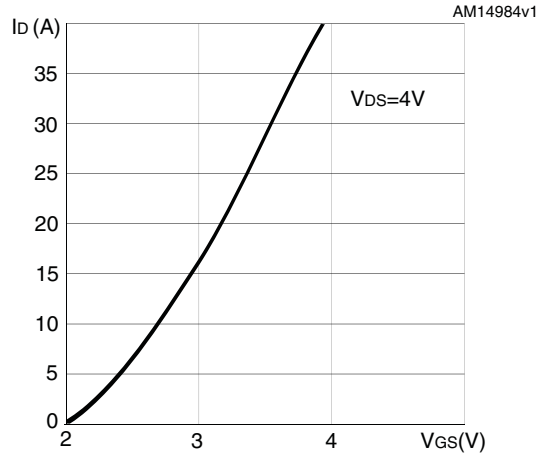


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

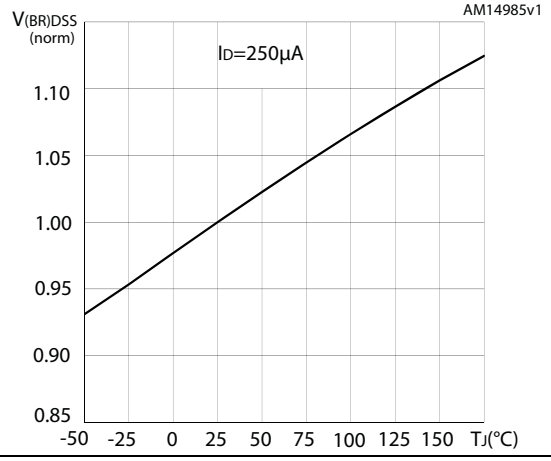


Figure 7. Static drain-source on-resistance

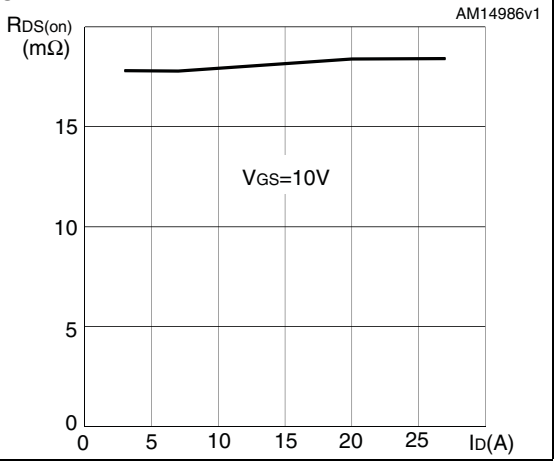


Figure 8. Gate charge vs gate-source voltage

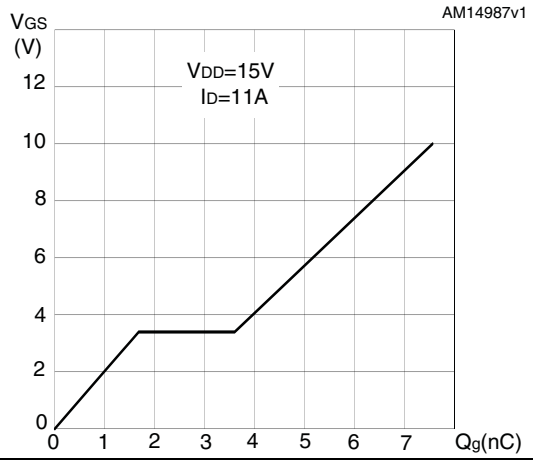


Figure 9. Capacitance variations

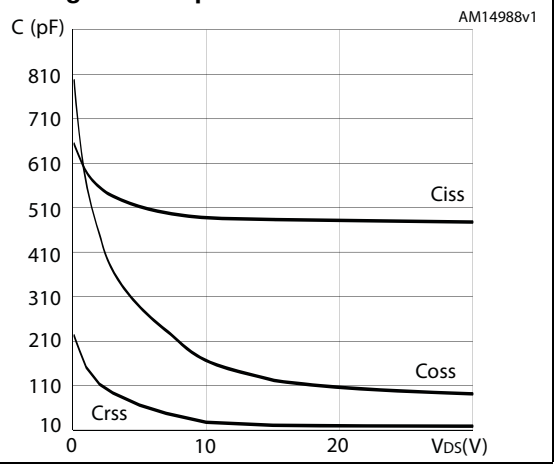


Figure 10. Normalized gate threshold voltage vs temperature

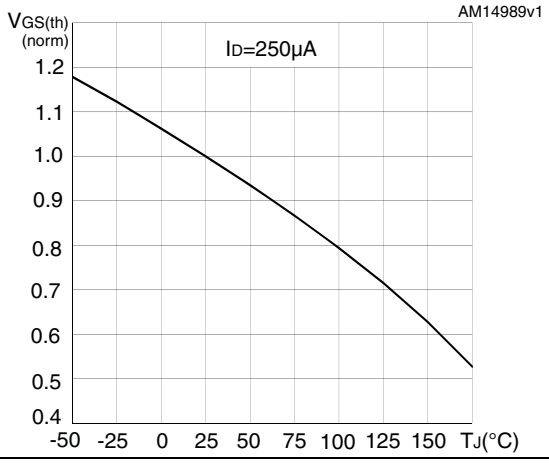
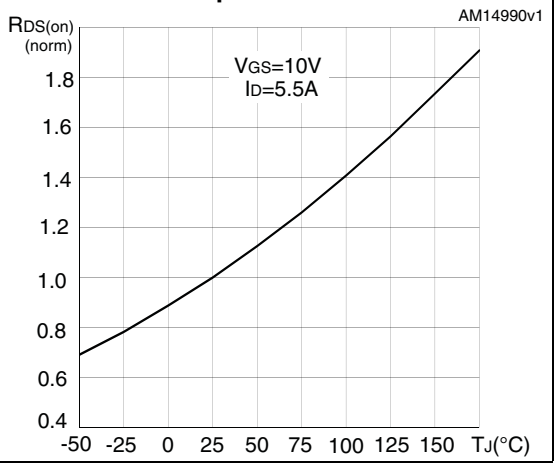


Figure 11. Normalized on-resistance vs temperature



3 Test circuits

Figure 12. witching times test circuit for resistive load

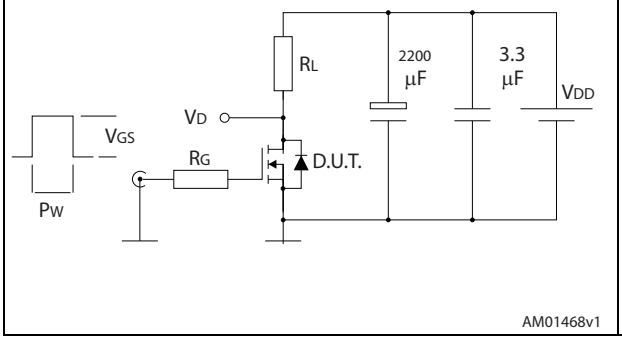


Figure 13. Gate charge test circuit

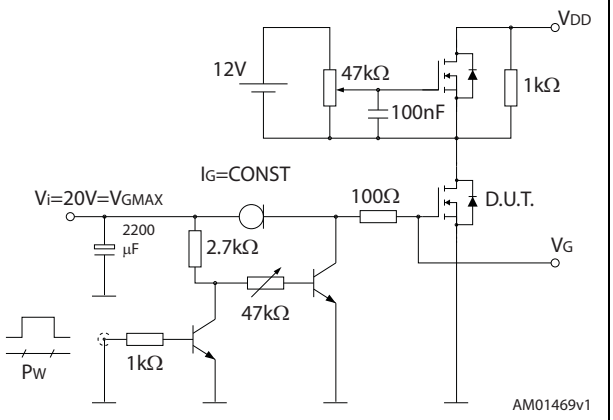


Figure 14. est circuit for inductive load switching and diode recovery times

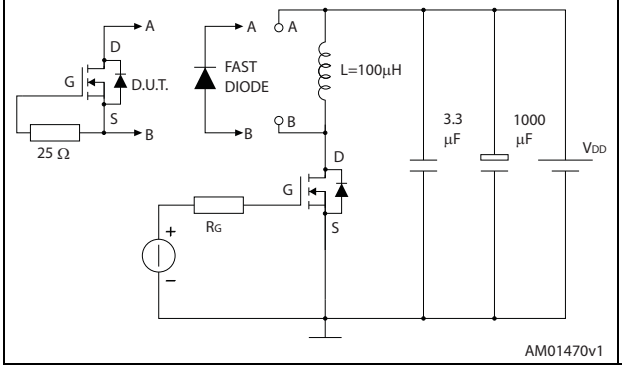


Figure 15. Unclamped inductive load test circuit

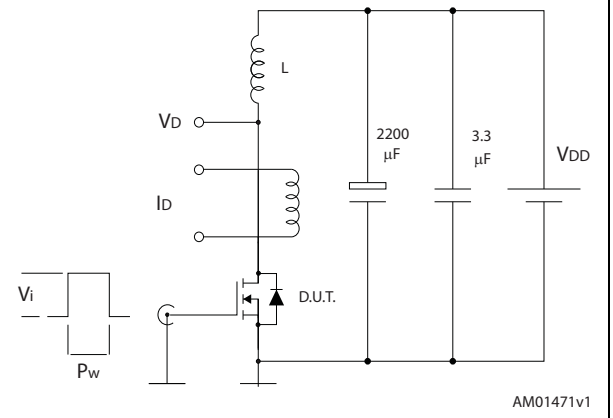


Figure 16. Unclamped inductive waveform

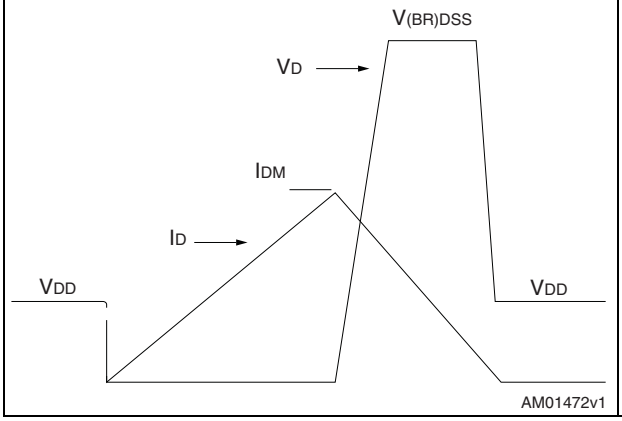
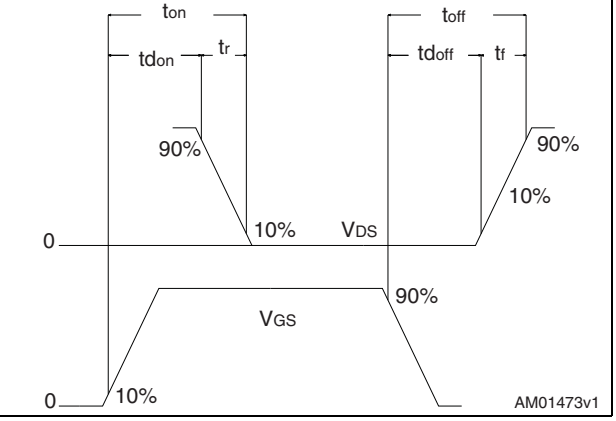


Figure 17. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

4.1 PowerFLAT 5x6 double island WF type R

Figure 18. PowerFLAT 5x6 double island WF type R outline

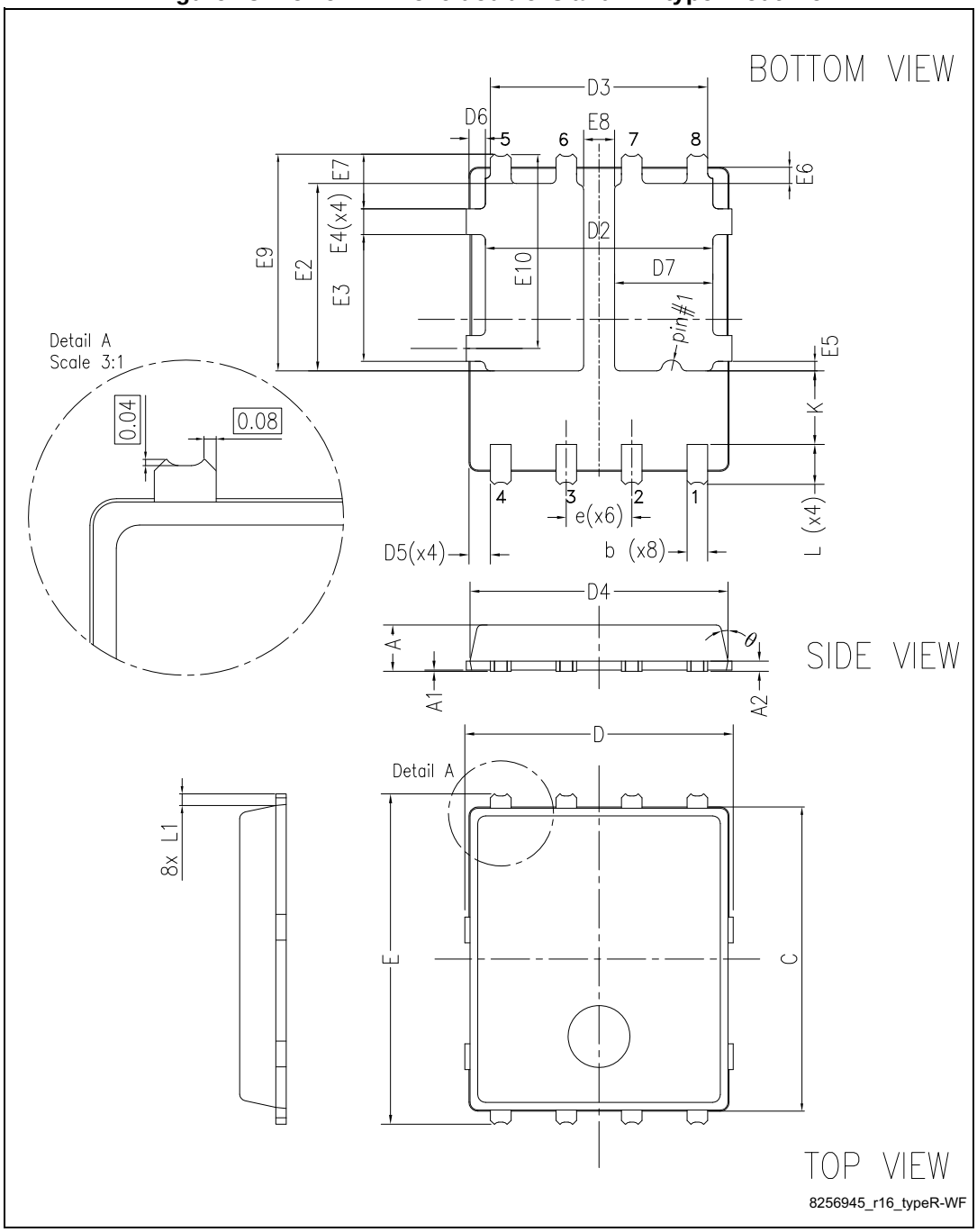
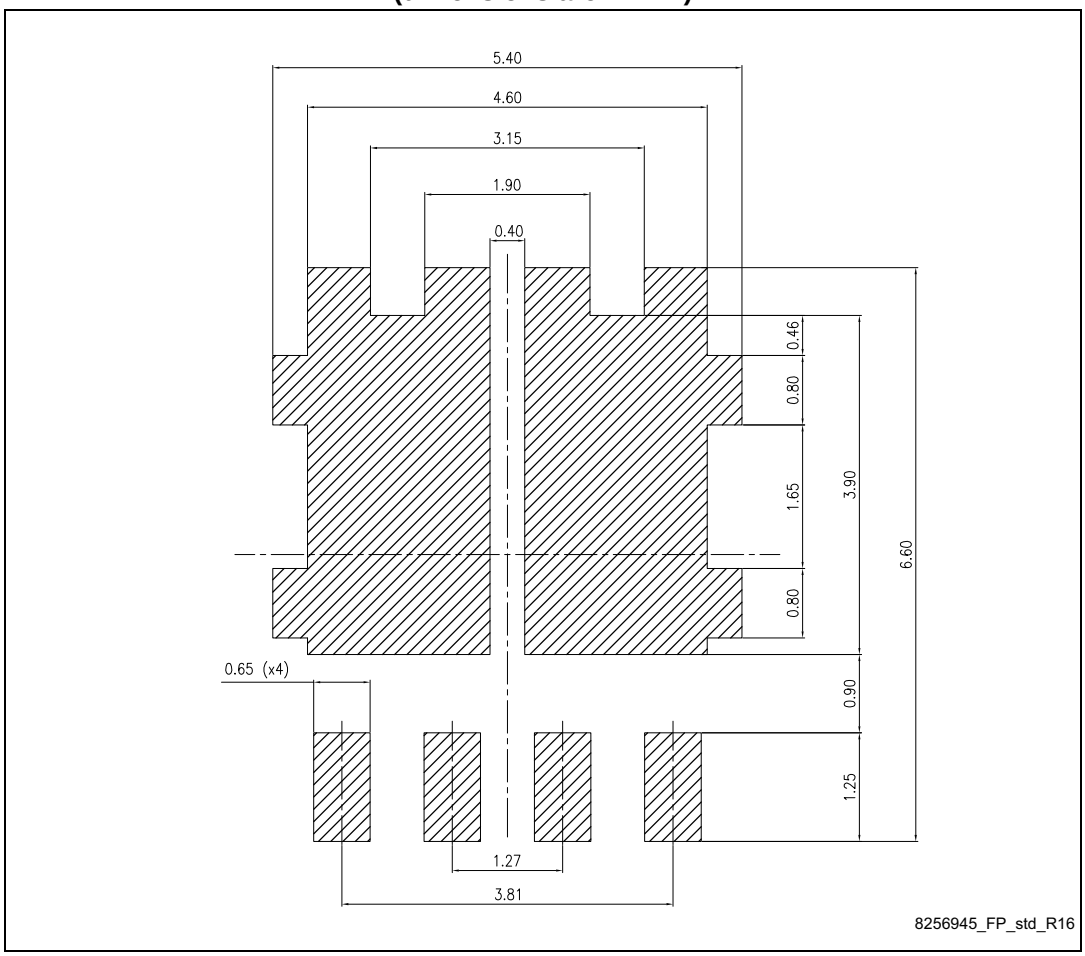


Table 8. PowerFLAT 5x6 double island WF type R mechanical data

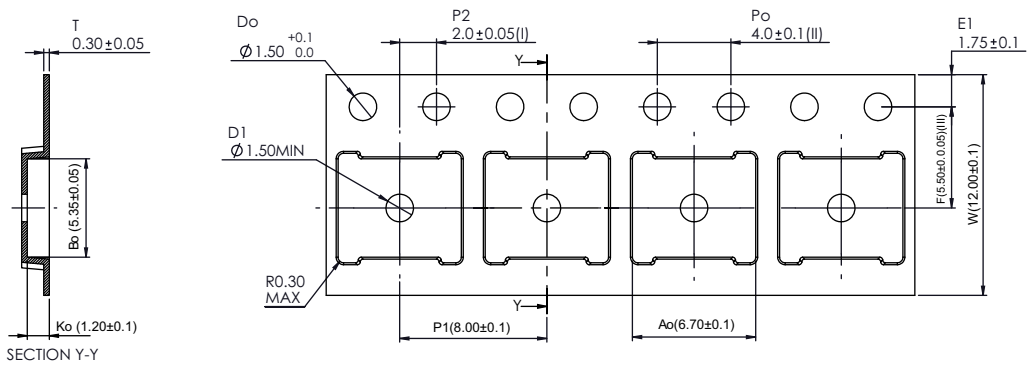
Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E8	0.55	1.00	0.75
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
θ	0°		12°

Figure 19. PowerFLAT™ 5x6 double island recommended footprint (dimensions are in mm)



5 Packing information

Figure 20. PowerFLAT™ 5x6 WF tape



(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.

Base and bulk quantity 3000 pcs

8234350_TapeWF_rev_C

Figure 21. PowerFLAT™ 5x6 package orientation in carrier tape

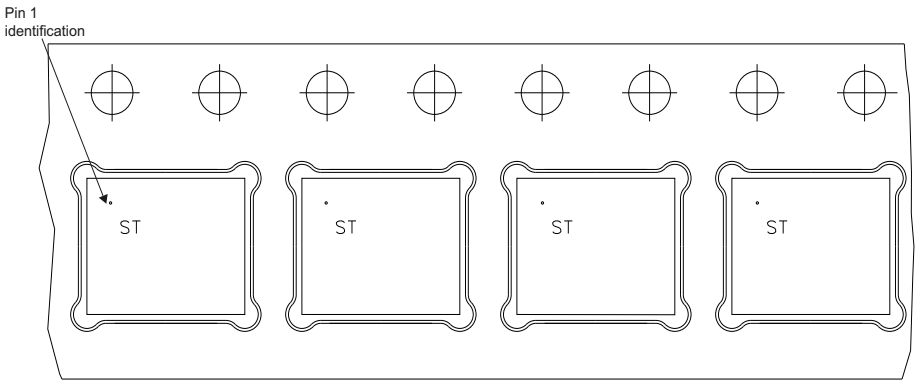
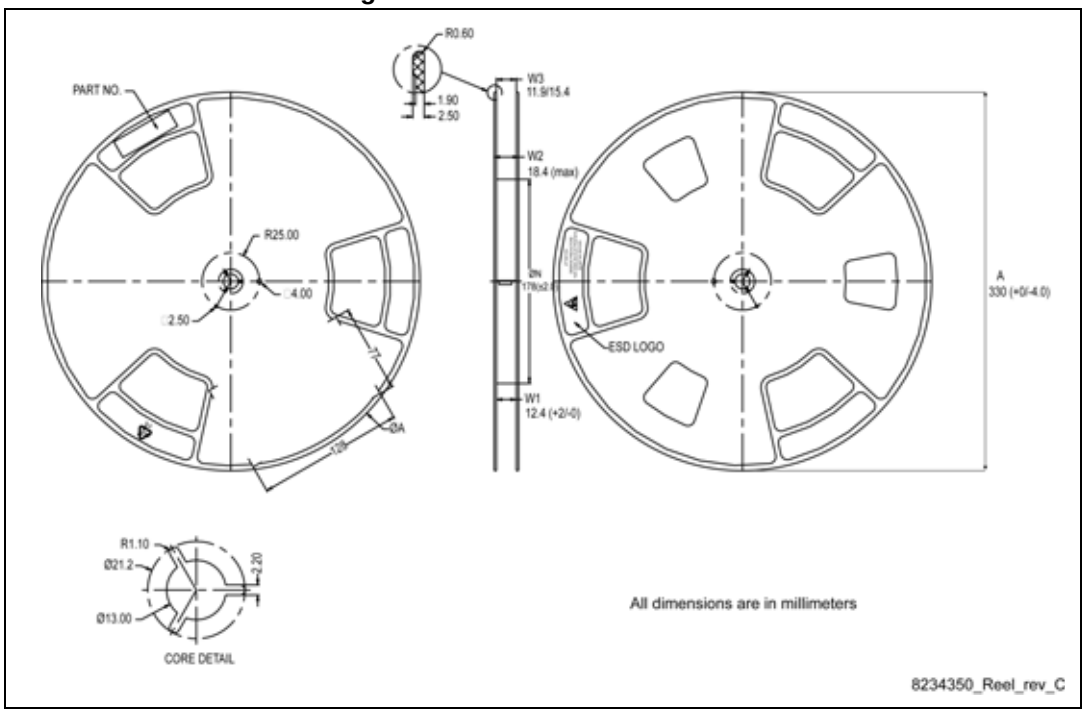


Figure 22. PowerFLAT™ 5x6 reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
24-Jan-2011	1	First release.
03-Oct-2012	2	Section 2.1: Electrical characteristics (curves) has been added. Document status promoted from preliminary data to datasheet. Minor text changes.
14-Dec-2012	3	Modified the Applications section on the coverpage to “Automotive switching applications”.
23-Feb-2015	4	Updated Section 4: Package mechanical data and added Section 5: Packing information. Updated title and features in cover page. Minor text changes.
27-Oct-2015	5	Updated title and features in cover page. Updated *Table 2, Table 3, Table 4 and Table 7.* Updated *Section 4: Package information* Minor text changes.
11-Mar-2016	6	Updated silhoette in cover page. Updated *Table 1: Device summary, Table 2: Absolute maximum ratings, Table 3: Thermal resistance and Table 4: On/off states*. Updated *Figure 2: Safe operating area*. Updated *Section 4.1: PowerFLAT 5x6 double island WF type R* Updated *Section 5: Packing information.* Minor text changes.
7-Oct-2016	7	Updated marking and *Section 4.1: PowerFLAT 5x6 double island WF type R*. Minor text changes.

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