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FDC634P

P-Channel 2.5V Specified PowerTrench MOSFET

General Description

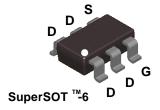
This P-Channel 2.5V specified MOSFET uses Fairchild's low voltage PowerTrench process. It has been optimized for battery power management applications.

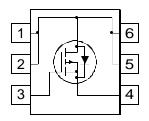
Applications

- Battery management
- · Load switch
- Battery protection

Features

- -3.5 A, -20 V. $R_{DS(ON)} = 80 \text{ m}\Omega$ @ $V_{GS} = -4.5 \text{ V}$ $R_{DS(ON)} = 110 \text{ m}\Omega$ @ $V_{GS} = -2.5 \text{ V}$
- Low gate charge (7.2 nC typical)
- High performance trench technology for extremely low $R_{\text{DS}(\text{ON})}$





Absolute Maximum Ratings T_A=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|-------------------|--|-----------|-------------|-------|
| V _{DSS} | Drain-Source Voltage | | -20 | V |
| V _{GSS} | Gate-Source Voltage | | ±8 | V |
| l _D | Drain Current - Continuous | (Note 1a) | -3.5 | A |
| | – Pulsed | | -20 | |
| P _D | Maximum Power Dissipation | (Note 1a) | 1.6 | W |
| | | (Note 1b) | 0.8 | |
| T_J , T_{STG} | Operating and Storage Junction Temperature Range | | -55 to +150 | °C |

Thermal Characteristics

| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 78 | °C/W |
|-------------------|---|-----------|----|------|
| R ₀ JC | Thermal Resistance, Junction-to-Case | (Note 1) | 30 | °C/W |

Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|----------------|---------|-----------|------------|------------|
| .634 | FDC634P | 7" | 8mm | 3000 units |

| Symbol | Parameter | Test Conditions | Min | Тур | Max | Units |
|---|---|--|------|----------------|------------------|----------|
| Off Char | acteristics | | | l | ı | <u>l</u> |
| BV _{DSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$ | -20 | | | V |
| <u>ΔBVpss</u> ΔT,j | Breakdown Voltage Temperature Coefficient | $I_D = -250 \mu\text{A}$, Referenced to 25°C | | -12 | | mV/°C |
| l _{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$ | | | -1 | μΑ |
| GSSF | Gate-Body Leakage, Forward | $V_{GS} = 8 \text{ V}, \qquad V_{DS} = 0 \text{ V}$ | | | 100 | nA |
| I _{GSSR} | Gate-Body Leakage, Reverse | $V_{GS} = -8 \text{ V}$ $V_{DS} = 0 \text{ V}$ | | | -100 | nA |
| On Char | acteristics (Note 2) | | | | | |
| V _{GS(th)} | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$ | -0.4 | -0.8 | -1.5 | V |
| ΔV _{GS(th)} ΔT _J | Gate Threshold Voltage Temperature Coefficient | I_D = -250 μ A, Referenced to 25°C | | 3 | | mV/°C |
| R _{DS(on)} | Static Drain–Source On–Resistance | $V_{GS} = -4.5 \text{ V}, I_D = -3.5 \text{ A}$ $V_{GS} = -2.5 \text{ V}, I_D = -3.1 \text{ A}$ $V_{GS} = -4.5 \text{ V}, I_D = -3.5 \text{A}, T_J = 125^{\circ}\text{C}$ | | 60 82 77 | 80 110 130 | mΩ |
| I _{D(on)} | On-State Drain Current | $V_{GS} = -4.5 \text{ V}, V_{DS} = -5 \text{ V}$ | -10 | | | Α |
| g FS | Forward Transconductance | $V_{DS} = -5 \text{ V}, \qquad I_{D} = -3.5 \text{ A}$ | | 11 | | S |
| Dynamic | : Characteristics | | | | | |
| Ciss | Input Capacitance | $V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V},$ | | 779 | | pF |
| Coss | Output Capacitance | f = 1.0 MHz | | 121 | | pF |
| C _{rss} | Reverse Transfer Capacitance | | | 56 | | pF |
| Switchin | g Characteristics (Note 2) | | | | | |
| t _{d(on)} | Turn-On Delay Time | $V_{DD} = -10 \text{ V}, \qquad I_D = -1 \text{ A},$ | | 10 | 20 | ns |
| t _r | Turn-On Rise Time | $V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$ | | 9 | 19 | ns |
| t _{d(off)} | Turn-Off Delay Time | 1 | | 27 | 43 | ns |
| t _f | Turn-Off Fall Time | | | 11 | 20 | ns |
| Qg | Total Gate Charge | $V_{DS} = -10 \text{ V}, I_{D} = -3.5 \text{ A},$ | | 7.2 | 10 | nC |
| Q _{gs} | Gate-Source Charge | V _{GS} = -4.5 V | | 1.7 | | nC |
| Q _{gd} | Gate-Drain Charge | | | 1.5 | | nC |
| Drain-S | ource Diode Characteristics | and Maximum Ratings | | | | |
| ls | Maximum Continuous Drain-Source | | | | -1.3 | Α |
| V_{SD} | Drain-Source Diode Forward Voltage | $V_{GS} = 0 \text{ V}, I_S = -1.3 \text{ A} \text{(Note 2)}$ | | -0.8 | -1.2 | V |

Notes

R_{0,N} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0,C} is guaranteed by design while R_{0,CA} is determined by the user's board design.



a) 78°C/W when mounted on a 1in² pad of 2 oz copper



b) 156°C/W when mounted on a minimum pad of 2 oz copper

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300 μ s, Duty Cycle < 2.0%

Typical Characteristics

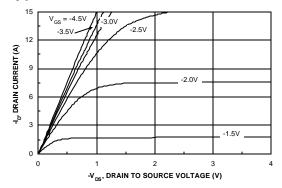


Figure 1. On-Region Characteristics.

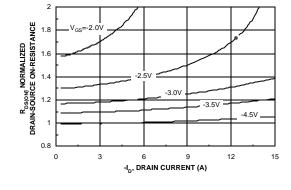


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

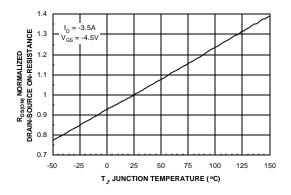


Figure 3. On-Resistance Variation with Temperature.

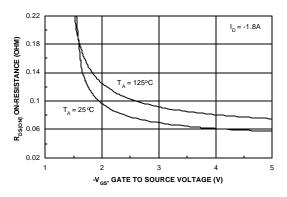


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

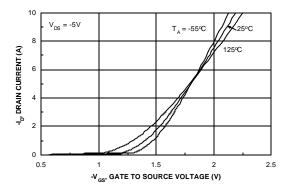


Figure 5. Transfer Characteristics.

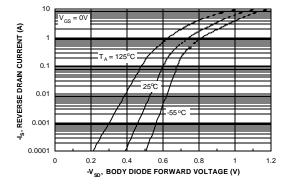
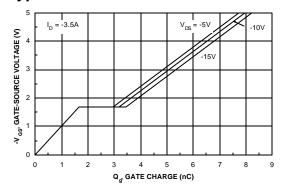


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics



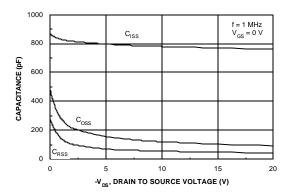
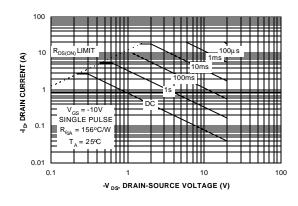


Figure 7. Gate Charge Characteristics.





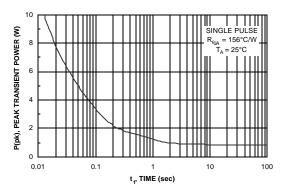


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

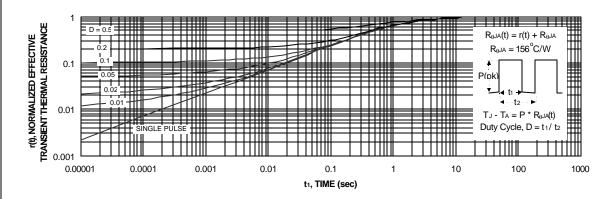


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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