2.5V / 3.3V Dual 2:1 Differential Clock / Data Multiplexer with LVPECL Outputs

Multi-Level Inputs w/ Internal Termination

The NB6L56 is a high performance Dual 2–to–1 Differential Clock or Data multiplexer. The differential inputs incorporate internal 50 Ω termination resistors that are accessed through the VT pin. This feature allows the NB6L56 to accept various Differential logic level standards, such as LVPECL, CML or LVDS. Outputs are 800 mV LVPECL signals. For interface options see Figures 12 – 15.

The NB6L56 produces minimal Clock or Data jitter operating up to 2.5 GHz or 2.5 Gbps, respectively. As such, the NB6L56 is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data distribution applications.

The NB6L56 is offered in a low profile 5 mm x 5 mm 32-pin QFN package and is a member of the ECLinPS MAX™ family of high performance Clock / Data products. Application notes, models, and support documentation are available at www.onsemi.com.

Features

- Maximum Input Data Rate > 2.5 Gbps
- Maximum Input Clock Frequency > 2.5 GHz
- Jitter
 - < 1 ps RMS RJ (Data)
 - < 10 ps PP DJ (Data)
 - < 0.7 ps RMS Crosstalk induced jitter (CLOCK)
- 360 ps Max Propagation Delay
- 180 ps Max Rise and Fall Times
- Operating Range:

 $V_{CC} = 2.5 \pm 5\%$ (2.375 V to 2.625 V)

 $V_{CC} = 3.3 \pm 10\%$ (3.0 V to 3.6 V)

- Internal 50 Ω Input Termination Resistors
- Industrial Temp. Range (-40°C to 85°C)
- QFN-32 Package
- These are Pb-Free Devices

Applications

- Clock and Data Distribution
- Networking and Communications
- High End Computing
- Wireless and Wired Infrastructure

End Products

- Servers
- Ethernet Switch/Routers
- ATE
- Test and Measurement



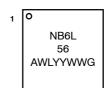
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QFN32 MN SUFFIX CASE 488AM

MARKING DIAGRAM*



A = Assembly Location

WL = Wafer Lot
 YY = Year
 WW = Work Week
 G = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

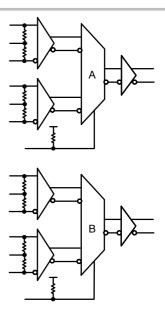


Figure 1. Simplified Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

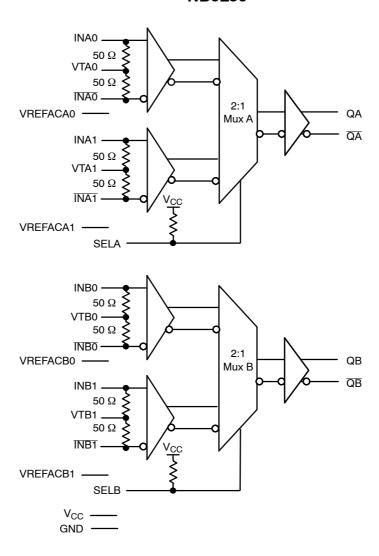


Figure 2. Pin Configuration (Top View)

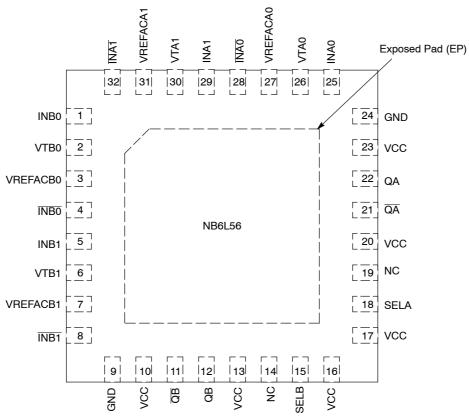


Figure 3. NB6L56 Pinout: QFN-32 (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Pin Description
1, 4 5, 8 25, 28 29, 32	INBO, ĪNBO INB1, ĪNB1 INAO, ĪNĀO INA1, ĪNĀ1	LVPECL, CML, LVDS Input	Noninverted, Inverted Differential Input pairs (Note 1). Default state is indeterminate if left floating open. Do not connect unused input pairs with one input connected to VCC and the complementary input to GND. For differential and single ended interface, see "Interface Applications".
2, 6 26, 30	VTB0, VTB1 VTA0, VTA1		Internal 100 Ω Center–tapped Termination Pin for Differential Input pairs (Figure 4)
3 7 27 31	VREFACB0 VREFACB1 VREFACA0 VREFACA1	ı	Output Voltage Reference for Capacitor-Coupled Inputs or Single Ended Interface (see "Interface Applications")
15 18	SELB SELA	LVTTL / LVCMOS Input	Input Select pin; LOW for IN0 Inputs, HIGH for IN1 Inputs; defaults HIGH when left open
14, 19	NC	-	No Connect
10, 13,16,17 20, 23	VCC	Power	Positive Supply Voltage. All VCC pins must be connected to the positive power supply for correct DC and AC operation.
11, 12 21, 22	QB, QB QA, QA	LVPECL Output	Inverted, Non-inverted Differential Outputs Note 1.
9, 24	GND	Ground	Negative Supply Voltage, connected to Ground
-	EP	-	The Exposed Pad (EP) on the package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat–sinking conduit. The pad is connected to the die and must only be connected electrically to GND on the PC board.

If no signal is applied on any INxn input pair, the device will be susceptible to self-oscillation.
 All V_{CC} and GND pins must be externally connected to a power supply for proper operation.

Table 2. INPUT SELECT FUNCTION TABLE

SELA/SELB	Q	Q
L	INx0	ĪNx0
Н	INx1	ĪNx1

Table 3. ATTRIBUTES

Characte	Value			
ESD Protection	Human Body Model Machine Model	>2 kV 200 V		
Input Pullup resistor (R _{PU})		75 kΩ		
Moisture Sensitivity (Note 3)	QFN32	Level 1		
Flammability Rating	UL 94 V-0 @ 0.125 in			
Transistor Count	1023			
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test				

^{3.} For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 4)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	GND = 0 V		4.0	V
V _{INPP}	Differential Input Voltage INx - INx			1.89	V
I _{IN}	Input Current Through RT (50 Ω Resistor)			±40	mA
l _{OUT}	Output Current	Continuous Surge		±50 ±100	mA
I _{VREFAC}	VREFAC Sink/Source Current			±1.5	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 4)	0 lfpm 500 lfpm	QFN – 32 QFN – 32	31 27	°C/W
θJC	Thermal Resistance (Junction-to-Case) (Note 4)	Standard Board	QFN - 32	12	°C/W
ψιс	Thermal Resistance (Junction-to-Board)			16	°C/W
T _{sol}	Wave Solder Pb-Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

^{4.} JEDEC standard 51-6, multilayer board - 2S2P (2 signal, 2 power) with eight filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS V_{CC} = 2.5 \pm 5% (2.375 V to 2.625 V); V_{CC} = 3.3 \pm 10% (3.0 V to 3.6 V) (Note 5)

Symbol	Characteristic	Min	Тур	Max	Unit
Icc	Power Supply Current (Inputs and Outputs Open)		65	85	mA
LVPECL OL	JTPUTS	•	•		
V _{OH}	Output HIGH Voltage	V _{CC} – 1.145		V _{CC} - 0.895	mV
V _{OL}	Output LOW Voltage	V _{CC} – 2.000		V _{CC} - 1.695	mV
V _{OUT}	Output Swing (Single Ended) Output Swing (Differential)	400 800	800 1600		mV
DIFFERENT	FIAL INPUT DRIVEN SINGLE-ENDED (Note 6) (Figures 5 and 6)	•	•		
V _{th}	Input Threshold Reference Voltage Range	1125		V _{CC} – 75	mV
V _{IH}	Single-ended Input HIGH Voltage	V _{th} + 75		V _{CC}	mV
V _{IL}	Single-ended Input LOW Voltage	GND		V _{th} – 75	mV
V _{ISE}	Single-ended Input Voltage (V _{IH} - V _{IL}) (Note 6)	150		3015	mV
DIFFERENT	TIAL INPUTS DRIVEN DIFFERENTIALLY (Note 7) (Figures 7 and 8)				
V_{IHD}	Differential Input HIGH Voltage	1200		V _{CC}	mV
V_{ILD}	Differential Input LOW Voltage	GND		V _{IHD} – 100	mV
V_{ID}	Differential Input Voltage (V _{IHD} - V _{ILD})	100		1890	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Figure 9)	1150		V _{CC} – 50	mV
I _{IH}	Input HIGH Current (VTnx Open)	-150		150	μΑ
I _{IL}	Input LOW Current (VTnx Open)	-150		150	μΑ
LVTTL / LVC	CMOS INPUTS (SELA/SELB)				
V _{IH}	Input HIGH Voltage	2.0			V
V _{IL}	Input LOW Voltage			0.8	٧
I _{IL}	Input LOW Current (V _{IN} = 0.5 V)	-300			μΑ
I _{IH}	Input HIGH Current (V _{CC})			75	μΑ
TERMINATI	ON RESISTORS				
R _{TIN}	Internal Input Termination Resistor INxn/INxn to VTxn	45	50	55	Ω
REFERENC	E VOLTAGE				
VREF-AC	Output Reference Voltage	V _{CC} - 1.35	V _{CC} - 1.2	V _{CC} – 1.1	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 5. Outputs evaluated with 50 Ω resistors to V_{TT} = V_{CC} 2.0 V for proper operation (See Figure 16).
 6. VTH is applied to the complementary input when operating in single–ended mode. VIH, VIL and VTH parameters must be complied with simultaneously.
- 7. VIHD, VILD and VCMR parameters must be complied with simultaneously. VCMR max varies 1:1 with V_{CC}.

Table 6. AC CHARACTERISTICS V_{CC} = 2.5 \pm 5% (2.375 V to 2.625 V); V_{CC} = 3.3 \pm 10% (3.0 V to 3.6 V) (Note 8)

Symbol	Characteristic	Min	Тур	Max	Unit
f _{MAX}	$\begin{array}{ll} \text{Maximum Input Clock Frequency} & \text{$V_{outpp} \geq 400 \text{ mV}$} \\ \text{Maximum Operating Data Rate (NRZ)} & \text{$V_{outpp} \geq 400 \text{ mV}$} \end{array}$	2.5 2.5			Ghz Gbps
fSEL	Maximum Toggle Frequency, SELA/SELB	25	50		MHz
V _{OUTPP}	Output Voltage Amplitude (Differential Interconnect) $f_{in} \le 2.5 \text{ GHz}$	400			mVpp
t _{PLH} , t _{PHL}	Propagation Delay to Differential Outputs, @ 1 GHz, INxn/INxn to Qx, Qx SELx to Qx, Qx	160 100	250 260	360 400	ps
t _{PLH} Tempco	Differential Propagation Delay Temperature Coefficient		143		Δfs/°C
tskew	Input to Input per Bank Within Device Output Bank to Output Bank Within Device		10 12	20 25	ps
UITTER	DATA JITTER R _J for K28.7 at 2.5 GHz (RMS) D _J for NRZ PRBS23 / K28.5 at 2.5 Gbps CLOCK JITTER Cycle to Cycle (1K WFMS; RMS) Total Jitter TJ (PP)			1 10 1 10	ps
tjit(φ)	Integrated Phase Jitter fin = 155.52 MHz and 1GHz 12 kHz $-$ 20 MHz Offset (RMS)		35		fs
t _{JITTER}	Crosstalk Induced Jitter Input to Input per Output Bank Within Device (Note 9)			0.7	psRMS
V _{INPP}	Input Voltage Swing (Differential Configuration) (Note 10)	100		1200	mV
t _{r,} , t _f	Output Rise/Fall Times @ 1 GHz (20% – 80%), Q _x , Q _x		100	180	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

^{8.} Differential 50% duty cycle at V_{INPPmin} clock source. Outputs evaluated with 50 Ω resistors to V_{TT} = V_{CC} – 2.0 V (See Figure 16). Input crosspoint to output crosspoint for INxn/INxn to Qx, Qx; 50% input to output crosspoint for SELx to Qx, Qx. See Figures 5, 10 and 11.

^{9.} Crosstalk is measured at the output while applying two similar clock frequencies that are asynchronous with respect to each other at the inputs.

^{10.} Input voltage swing is a single-ended measurement operating in differential mode.

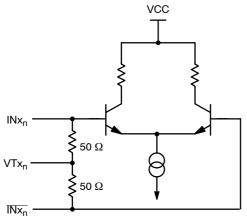


Figure 4. Simplified Input Structure

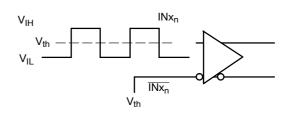


Figure 5. Differential Input Driven Single-Ended

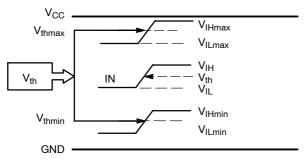


Figure 6. V_{th} Diagram

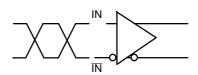
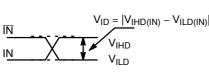


Figure 7. Differential Inputs Driven Differentially



 $V_{ID} = |V_{IHD(IN)} - V_{ILD(IN)}|$

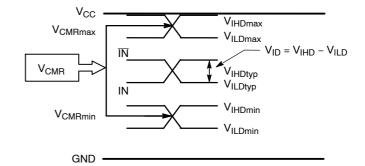


Figure 8. Differential Inputs Driven Differentially Figure 9. VCMR Diagram

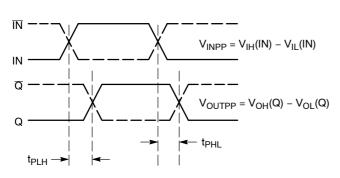


Figure 10. AC Reference Measurement

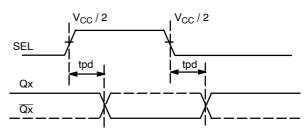


Figure 11. SEL to Qx Timing Diagram

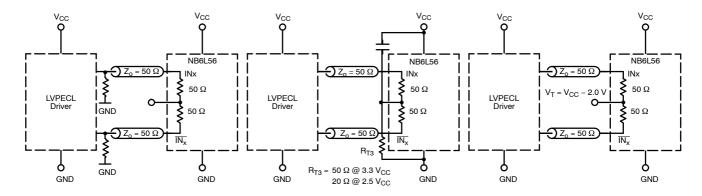


Figure 12. Typical LVPECL Interface (see AND8020)

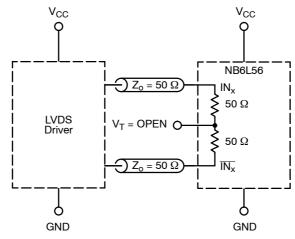


Figure 13. Typical LVDS Interface

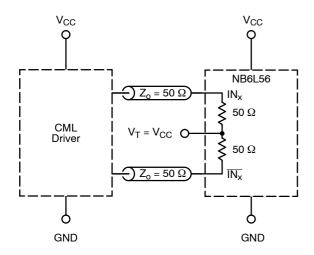


Figure 14. Typical Standard 50 Ω Load CML Interface

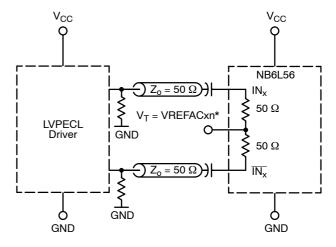


Figure 15. Typical LVPECL Capacitor–Coupled Differential Interface (V_T Connected to V_{REFAC}) *VREFAC bypassed to ground with a 0.01 μF capacitor.

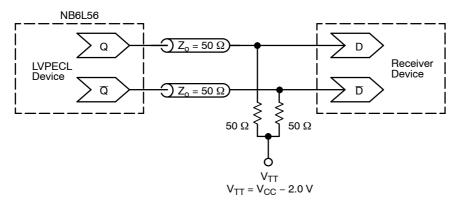


Figure 16. Typical Termination for LVPECL Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

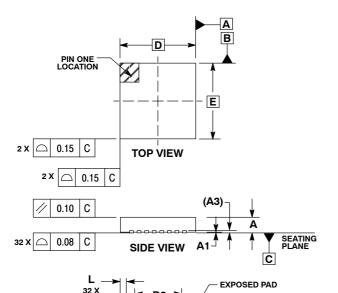
ORDERING INFORMATION

Device	Package	Shipping [†]
NB6L56MNG	QFN32 (Pb-Free)	74 Units / Rail
NB6L56MNTXG	QFN32 (Pb-Free)	1000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

QFN32 5*5*1 0.5 P CASE 488AM-01 **ISSUE O**



BOTTOM VIEW

0.10 С A B

0.05 С

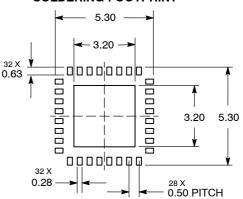
NOTES:

- NOTES:

 1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED
- TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
- COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS			
DIM	MIN	NOM	MAX	
Α	0.800	0.900	1.000	
A1	0.000	0.025	0.050	
A3	0.	200 REI	=	
b	0.180	0.250	0.300	
D	5	.00 BSC		
D2	2.950	3.100	3.250	
E	5	.00 BSC		
E2	2.950	3.100	3.250	
е	0.500 BSC			
K	0.200	-		
L	0.300	0.400	0.500	

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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