SP3T SWITCH WITH IMPEDANCE DETECTION MICRO-USB SWITCH TO SUPPORT USB, UART, AUDIO, AND CHARGER

Check for Samples: TSU5511

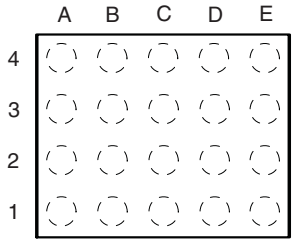
FEATURES

- **Compatible Accessories**
  - **USB Data Cable**
  - **UART Cable**
  - **Charger (Dedicated Charger or Host/Hub Charger)**
  - **Stereo Headset With Mic**
- **Integrated LDOs for V_{REF} and Mic Bias**
- **USB Path Supports USB 2.0 High Speed**
- **Audio Path Provides Negative Rail Support and Click/Pop Reduction**
- **Supports Factory Test Mode**
- **1.8-V Compatible I^2C Interface**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **ESD Performance DP/DM/ID/V_{BUS} to GND**
  - **±8-kV Contact Discharge (IEC 61000-4-2)**
  - **±15-kV Air Gap Discharge (IEC 61000-4-2)**

APPLICATIONS

- **Cellular Telephones**

YZP PACKAGE
(LASER SCRIBE VIEW)



PIN ASSIGNMENTS

	A	B	C	D	E
4	MIC	ISET	UART_TX	USB_DM	USB_DP
3	R2.2K	$\overline{INT}$	UART_RX	ID	DP
2	SDA	SCL	DSS	GND	DM
1	CLDO	V_{SUPPLY}	AUDIO_R	AUDIO_L	V_{BUS}

DESCRIPTION

The TSU5511 is designed to interface the cell phone UART, USB, and audio chips with external peripherals via a micro-USB connector. The switch features impedance detection for identification of various accessories that are attached through DP and DM of the micro-USB port. When an accessory is plugged into the micro-USB port, the switch uses a detection mechanism to identify the accessory (see State Machine for details). It will then switch to the appropriate channel—data, audio, or UART.

The TSU5511 has an I^2C interface for communication with the cellphone baseband or applications processor. An interrupt is generated when anything plugged into the micro-USB is detected. Another interrupt is generated when the device is unplugged.

Table 1. ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	WCSP – YZP (0.5-mm pitch)	Tape and reel	TSU5511YZPR	A62

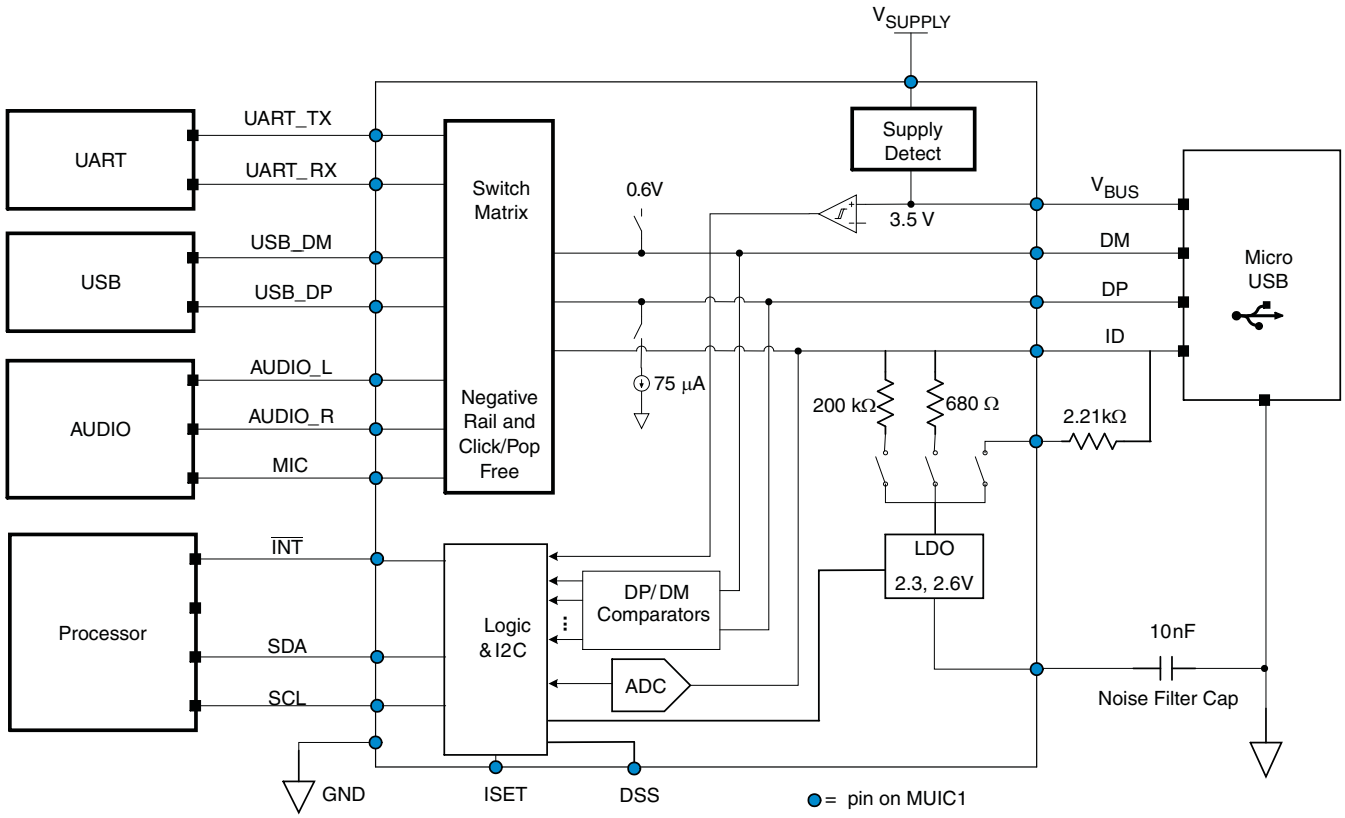
(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

Table 2. SUMMARY OF TYPICAL CHARACTERISTICS

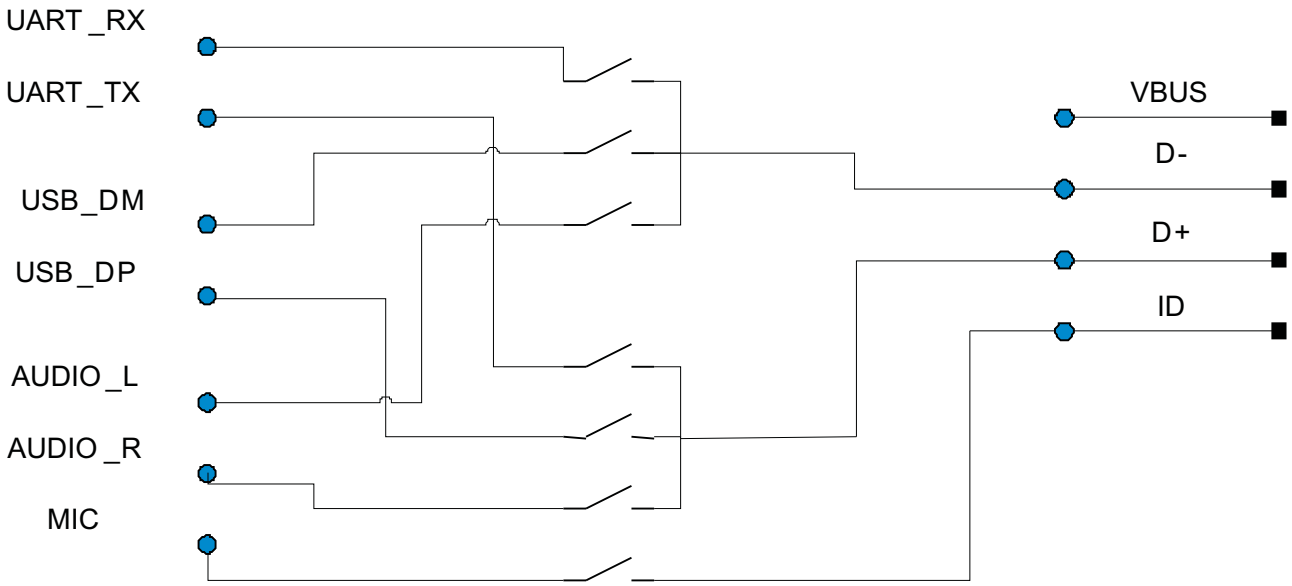
T_A = 25°C

	USB PATH	UART PATH	AUDIO PATH	MIC PATH
Number of switches	2	2	2	1
ON-state resistance (r_{ON})	4.5 Ω	37 Ω	3.8 Ω	9 Ω
ON-state resistance match (Δr_{ON})	1 Ω	2 Ω	1 Ω	N/A
ON-state resistance flatness ($r_{ON(flat)}$)	0.5 Ω	20 Ω	0.1 Ω	0.5 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	1 ms	1 ms	1 ms	1 ms
Bandwidth (BW)	830 MHz	295 MHz	788 MHz	573 MHz
OFF isolation (O_{ISO})	–20 dB	-100 dB	–100 dB	–37 dB
Crosstalk (X_{TALK})	–42 dB	-98 dB	–120 dB	–125 dB
Total harmonic distortion (THD)	N/A	N/A	0.087%	0.07%
Leakage current ($I_{NO(OFF)}/I_{NC(OFF)}$)	25 nA	100 nA	25 nA	5 nA
Package options	YZP package, 0.5-mm pitch			

BLOCK DIAGRAM



SWITCH MATRIX BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
AUDIO_L	D1	I/O	Stereo audio left channel
AUDIO_R	C1	I/O	Stereo audio right channel
CLDO	A1	O	Capacitor connection for LDO noise filtering
DM	E2	I/O	Common I/O port for USB, UART, Audio. Connected to USB receptacle.
DP	E3	I/O	Common I/O port for USB, UART, Audio. Connected to USB receptacle.
DSS	C2	I	Pulldown or pullup resistor connection to determine default switch
GND	D2	GND	Ground
ID	D3	I/O	Common I/O port for microphone, ID detection
$\overline{INT}$	B3	O	Open-drain interrupt output. Connect an external pullup resistor.
ISET	B4	O	Output to charger for high-current charging mode. Open-drain output.
MIC	A4	I/O	Microphone signal
R2.2K	A3	I	2.21 kΩ connection for microphone bias
SCL	B2	I	I^2C clock input. Connect an external pullup resistor.
SDA	A2	I/O	I^2C data. Connect an external pullup resistor.
UART_RX	C3	I/O	UART receive data
UART_TX	C4	I/O	UART transmit data
USB_DM	D4	I/O	USB D– connected to host
USB_DP	E4	I/O	USB D+ connected to host
V_{BUS}	E1	I	V_{BUS} power supply from USB receptacle
V_{SUPPLY}	B1	I	2.8-V to 4.4-V battery supply voltage

ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{BUS}	Supply voltage from USB connector		–0.5	28	V
V_{SUPPLY}	Supply voltage from battery		–0.5	6	V
V_{USBIO}	Switch I/O voltage range	USB switch	–0.5	V_{SUPPLY}+0.5	V
V_{UARTIO}		UART switch	–0.5	V_{SUPPLY}+0.5	V
V_{AUDIO}		Audio switch	–1.5	V_{SUPPLY}+0.5	V
V_{MICIO}		Mic switch	–0.5	V_{SUPPLY}+0.5	
$V_{LOGICIO}$	Logic input, output and I/O voltage ranges	DSS, SCL, SDA	–0.5	V_{SUPPLY}+0.5	V
I_{BUS}	Input current on V_{BUS} pin			100	mA
I_{SUPPLY}	Input current on V_{SUPPLY} pin			100	mA
I_{GND}	Continuous current through GND			100	mA
I_K	Analog port diode current		–50	50	mA
I_{SW-DC}	ON-state continuous switch current		–60	60	mA
$I_{SW-PEAK}$	ON-state peak switch current		–150	150	mA
I_{IK}	Digital logic input clamp current	V_L < 0		–50	mA
I_{LOGIC_O}	Continuous current through logic output			50	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

THERMAL IMPEDANCE RATINGS

				UNIT
θ_{JA}	Package thermal impedance	YZP package	75.5	°C/W

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{BUS}	Supply voltage from USB connector		4.35	6.7	V
V_{SUPPLY}	Supply voltage from battery		2.8	4.4	V
V_{USBIO}	Switch I/O voltage range	USB switch	0	3.6	V
V_{UARTIO}		UART switch	0	V_{SUPPLY}	
V_{AUDIO}		Audio switch	–1.3	1.3	
V_{MICIO}		Mic switch	0	2.3	
$V_{LOGICIO}$	Logic input, output and I/O voltage ranges	DSS, SCL, SDA	0	V_{SUPPLY}	V
I_{SW-DC}	ON-state continuous switch current				mA
I_{SWPEAK}	ON-state peak switch current				mA
T_A	Ambient temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, typical values are at V_{SUPPLY} = 3.6 V, V_{BUS} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{SUPPLY} supply current	$I_{VSUPPLY}$	V_{SUPPLY} = 4.2 V, V_{BUS} = 0 V, ADC_EN = 0,	CP_EN = 0, SEMREN = 0		6	10	µA
			CP_EN = 0, SEMREN = 1		6	10	
			CP_EN = 1, SEMREN = 1		60	70	
V_{BUS} supply current	I_{VBUS}	V_{SUPPLY} = 3.6 V, V_{BUS} = 5 V, ADC_EN = 0,	CP_EN = 0, SEMREN = 0		45	60	µA
			CP_EN = 0, SEMREN = 1		45	60	
			CP_EN = 1, SEMREN = 1		80	98	
V_{BUS} detect threshold	V_{BUSDET}	V_{BUS} = 0 to 5 V, read the INT		3	3.5	4	V
Microphone removal threshold	V_{MRCOMP}	Ramp ID down, read the INT	LDO voltage = 2.6 V		2.2		V
			LDO voltage = 2.3 V		1.95		
SEND/END threshold	V_{SECOMP}	LDO voltage = 2.3 or 2.6 V, ramp ID up from 0 V, read the INT			0.15		V
ID resistance 1	R_{ID1}	ID_200 = 1, V_{SUPPLY} = 3.6 V		160	200	240	kΩ
ID resistance 2	R_{ID2}	ID_620 = 1, V_{SUPPLY} = 3.6 V		496	620	744	Ω

LDO ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, typical values are at V_{SUPPLY} = 3.6 V, V_{BUS} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage	V_{BUS}			4.35	5	6.7	V
	V_{SUPPLY}			2.8		4.4	
Output voltage	V_{OUT-26}	I_O = 0 mA		2.54	2.6	2.65	V
	V_{OUT-23}			2.2	2.3	2.35	
Max output current	I_{O-26}	Measured at R2.2K pin				10	µA
	I_{O-23}					500	
Power supply rejection	PSR_{217}	V_{OUT} = 2.3 V, V_{SUPPLY} = 3.2 V, I_O = 150 to 450 µA,	f = 217 Hz		–50		dB
	PSR_{1k}		f = 1 kHz		–42		dB
Integrated output noise	e_{n-OUT}	V_{OUT} = 2.3 V, V_{SUPPLY} = 3.2 V, I_O = 150 to 450 µA,	f = 20 Hz to 20 kHz (A-weighted)		1	50	µV
Rise time 1	t_{r1}	I_O = 20 µA, R2.2K = 0 to 2.6 V			178		ms
Rise time 2	t_{r2}	I_O = 20 µA, R2.2K = 2.3 to 2.6 V			260		ms
Fall time	t_f	I_O = 0 µA, R2.2K = 2.6 to 2.3 V			2.5		ms

USB SWITCH ELECTRICAL CHARACTERISTICS FOR 2.8 V to 4.4 V SUPPLY

T_A = –40°C to 85°C, typical values are at V_{SUPPLY} = 3.6 V, V_{BUS} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analog Switch							
Analog signal range	V_{USBIO}			0		3.6	V
ON-state resistance	r_{ON}	V_I = 0 V to 3.6 V, I_O = –2 mA,	V_{SUPPLY} = 3.0 V, CP_EN = 1, Switch ON		4.5	10	Ω
ON-state resistance match between channels	Δr_{ON}	V_I = 0.4 V, I_O = –2 mA,	V_{SUPPLY} = 3.0 V, CP_EN = 1, Switch ON		1	1.5	Ω
ON-state resistance flatness	$r_{ON(flat)}$	V_I = 0 V to 3.6 V, I_O = –2 mA, V_{SUPPLY} = 3.0 V	CP_EN = 1, Switch ON		0.5	1	Ω
V_I or V_O OFF leakage current (1)	$I_{IO(OFF)}$	V_I = 0.3 V, V_O = 2.5 V or V_I = 2.5 V, V_O = 0.3 V,	V_{SUPPLY} = 4.4 V, Switch OFF		25	360	nA
V_O ON leakage current (1)	$I_{IO(ON)}$	V_I = OPEN, V_O = 0.3 V or 2.5 V,	V_{SUPPLY} = 4.4 V, CP_EN = 1, Switch ON		10	360	nA
Dynamic							
Turn-ON time	t_{ON}	V_I or V_O = V_{SUPPLY}, R_L = 50 Ω, C_L = 35 pF	CP_EN = 1 From receipt of I^2C ACK bit		1		ms
Turn-OFF time	t_{OFF}	V_I or V_O = V_{SUPPLY}, R_L = 50 Ω, C_L = 35 pF,	CP_EN = 0 From receipt of I^2C ACK bit		1		ms
V_I OFF capacitance (1)	$C_{I(OFF)}$	DC bias = 0 V or 3.6 V f = 10 MHz,	CP_EN = 0, Switch OFF		6.5		pF
V_O OFF capacitance (1)	$C_{O(OFF)}$	DC bias = 0 V or 3.6 V f = 10 MHz,	CP_EN = 0, Switch OFF		3		pF
V_I, V_O ON capacitance (1)	$C_{I(ON)}$, $C_{O(ON)}$	DC bias = 0 V or 3.6 V f = 10 MHz,	CP_EN = 1, Switch ON		9		pF
Bandwidth	BW	R_L = 50 Ω,	CP_EN = 1, Switch ON		830		MHz
OFF Isolation	O_{ISO}	f = 240 MHz, R_L = 50 Ω, C_L = 20 pF,	CP_EN = 0, Switch OFF		–20		dB
Crosstalk	X_{TALK}	f = 240 MHz, R_L = 50 Ω, C_L = 20 pF,	CP_EN = 1, Switch ON		–42		dB

(1) V_I = voltage asserted on DP and DM pins. V_O = voltage asserted on USB_DP and USB_DM pins. I_O = current on the USB_DP or USB_DM pins.

UART SWITCH ELECTRICAL CHARACTERISTICS FOR 2.8 V to 4.4 V SUPPLY

T_A = –40°C to 85°C, typical values are at V_{SUPPLY} = 3.6 V, V_{BUS} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analog Switch							
Analog signal range	V_{UARTIO}			0		V_{SUPPLY}	V
ON-state resistance	r_{ON}	V_I = 0 V to 2.8 V, I_O = –2 mA,	V_{SUPPLY} = 2.8 V, CP_EN = 1, Switch ON		37	61	Ω
ON-state resistance match between channels	Δr_{ON}	V_I = 0.4 V, I_O = –2 mA,	V_{SUPPLY} = 2.8 V, Switch ON		2	3.5	Ω
ON-state resistance flatness	$r_{ON(flat)}$	V_I = 0 V to 2.8 V, I_O = –2 mA, V_{SUPPLY} = 2.8 V	Switch ON		20	27	Ω
V_I or V_O OFF leakage current (1)	$I_{IO(OFF)}$	V_I = 0.3 V, V_O = 3.3 V or V_I = 3.3 V, V_O = 0.3 V,	V_{SUPPLY} = 3.6 V, Switch OFF		100	360	nA
V_O ON leakage current (1)	$I_{IO(ON)}$	V_I = OPEN, V_O = 0.3 V or 3.3 V,	V_{SUPPLY} = 3.6 V, CP_EN = 1, Switch ON		100	360	nA
Dynamic							
Turn-ON time	t_{ON}	V_I or V_O = V_{SUPPLY}, R_L = 50 Ω, C_L = 35 pF	From receipt of I^2C ACK bit		1		ms
Turn-OFF time	t_{OFF}	V_I or V_O = V_{SUPPLY}, R_L = 50 Ω, C_L = 35 pF	From receipt of I^2C ACK bit		1		ms
V_I OFF capacitance (1)	$C_{I(OFF)}$	DC bias = 0 V or V_{SUPPLY}, f = 10 MHz,	Switch OFF		6.5		pF
V_O OFF capacitance (1)	$C_{O(OFF)}$	DC bias = 0 V or V_{SUPPLY}, f = 10 MHz,	Switch OFF		8		pF
V_I, V_O ON capacitance (1)	$C_{I(ON)}$, $C_{O(ON)}$	DC bias = 0 V or V_{SUPPLY}, f = 10 MHz,	Switch ON		22		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON		295		MHz
OFF Isolation	O_{ISO}	f = 250 kHz, R_L = 50 Ω, C_L = 20 pF,	Switch OFF		–100		dB
Crosstalk	X_{TALK}	f = 250 kMHz, R_L = 50 Ω, C_L = 20 pF,	Switch ON		–98		dB

(1) V_I = voltage asserted on DP and DM pins. V_O = voltage asserted on UART_RX and UART_TX pins. I_O = current on the UART_RX and UART_TX pins.

AUDIO SWITCH ELECTRICAL CHARACTERISTICS FOR 2.8 V to 4.4 V SUPPLY

T_A = –40°C to 85°C, typical values are at V_{SUPPLY} = 3.6 V, V_{BUS} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analog Switch							
Analog signal range	$V_{AUDIOIO}$			–1.3		1.3	V
ON-state resistance	r_{ON}	V_I = ±1.3 V, I_O = –20 mA, V_{SUPPLY} = 2.8 V,	AUDIO_L or AUDIO R, DM or DP		3.8	6	Ω
ON-state resistance match between channels	Δr_{ON}	V_I = 1.3 V, I_O = –20 mA, V_{SUPPLY} = 2.8 V,	AUDIO_L or AUDIO R, DM or DP		1	1.3	Ω
ON-state resistance flatness	$r_{ON(flat)}$	V_I = ±1.3 V, I_O = –20 mA, V_{SUPPLY} = 2.8 V,	AUDIO_L or AUDIO R, DM or DP		0.1	0.25	Ω
V_I or V_O OFF leakage current(1)	$I_{IO(OFF)}$	V_I = 0 V, V_O = 1.3 V or V_I = 1.3 V, V_O = 0.3 V,	Switch OFF		25	400	nA
V_O ON leakage current(1)	$I_{IO(ON)}$	V_I = OPEN, V_O = ±1.3 V, V_{SUPPLY} = 4.4 V,	Switch ON		25	400	nA
Dynamic							
Turn-ON time	t_{ON}	V_I or V_O = V_{SUPPLY}, R_L = 50 Ω, C_L = 35 pF	From receipt of I^2C ACK bit		1		ms
Turn-OFF time	t_{OFF}	V_I or V_O = V_{SUPPLY}, R_L = 50 Ω, C_L = 35 pF	From receipt of I^2C ACK bit		1		ms
V_I OFF capacitance (1)	$C_{I(OFF)}$	DC bias = 0 V or 2.6 V, f = 10 MHz,	Switch OFF		4.5		pF
V_O OFF capacitance(1)	$C_{O(OFF)}$	DC bias = 0 V or 2.6 V , f = 10 MHz,	Switch OFF		6.5		pF
V_I, V_O ON capacitance (1)	$C_{I(ON)}$, $C_{O(ON)}$	DC bias = 0 V or 2.6 V, f = 10 MHz,	Switch ON		9		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON		788		MHz
OFF Isolation	O_{ISO}	f = 20 kHz, R_L = 50 Ω,	Switch OFF		–100		dB
Crosstalk	X_{TALK}	f = 20 kHz, R_L = 50 Ω,	Switch ON		–120		dB
Total harmonic distortion	THD	R_L = 16 Ω, C_L = 20 pF,	f = 20 Hz to 20 kHz, 2.6 Vpp		0.087	0.12	%

(1) V_O = voltage asserted on DP and DM pins. V_I = voltage asserted on AUDIO_R and AUDIO_L pins. I_O = current on the DP and DM pins.

MIC SWITCH ELECTRICAL CHARACTERISTICS FOR 2.8 V to 4.4 V SUPPLY

T_A = –40°C to 85°C, typical values are at V_{SUPPLY} = 3.6 V, V_{BUS} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analog Switch							
Analog signal range	V_{MICIO}			0		2.3	V
ON-state resistance	r_{ON}	V_I = 2.3 V, I_O = –2 mA, V_{SUPPLY} = 2.8 V,	MIC ID		9	12	Ω
ON-state resistance flatness	$r_{ON(flat)}$	V_I = 2.3 V , I_O = –2 mA, V_{SUPPLY} = 2.8 V	MIC ID		0.5	1	Ω
V_I or V_O OFF leakage current (1)	$I_{IO(OFF)}$	V_I = 0.3 V, V_O = 2.3 V or V_I = 2.3 V, V_O = 0.3 V, V_{SUPPLY} = 4.4 V	Switch OFF		5	200	nA
V_O ON leakage current (1)	$I_{IO(ON)}$	V_I = OPEN V_O = 0.3 V or 2.5 V V_{SUPPLY} = 4.4 V	Switch ON		2	200	nA
Dynamic							
Turn-ON time	t_{ON}	V_I or V_O = V_{SUPPLY}, R_L = 50 Ω, C_L = 35 pF	From receipt of I^2C ACK bit		1		ms
Turn-OFF time	t_{OFF}	V_I or V_O = V_{SUPPLY}, R_L = 50 Ω, C_L = 35 pF	From receipt of I^2C ACK bit		1		ms
V_I OFF capacitance (1)	$C_{I(OFF)}$	DC bias = 0 V or 3.6 V, f = 10 MHz,	Switch OFF		6		pF
V_O OFF capacitance (1)	$C_{O(OFF)}$	DC bias = 0 V or 3.6 V , f = 10 MHz,	Switch OFF		6		pF
V_I, V_O ON capacitance (1)	$C_{I(ON)}$, $C_{O(ON)}$	DC bias = 0 V or 3.6 V, f = 10 MHz,	Switch ON		12		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON		573		MHz
OFF Isolation	O_{ISO}	f = 20 kHz, R_L = 50 Ω,	Switch OFF		–37		dB
Crosstalk	X_{TALK}	f = 20 kHz to audio input, R_L = 50 Ω,	Switch ON		–125		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 20 pF,	f = 20 Hz to 20 kHz, 2.6 Vpp		0.07	0.075	%

(1) V_I = voltage asserted on the ID pin. V_O = voltage asserted on MIC pin. I_O = current on the MIC pin.

DIGITAL SIGNALS

T_A = –40°C to 85°C (unless otherwise noted), typical values are at V_{SUPPLY} = 3.6 V, V_{BUS} = 5 V, T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
DSS					
High-level input logic	V_{IH}		V_{SUPPLY} × 0.7	V_{SUPPLY}	V
Low-level input logic	V_{IL}		0	V_{SUPPLY} × 0.3	V
Input leakage current	I_{INLEAK}	V_I = 0 V to V_{SUPPLY}	–1	1	µA
SCL, SDA					
High-level input logic	V_{IH}		1.4		V
Low-level input logic	V_{IL}			0.4	V
Input leakage current	I_{INLEAK}	V_I = 0 V to V_{SUPPLY}	–1	1	µA
$\overline{INT}$, ISET					
Open-drain low	V_{ODOL}	I_{ODL} = 4 mA		0.4	V

APPLICATION INFORMATION

Default Switch Position

The default switch state (DSS) pin determines if the USB switches or UART switches are selected at startup. An internal pulldown resistor is present on the DSS pin, which selects the USB switches as the default at start-up. If the user wants to default to the UART switches at startup, the DSS pin must be pulled high to V_{SUPPLY}. If the user wants to disable the switches, this must be done using an I^2C write to the SW_Control register after initialization is complete.

The default configuration with V_{BAT} power disables the switches. If the user wants to use the switches, this must be done using an I^2C write to the SW_Control register after initialization is complete.

V_{BUS} PRESENT ON POWER UP	DSS	SWITCH STATES
Yes	OPEN / PD	USB
	PU	UART
No	x	Disable

ID Impedance Detection

The TSU5511 features impedance detection for identification of various accessories that are attached to the microUSB port. Each accessory is identified by a unique resistor value on the ID pin to ground. During ID detection, the device auto-calibrates an internal current source, using an external 2.21K ±1% resistor. The current source is then applied to the ID pin while an internal voltage reference is incremented until it matches the ID pin voltage. This produces a 4-bit ADC value corresponding to the ID resistance found.

ID Resistor	Tolerance	ID No.	ADC Value
0 Ω	1%	0	0000
24 kΩ	1%	1	0001
56 kΩ	1% or 20%	2	0010
100 kΩ	1%	3	0011
130 kΩ	1%	4	0100
180 kΩ	1%	5	0101
240 kΩ	1%	6	0110
330 kΩ	1%	7	0111
430 kΩ	1%	8	1000
620 kΩ	1%	9	1001
910 kΩ	1%	10	1010
Open	N/A	11	1011

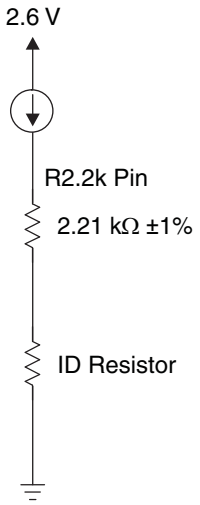


Figure 1. Figure 1. Impedance Detection Circuitry

Supply Detection

The TSU5511 can be powered by either V_{SUPPLY} or V_{BUS}. The TSU5511 will select V_{BUS} as the power source when present and otherwise will select V_{SUPPLY} as the power source when V_{SUPPLY} is present and V_{BUS} is not.

Supply Selection and Shutdown Sequence

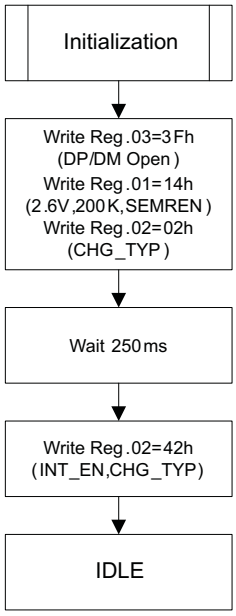
	V_{SUPPLY}	HANDSET STATUS	MUIC STATUS	POWER SUPPLY
NORMAL CASE	Yes	ON	Active	V_{SUPPLY}
	Yes	OFF (S/W off)	Shutdown	
SUDDEN POWER LOSS	Yes	ON	Active	V_{SUPPLY}
	No	OFF	Shutdown	
NO BATTERY	No	OFF	Shutdown	
	No	ON (V_{BUS})	Active	V_{BUS}
USB CHARGING	Yes (charging)	ON (V_{BUS})	Active	V_{BUS}

I²C Controlled Internal Comparator Operation

Internal Comparator Logic Table

I²C CONTROL REGISTER BIT			COMPARATORS			
USB_DET_DIS	ADC_EN	SEMREN	V_{BUS}	SE	MR	LDO
0	0	0	ON	OFF	OFF	OFF
0	0	1	ON	ON	ON	ON
0	1	0	ON	OFF	ON	ON
0	1	1	ON	ON	ON	ON
1	0	0	OFF	OFF	OFF	OFF
1	0	1	ON	ON	ON	ON
1	1	0	ON	OFF	ON	ON
1	1	1	ON	ON	ON	ON

Software Flowchart



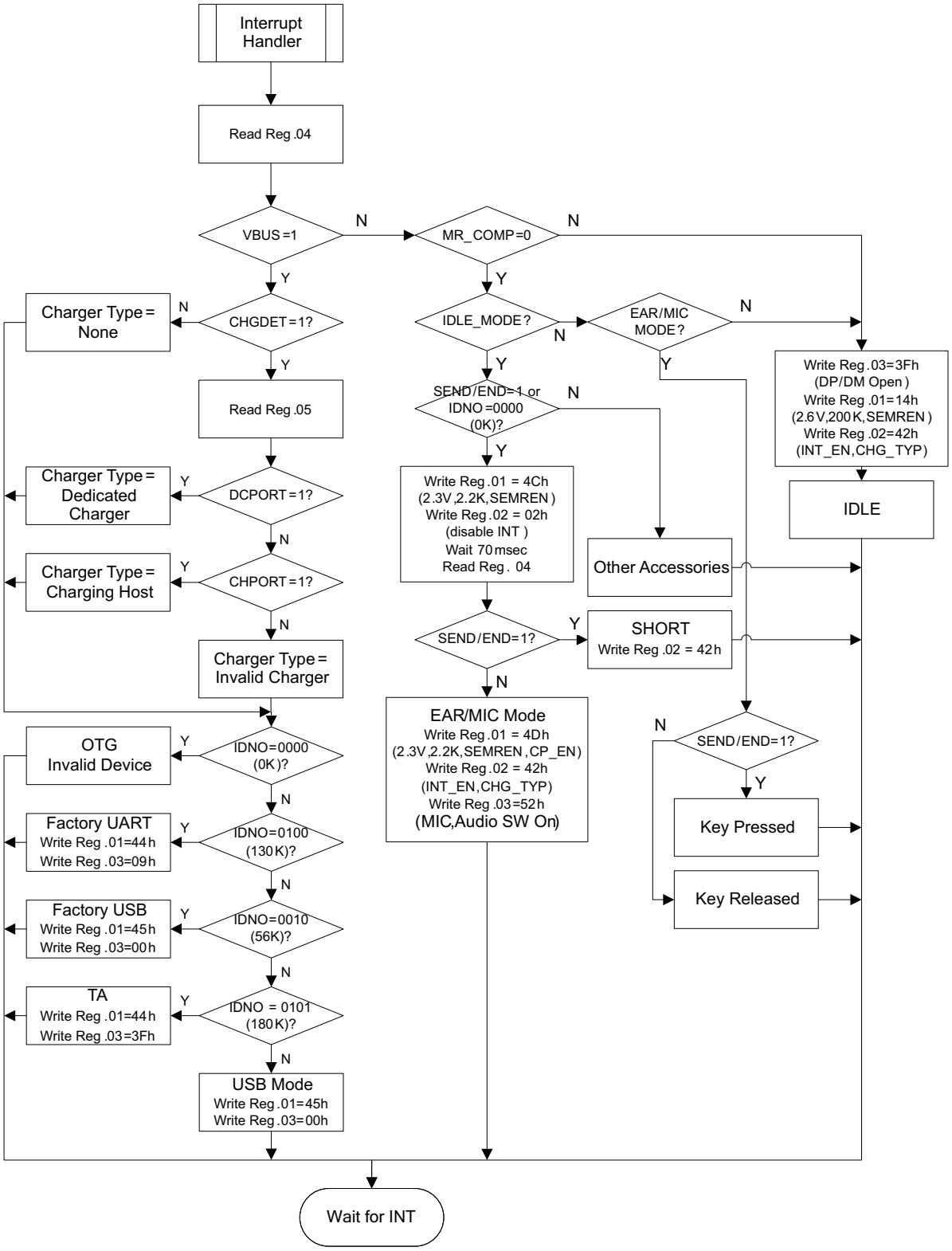
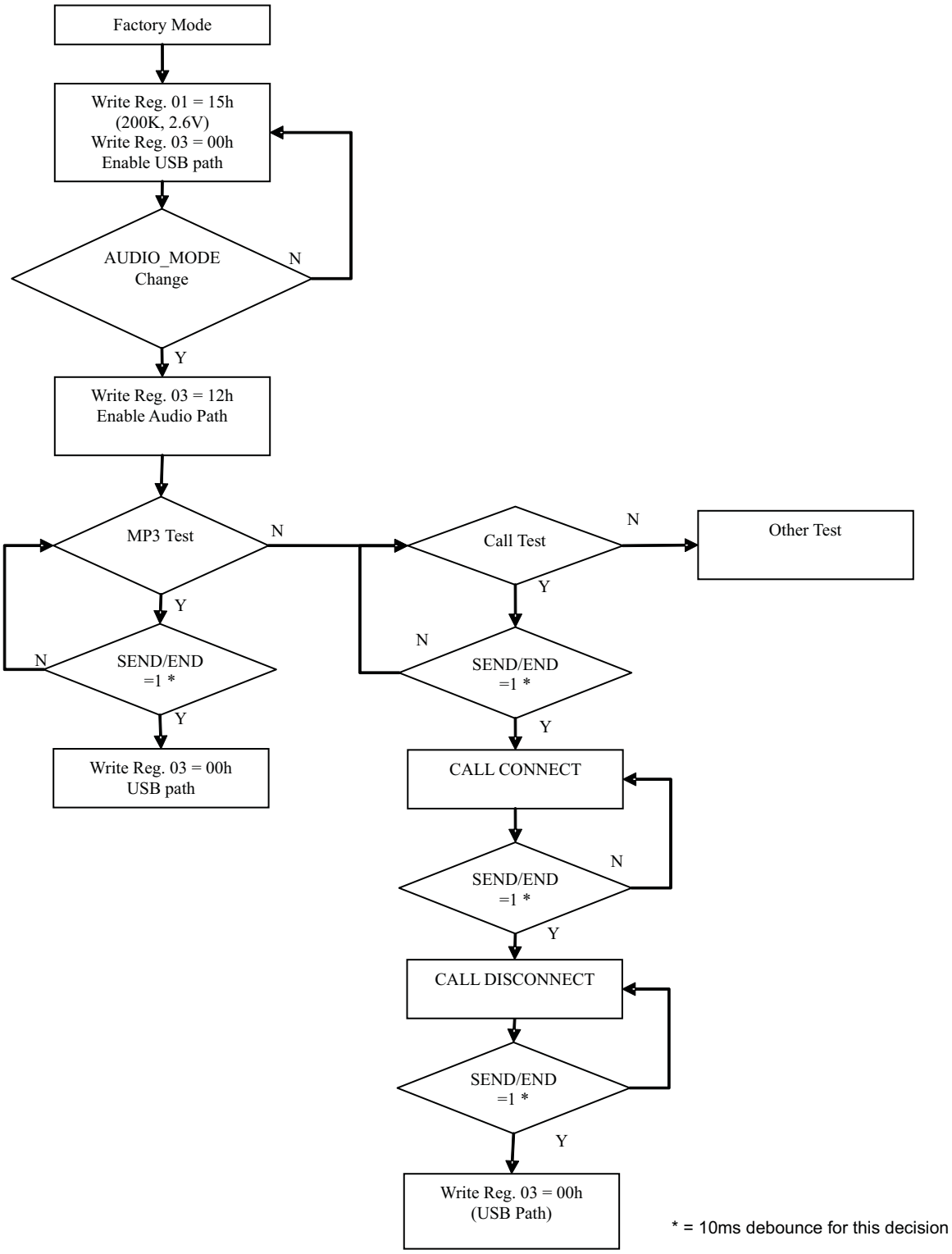


Figure 2. FACTORY MODE FLOWCHART



I²C Register Map

ADDRESS (xxh)	NAME	TYPE	RESET VALUE	b7	b6	b5	b4	b3	b2	b1	b0
0	Device ID	R	TBD	VENDOR ID BITS (TI=0001)				REVISION BITS			
1	Control 1	R/W	X0000000	RFU	ID_2P2	ID_620	ID_200	VLDO	SEMREN	ADC_EN	CP_EN
2	Control 2	R/W	0000XX01	INTPOL	INT_EN	MIC_LP	CP_AUD	RFU	RFU	CHG_TYP	USB_DET_DIS
3	SW Control	R/W	See (1)	RFU	MIC_ON	DP[2:0]		DM[2:0]			
4	INT_Status	R	00000000 (1)	CHGDET	MR_COMP	SEND/END	VBUS	IDNO[3: 0]			
5	Status	R	00XXXXXX	DCPORT	CHPORT	RFU	RFU	RFU	RFU	RFU	RFU

(1) Refer INT_Status

Slave Address

NAME	SIZE (BITS)	DESCRIPTION							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave address	8	1	0	0	0	1	0	0	R/W

Register Descriptions

Device ID

Address: 00h
Reset Value: 14h
Type: Read

NAME	SIZE (BITS)	DESCRIPTION
Device ID	8	A unique number for chip version 00010100 bits 0–3 = chip revision, bits 4–7 = Vendor ID (TI = 1h)

Control 1

Address: 01H
Reset Value: x0000000
Type: Read/Write

NAME	SIZE (BITS)	DESCRIPTION
ID_2P2	1	0: 2.21 kΩ switch open 1: Connect LDO to ID through 2.21 kΩ external resistor
ID_620	1	0: 620 Ω switch open 1: Connect LDO to ID through 620 Ω internal resistor (used for video)
ID_200	1	0: 200 kΩ switch open 1: Connect LDO to ID through 200 kΩ internal resistor
VLDO	1	0: LDO voltage = 2.6 V (if manual switching mode) 1: LDO voltage = 2.3 V (if manual switching mode)
SEMREN	1	0: Disable send/end and MIC removal comparators and LDO 1: Enable send/end and MIC removal comparators and LDO

NAME	SIZE (BITS)	DESCRIPTION
ADC_EN	1	0: ADC and LDO disabled 1: ADC and LDO enabled
CP_EN	1	0: charge pump disabled 1: charge pump enabled

Control 2

Address: 02H

ADDRESS (xxh)	NAME	TYPE	b7	b6	b5	b4	b3	b2	b1	b0
2	Control 2	R/W	INTPOL	INT_EN	MIC_LP	CP_AUD	RFU	RFU	CHG_TYP	USB_DET_DIS
Reset Value			0	0	0	0	X	X	0	1

NAME	SIZE (BITS)	DESCRIPTION
INT_POL	1	0: Interrupt polarity = active low 1: interrupt polarity = active high
INT_EN	1	0: All interrupts disabled (masked) 1: All interrupts enabled
MIC_LP	1	0: Low power mode - MIC power pulsing disabled 1: Low power mode - MIC power pulsing enabled
CP_AUD	1	0: Click/pop resistors on AUDIO_L and AUDIO_R disabled 1: Click/pop resistors on AUDIO_L and AUDIO_R enabled
CHG_TYP	1	0: Charger type detection disabled 1: Charger type detection enabled
USB_DET_DIS	1	0: USB detection enabled 1: USB detection disabled

SW_Control

Address: 03H

ADDRESS (xxh)	NAME	TYPE	b7	b6	b5	b4	b3	b2	b1	b0
03	SW Control	R/W	RFU	MIC_ON	DP[2:0]			DM[2:0]		
Reset Value			X	0	See (1)			See (1)		

(1) The reset value depends on V_{BUS} status at power up. If V_{BUS} presents, the default value depends on DSS pin state (refer to Default Switch Position section). If V_{BUS} does not present, the default value is 111b (DM/DP switch is open).

NAME	SIZE (BITS)	DESCRIPTION
MIC_ON	1	0: MIC switching path open 1: MIC switching path connected to ID line
DP	3	000: DP connected to USB_DP 001: DP connected to UART_TX 010: DP connected to AUDIO_R 011: Future Use (right Audio for Video)

NAME	SIZE (BITS)	DESCRIPTION
DM	3	000: DM connected to USB_DM 001: DM connected to UART_RX 010: DM connected to AUDIO_L 011: Future Use (left Audio for Video) 100–111: DM switching path open

INT_Status

Address: 04H

ADDRESS (xxh)	NAME	TYPE	b7	b6	b5	b4	b3	b2	b1	b0
04	INT_Status	R	CHGDET	MR_COMP	SEND/END	VBUS	IDNO[3:0]			
Reset Value			0	0	0	0	See (1)			

(1) ADC value of the ID pin

NAME	SIZE (BITS)	DESCRIPTION
CHGDET	1	0: High-current charger not detected 1: High-current charger detected
MR_COMP	1	0: MIC removal comparator low 1: MIC removal comparator high
SEND/END	1	0: ID line not grounded 1: ID line grounded (send/end button pressed)
V_{BUS}	1	0: No power detected on V_{BUS} 1: Power detected on V_{BUS}
IDNO	1	0000: ADC determined ID impedance = 0 Ω (grounded) 0001: ADC determined ID impedance = 24 kΩ 0010: ADC determined ID impedance = 56 kΩ 0011: ADC determined ID impedance = 100 kΩ 0100: ADC determined ID impedance = 130 kΩ 0101: ADC determined ID impedance = 180 kΩ 0110: ADC determined ID impedance = 240 kΩ 0111: ADC determined ID impedance = 330 kΩ 1000: ADC determined ID impedance = 430 kΩ 1001: ADC determined ID impedance = 620 kΩ 1010: ADC determined ID impedance = 910 kΩ 1011: ADC determined ID impedance = open

Status

Address: 05H

ADDRESS (xxh)	NAME	TYPE	b7	b6	b5	b4	b3	b2	b1	b0
5	Status	R	DCPORT	CHPORT	RFU	RFU	RFU	RFU	RFU	RFU
Reset Value			0	0	X	X	X	X	X	X

NAME	SIZE (BITS)	DESCRIPTION
DCPORT	1	0: Dedicated charger not detected 1: Dedicated charger detected
CHPORT	1	0: Charging host port not detected 1: Charging host port detected

Power Consumption

Operating Modes Summary (with estimated power consumption)

	BAND GAP	UVLO	I^2C	DETECTION PLUG	Z DETECTION	CHARGE PUMP	CHARGE PUMP (LOW CURRENT)	TOTAL I_{CC} (µA)
Audio	ON	ON	ON	ON	ON	ON	OFF	59
Audio (no active signal)	ON	ON	ON	ON	ON	OFF	ON	14
UART	ON	ON	ON	ON	ON	OFF	OFF	9
USB	ON	ON	ON	ON	ON	ON	OFF	59
Travel Adapter	ON	ON	ON	ON	OFF	OFF	OFF	8
IDLE	ON	ON	ON	ON	OFF	OFF	OFF	8
Sleep	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
I_{CC} (µA)	3	2	1	2	1	50	5	

PARAMETER MEASUREMENT INFORMATION

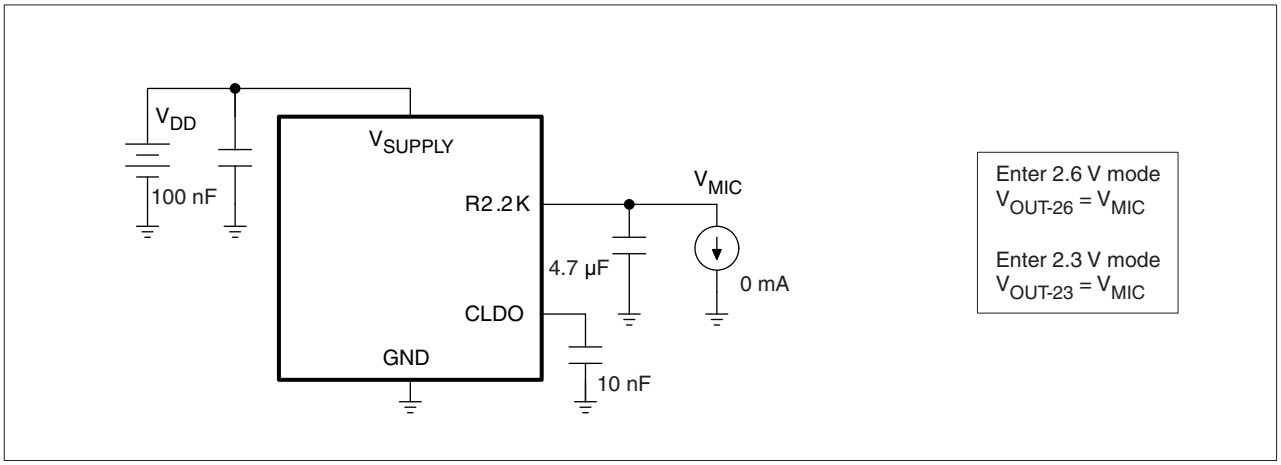


Figure 3. LDO Output Voltage

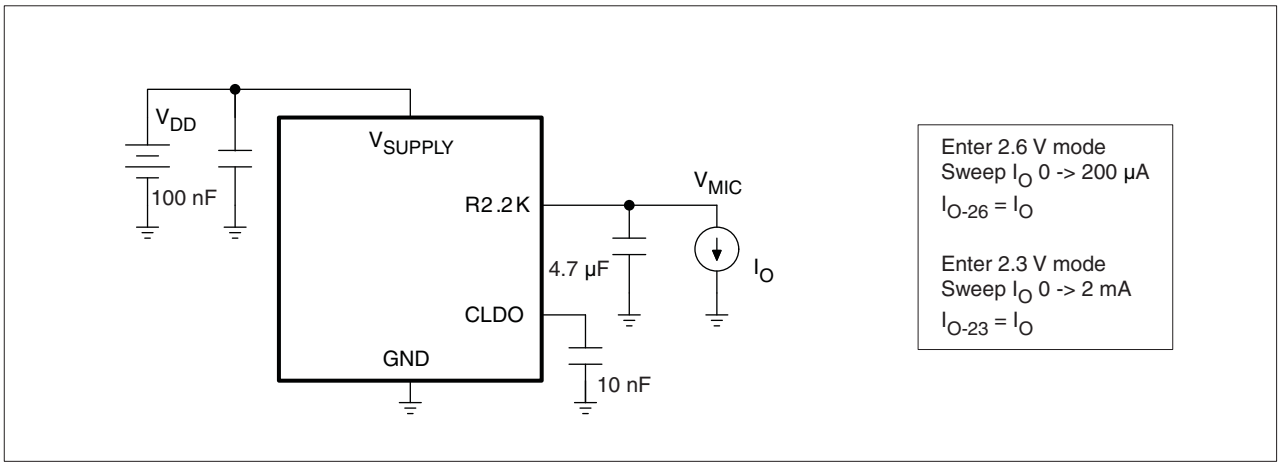


Figure 4. Max Output Current

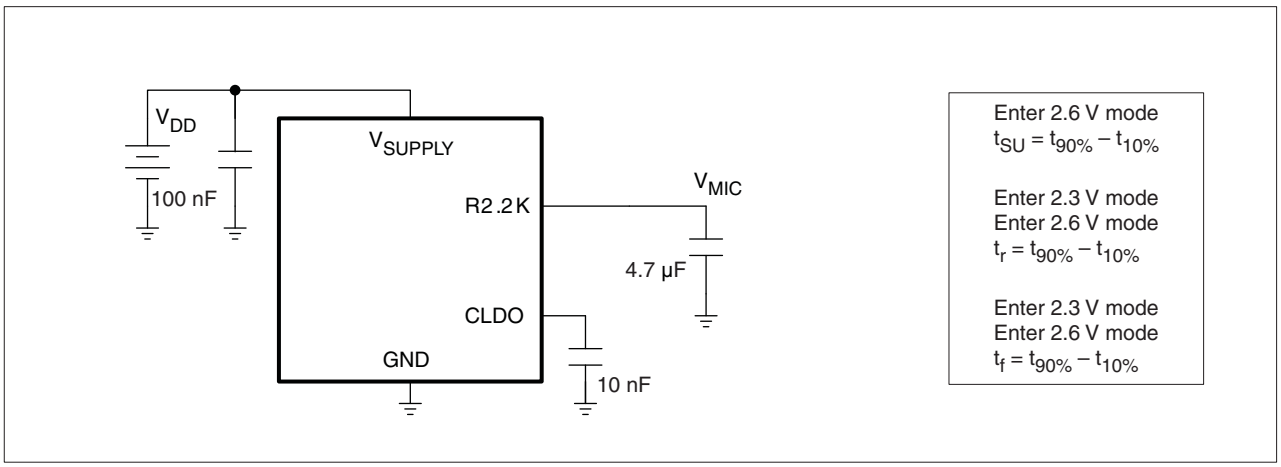


Figure 5. LDO Rise/Fall Time

A. I_O can be set with a resistor.

PARAMETER MEASUREMENT INFORMATION (continued)

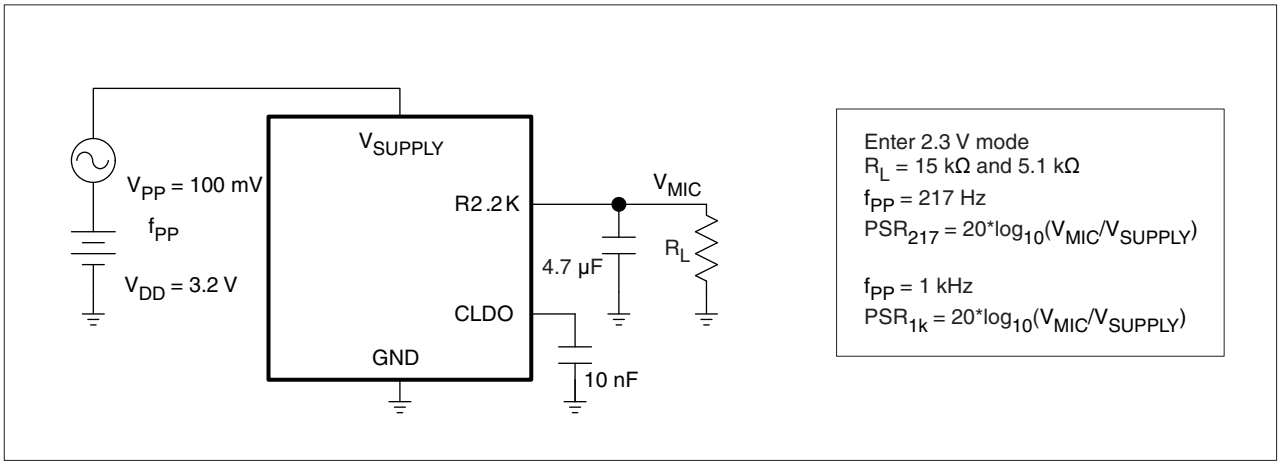


Figure 6. Power Supply Rejection

A. V_{MIC} should be V2.2K; add 200 pF on V_{SUPPLY} in LDO output noise.

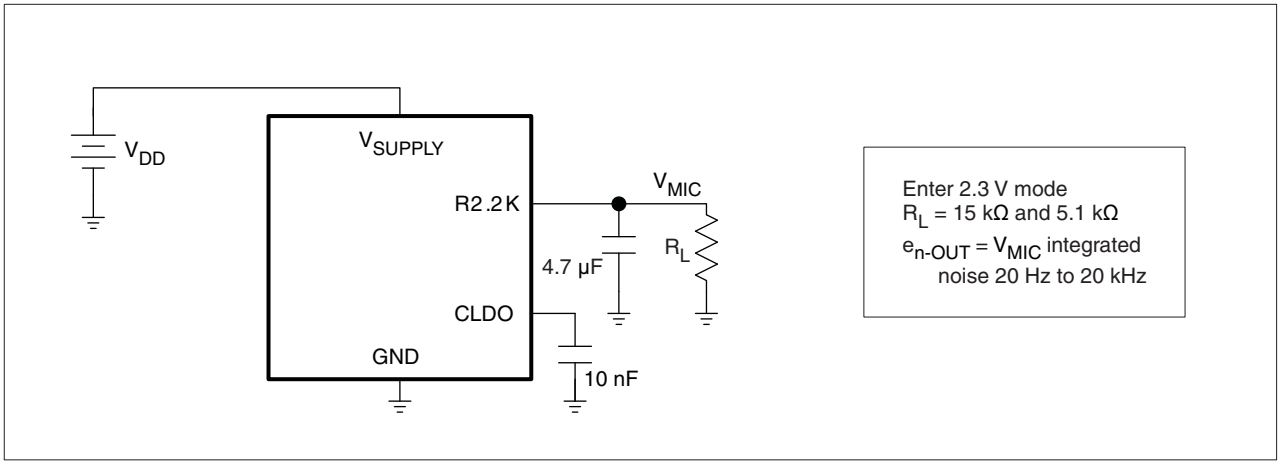


Figure 7. Integrated Output Noise

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSU5511YZPR	ACTIVE	DSBGA	YZP	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A6N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

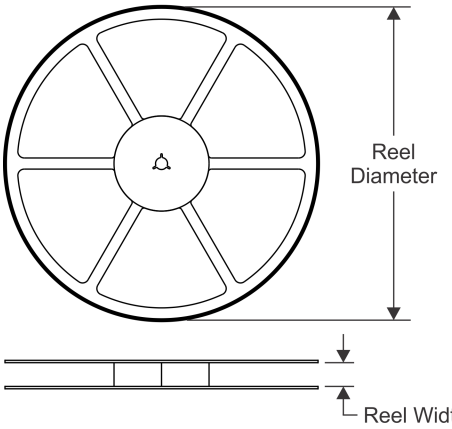
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

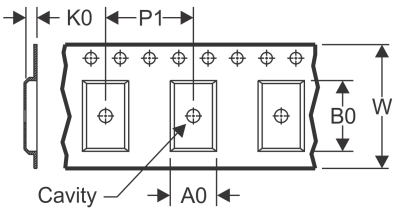
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

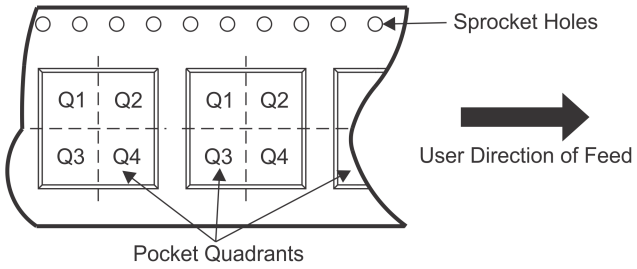


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

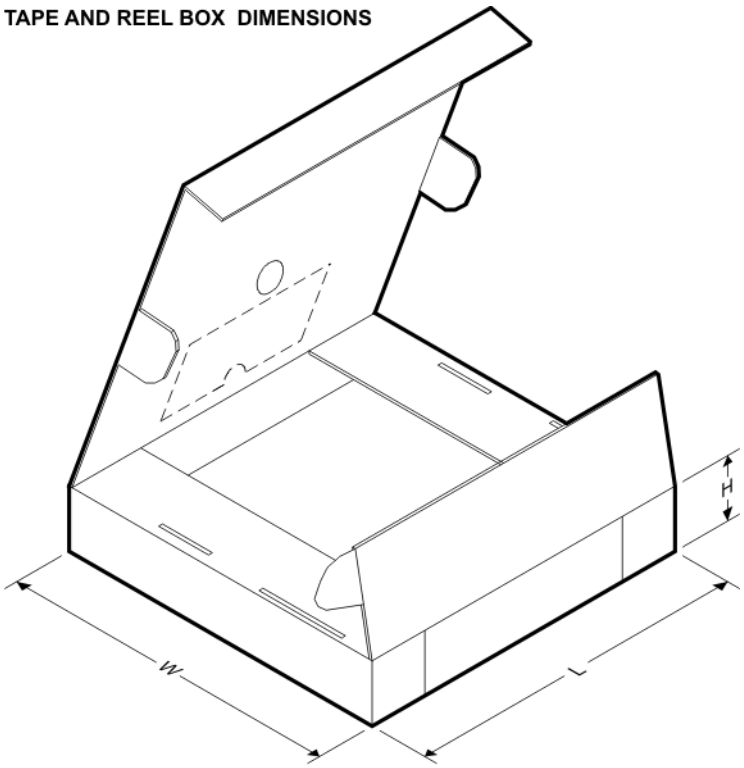
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSU5511YZPR	DSBGA	YZP	20	3000	178.0	9.2	2.02	2.52	0.63	4.0	8.0	Q1

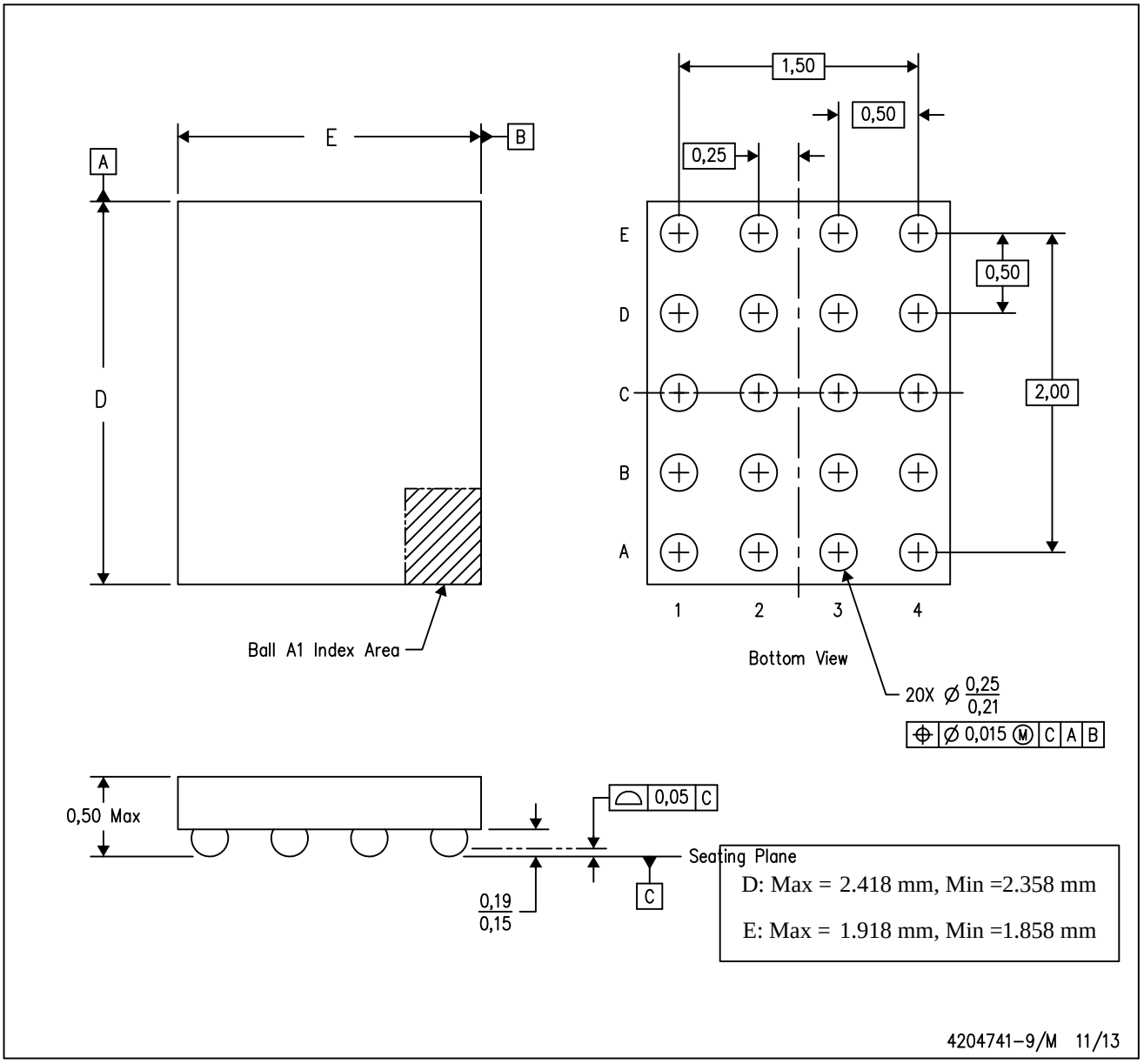
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSU5511YZPR	DSBGA	YZP	20	3000	220.0	220.0	35.0

YZP (R–XBGA–N20) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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