

Low Harmonic Distortion 32-Channel SPST High Voltage Analog Switch with Bleed Resistors

Features

- ▶ 32-channel high voltage analog switch
- ▶ Integrated bleed resistors on the outputs
- ▶ 3.3V or 5.0V CMOS input logic level
- ▶ 30MHz data shift clock frequency
- ▶ HVCMOS technology for high performance
- ▶ Very low quiescent power dissipation (10 μ A)
- ▶ Low parasitic capacitance
- ▶ DC to 50MHz analog signal frequency
- ▶ -60dB typical off isolation at 5.0MHz
- ▶ CMOS logic circuitry for low power
- ▶ Excellent noise immunity
- ▶ Cascadable serial data register with latches
- ▶ Flexible operating supply voltages

Applications

- ▶ Medical ultrasound imaging
- ▶ NDT metal flaw detection
- ▶ Piezoelectric transducer drivers
- ▶ Inkjet printer heads
- ▶ Optical MEMS modules

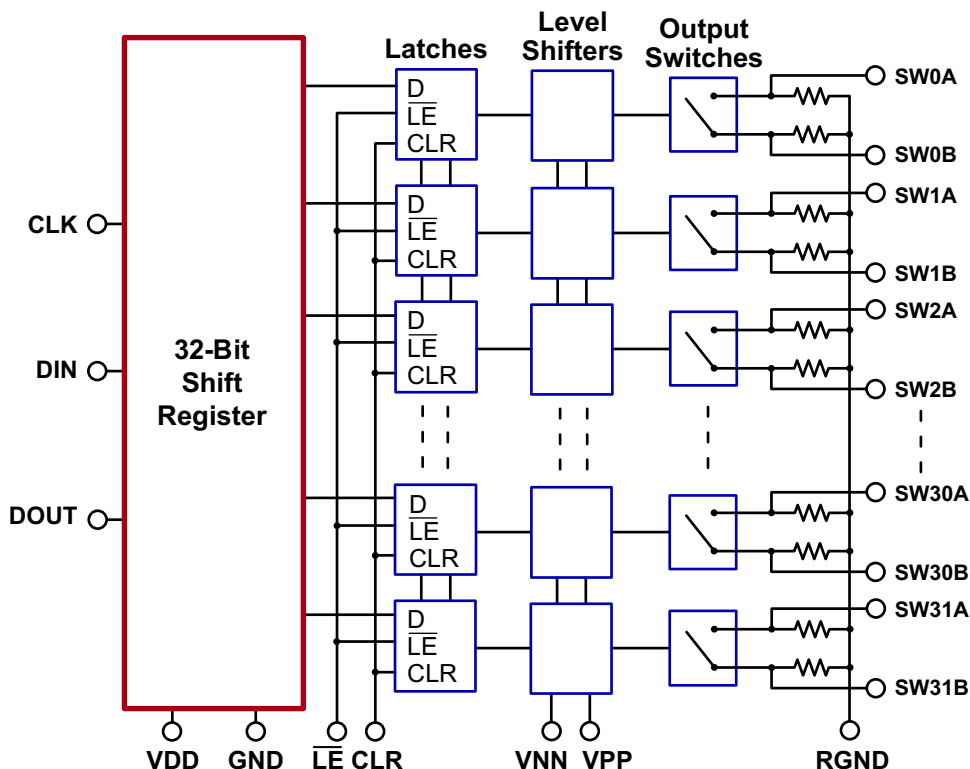
General Description

The HV2802 is a low charge injection, 32-channel, high voltage analog switch intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as medical ultrasound imaging, driving piezoelectric transducers, and printers. The bleed resistors eliminate voltage built up on capacitive loads such as piezoelectric transducers.

Input data are shifted into a 32-bit shift registers that can then be retained in a 32-bit latch. To reduce any possible clock feed through noise, the latch enable bar should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN} : +40V/-160V, +100V/-100V, and +160V/-40V.

Block Diagram

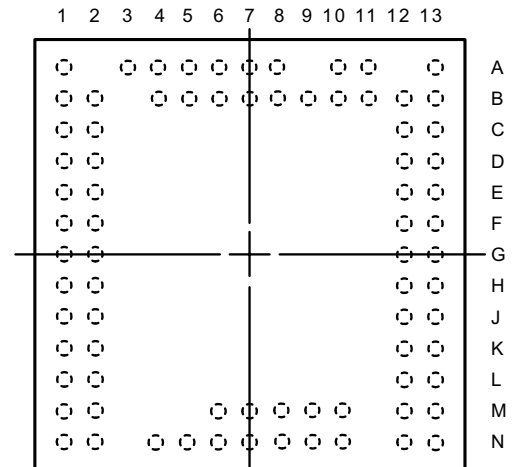


Ordering Information

Part Number	Package Option	Packing
HV2902LB-G	78-Ball LFGA	260/Tray

-G denotes a lead (Pb)-free / RoHS compliant package

Pin Configuration

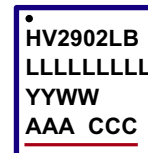


78-Ball LFGA

Top View

(Balls on the bottom of the package.)

Product Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
— = "Green" Packaging

Package may or may not include the following marks: Si or

78-Ball LFGA

Absolute Maximum Ratings

Parameter	Value
V_{DD} logic supply	-0.5V to +6.5V
V_{PP} - V_{NN} differential supply	220V
V_{PP} positive supply	-0.5V to V_{NN} +200V
V_{NN} negative supply	+0.5V to -200V
Logic input voltage	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to 150°C
Power dissipation	1.5W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Typical Thermal Resistance

Package	θ_{ja}
78-Ball LFGA	36°C/W

Recommended Operating Conditions

Sym	Parameter	Value
V_{DD}	Logic power supply voltage	3.0V to 5.5V
V_{PP}	Positive high voltage supply	+40V to V_{NN} +200V
V_{NN}	Negative high voltage supply	-40V to -160V
V_{IH}	High level input voltage	$0.9V_{DD}$ to V_{DD}
V_{IL}	Low level input voltage	0V to $0.1V_{DD}$
V_{SIG}	Analog signal voltage peak-to-peak	V_{NN} +10V to V_{PP} -10V
T_A	Operating free air temperature	0°C to 70°C

Notes:

- Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
- V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transition.
- Rise and fall times of power supplies V_{DD} , V_{PP} and V_{NN} should not be less than 1.0msec.

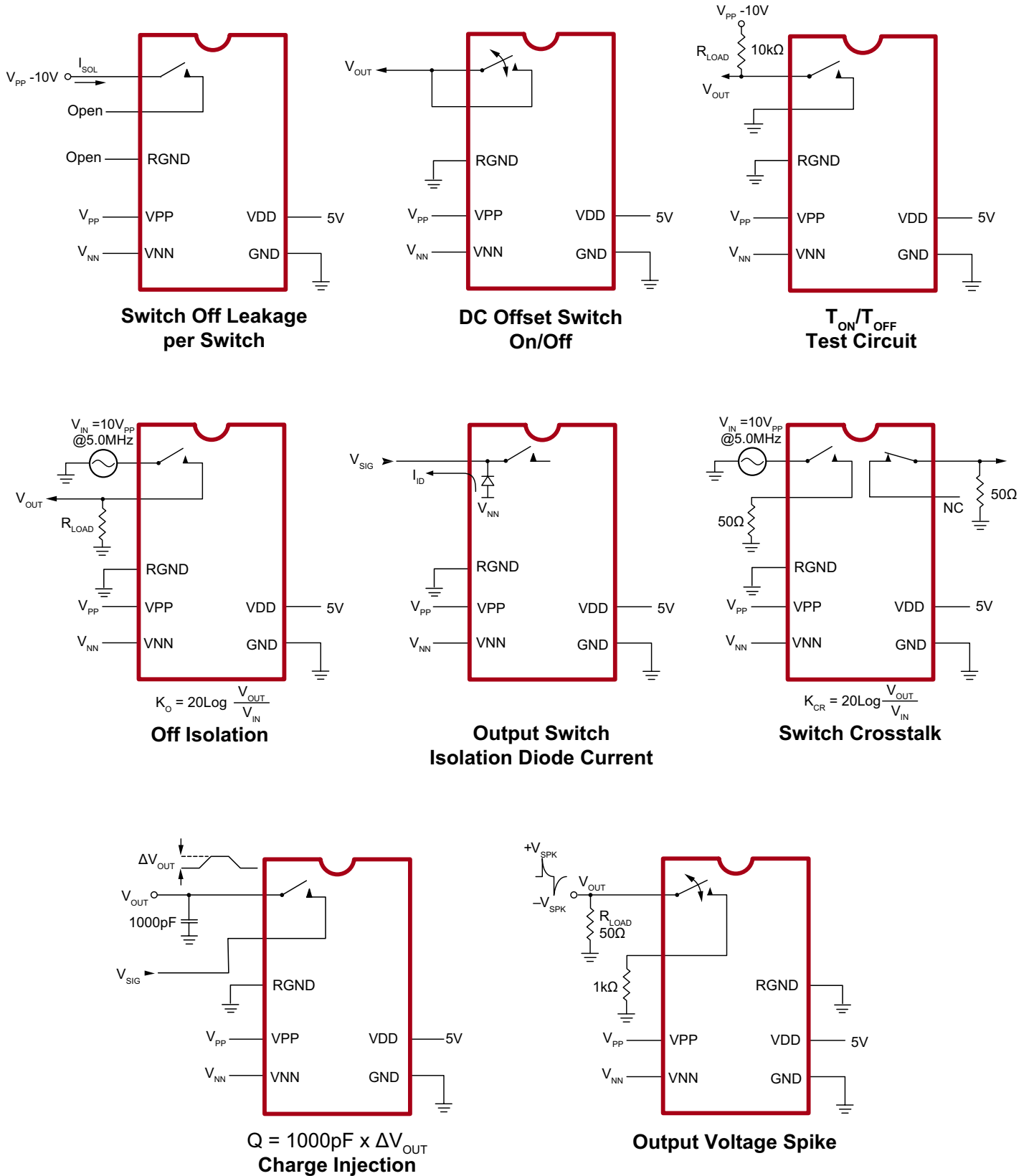
DC Electrical Characteristics (Over recommended operating conditions unless otherwise specified)

Sym	Parameter	0°C		+25°C			+70°C		Unit	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R _{ONS}	Small signal switch ON-resistance	-	30	-	26	38	-	48	Ω	I _{SIG} = 5.0mA	V _{PP} = +40V, V _{NN} = -160V
		-	25	-	22	27	-	32		I _{SIG} = 200mA	V _{NN} = -100V
		-	25	-	22	27	-	30		I _{SIG} = 5.0mA	V _{PP} = +100V, V _{NN} = -100V
		-	18	-	18	24	-	27		I _{SIG} = 200mA	V _{NN} = -100V
		-	23	-	20	25	-	30		I _{SIG} = 5.0mA	V _{PP} = +160V, V _{NN} = -40V
		-	22	-	16	25	-	27		I _{SIG} = 200mA	V _{NN} = -40V
ΔR _{ONS}	Small signal switch ON-resistance matching	-	20	-	5.0	20	-	20	%	I _{SIG} = 5.0mA, V _{PP} = +100V, V _{NN} = -100V	
R _{ONL}	Large signal switch ON-resistance	-	-	-	15	-	-	-	Ω	V _{SIG} = V _{PP} -10V, I _{SIG} = 1A	
R _{INT}	Value of output bleed resistor	-	-	20	35	50	-	-	kΩ	Output switch to R _{GND} I _{RINT} = 0.5mA	
I _{SOL}	Switch off leakage per switch	-	5.0	-	1.0	10	-	15	μA	V _{SIG} = V _{PP} -10V, V _{NN} +10V	
V _{OS}	DC offset switch off	-	300	-	100	300	-	300	mV	No load	
	DC offset switch on	-	500	-	100	500	-	500			
I _{PPQ}	Quiescent V _{PP} supply current	-	-	-	10	50	-	-	μA	All switches off	
I _{NNQ}	Quiescent V _{NN} supply current	-	-	-	-10	-50	-	-			
I _{PPQ}	Quiescent V _{PP} supply current	-	-	-	10	50	-	-	μA	All switches on, I _{SW} = 5.0mA	
I _{NNQ}	Quiescent V _{NN} supply current	-	-	-	-10	-50	-	-			
I _{SW}	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V _{SIG} duty cycle < 0.1%	
f _{SW}	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I _{PP}	Average V _{PP} supply current	-	16	-	-	20	-	22	mA	V _{PP} = +40V, V _{NN} = -160V	All output switches are turning on and off at 50kHz with no load
		-	14	-	-	14	-	14		V _{PP} = +100V, V _{NN} = -100V	
		-	14	-	-	14	-	14		V _{PP} = +160V, V _{NN} = -40V	
I _{NN}	Average V _{NN} supply current	-	16	-	-	20	-	22	mA	V _{PP} = +40V, V _{NN} = -160V	All output switches are turning on and off at 50kHz with no load
		-	14	-	-	14	-	14		V _{PP} = +100V, V _{NN} = -100V	
		-	14	-	-	14	-	14		V _{PP} = +160V, V _{NN} = -40V	
I _{DD}	Average V _{DD} supply current	-	8.0	-	-	8.0	-	8.0	mA	f _{CLK} = 5.0MHz, V _{DD} = 5.0V	
I _{DDQ}	Quiescent V _{DD} supply current	-	10	-	-	10	-	10	μA	All logic inputs are static	
I _{SOR}	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V _{OUT} = V _{DD} -0.7V	
I _{SINK}	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V _{OUT} = 0.7V	
C _{IN}	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

AC Electrical Characteristics (Over recommended operating conditions unless otherwise specified)

Sym	Parameter	0°C		+25°C			+70°C		Unit	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
t_{SD}	Set up time before $\overline{LE}$ rises	25	-	25	-	-	25	-	ns	---
t_{WLE}	Time width of $\overline{LE}$	56	-	-	56	-	56	-	ns	$V_{DD} = 3.0V$
		12	-	-	12	-	12	-		$V_{DD} = 5.0V$
t_{DO}	Clock delay time to data out	8.0	40	8.0	19	40	8.0	40	ns	$V_{DD} = 3.0V$
		8.0	30	8.0	15	30	8.0	30		$V_{DD} = 5.0V$
t_{WCLR}	Time width of CLR	55	-	55	-	-	55	-	ns	---
t_{SU}	Set up time data to clock	21	-	21	-	-	21	-	ns	$V_{DD} = 3.0V$
		7.0	-	7.0	-	-	7.0	-		$V_{DD} = 5.0V$
t_H	Hold time data from clock	5.0	-	5.0	-	-	5.0	-	ns	$V_{DD} = 3.0V$
		7.0	-	7.0	-	-	7.0	-		$V_{DD} = 5.0V$
f_{CLK}	Clock frequency	-	8	-	-	8	-	8	MHz	$V_{DD} = 3.0V$
		-	20	-	-	20	-	20		$V_{DD} = 5.0V$
t_R, t_F	Clock rise and fall times	-	50	-	-	50	-	50	ns	---
t_{ON}	Turn on time	-	5.0	-	-	5.0	-	5.0	μs	$V_{SIG} = V_{PP} - 10V$, $R_{LOAD} = 10k\Omega$
t_{OFF}	Turn off time	-	5.0	-	-	5.0	-	5.0		
dv/dt	Maximum V_{SIG} slew rate	-	20	-	-	20	-	20	V/ns	$V_{PP} = +40V, V_{NN} = -160V$
		-	20	-	-	20	-	20		$V_{PP} = +100V, V_{NN} = -100V$
		-	20	-	-	20	-	20		$V_{PP} = +160V, V_{NN} = -40V$
K_O	Off isolation	-30	-	-30	-33	-	-30	-	dB	$f = 5.0MHz$, 1.0k Ω /15pF load
		-58	-	-58	-60	-	-58	-		$f = 5.0MHz$, 50 Ω load
K_{CR}	Switch crosstalk	-60	-	-60	-70	-	-60	-	dB	$f = 5.0MHz$, 50 Ω load
I_{ID}	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	Off capacitance SW to GND	5.0	17	5.0	12	17	5.0	17	pF	0V, $f = 1.0MHz$
$C_{SG(ON)}$	On capacitance SW to GND	25	50	25	38	50	25	50		
$+V_{SPK}$	Output voltage spike SWA	-	-	-	-	+150	-	-	mV	$V_{PP} = +40V, V_{NN} = -160V$ $R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	-150	-	-		$V_{PP} = +100V, V_{NN} = -100V$ $R_{LOAD} = 50\Omega$
$+V_{SPK}$		-	-	-	-	+150	-	-		
$-V_{SPK}$		-	-	-	-	-150	-	-		$V_{PP} = +160V, V_{NN} = -40V$ $R_{LOAD} = 50\Omega$
$+V_{SPK}$		-	-	-	-	+150	-	-		
$-V_{SPK}$		-	-	-	-	-150	-	-		
$+V_{SPK}$ $-V_{SPK}$ $+V_{SPK}$ $-V_{SPK}$ $+V_{SPK}$ $-V_{SPK}$	Output voltage spike SWB	-	-	-	-	+150	-	-	mV	$V_{PP} = +40V, V_{NN} = -160V$ $R_{LOAD} = 50\Omega$
		-	-	-	-	-150	-	-		$V_{PP} = +100V, V_{NN} = -100V$ $R_{LOAD} = 50\Omega$
		-	-	-	-	+150	-	-		
		-	-	-	-	-150	-	-		$V_{PP} = +160V, V_{NN} = -40V$ $R_{LOAD} = 50\Omega$
		-	-	-	-	+150	-	-		
		-	-	-	-	-150	-	-		
QC	Charge injection (per switch)	-	-	-	820	-	-	-	pC	$V_{PP} = +40V, V_{NN} = -160V$
		-	-	-	600	-	-	-		$V_{PP} = +100V, V_{NN} = -100V$
		-	-	-	350	-	-	-		$V_{PP} = +160V, V_{NN} = -40V$

Test Circuits



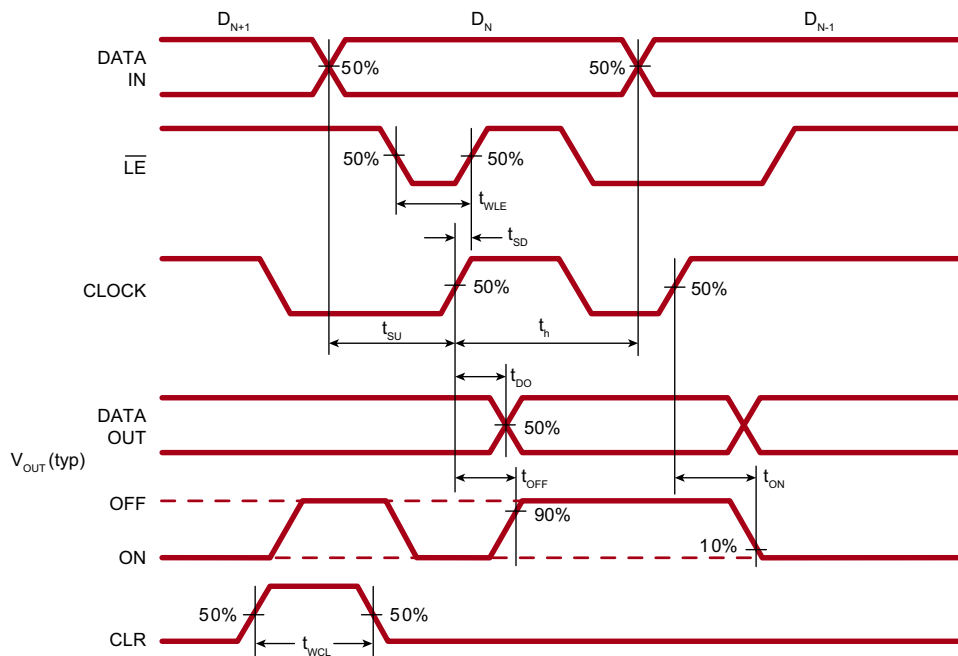
Truth Table

D0	D1	...	D15	D16	...	D31	$\overline{LE}$	CLR	SW0	SW1	...	SW15	SW16	...	SW31
L	-	...	-	-	...	-	L	L	OFF	-	...	-	-	...	-
H	-		-	-		-	L	L	ON	-		-	-		
-	L		-	-		-	L	L	-	OFF		-	-		
-	H		-	-		-	L	L	-	ON		-	-		
-	-		-	-		-	L	L	-	-		-	-		
-	-		-	-		-	L	L	-	-		-	-		
-	-		L	-		-	L	L	-	-		OFF	-		
-	-		H	-		-	L	L	-	-		ON	-		
-	-		-	L		-	L	L	-	-		-	OFF		
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-	-	-	-	-	L	L	-	-	-	-					
-	-	-	-	-	L	L	-	-	-	-					

Notes:

1. The 32 switches operate independently.
2. Serial data is clocked in on the L to H transition of the CLK.
3. All 32 switches go to a state retaining their latched condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift registers data flow through the latch.
4. D_{OUT} is high when data in the register 31 is high.
5. Shift registers clocking has no effect on the switch states if $\overline{LE}$ is high.
6. The CLR clear input overrides all other inputs.

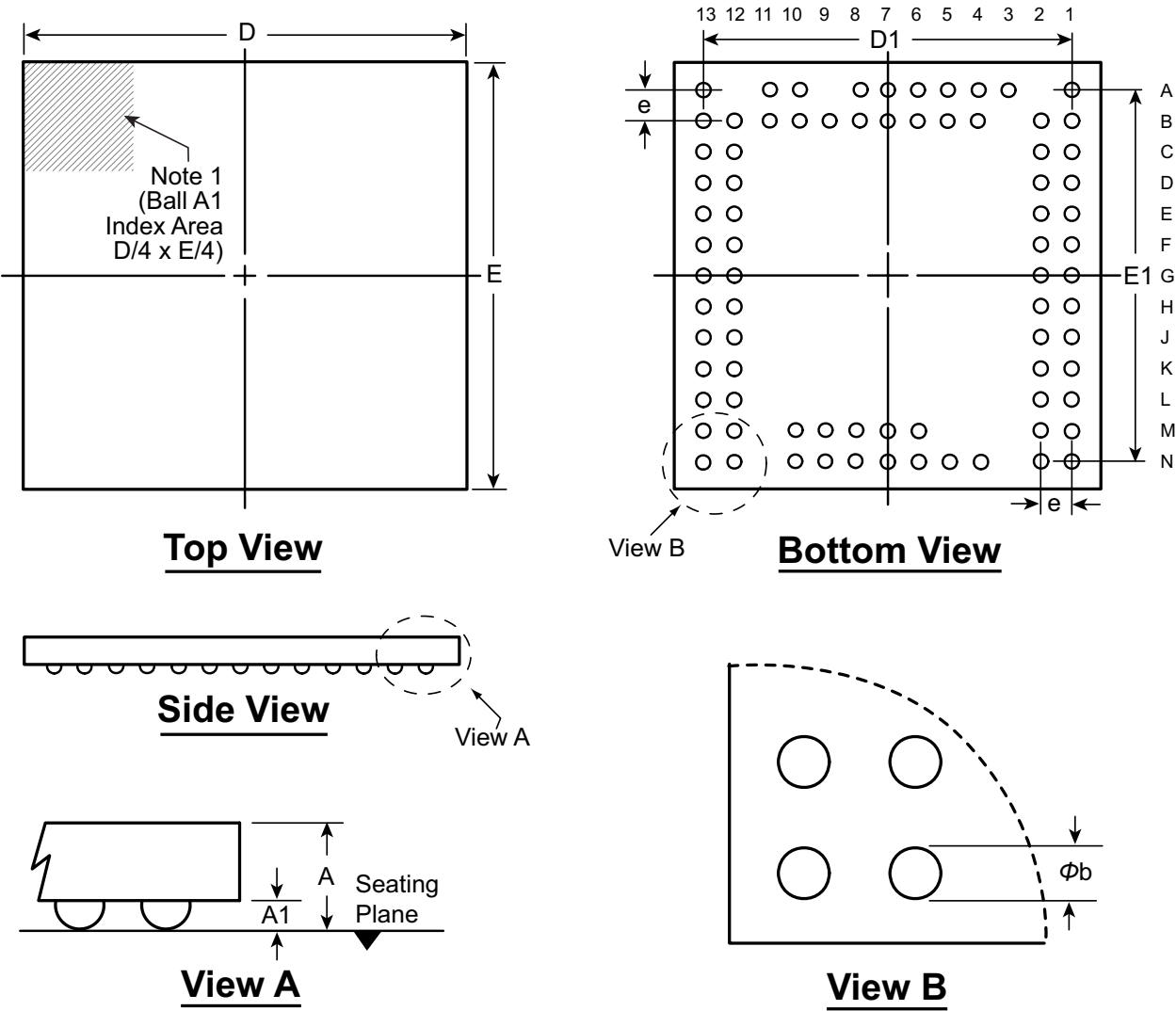
Logic Timing Waveforms



Pin Function

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	SW2B	B10	SW31B	G12	SW23B	-	-
-	-	B11	SW30B	G13	SW24A	M6	SW14A
A3	SW1B	B12	SW28B	H1	SW9A	M7	SW15A
A4	SW0B	B13	SW29A	H2	SW8B	M8	SW16A
A5	DOUT	C1	SW4A	H12	SW22B	M9	SW17A
A6	GND	C2	SW3B	H13	SW23A	M10	RGND
A7	VDD	C12	SW27B	J1	SW10A	-	-
A8	$\overline{\text{LE}}$	C13	SW28A	J2	SW9B	M12	SW18A
-	-	D1	SW5A	J12	SW21B	M13	SW19A
A10	SW31A	D2	SW4B	J13	SW22A	N1	SW13B
A11	SW30A	D12	SW26B	K1	SW11A	N2	VNN
-	-	D13	SW27A	K2	SW10B	-	-
A13	SW29B	E1	SW6A	K12	SW20B	N4	VPP
B1	SW3A	E2	SW5B	K13	SW21A	N5	RGND
B2	SW2A	E12	SW25B	L1	SW12A	N6	SW14B
-	-	E13	SW26A	L2	SW11B	N7	SW15B
B4	SW1A	F1	SW7A	L12	SW19B	N8	SW16B
B5	SW0A	F2	SW6B	L13	SW20A	N9	SW17B
B6	RGND	F12	SW24B	M1	SW13A	N10	VPP
B7	DIN	F13	SW25A	M2	SW12B	-	-
B8	CLK	G1	SW8A	-	-	N12	VNN
B9	CLR	G2	SW7B	-	-	N13	SW18B

78-Ball LFGA Package Outline (LB)
9.00x9.00mm body, 1.00mm height (max), 0.65mm pitch



Notes:
1. Ball A1 identifier must be located in the index area indicated. Ball A1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	b	D	D1	E	E1	e
Dimension (mm)	MIN	0.90	0.10	0.25	8.925	7.80 BSC	8.925	7.80 BSC	0.65 BSC
	NOM	0.95	0.15	0.30	9.000		9.000		
	MAX	1.00	0.20	0.35	9.075		9.075		

Drawings not to scale.
Supertex Doc. #: DSPD-78LFGALB, Version A092612.

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