



## CAN TRANSCEIVER

### FEATURES

- Qualified for Automotive Applications
- Drop-In Improved Replacement for the PCA82C250 and PCA82C251
- Bus-Fault Protection of  $\pm 36$  V
- Meets or Exceeds ISO 11898
- Signaling Rates<sup>(1)</sup> up to 1 Mbps
- High Input Impedance Allows up to 120 SN65HVD251 Nodes on a Bus
- Bus Pins ESD Protection Exceeds 9 kV (HBM)
- Unpowered Node Does Not Disturb the Bus
- Low-Current Standby Mode: 200  $\mu$ A Typical
- Thermal Shutdown Protection
- Glitch-Free Power-Up and Power-Down Bus Protection for Hot Plugging
- DeviceNet™ Vendor ID #806

<sup>(1)</sup> The signaling rate of a line is the number of voltage transitions that are made per second expressed in bps (bits per second).

### APPLICATIONS

- CAN Data Buses
- Industrial Automation
  - DeviceNet Data Buses
  - Smart Distributed Systems (SDS™)
- SAE J1939 Standard Data Bus Interface
- NMEA 2000 Standard Data Bus Interface
- ISO 11783 Standard Data Bus Interface

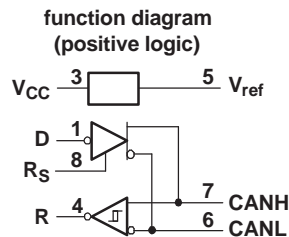
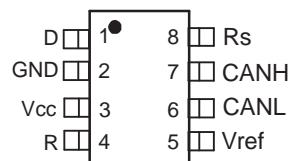
### DESCRIPTION

The SN65HVD251 is intended for use in applications employing the Controller Area Network (CAN) serial communication physical layer in accordance with the ISO 11898 Standard. The SN65HVD251 provides differential transmit capability to the bus and differential receive capability to a CAN controller at speeds up to 1 megabit per second (Mbps).

Designed for operation in harsh environments, the device features crosswire, overvoltage, and loss of ground protection to  $\pm 36$  V. Also featured are overtemperature protection as well as  $-7$ -V to  $12$ -V common-mode range, and tolerance to transients of  $\pm 200$  V. The transceiver interfaces the single-ended CAN controller with the differential CAN bus found in industrial, building automation, and automotive applications.

Rs, pin 8, selects one of three different modes of operation: high-speed, slope control, or low-power mode. The high-speed mode of operation is selected by connecting pin 8 to ground, allowing the transmitter output transistors to switch as fast as possible with no limitation on the rise and fall slope. The rise and fall slope can be adjusted by connecting a resistor to ground at pin 8; the slope is proportional to the pin's output current. Slope control with an external resistor value of 10 k $\Omega$  gives  $\sim 15$  V/ $\mu$ s slew rate; 100 k $\Omega$  gives  $\sim 2$  V/ $\mu$ s slew rate.

If a high logic level is applied to the Rs pin 8, the device enters a low-current standby mode where the driver is switched off and the receiver remains active. The local protocol controller returns the device to the normal mode when it transmits to the bus.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ORDERING INFORMATION<sup>(1)</sup>

| PART NUMBER     | PACKAGE                    | MARKED AS |
|-----------------|----------------------------|-----------|
| SN65HVD251QDRQ1 | 8-pin SOIC (Tape and Reel) | 251Q1     |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

|  |                                     |                 | SN65HVD251                   |
|--|-------------------------------------|-----------------|------------------------------|
| Supply voltage range, $V_{CC}$                     |                                     |                 | –0.3 V to 7 V                |
| Voltage range at any bus terminal                  |                                     | CANH, CANL      | –36 V to 36 V                |
| Transient voltage per ISO 7637, pulse 1, 2, 3a, 3b |                                     | CANH, CANL      | ±200 V                       |
| Input voltage range, $V_I$                         |                                     | D, Rs, R        | –0.3 V to $V_{CC} + 0.5$     |
| Receiver output current, $I_O$                     |                                     |                 | –10 mA to 10 mA              |
| Electrostatic discharge                            | Human-Body Model <sup>(3)</sup>     | CANH, CANL, GND | 9 kV                         |
|  |                                     | All pins        | 6 kV                         |
|  | Charged-Device Model <sup>(4)</sup> | All pins        | 1 kV                         |
|  |                                     | Machine Model   | All pins                     |
| Continuous total power dissipation                 |                                     |                 | See Dissipation Rating Table |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101

### ABSOLUTE MAXIMUM POWER DISSIPATION RATINGS

| PACKAGE  | CIRCUIT BOARD MODEL   | $T_A = 25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR <sup>(1)</sup><br>ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 85^\circ\text{C}$ POWER<br>RATING | $T_A = 125^\circ\text{C}$ POWER<br>RATING |
|----------|-----------------------|--|--|--|---|
| SOIC (D) | Low-K <sup>(2)</sup>  | 576 mW                                   | 4.8 mW/°C  | 288 mW                                   | 96 mW                                     |
|          | High-K <sup>(3)</sup> | 924 mW                                   | 7.7 mW/°C  | 462 mW                                   | 154 mW                                    |

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
- (2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3
- (3) In accordance with the High-K thermal metric definitions of EIA/JESD51-7

**THERMAL CHARACTERISTICS**

| PARAMETER  | TEST CONDITIONS  | VALUE |      |      | UNIT |
|--|--|-------|------|------|------|
|  |  | MIN   | TYP  | MAX  |      |
| $\theta_{JB}$ Junction-to-board thermal resistance |  |       | 78.7 |      | °C/W |
| $\theta_{JC}$ Junction-to-case thermal resistance  |  |       | 44.6 |      | °C/W |
| $P_D$ Device power dissipation                     | $V_{CC} = 5\text{ V}$ , $T_J = 27^\circ\text{C}$ , $R_L = 60\ \Omega$ ,<br>$R_S$ at 0 V, Input to D a 500-kHz<br>50% duty cycle square wave    |       |      | 97.7 | mW   |
|  | $V_{CC} = 5.5\text{ V}$ , $T_J = 130^\circ\text{C}$ , $R_L = 60\ \Omega$ ,<br>$R_S$ at 0 V, Input to D a 500-kHz 50%<br>duty cycle square wave |       |      | 142  | mW   |
| $T_{SD}$ Thermal shutdown junction temperature     |  |       | 165  |      | °C   |

**RECOMMENDED OPERATING CONDITIONS**

over recommended operating conditions (unless otherwise noted)

| PARAMETER   |          | MIN               | NOM | MAX          | UNIT       |
|---|----------|-------------------|-----|--------------|------------|
| Supply voltage, $V_{CC}$  |          | 4.5               |     | 5.5          | V          |
| Voltage at any bus terminal (separately or common mode) $V_I$ or $V_{IC}$ |          | -7 <sup>(1)</sup> |     | 12           | V          |
| High-level input voltage, $V_{IH}$  | D input  | 0.7 $V_{CC}$      |     |              | V          |
| Low-level input voltage, $V_{IL}$   | D input  |                   |     | 0.3 $V_{CC}$ | V          |
| Differential input voltage, $V_{ID}$                                      |          | -6                |     | 6            | V          |
| Input voltage to $R_S$ , $V_{I(R_S)}$                                     |          | 0                 |     | $V_{CC}$     | V          |
| Input voltage at $R_S$ for standby, $V_{I(R_S)}$                          |          | 0.75 $V_{CC}$     |     | $V_{CC}$     | V          |
| $R_S$ wave-shaping resistance   |          | 0                 |     | 100          | k $\Omega$ |
| High-level output current, $I_{OH}$                                       | Driver   | -50               |     |              | mA         |
|   | Receiver | -4                |     |              |            |
| Low-level output current, $I_{OL}$  | Driver   |                   |     | 50           | mA         |
|   | Receiver |                   |     | 4            |            |
| Operating free-air temperature, $T_A$                                     |          | -40               |     | 125          | °C         |
| Junction temperature, $T_j$   |          |                   |     | 145          | °C         |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

## DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER           |   | TEST CONDITIONS   | MIN   | TYP <sup>(1)</sup> | MAX  | UNIT |    |
|---------------------|---|---|---|--------------------|------|------|----|
| V <sub>OD(D)</sub>  | Bus output voltage (Dominant)             | CANH  | Figure 1 and Figure 2, D at 0 V, Rs at 0 V                  |                    |      | V    |    |
|                     |   | CANL  | 2.75  | 3.5                | 4.5  |      |    |
| V <sub>OD(R)</sub>  | Bus output voltage (Recessive)            | CANH  | Figure 1 and Figure 2, D at 0.7 V <sub>CC</sub> , Rs at 0 V |                    |      | V    |    |
|                     |   | CANL  | 0.5   |                    | 2    |      |    |
| V <sub>OD(D)</sub>  | Differential output voltage (Dominant)    | Figure 1 and Figure 2, D at 0.7 V <sub>CC</sub> , Rs at 0 V | 2   | 2.5                | 3    | V    |    |
| V <sub>OD(D)</sub>  | Differential output voltage (Dominant)    | Figure 1, D at 0 V, Rs at 0 V                               | 1.5   | 2                  | 3    | V    |    |
| V <sub>OD(D)</sub>  | Differential output voltage (Dominant)    | Figure 2 and Figure 3, D at 0 V, Rs at 0 V                  | 1.2   | 2                  | 3.1  | V    |    |
| V <sub>OD(R)</sub>  | Differential output voltage (Recessive)   | Figure 1 and Figure 2, D at 0.7 V <sub>CC</sub>             | -120  |                    | 12   | mV   |    |
| V <sub>OD(R)</sub>  | Differential output voltage (Recessive)   | D at 0.7 V <sub>CC</sub> , No load                          | -0.5  |                    | 0.05 | V    |    |
| V <sub>OC(pp)</sub> | Peak-to-peak common-mode output voltage   | Figure 9, Rs at 0 V   |   | 600                |      | mV   |    |
| I <sub>IH</sub>     | High-level input current, D input         | D at 0.7 V <sub>CC</sub>                                    | -40   |                    | 0    | μA   |    |
| I <sub>IL</sub>     | Low-level input current, D input          | D at 0.3 V <sub>CC</sub>                                    | -60   |                    | 0    | μA   |    |
| I <sub>OS(SS)</sub> | Short-circuit steady-state output current | Figure 11, V <sub>CANH</sub> at -7 V, CANL open             | -200  |                    |      | mA   |    |
|                     |   | Figure 11, V <sub>CANH</sub> at 12 V, CANL open             |   |                    |      |      |    |
|                     |   | Figure 11, V <sub>CANL</sub> at -7 V, CANH open             | -2  |                    |      |      |    |
|                     |   | Figure 11, V <sub>CANL</sub> at 12 V, CANH open             | 2.5   |                    |      |      |    |
| C <sub>O</sub>      | Output capacitance                        | See receiver input capacitance                              |   |                    |      |      |    |
| I <sub>OZ</sub>     | High-impedance output current             | See receiver input current                                  |   |                    |      |      |    |
| I <sub>IRs(s)</sub> | Rs input current for standby              | Rs at 0.75 V <sub>CC</sub>                                  | -10   |                    |      | μA   |    |
| I <sub>IRs(f)</sub> | Rs input current for full-speed operation | Rs at 0 V   | -550  |                    | 0    | μA   |    |
| I <sub>CC</sub>     | Supply current                            | Standby   | Rs at V <sub>CC</sub> , D at V <sub>CC</sub>                |                    |      | 275  | μA |
|                     |   | Dominant  | D at 0 V, 60-Ω load, Rs at 0 V                              |                    |      | 65   | mA |
|                     |   | Recessive   | D at V <sub>CC</sub> , No load, Rs at 0 V                   |                    |      | 14   |    |

(1) All typical values are at 25°C and with a 5-V supply.

## DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER          |   | TEST CONDITIONS                    | MIN | TYP  | MAX  | UNIT |
|--------------------|---|------------------------------------|-----|------|------|------|
| t <sub>pLH</sub>   | Propagation delay time, low-to-high-level output    | Figure 4, Rs at 0 V                |     | 40   | 70   | ns   |
|                    |   | Figure 4, Rs with 10 kΩ to ground  |     | 90   | 125  |      |
|                    |   | Figure 4, Rs with 100 kΩ to ground |     | 500  | 800  |      |
| t <sub>pHL</sub>   | Propagation delay time, high-to-low-level output    | Figure 4, Rs at 0 V                |     | 85   | 125  | ns   |
|                    |   | Figure 4, Rs with 10 kΩ to ground  |     | 200  | 260  |      |
|                    |   | Figure 4, Rs with 100 kΩ to ground |     | 1150 | 1450 |      |
| t <sub>sk(p)</sub> | Pulse skew ( t <sub>pHL</sub> - t <sub>pLH</sub>  ) | Figure 4, Rs at 0 V                |     | 45   | 85   | ns   |
|                    |   | Figure 4, Rs with 10 kΩ to ground  |     | 110  | 180  |      |
|                    |   | Figure 4, Rs with 100 kΩ to ground |     | 650  | 900  |      |
| t <sub>r</sub>     | Differential output signal rise time                | Figure 4, Rs at 0 V                | 35  |      | 100  | ns   |
| t <sub>f</sub>     | Differential output signal fall time                |                                    | 35  |      | 100  | ns   |
| t <sub>r</sub>     | Differential output signal rise time                | Figure 4, Rs with 10 kΩ to ground  | 100 |      | 250  | ns   |
| t <sub>f</sub>     | Differential output signal fall time                |                                    | 100 |      | 250  | ns   |
| t <sub>r</sub>     | Differential output signal rise time                | Figure 4, Rs with 100 kΩ to ground | 600 |      | 1550 | ns   |
| t <sub>f</sub>     | Differential output signal fall time                |                                    | 600 |      | 1550 | ns   |
| t <sub>en</sub>    | Enable time from standby to dominant                | Figure 8                           |     |      | 0.5  | μs   |

## RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER |  | TEST CONDITIONS  | MIN   | TYP | MAX          | UNIT       |
|-----------|--|--|---|-----|--------------|------------|
| $V_{IT+}$ | Positive-going input threshold voltage     | $R_s$ at 0 V, (See <a href="#">Table 1</a> )                         |   | 750 | 900          | mV         |
| $V_{IT-}$ | Negative-going input threshold voltage     |  |   | 500 | 650          |            |
| $V_{hys}$ | Hysteresis voltage ( $V_{IT+} - V_{IT-}$ ) |  |   | 100 |              |            |
| $V_{OH}$  | High-level output voltage                  | <a href="#">Figure 6</a> , $I_O = -4$ mA                             | 0.8 $V_{CC}$  |     |              | V          |
| $V_{OL}$  | Low-level output voltage                   | <a href="#">Figure 6</a> , $I_O = 4$ mA                              |   |     | 0.2 $V_{CC}$ | V          |
| $I_I$     | Bus input current                          | CANH or CANL at 12 V   |   |     | 600          | A          |
|           |  | CANH or CANL at 12 V, $V_{CC}$ at 0 V                                |   |     | 715          |            |
|           |  | CANH or CANL at -7 V   | Other bus pin at 0 V, $R_s$ at 0 V, D at 0.7 $V_{CC}$ |     | -460         |            |
|           |  | CANH or CANL at -7 V, $V_{CC}$ at 0 V                                |   |     | -340         |            |
| $C_I$     | Input capacitance (CANH or CANL)           | Pin-to-ground, $V_I = 0.4 \sin(4E6\pi t) + 0.5$ V, D at 0.7 $V_{CC}$ | 20  |     |              | pF         |
| $C_{ID}$  | Differential input capacitance             | Pin-to-pin, $V_I = 0.4 \sin(4E6\pi t) + 0.5$ V, D at 0.7 $V_{CC}$    | 10  |     |              | pF         |
| $R_{ID}$  | Differential input resistance              | D at 0.7 $V_{CC}$ , $R_s$ at 0 V                                     | 40  |     | 100          | k $\Omega$ |
| $R_{IN}$  | Input resistance (CANH or CANL)            | D at 0.7 $V_{CC}$ , $R_s$ at 0 V                                     | 20  |     | 50           | k $\Omega$ |
| $I_{CC}$  | Supply current                             | Standby  | $R_s$ at $V_{CC}$ , D at $V_{CC}$                     |     | 275          | mA         |
|           |  | Dominant   | D at 0 V, 60- $\Omega$ load, $R_s$ at 0 V             |     | 65           |            |
|           |  | Recessive  | D at $V_{CC}$ , No load, $R_s$ at 0 V                 |     | 14           |            |

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER   |  | TEST CONDITIONS          | MIN   | TYP | MAX | UNIT |
|-------------|--|--------------------------|---|-----|-----|------|
| $t_{pLH}$   | Propagation delay time, low-to-high-level output | <a href="#">Figure 6</a> |   | 35  | 50  | ns   |
| $t_{pHL}$   | Propagation delay time, high-to-low-level output |                          |   | 35  | 50  | ns   |
| $t_{sk(p)}$ | Pulse skew ( $t_{pHL} - t_{pLH}$ )               |                          |   |     | 20  | ns   |
| $t_r$       | Output signal rise time                          |                          |   | 2   | 4   | ns   |
| $t_f$       | Output signal fall time                          |                          |   | 2   | 4   | ns   |
| $t_{p(sb)}$ | Propagation delay time in standby                |                          | <a href="#">Figure 12</a> , $R_s$ at $V_{CC}$ |     |     | 500  |

## VREF PIN CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER |                          | TEST CONDITIONS              | MIN           | MAX           | UNIT |
|-----------|--------------------------|------------------------------|---------------|---------------|------|
| $V_O$     | Reference output voltage | $-5 \mu A < I_O < 5 \mu A$   | 0.45 $V_{CC}$ | 0.55 $V_{CC}$ | V    |
|           |                          | $-50 \mu A < I_O < 50 \mu A$ | 0.4 $V_{CC}$  | 0.6 $V_{CC}$  |      |

**DEVICE SWITCHING CHARACTERISTICS**

over recommended operating conditions (unless otherwise noted)

| PARAMETER   |  | TEST CONDITIONS                                    | MIN | TYP  | MAX  | UNIT |
|-------------|--|--|-----|------|------|------|
| $t_{loop1}$ | Total loop delay, driver input to receiver output, recessive to dominant | Figure 10, Rs at 0 V                               |     | 60   | 100  | ns   |
|             |  | Figure 10, Rs with 10 k $\Omega$ to ground         |     | 100  | 150  |      |
|             |  | Figure 10, Rs with 100 k $\Omega$ to ground        |     | 440  | 800  |      |
| $t_{loop2}$ | Total loop delay, driver input to receiver output, dominant to recessive | Figure 10, Rs at 0 V                               |     | 115  | 150  | ns   |
|             |  | Figure 10, Rs with 10 k $\Omega$ to ground         |     | 235  | 290  |      |
|             |  | Figure 10, Rs with 100 k $\Omega$ to ground        |     | 1070 | 1450 |      |
| $t_{loop2}$ | Total loop delay, driver input to receiver output, dominant to recessive | Figure 10, Rs at 0 V, $V_{CC}$ from 4.5 V to 5.1 V |     | 105  | 145  | ns   |

PARAMETER MEASUREMENT INFORMATION

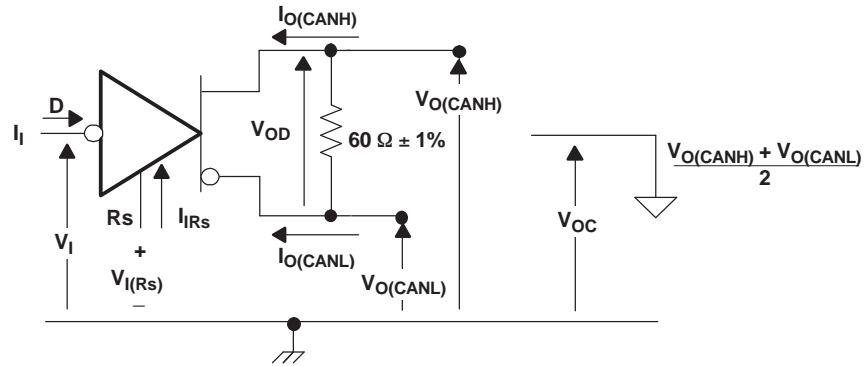


Figure 1. Driver Voltage, Current, and Test Definition

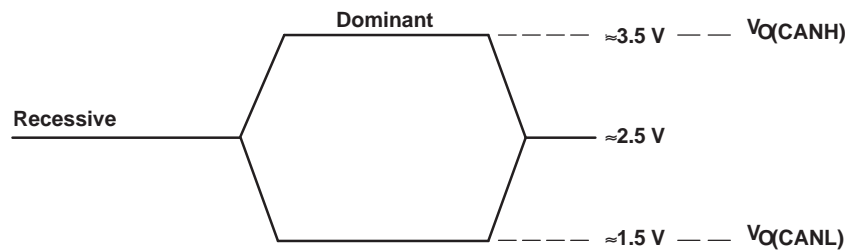


Figure 2. Bus Logic State Voltage Definitions

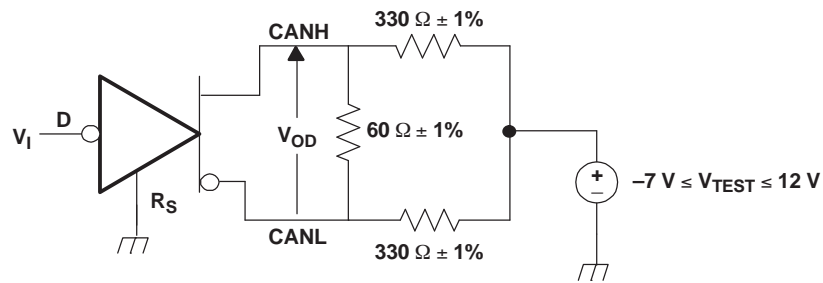


Figure 3. Driver  $V_{OD}$

PARAMETER MEASUREMENT INFORMATION (continued)

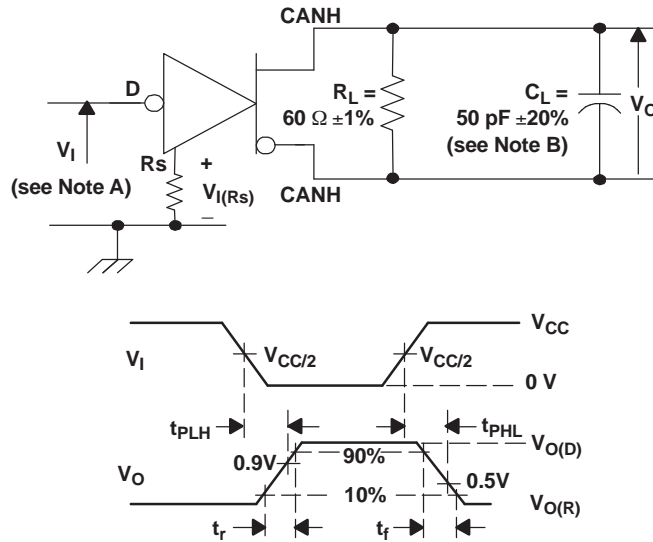


Figure 4. Driver Test Circuit and Voltage Waveforms

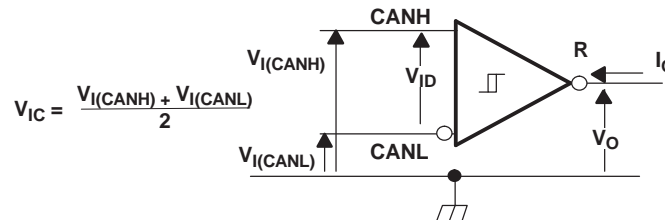
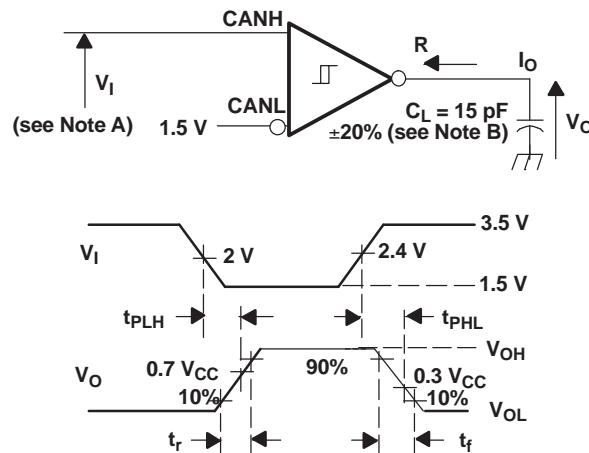


Figure 5. Receiver Voltage and Current Definitions

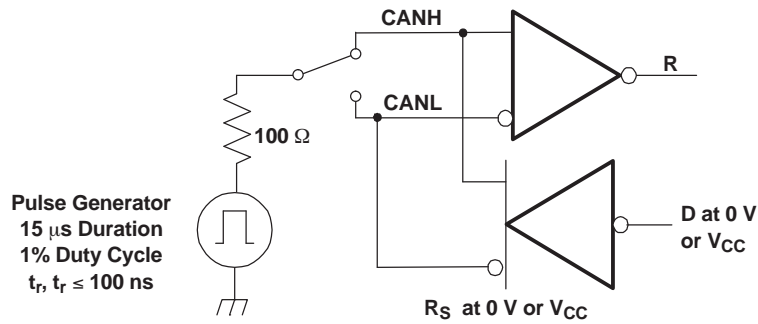


- A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, tr ≤ 6ns, tf ≤ 6 ns, ZO = 50 Ω.
- B. CL includes instrumentation and fixture capacitance within ±20%.

Figure 6. Receiver Test Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION (continued)



A. This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 7. Test Circuit, Transient Overvoltage Test

Table 1. Receiver Characteristics Over Common Mode Voltage

| INPUT      |            | MEASURED   | OUTPUT |          |
|------------|------------|------------|--------|----------|
| $V_{CANH}$ | $V_{CANL}$ | $ V_{ID} $ | R      |          |
| 12 V       | 11.1 V     | 900 mV     | L      | $V_{OL}$ |
| -6.1 V     | -7 V       | 900 mV     | L      |          |
| -1 V       | -7 V       | 6 V        | L      |          |
| 12 V       | 6 V        | 6 V        | L      |          |
| -6.5 V     | -7 V       | 500 mV     | H      | $V_{OH}$ |
| 12 V       | 11.5 V     | 500 mV     | H      |          |
| -7 V       | -1 V       | 6 V        | H      |          |
| 6 V        | 12 V       | 6 V        | H      |          |
| open       | open       | X          | H      |          |

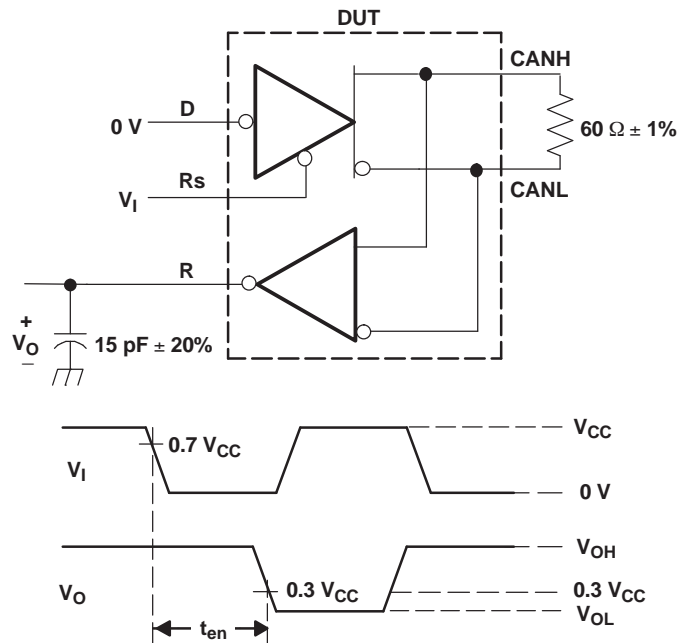
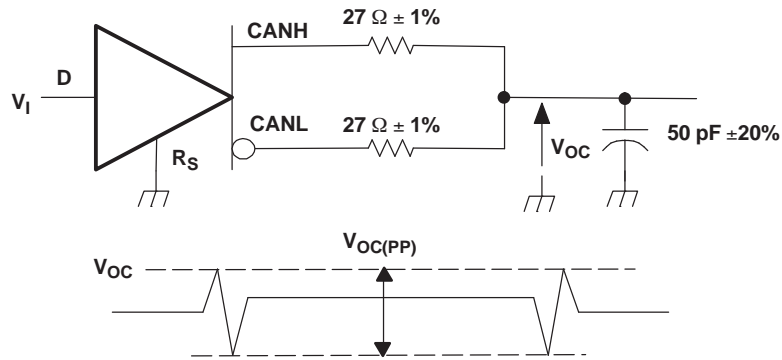


Figure 8.  $t_{en}$  Test Circuit and Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq 125\ \text{kHz}$ , 50% duty cycle,  $t_r \leq 6\ \text{ns}$ ,  $t_f \leq 6\ \text{ns}$ ,  $Z_O = 50\ \Omega$ .

Figure 9. Peak-to-Peak Common Mode Output Voltage

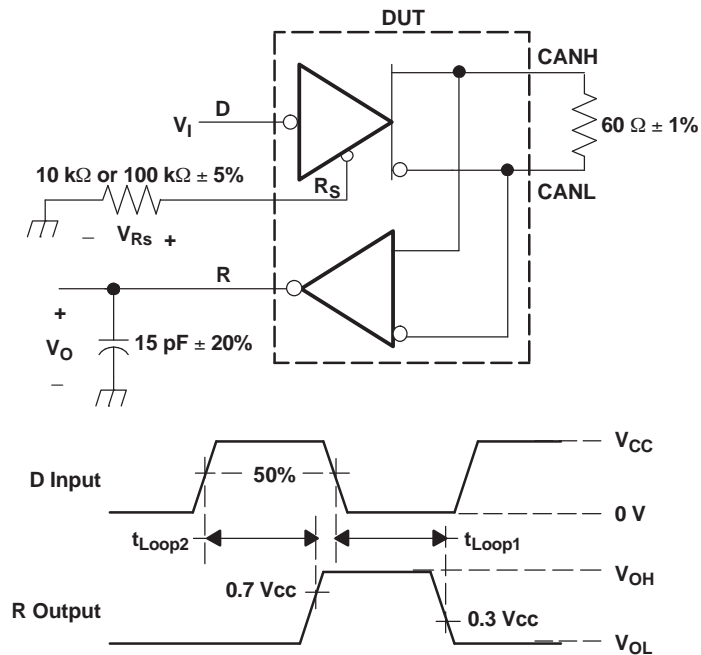


Figure 10.  $t_{LOOP}$  Test Circuit and Voltage Waveforms

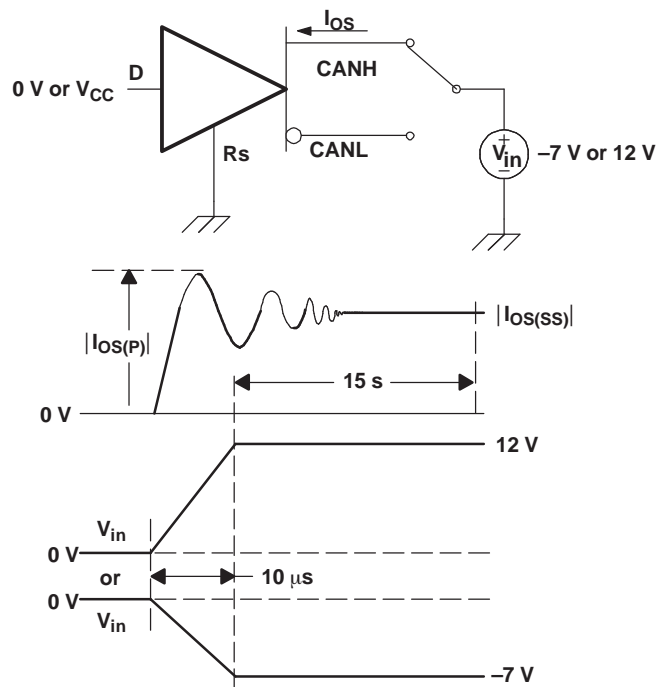
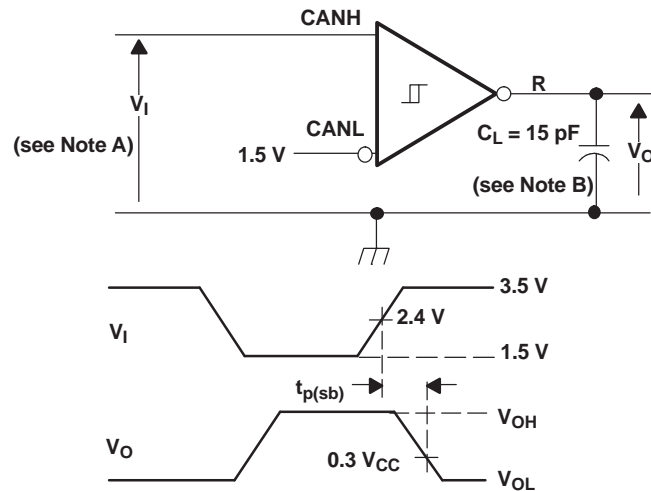


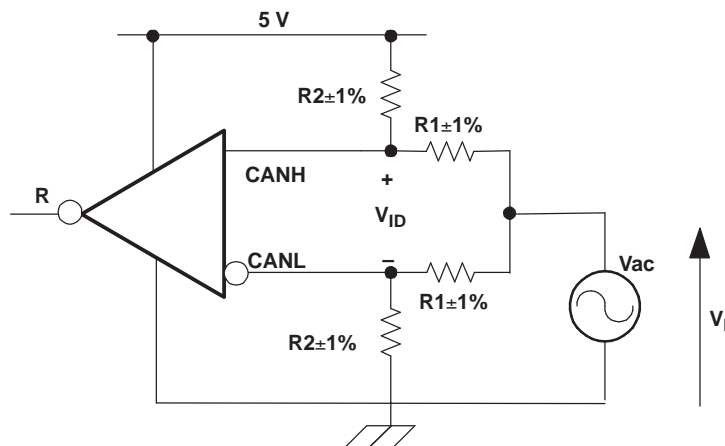
Figure 11. Driver Short-Circuit Test



- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  125 kHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 12. Receiver Propagation Delay in Standby Test Circuit and Waveforms

DEVICE INFORMATION



| $V_{ID}$ | R1          | R2           |
|----------|-------------|--------------|
| 500 mV   | 50 $\Omega$ | 450 $\Omega$ |
| 900 mV   | 50 $\Omega$ | 227 $\Omega$ |



A. All input pulses are supplied by a generator having the following characteristics:  $f < 1.5$  MHz,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5$  V.

Figure 13. Common-Mode Input Voltage Rejection Test

FUNCTION TABLES

Table 2. DRIVER

| INPUTS<br>D | Voltage at $R_s$ , $V_{Rs}$ | OUTPUTS |      | BUS STATE |
|-------------|-----------------------------|---------|------|-----------|
|             |                             | CANH    | CANL |           |
| L           | $V_{Rs} < 1.2$ V            | H       | L    | Dominant  |
| H           | $V_{Rs} < 1.2$ V            | Z       | Z    | Recessive |
| Open        | X                           | Z       | Z    | Recessive |
| X           | $V_{Rs} > 0.75 V_{CC}$      | Z       | Z    | Recessive |

Table 3. RECEIVER

| DIFFERENTIAL INPUTS [ $V_{ID} = V(\text{CANH}) - V(\text{CANL})$ ] | OUTPUT R <sup>(1)</sup> |
|--|-------------------------|
| $V_{ID} \geq 0.9$ V  | L                       |
| $0.5\text{V} < V_{ID} < 0.9$ V                                     | ?                       |
| $V_{ID} \leq 0.5$ V  | H                       |
| Open   | H                       |

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

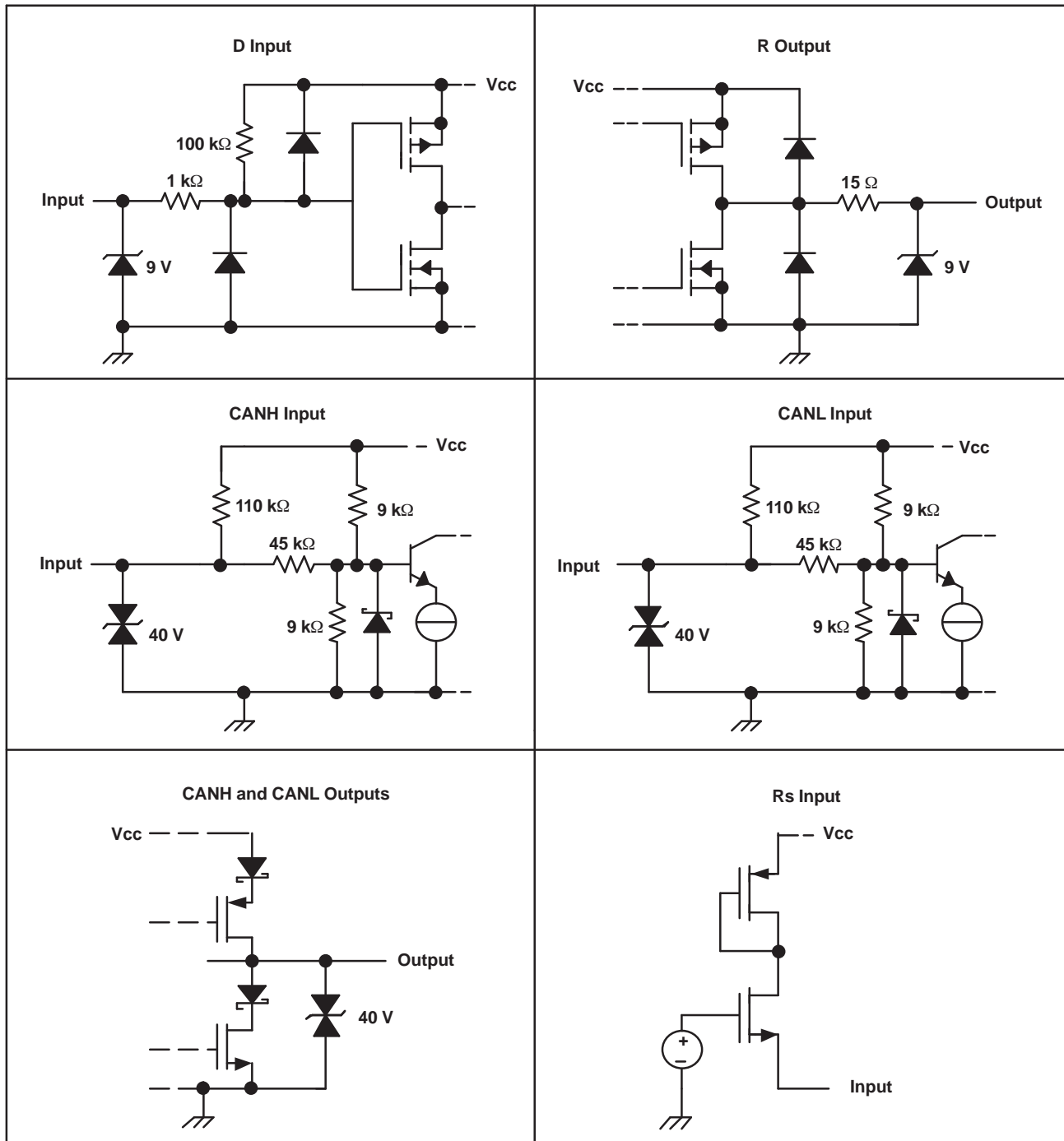


Figure 14. Equivalent Input and Output Schematic Diagrams

TYPICAL CHARACTERISTICS

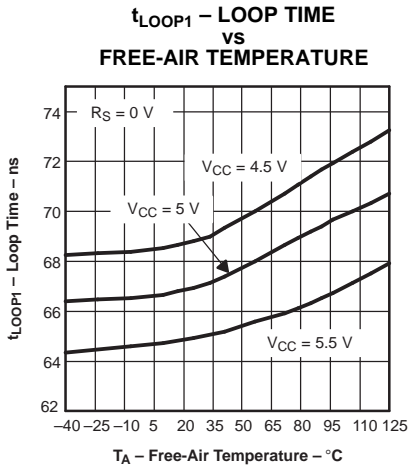


Figure 15.

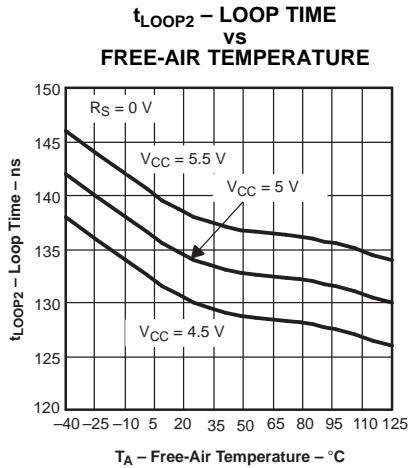


Figure 16.

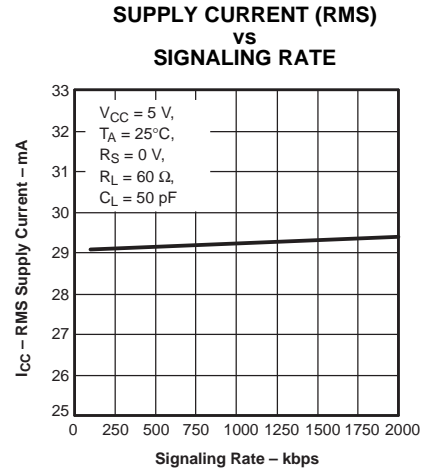


Figure 17.

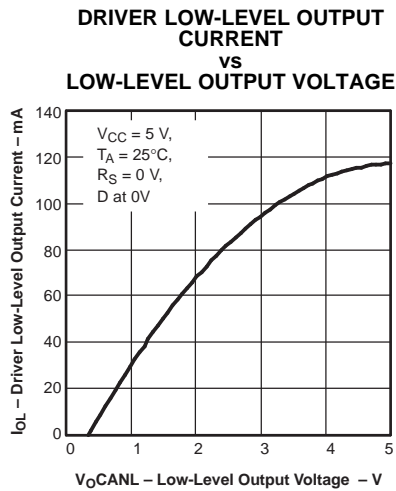


Figure 18.

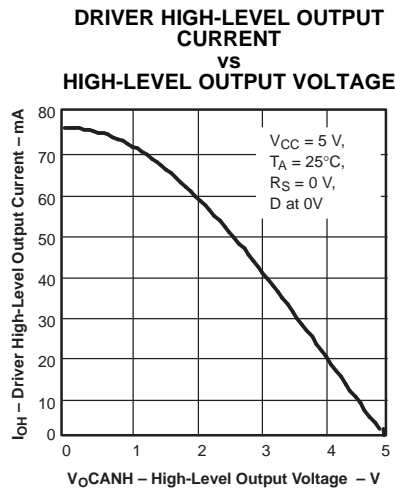


Figure 19.

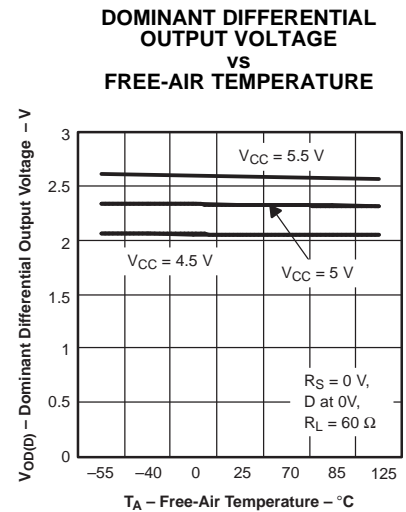


Figure 20.

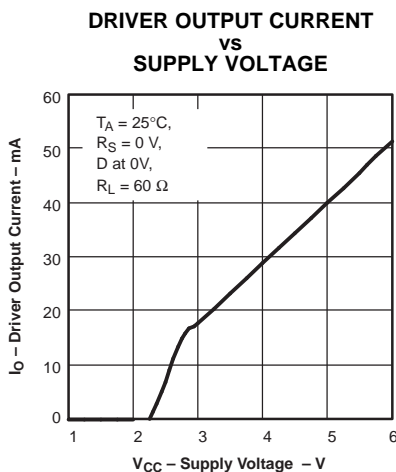


Figure 21.

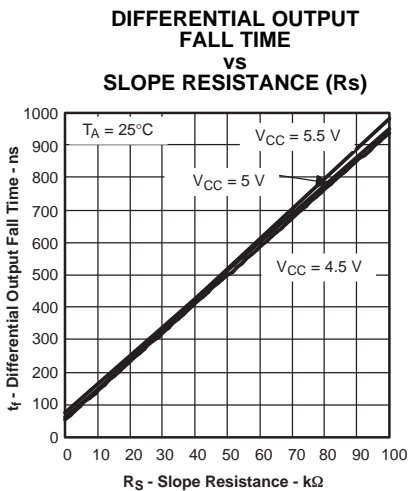


Figure 22.

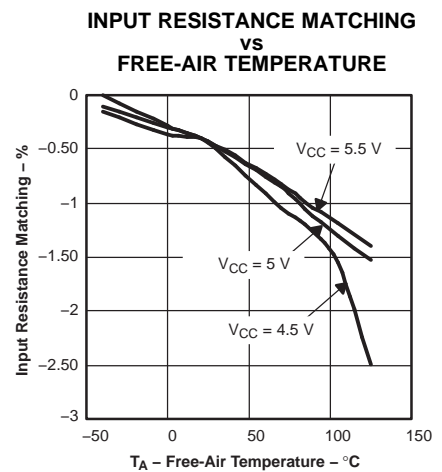


Figure 23.

## APPLICATION INFORMATION

The basics of bus arbitration require that the receiver at the sending node designate the first bit as dominant or recessive after the initial wave of the first bit of a message travels to the most remote node on a network and back again. Typically, this *sample* is made at 75% of the bit width, and within this limitation, the maximum allowable signal distortion in a CAN network is determined by network electrical parameters.

Factors to be considered in network design include the 5 ns/m propagation delay of typical twisted-pair bus cable; signal amplitude loss due to the loss mechanisms of the cable; and the number, length, and spacing of drop-lines (stubs) on a network. Under strict analysis, variations among the different

oscillators in a system must also be accounted for with adjustments in signaling rate and stub and bus length. Table 4 lists the maximum signaling rates achieved with the SN65HVD251 in high-speed mode with several bus lengths of category 5, shielded twisted-pair (CAT 5 STP) cable.

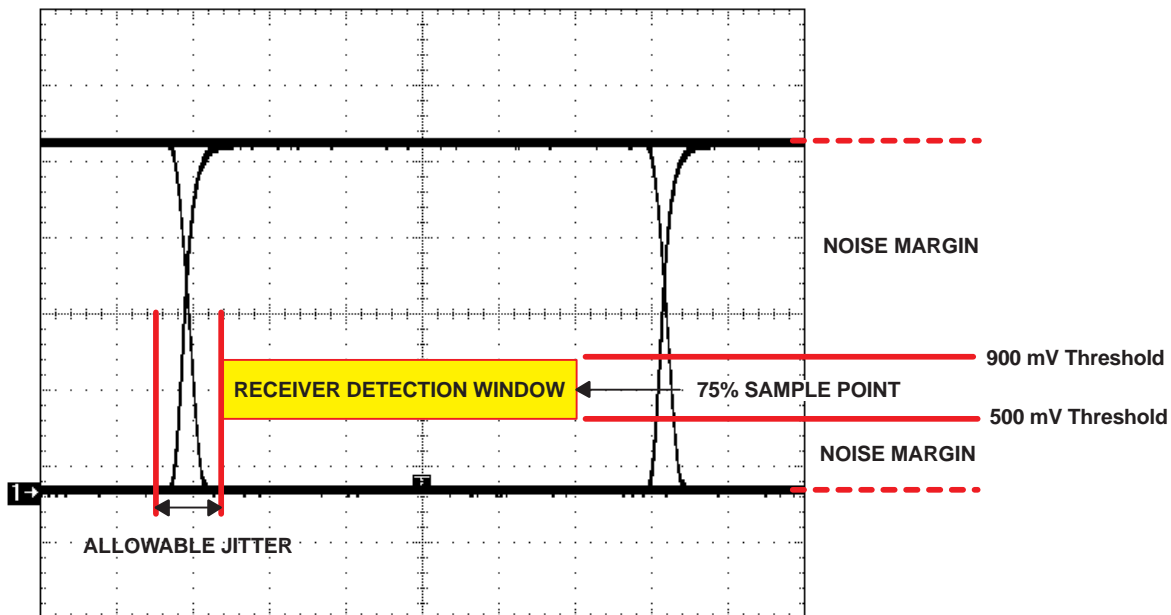
**Table 4. Maximum Signaling Rates for Various Cable Lengths**

| BUS LENGTH (m) | SIGNALING RATE (kbps) |
|----------------|-----------------------|
| 30             | 1000                  |
| 100            | 500                   |
| 250            | 250                   |
| 500            | 125                   |
| 1000           | 62.5                  |

The ISO 11898 standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes on a bus. (Note: Non-standard application may come with a trade-off in signaling rate.) A bus with a large number of nodes requires a transceiver with high input impedance such as the HVD251.

The Standard specifies the interconnect to be a single twisted-pair cable (shielded or unshielded) with 120-Ω characteristic impedance ( $Z_0$ ). Resistors equal to the characteristic impedance of the line terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines connect nodes to the bus and should be kept as short as possible to minimize signal reflections.

Connectors, while not specified by the ISO 11898 standard, should have as little effect as possible on standard operating parameters such as capacitive loading. Although unshielded cable is used in many applications, data transmission circuits employing CAN transceivers are usually used in applications requiring a rugged interconnection with a wide common-mode voltage range. Therefore, shielded cable is recommended in these electronically harsh environments, and when coupled with the -2-V to 7-V common-mode range of tolerable ground noise specified in the standard, helps to ensure data integrity. The HVD251 extends data integrity beyond that of the standard with an extended -7-V to 12-V range of common-mode operation.



**Figure 24. Typical CAN Differential Signal Eye Pattern**

An eye pattern is a useful tool for measuring overall signal quality. As displayed in Figure 24, the differential signal changes logic states in two places on the display, producing an eye. Instead of viewing only one logic crossing on the scope, an entire *bit* of data is brought into view. The resulting eye pattern includes all effects of systemic and random distortion, and displays the time during which a signal may be considered valid.

The height of the eye above or below the receiver threshold voltage level at the sampling point is the noise margin of the system. Jitter is typically measured at the differential voltage zero-crossing during the logic state transition of a signal. Note that jitter present at the receiver threshold voltage level is considered by some to be a more effective representation of the jitter at the input of a receiver.

As the sum of skew and noise increases, the eye closes and data is corrupted. Closing the width decreases the time available for accurate sampling, and lowering the height enters the 900 mV or 500 mV threshold of a receiver.

Different sources induce noise onto a signal. The more obvious noise sources are the components of a transmission circuit themselves; the signal transmitter, traces and cables, connectors, and the receiver. Beyond that, there is a termination dependency, cross-talk from clock traces and other proximity effects,  $V_{CC}$  and ground bounce, and electromagnetic interference from nearby electrical equipment.

The balanced receiver inputs of the HVD251 mitigate most sources of signal corruption, and when used with a quality shielded twisted-pair cable, help ensure data integrity.

## Typical Application

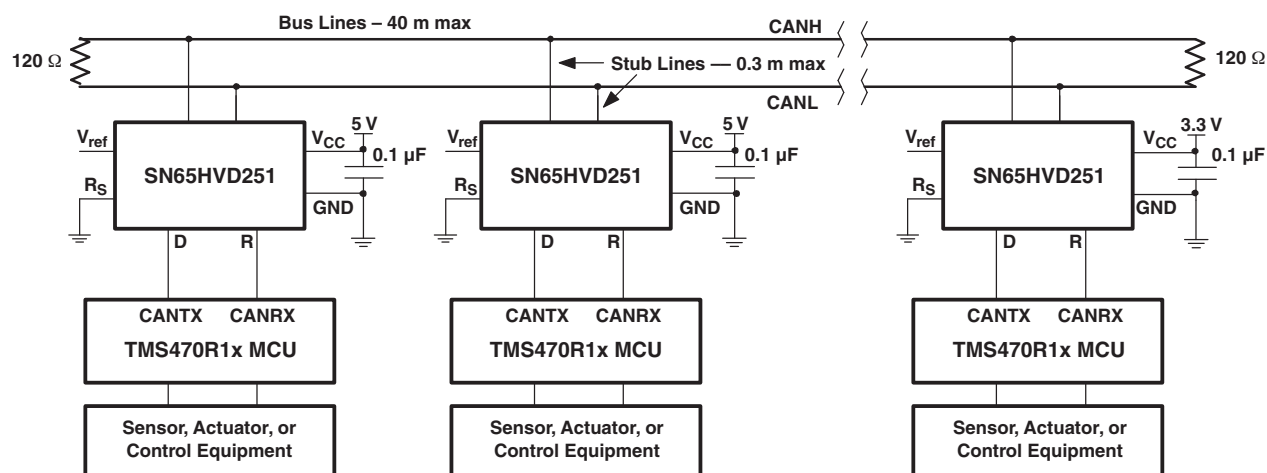


Figure 25. Typical HVD251 Application



**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN65HVD251QDRQ1  | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | 251Q1                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN65HVD251-Q1 :**

- Catalog: [SN65HVD251](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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