General Description

The 843004 is a 4 output LVPECL synthesizer optimized to generate Fibre Channel reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from IDT. Using a 26.5625MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL[1:0]): 212.5MHz, 187.5MHz, 159.375MHz, 156.25, 106.25MHz, and 53.125MHz. The 843004 uses IDT's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Fibre Channel jitter requirements. The 843004 is packaged in a small 24-pin TSSOP package.

Features

- Four 3.3Vdifferential LVPECL output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended clock input
- Supports the following output frequencies: 212.5MHz, 187.5MHz, 159.375MHz, 156.25MHz, 106.25MHz, 53.125MHz
- VCO range: 560MHz – 680MHz
- RMS phase jitter @ 212.5MHz, using a 26.5625MHz crystal (637kHz – 10MHz): 0.72ps (typical)

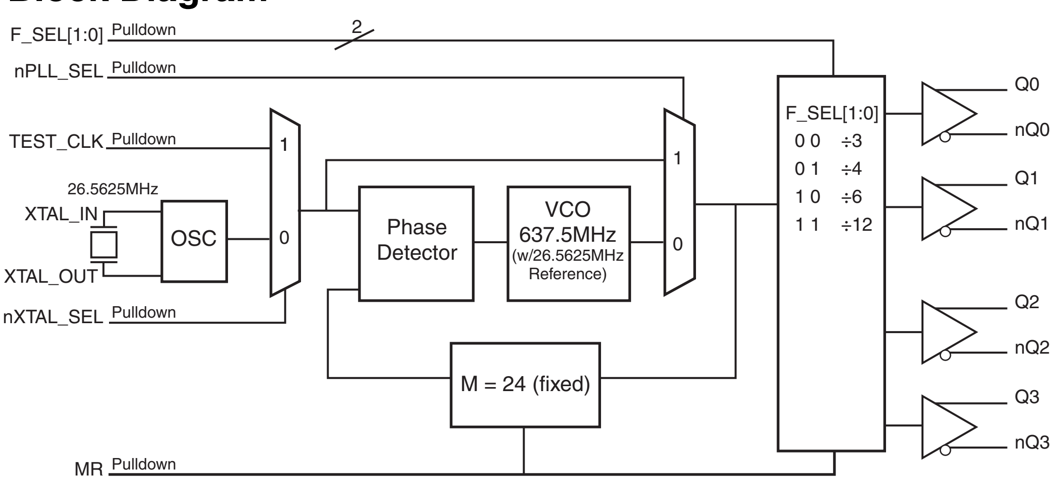
Offset	Noise Power
100Hz	-95.0 dBc/Hz
1kHz	-114.3 dBc/Hz
10kHz	-123.8 dBc/Hz
100kHz	-124.6 dBc/Hz

- Full 3.3V supply mode
- -30°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

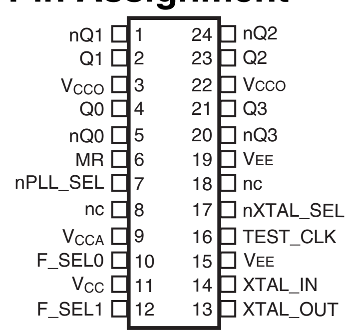
Table 3A. Bank A Frequency Table

Inputs						
Input Frequency (MHz)	F_SEL1	F_SEL0	M Div. Value	N Div. Value	M/N Div. Value	Output Frequency (MHz)
26.5625	0	0	24	3	8	212.5
26.5625	0	1	24	4	6	159.375
26.5625	1	0	24	6	4	106.25
26.5625	1	1	24	12	2	53.125
26.04166	0	1	24	4	6	156.25
23.4375	0	0	24	3	8	187.5

Block Diagram



Pin Assignment



ICS843004

24-Lead TSSOP
4.4mm x 7.8mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
3, 22	V_{CCO}	Power		Output supply pins.
4, 5	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
6	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7	nPLL_SEL	Input	Pulldown	Selects between the PLL and TEST_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, deselects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels.
8, 18	nc	Unused		No connect.
9	V_{CCA}	Power		Analog supply pin.
10, 12	F_SEL0. F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
11	V_{CC}	Power		Core supply pin.
13, 14	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
15, 19	V_{EE}	Power		Negative supply pins.
16	TEST_CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
17	nXTAL_SEL	Input	Pulldown	Selects between the single-ended TEST_CLK or crystal interface as the PLL reference source. When HIGH, selects TEST_CLK. When LOW, selects XTAL. LVCMOS/LVTTL interface levels.
20, 21	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
23, 24	Q2, nQ2	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V ± 5%, V_{EE} =0V, T_A = -30°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	3.135
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				135	mA
I_{CCA}	Analog Supply Current	Included in I_{EE}			15	mA

Table 3B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V ± 5%, V_{EE} =0V, T_A = -30°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	nPLL_SEL, nXTAL_SEL, MR, F_SEL[0:1]		-0.3		0.8	V
		TEST_CLK		-0.3		1.3	V
I_{IH}	Input High Current	TEST_CLK, MR, F_SEL[0:1], nPLL_SEL, nXTAL_SEL	$V_{CC} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	TEST_CLK, MR, F_SEL[0:1], nPLL_SEL, nXTAL_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA

Table 3C. LVPECL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -30°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		$V_{CCO} – 1.4$		$V_{CCO} – 0.9$	µA
V_{OL}	Output Low Current; NOTE 1		$V_{CCO} – 2.0$		$V_{CCO} – 1.7$	µA
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{CCO} – 2V.

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		23.33	26.5625	28.33	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

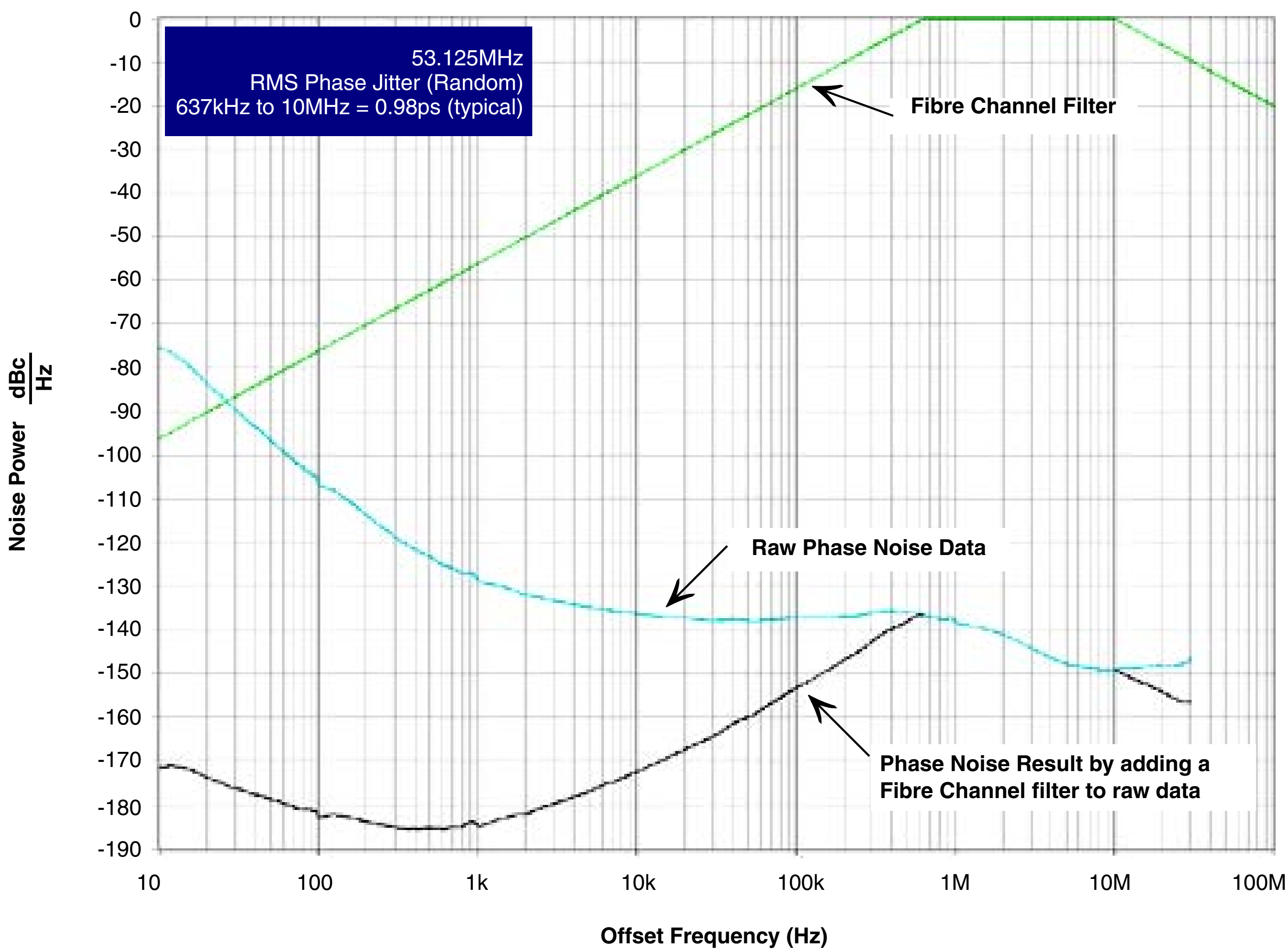
AC Electrical Characteristics

Table 5. AC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -30°C$ to $85°C$

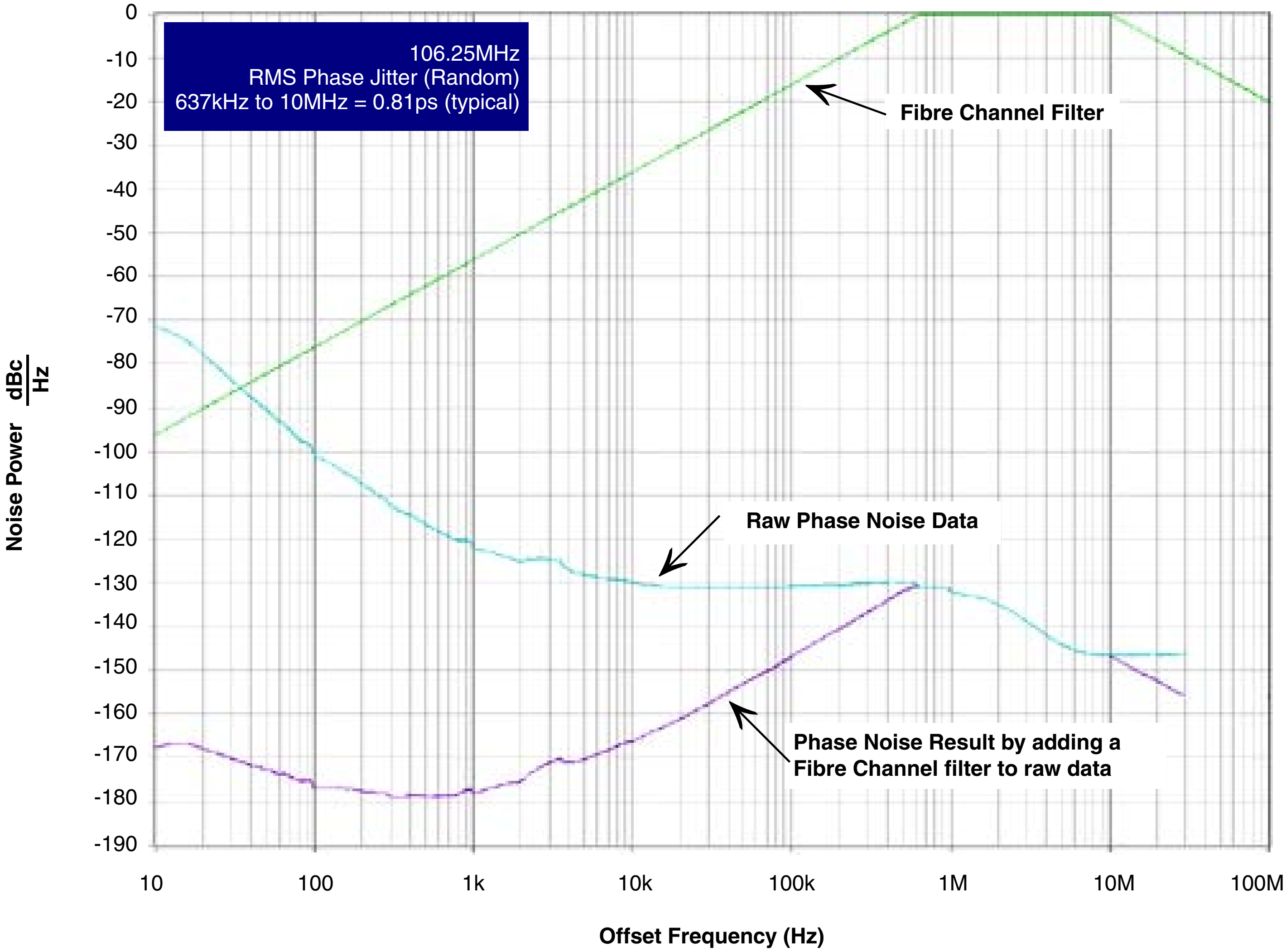
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range	F_SEL[1:0] = 00	186.67		226.66	MHz
		F_SEL[1:0] = 01	140		170	MHz
		F_SEL[1:0] = 10	93.33		113.33	MHz
		F_SEL[1:0] = 11	46.67		56.66	MHz
*t*sk(o)	Output Skew; NOTE 1, 2				30	ps
*t*jit(Ø)	RMS Phase Jitter, (Random); NOTE 3	212.5MHz, (637kHz – 10MHz)		0.70		ps
		159.375MHz, (637kHz – 10MHz)		0.75		ps
		156.25MHz, (637kHz – 10MHz)		0.58		ps
		106.25MHz, (637kHz – 10MHz)		0.81		ps
		53.125MHz, (637kHz – 10MHz)		0.98		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		600	ps
odc	Output Duty Cycle	F_SEL[1:0] ≠ 00	49		51	%
		F_SEL[1:0] = 00	45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{CCO}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plots.

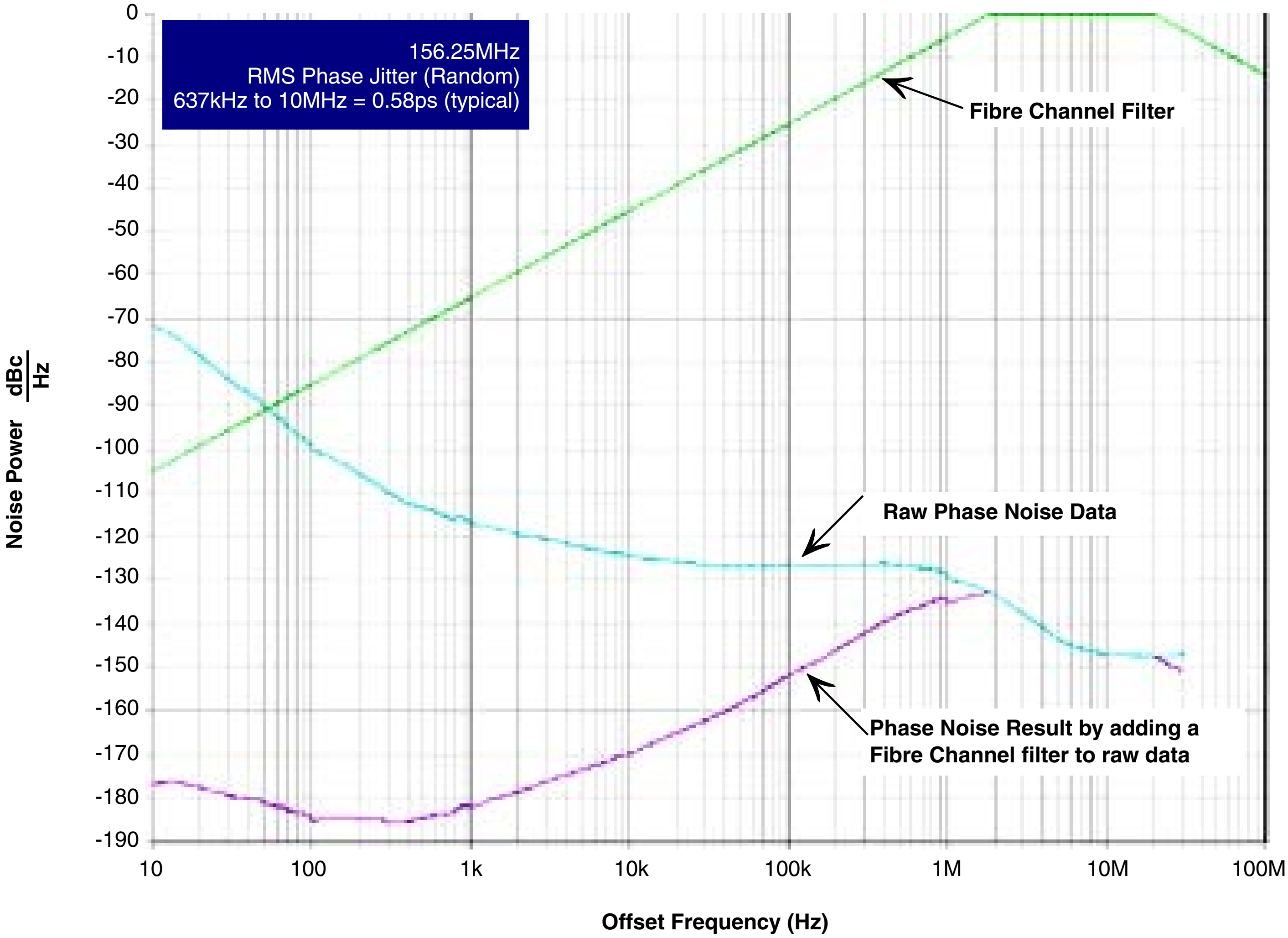
Typical Phase Noise at 53.125MHz


53.125MHz
RMS Phase Jitter (Random)
637kHz to 10MHz = 0.98ps (typical)
Fibre Channel Filter
Raw Phase Noise Data
Phase Noise Result by adding a Fibre Channel filter to raw data
Noise Power dBc/Hz
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
-130
-140
-150
-160
-170
-180
-190
10
100
1k
10k
100k
1M
10M
100M
Offset Frequency (Hz)

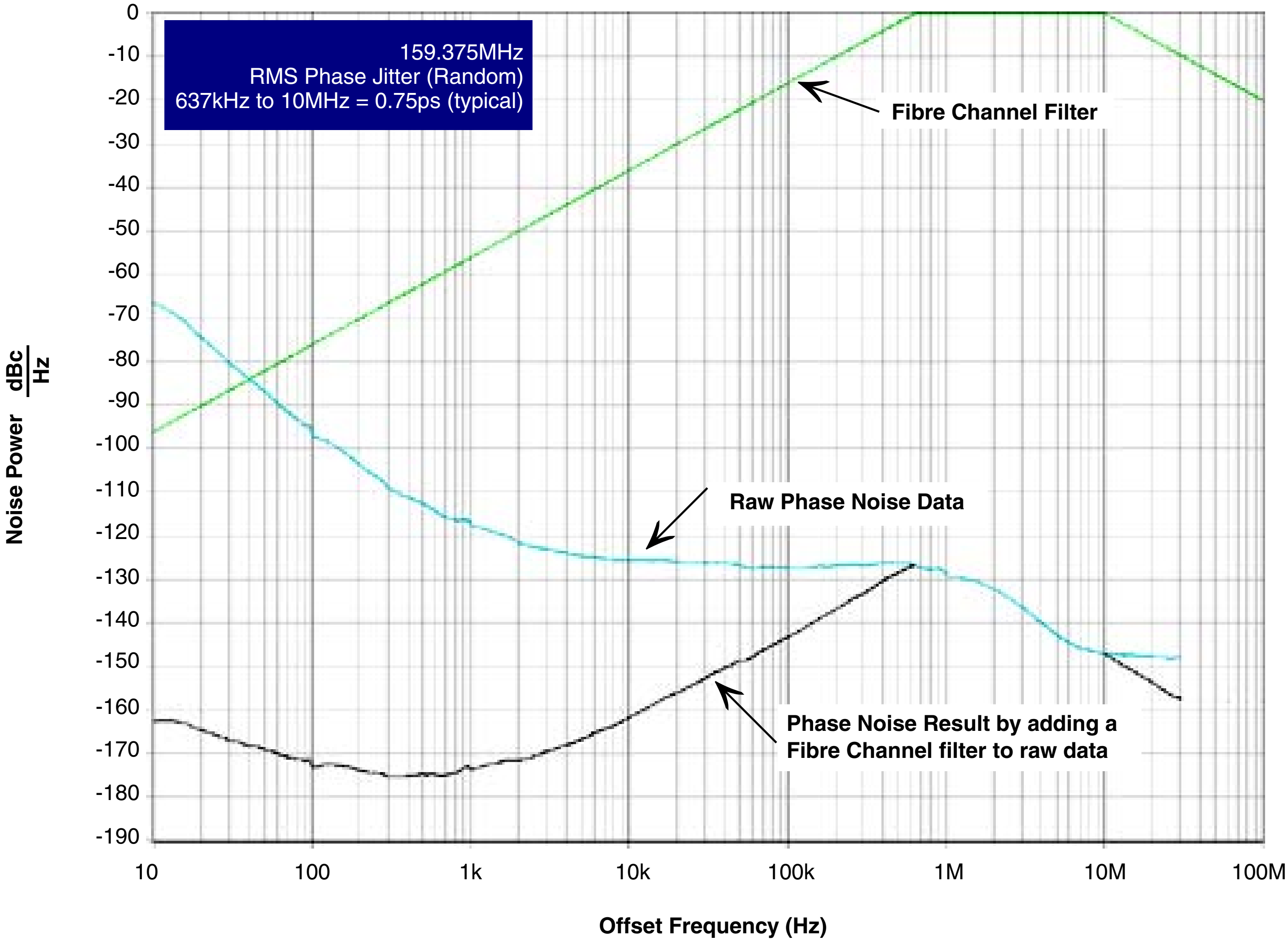
Typical Phase Noise at 106.25MHz



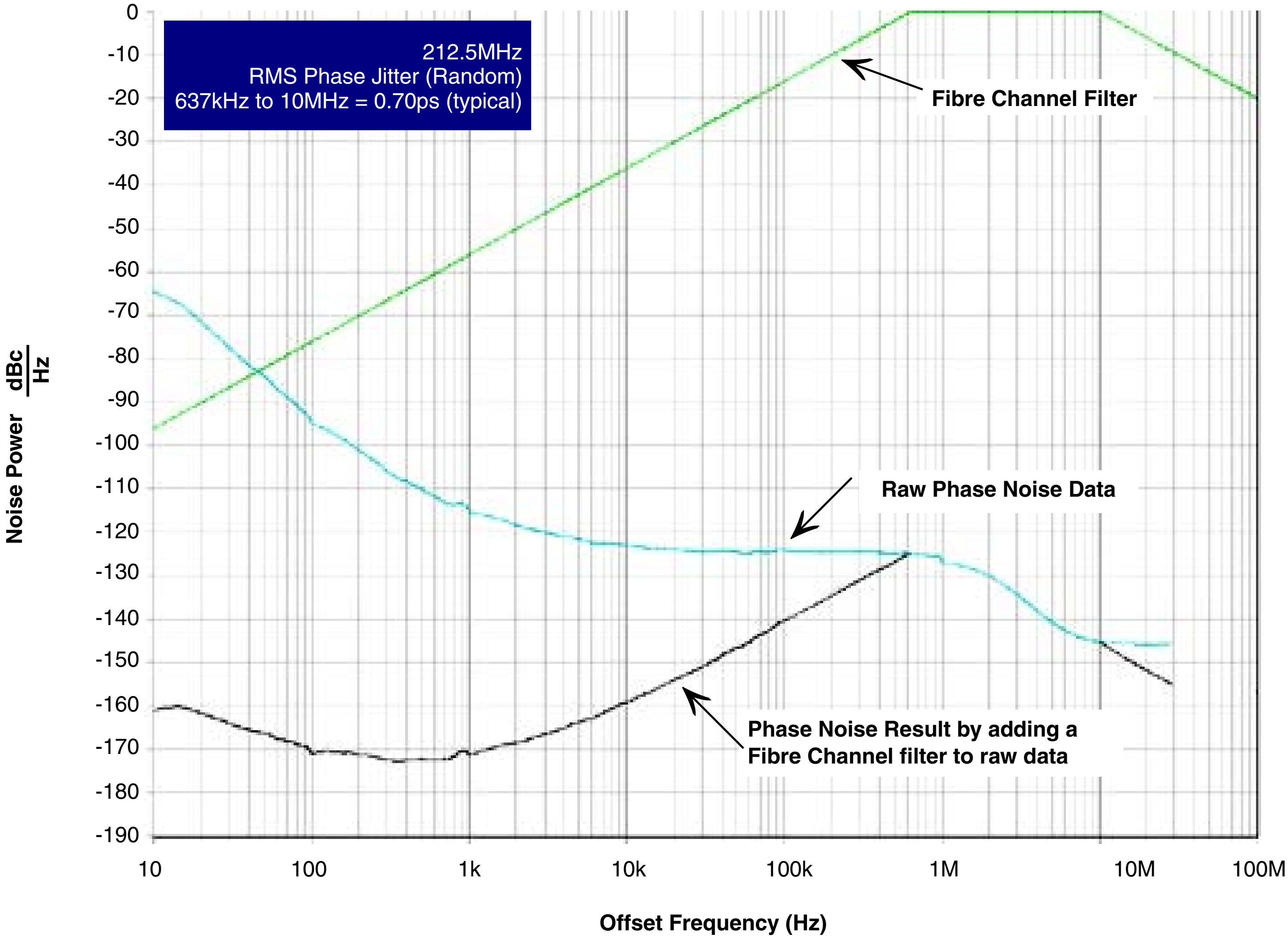
Typical Phase Noise at 156.25MHz



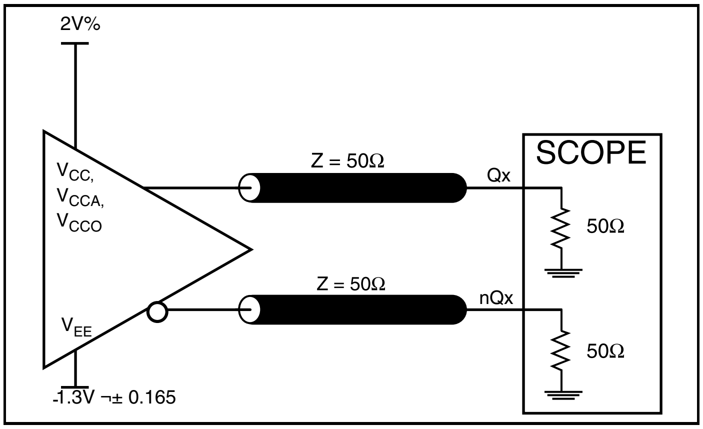
Typical Phase Noise at 159.375MHz



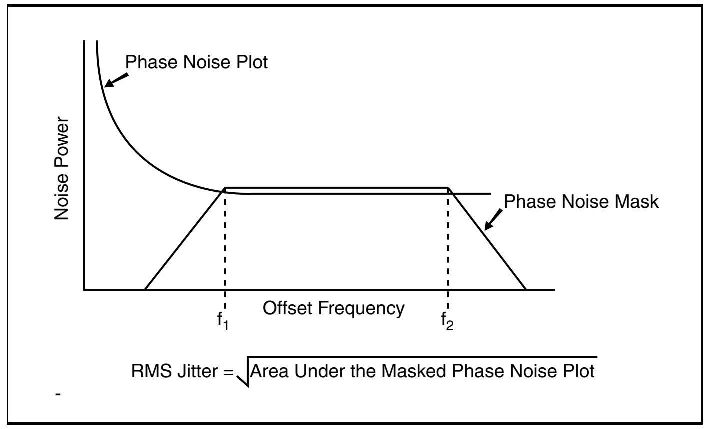
Typical Phase Noise at 212.5MHz



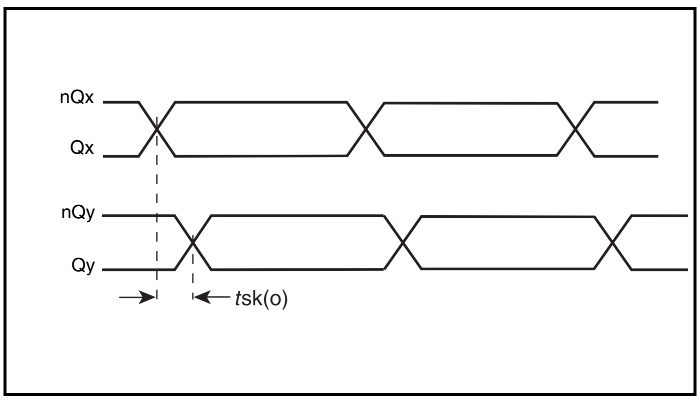
Parameter Measurement Information



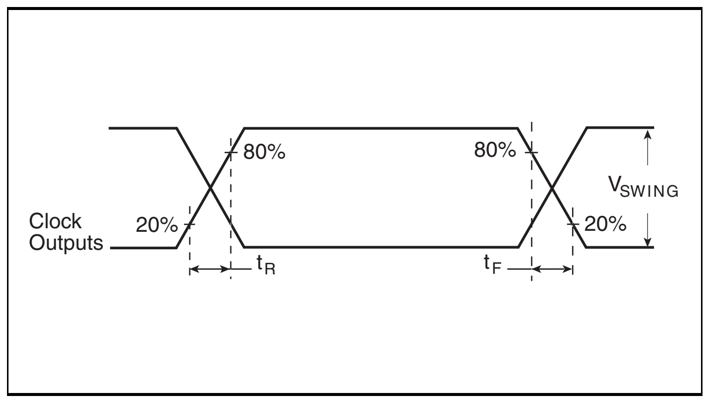
3.3V LVPECL Output Load AC Test Circuit



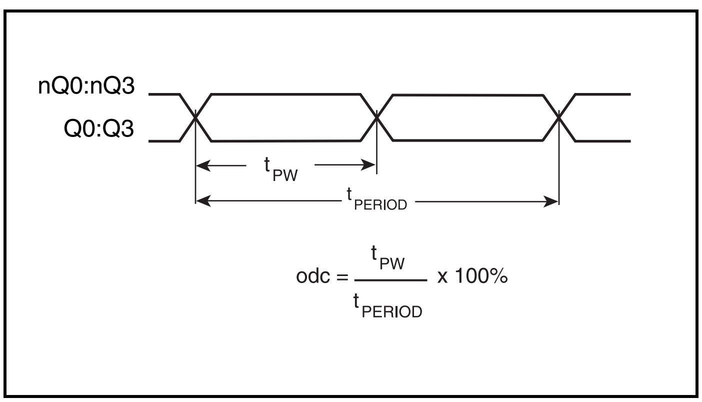
RMS Phase Jitter



Output Skew



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 843004 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA} and V_{CCO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

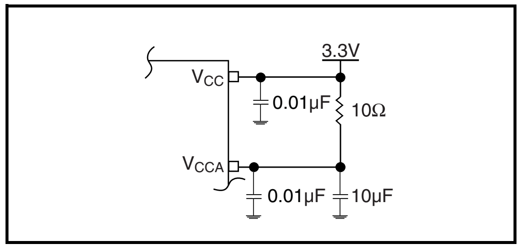


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

TEST_CLK Input

For applications not requiring the use of the clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST_CLK to ground.

LVCMOS Control Pins

All control pins have internal pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The 843004 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 26.5625MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

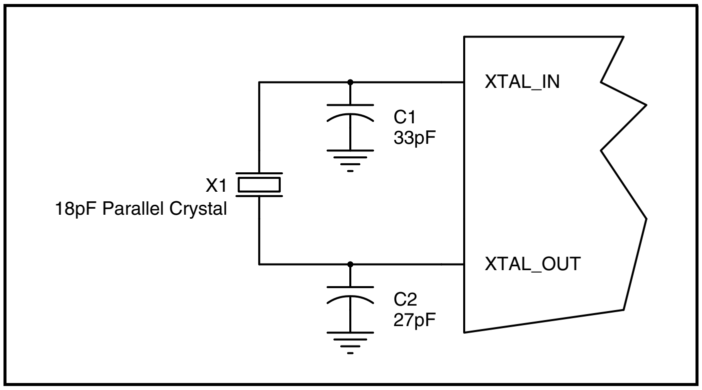


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

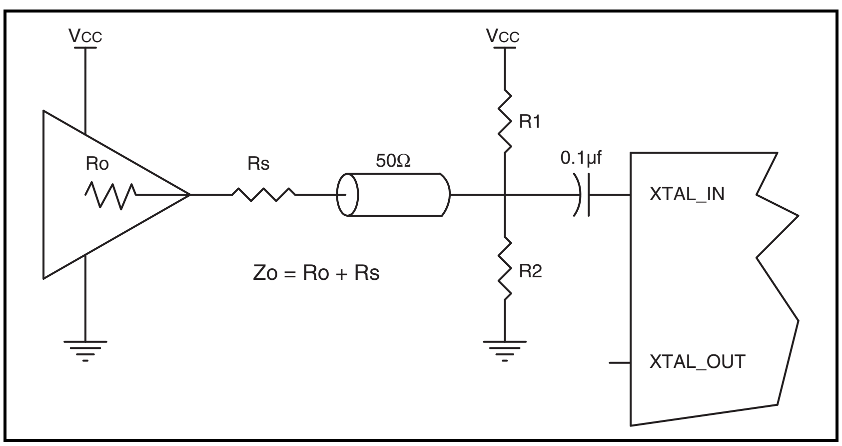


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

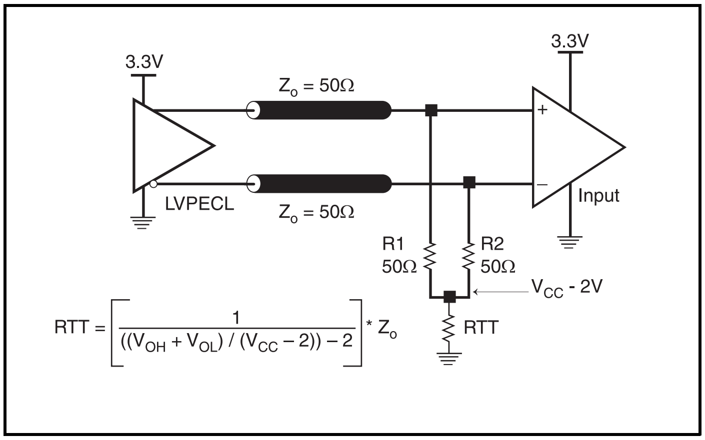


Figure 4A. 3.3V LVPECL Output Termination

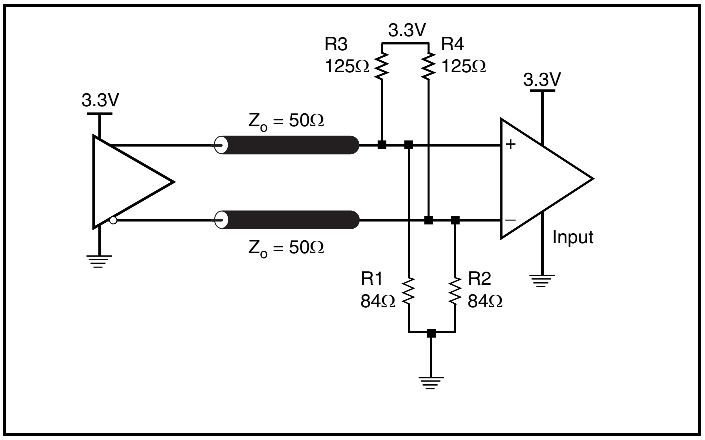


Figure 4B. 3.3V LVPECL Output Termination

Layout Guideline

Figure 4 shows a schematic example of the 843004. An example of LVEPCL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the LVPECL Termination Application Note. In this example, an 18 pF parallel resonant 26.5625MHz crystal is used. The C1= 27pF and C2 = 33pF are recommended for frequency accuracy. For a different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy.

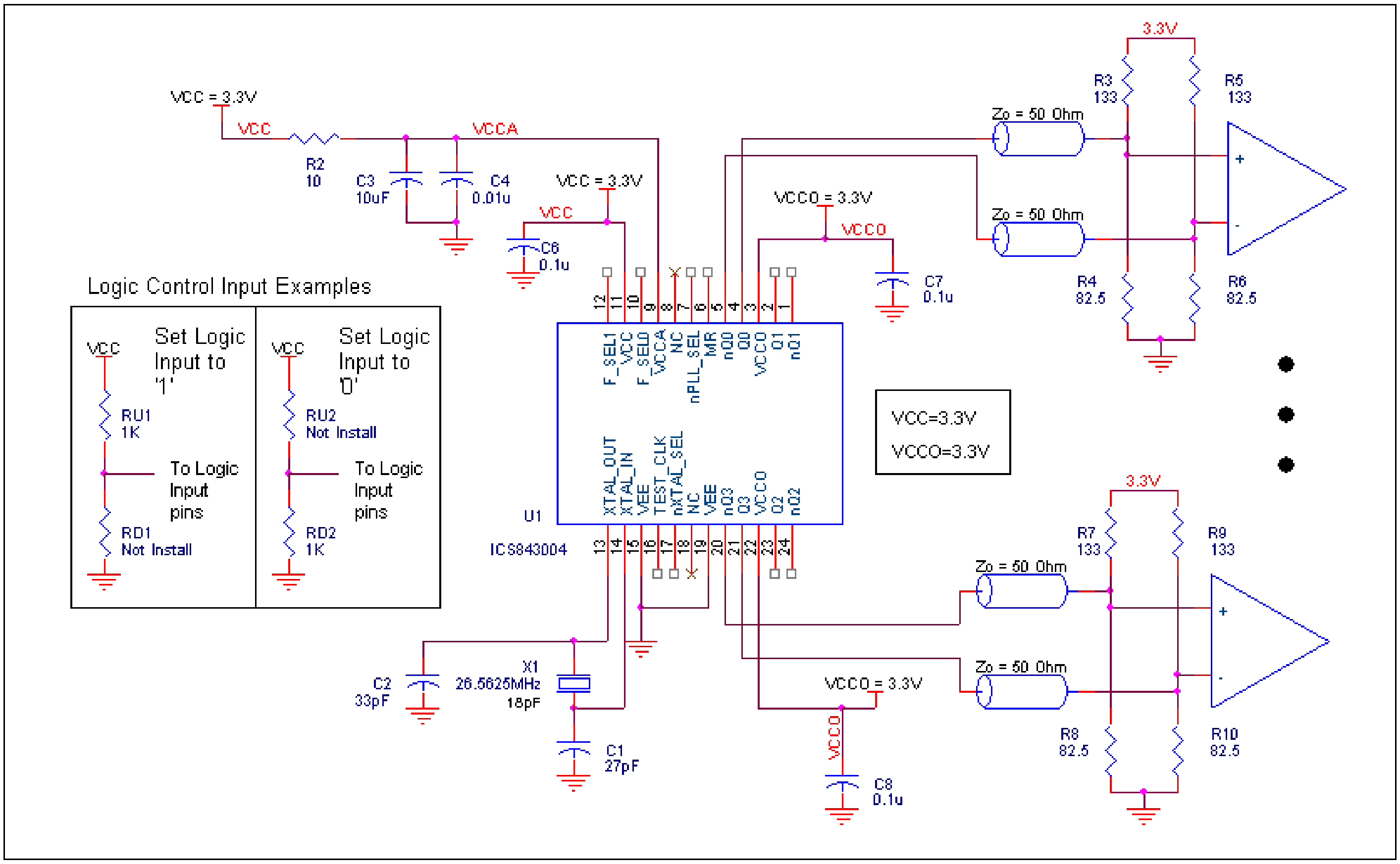


Figure 4. 843004 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 843004.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 843004 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 135mA = **467.8mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30mW = **120mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 467.8mW + 120mW = **587.8mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 6below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.588W * 65°C/W = 123.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

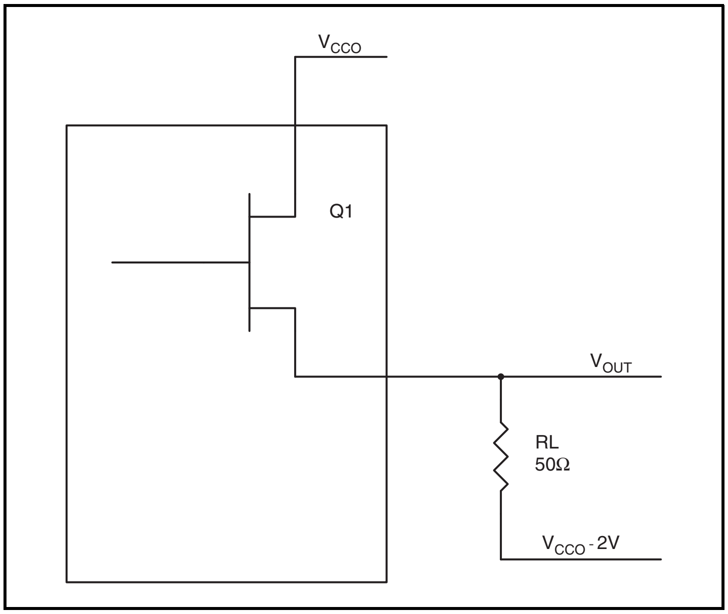


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$
  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{COO\_MAX} - 1.7V}$
  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

Transistor Count

The transistor count for 843004 is: 2578

Package Outline and Package Dimension

Package Outline - G Suffix for 24 Lead TSSOP

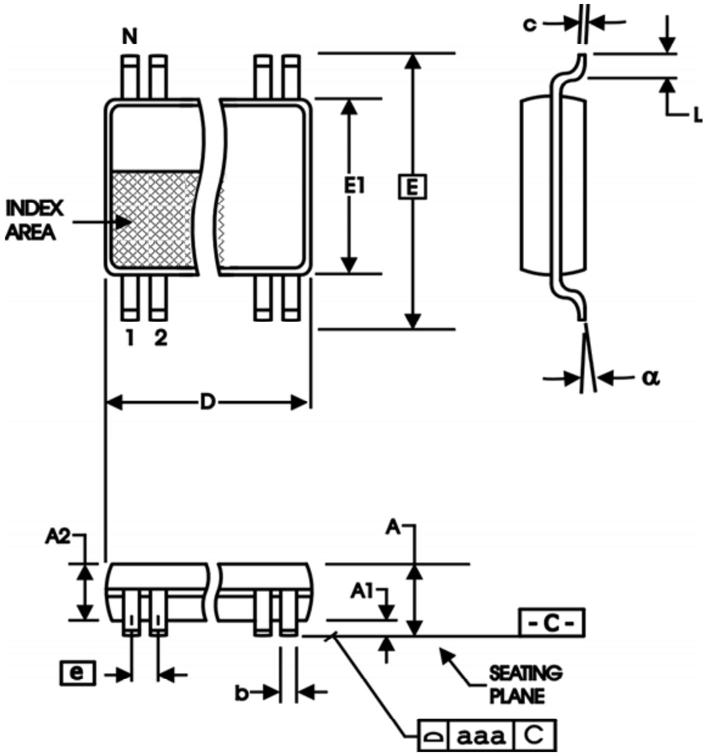


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843004AGLF	ICS843004AGL	"Lead-Free" 24 Lead TSSOP	Tube	-30°C to 85°C
843004AGLFT	ICS843004AGL	"Lead-Free" 24 Lead TSSOP	2500 Tape & Reel	-30°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		1	Added 187.5MHz to the Frequency Selection Function Table.	8/26/04
A		10	Added Schematic Layout.	11/18/04
A	 T9	1 15	Features Section - added Lead-Free bullet. Ordering Information Table - added Lead-Free part number.	3/21/05
B	T5	4	AC Characteristics Table - deleted Propagation Delay row.	5/5/05
C	T3B	3 11 12 14	LVCMOS/LVTTL DC Characteristics Table - corrected IIL spec. from -150µA min. to -5µA min. Added *Recommendations for Unused Input and Output Pins* section. Added *LVCMOS to XTAL Interface* section. Corrected Figure 4, Schematic Example, Pin 18 from V_{CC} to nc.	3/4/08
C	T5	1 4 20	Frequency Select Function Table - corrected F_SEL0 column, last 2 rows. AC Characteristics Table - Added Thermal Note. Contact Information - Updated	1/19/09
C	 T9	 18	Updated data sheet format. Ordering Information - Removed leaded devices.	5/26/15

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