

## N-channel 650 V, 0.061 $\Omega$ typ., 22.5 A MDmesh™ M5 Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data

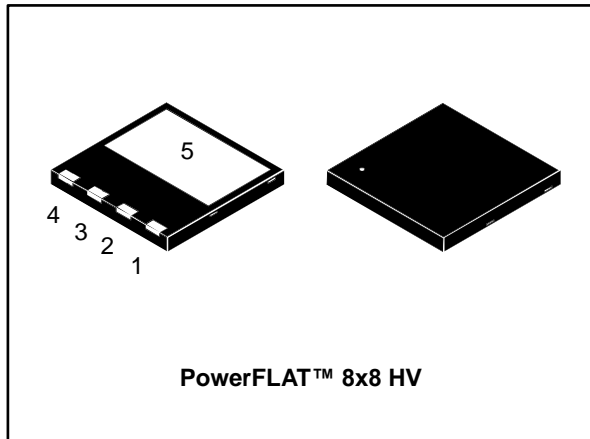
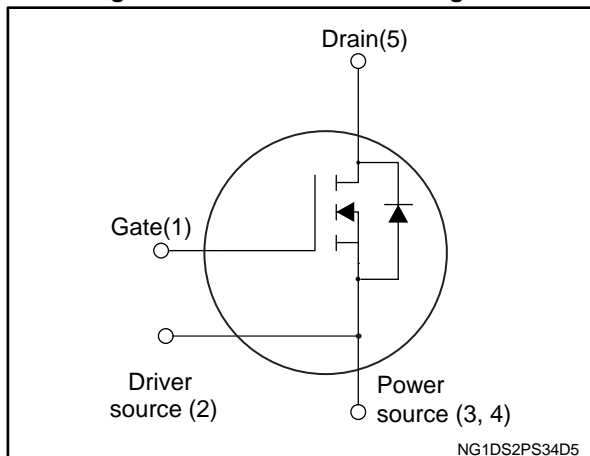


Figure 1: Internal schematic diagram



### Features

Order code	$V_{DS}$ @ $T_{Jmax}$	$R_{DS(on)}$ max.	$I_D$
STL57N65M5	710 V	0.069 $\Omega$	22.5 A

- Extremely low  $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STL57N65M5	57N65M5	PowerFLAT™ 8x8 HV	Tape and reel

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	650	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	22.5	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	22	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	90	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.3	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	2.7	A
$P_{TOT}^{(3)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	2.8	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	189	W
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_j$ max)	9	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	960	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	°C
$T_j$	Max. operating junction temperature	150	

**Notes:**

- (1) The value is rated according to  $R_{thj-case}$  rated and limited by package.  
 (2) Pulse width limited by safe operating area.  
 (3) When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu.  
 (4)  $I_{SD} \leq 22.5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.66	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	45	°C/W

**Notes:**

- (1) When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu.

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 4: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	650			V
$I_{DSS}$	Zero gate voltage Drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$ , $T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{GS} = \pm 25\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 17.5\text{ A}$		0.061	0.069	$\Omega$

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	4200	-	pF
$C_{oss}$	Output capacitance		-	100	-	pF
$C_{riss}$	Reverse transfer capacitance		-	6	-	pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ to }80\%$ $V_{(BR)DSS}$	-	97	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related		-	344	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	1.4	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}$ , $I_D = 17.5\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15: "Gate charge test circuit"</a> )	-	96	-	nC
$Q_{gs}$	Gate-source charge		-	24	-	nC
$Q_{gd}$	Gate-drain charge		-	40	-	nC

**Notes:**

<sup>(1)</sup> $C_{o(er)}$  is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

<sup>(2)</sup> $C_{o(tr)}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 400 \text{ V}$ , $I_D = 22.5 \text{ A}$ $R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$ (see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> and <a href="#">Figure 19: "Switching time waveform"</a> )	-	84	-	ns
$t_{r(V)}$	Voltage rise time		-	10.8	-	ns
$t_{f(i)}$	Crossing fall time		-	11	-	ns
$t_{C(off)}$	Crossing time		-	16.5	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		22.5	A
$I_{SDM}^{(1),(2)}$	Source-drain current (pulsed)		-		90	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0 \text{ V}$ , $I_{SD} = 22.5 \text{ A}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 22.5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 100 \text{ V}$ (see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )	-	378		ns
$Q_{rr}$	Reverse recovery charge		-	7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	37		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 22.5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 100 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )	-	454		ns
$Q_{rr}$	Reverse recovery charge		-	9.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	42		A

**Notes:**

<sup>(1)</sup>The value is rated according to  $R_{thj-case}$  and limited by package.

<sup>(2)</sup>Pulse width is limited by safe operating area

<sup>(3)</sup>Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

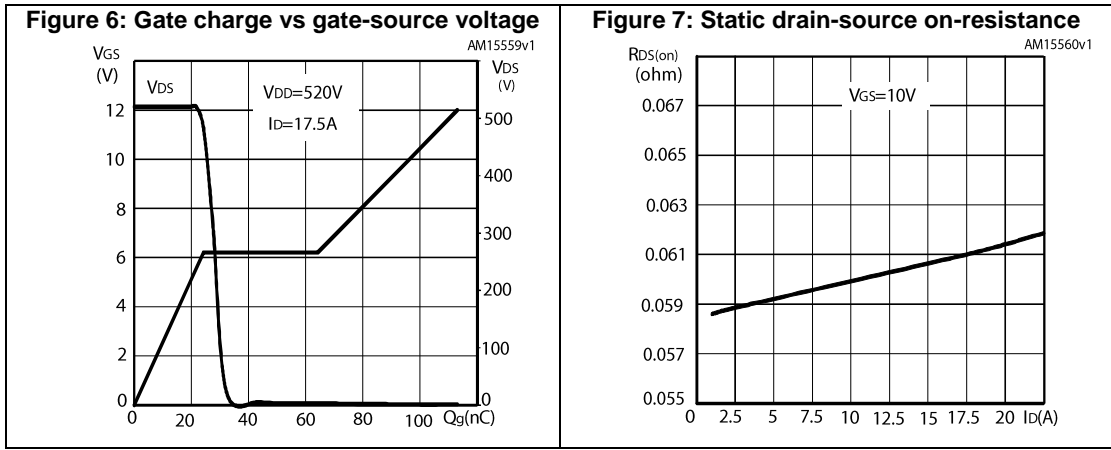
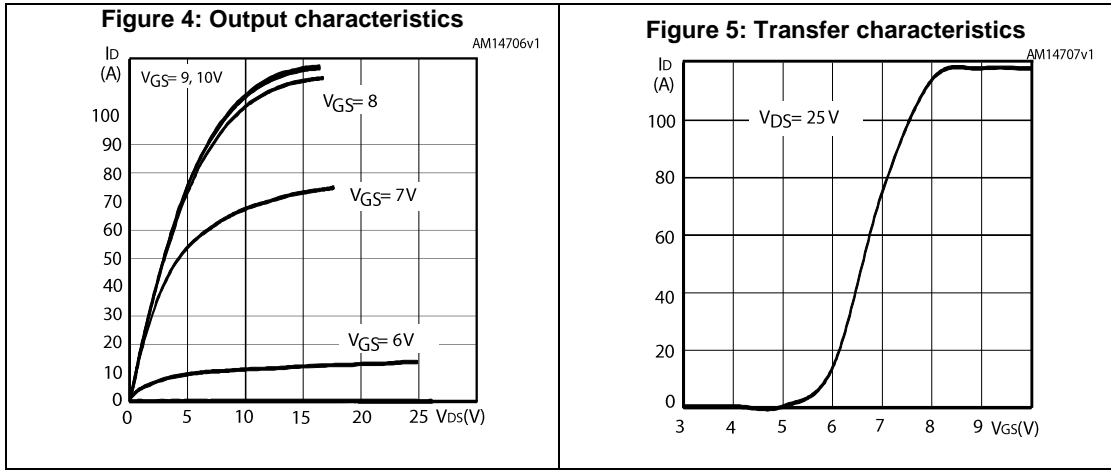
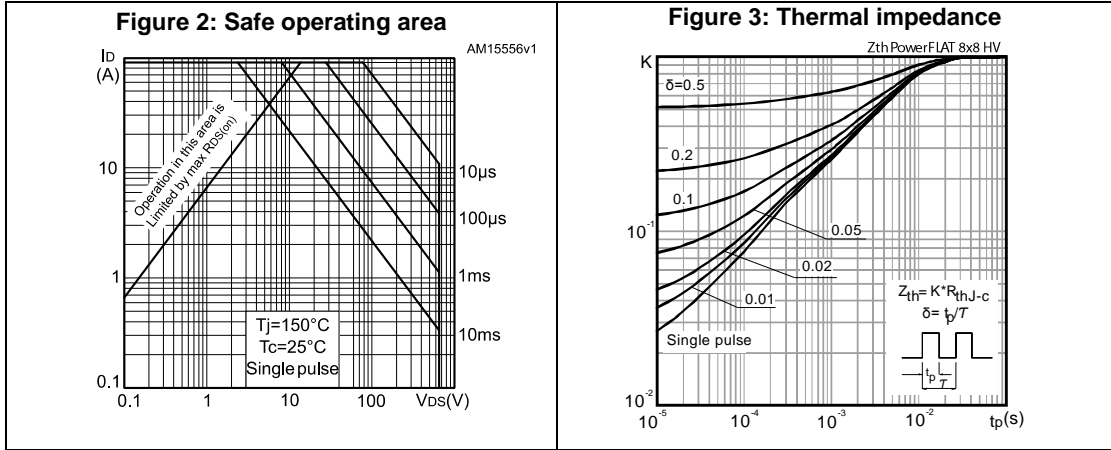


Figure 8: Capacitance variations

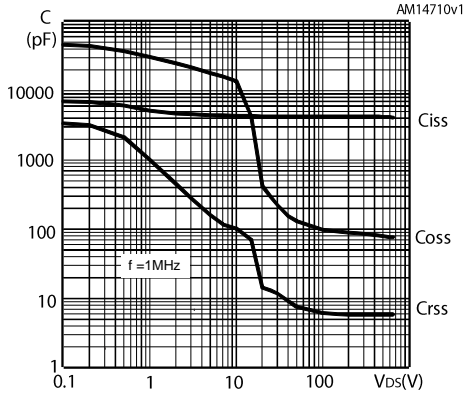


Figure 9: Normalized gate threshold voltage vs temperature

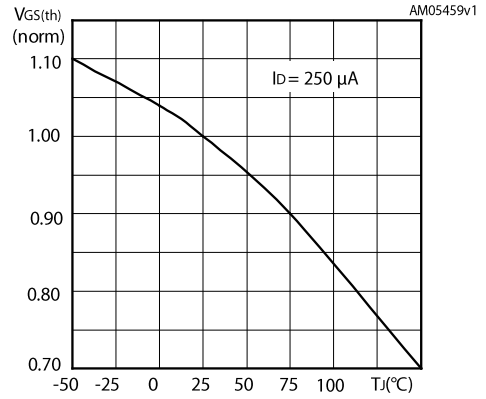


Figure 10: Normalized on-resistance vs temperature

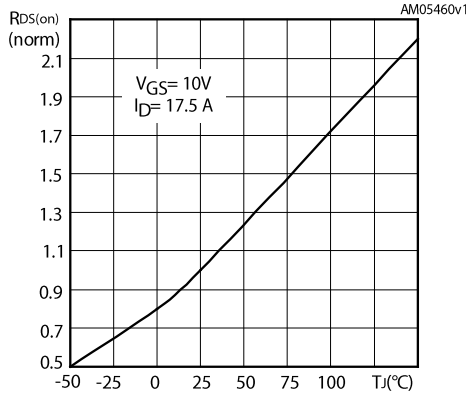


Figure 11: Normalized V(BR)DSS vs temperature

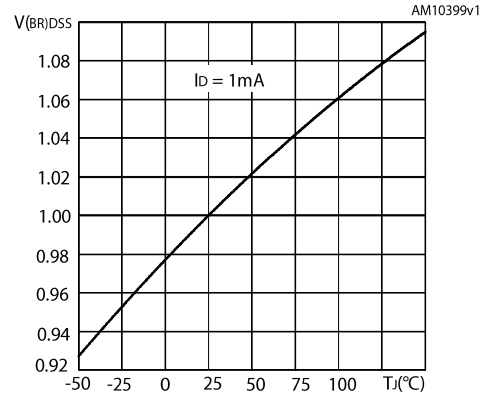


Figure 12: Output capacitance stored energy

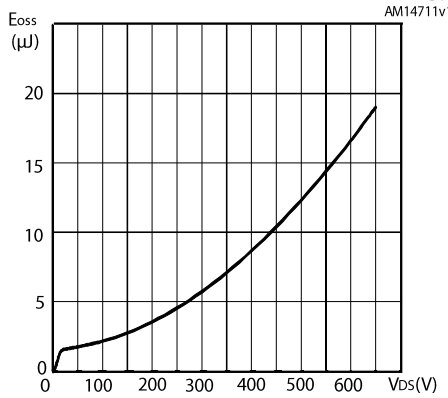
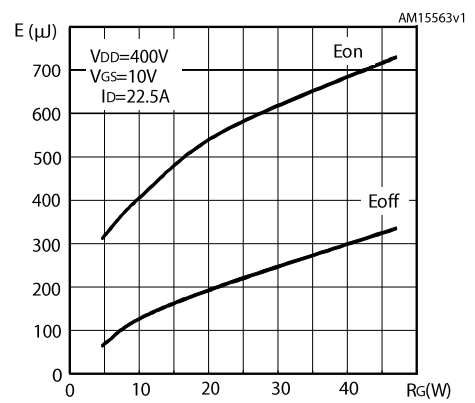


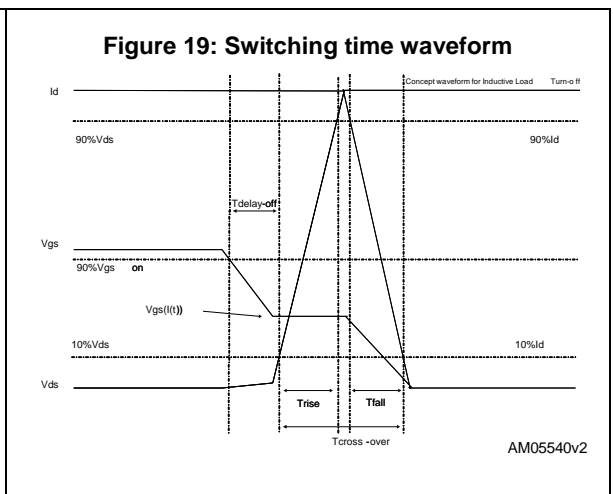
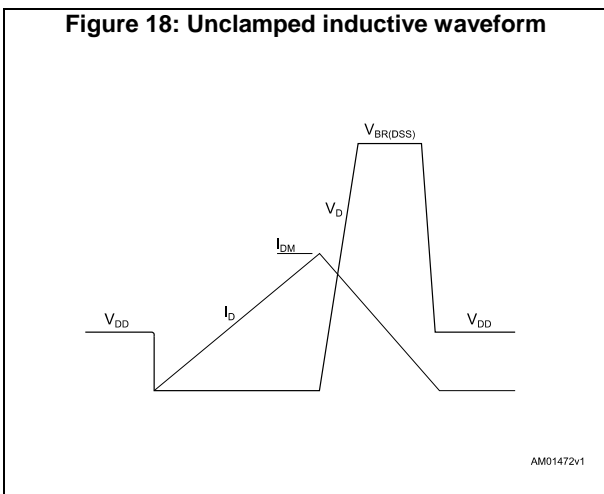
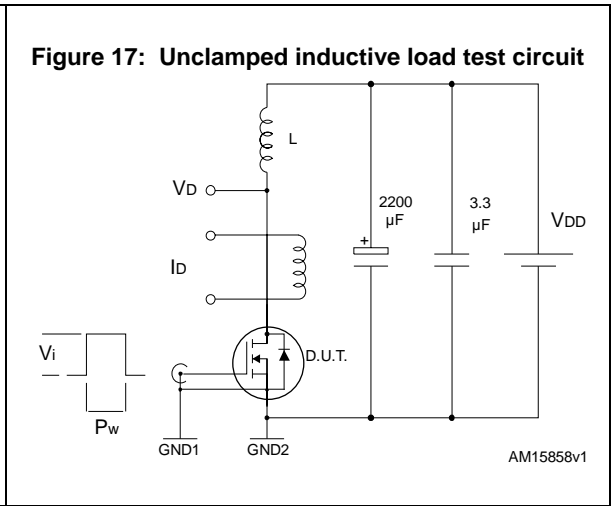
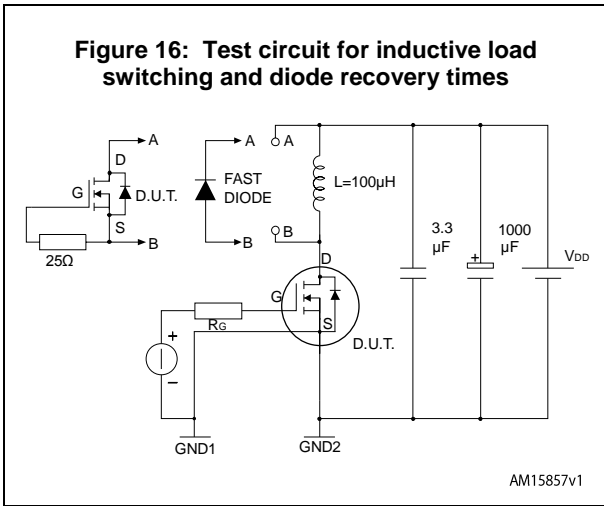
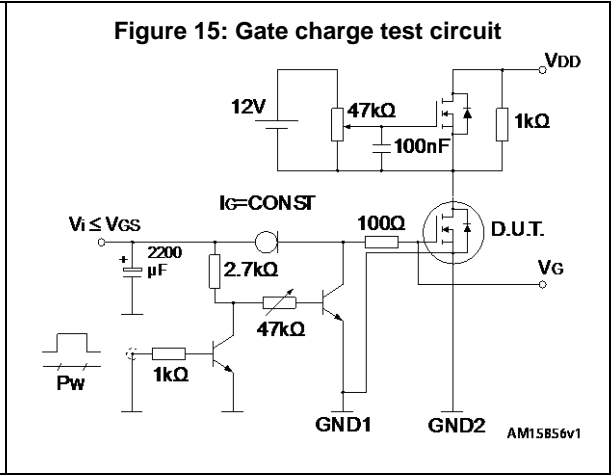
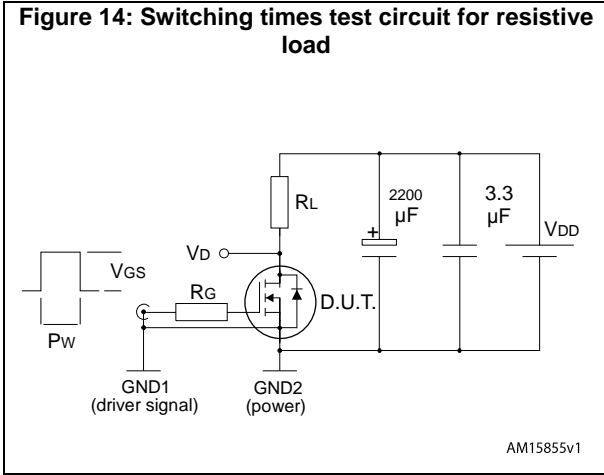
Figure 13: Switching losses vs gate resistance



The previous figure  $E_{on}$  includes reverse recovery of a SiC diode.



### 3 Test circuits

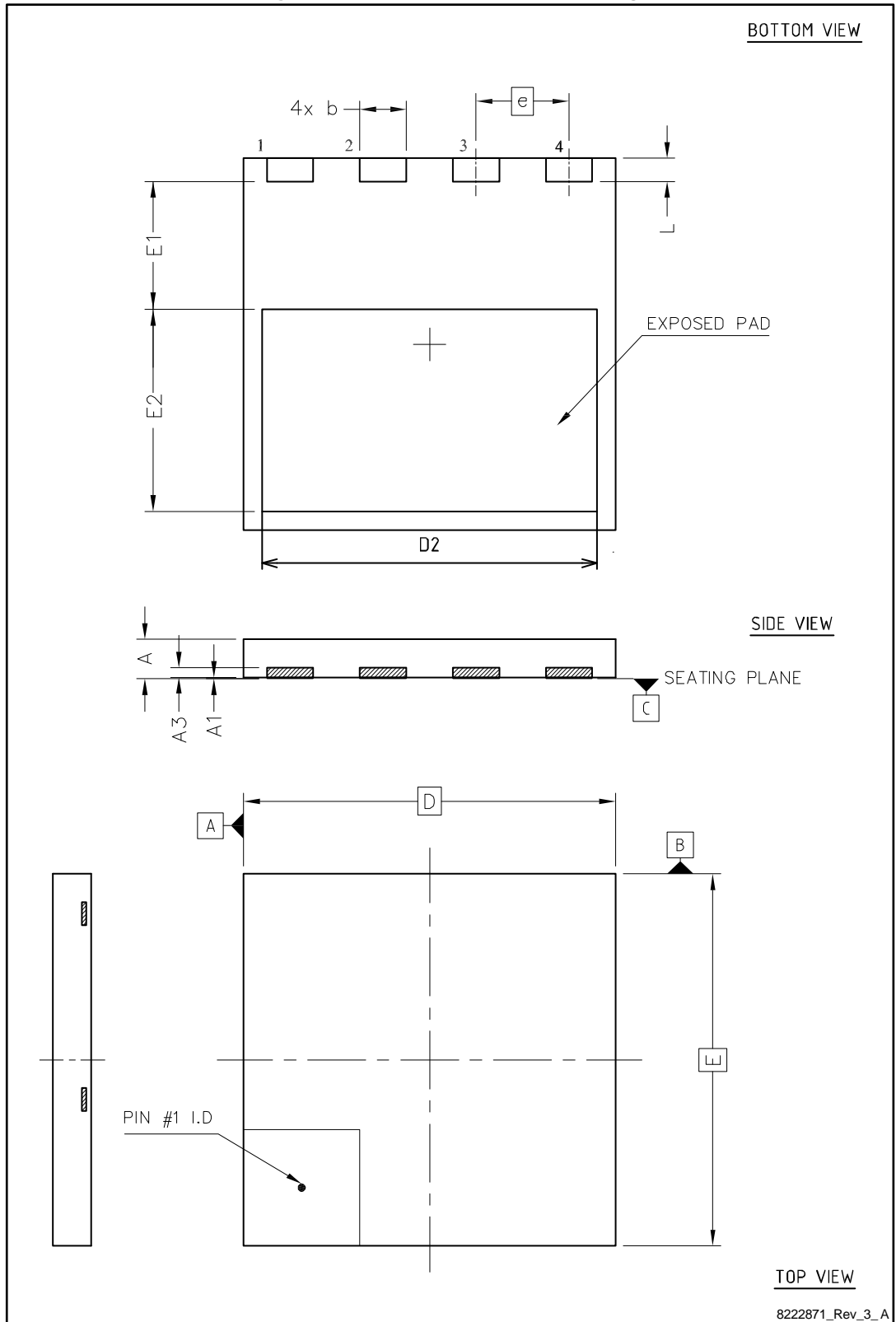


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 PowerFLAT™ 8x8 HV package information

Figure 20: PowerFLAT™ 8x8 HV drawing

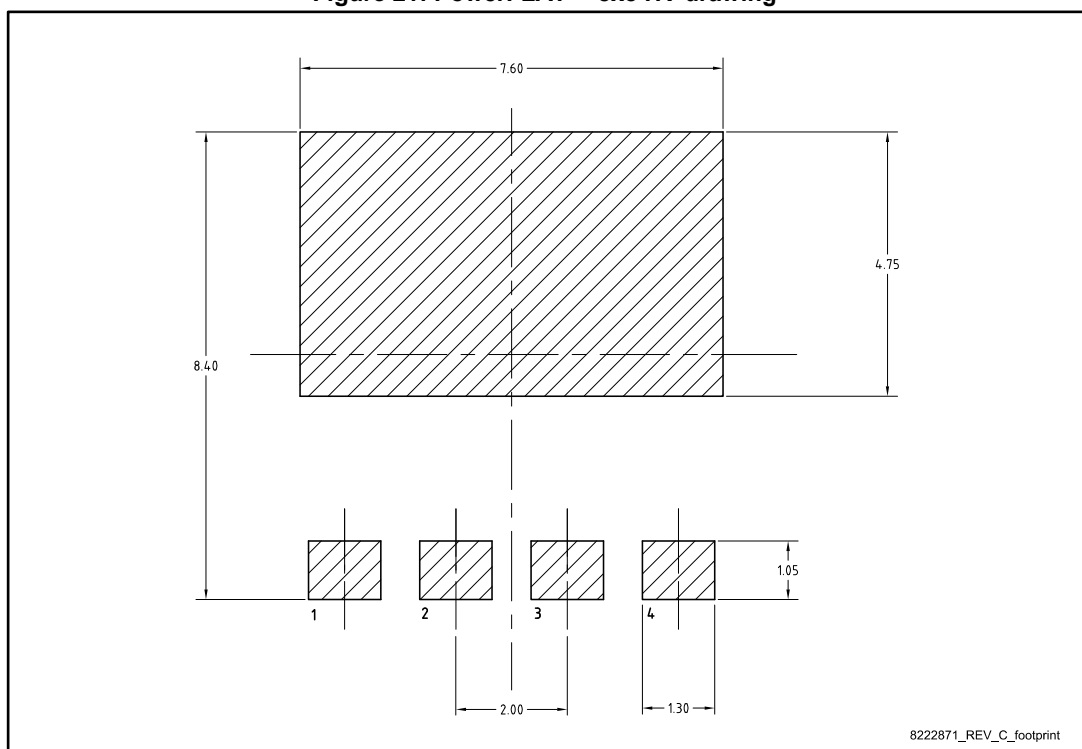


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Table 8: PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00	
L	0.40	0.50	0.60

Figure 21: PowerFLAT™ 8x8 HV drawing



All dimensions are in millimeters.

### 4.2 PowerFLAT™ 8x8 HV packing information

Figure 22: PowerFLAT™ 8x8 HV tape

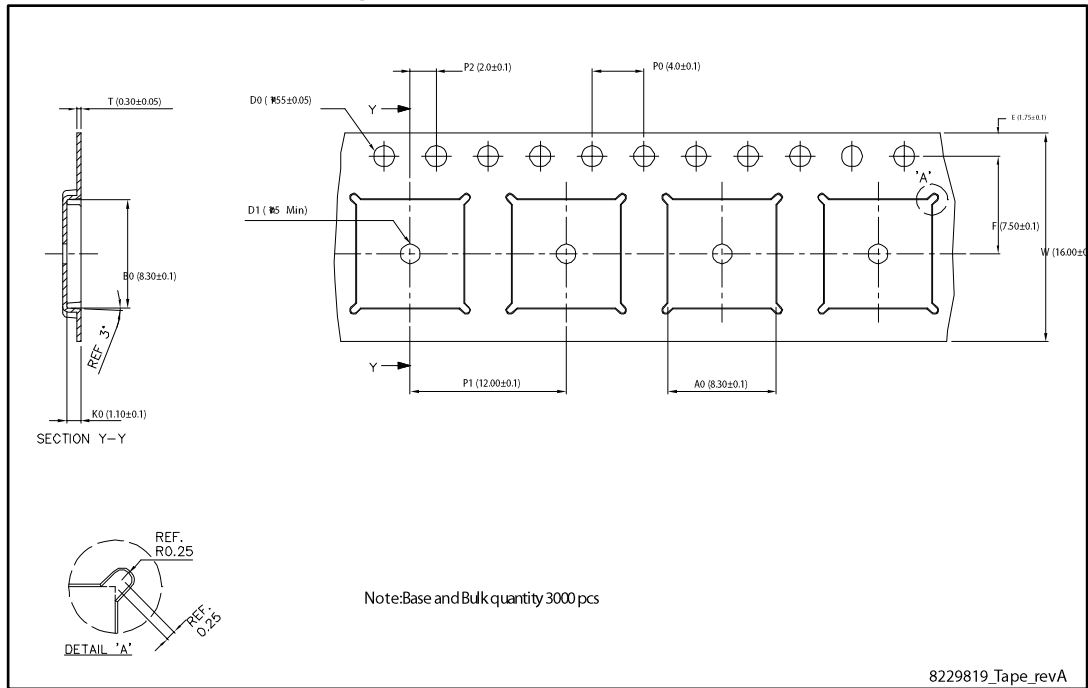


Figure 23: PowerFLAT™ 8x8 HV package orientation in carrier tape

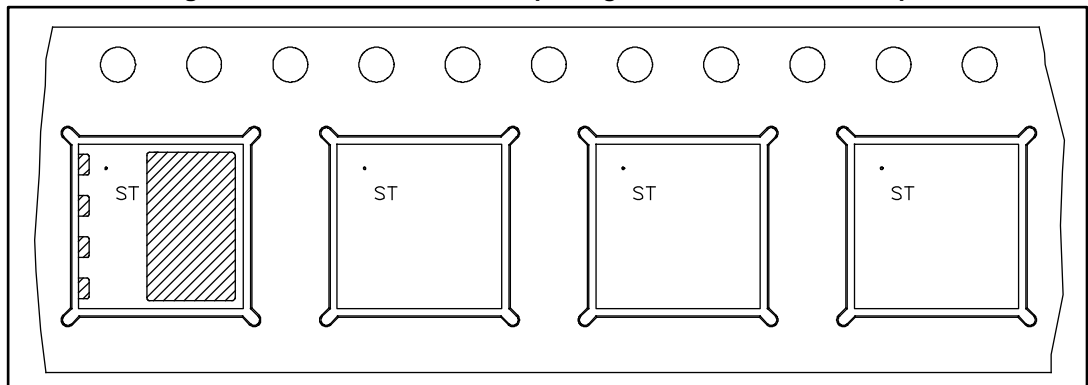
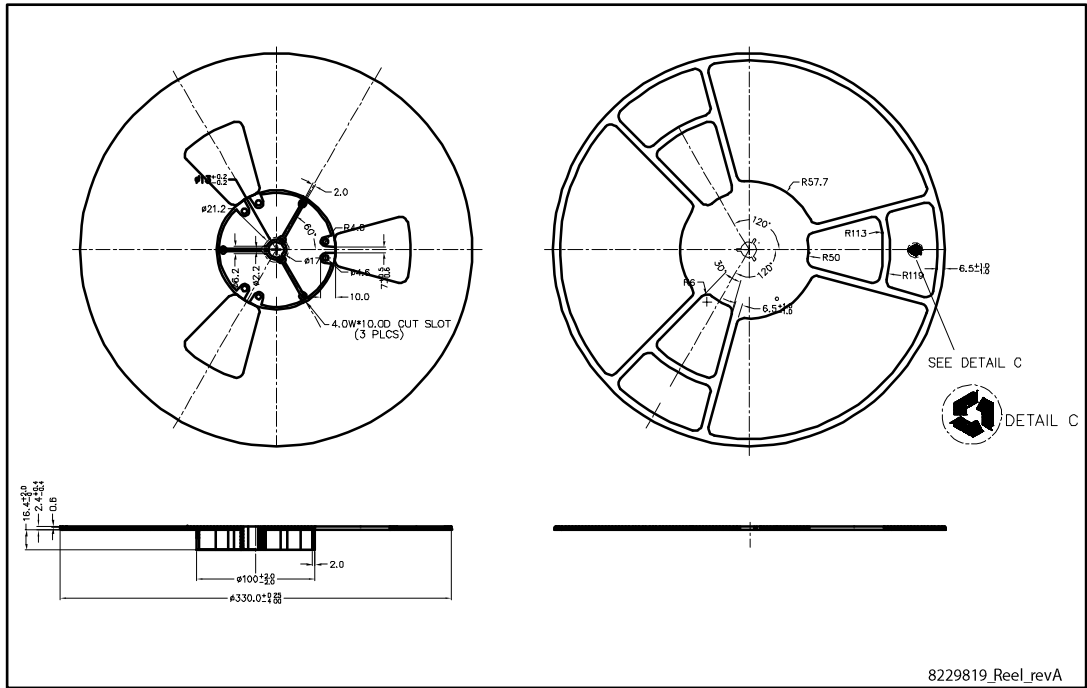


Figure 24: PowerFLAT™ 8x8 HV reel



8229819\_Reel\_revA

## 5 Revision history

Table 9: Document revision history

Date	Revision	Changes
14-May-2012	1	First release.
25-Jan-2013	2	<ul style="list-style-type: none"> <li>-Modified ID value and note 1 on first page</li> <li>-Modified: <math>I_D</math>, <math>P_{TOT}</math>, <math>I_{AR}</math> values, and note 1, 4 on Table 2</li> <li>-Modified: Rthj-case value on Table 3</li> <li>-Modified: <math>R_{DS(on)}</math> on Table 4</li> <li>-Modified: typical values on Table 5 and 6</li> <li>-Modified: typical and max values on Table 7</li> <li>-Inserted: Section 2.1: Electrical characteristics (curves)</li> <li>-Document status promoted from preliminary data to production data.</li> </ul>
09-Oct-2015	3	<p>Updated title, features and description Text and formatting changes throughout document.</p> <p>Updated <a href="#">Section 1: "Electrical ratings"</a> and <a href="#">Section 2: "Electrical characteristics"</a></p> <p>Changes according to PCN9187:</p> <p>Updated package silhouette and figure <a href="#">Figure 1: "Internal schematic diagram"</a> on cover page.</p> <p>Updated <a href="#">Section 4.1: "PowerFLAT™ 8x8 HV package information"</a>.</p>

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