BURR - BROWN®

OPA633

High Speed BUFFER AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 260MHz
- HIGH SLEW RATE: 2500V/μs
- HIGH OUTPUT CURRENT: 100mA
- LOW OFFSET VOLTAGE: 1.5mV
- REPLACES HA-5033
- IMPROVED PERFORMANCE/PRICE: LH0033, LTC1010, H0S200

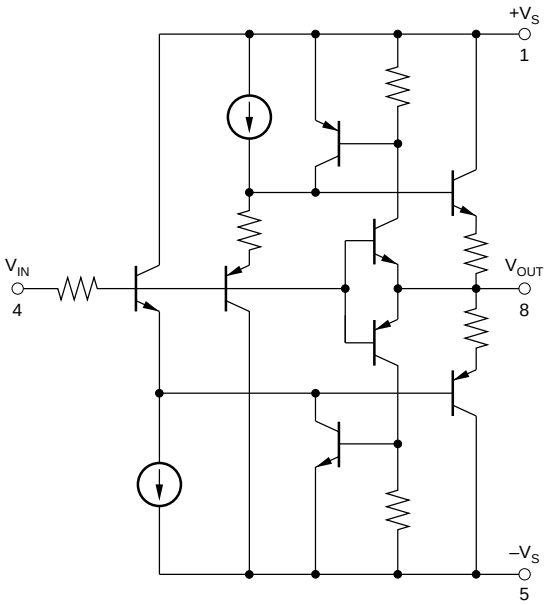
APPLICATIONS

- OP AMP CURRENT BOOSTER
- VIDEO BUFFER
- LINE DRIVER
- A/D CONVERTER INPUT BUFFER

DESCRIPTION

The OPA633 is a monolithic unity-gain buffer amplifier featuring very wide bandwidth and high slew rate. A dielectric isolation process incorporating both NPN and PNP high frequency transistors achieves performance unattainable with conventional integrated circuit technology. Laser trimming provides low input offset voltage.

High output current capability allows the OPA633 to drive 50Ω and 75Ω lines, making it ideal for RF, IF and video applications. Low phase shift allows the OPA633 to be used inside amplifier feedback loops. OPA633 is available in a low cost plastic DIP package specified for 0°C to +75°C operation.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-699B
Printed in U.S.A. October, 1993

SPECIFICATIONS

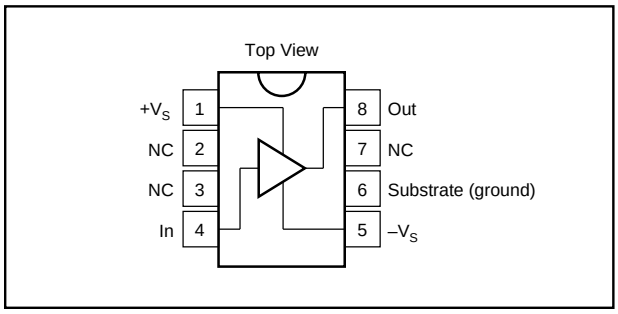
ELECTRICAL

At +25°C, V_S = ±12V, R_S = 50Ω, R_L = 100Ω, and C_L = 10pF, unless otherwise specified.

PARAMETER	CONDITIONS	OPA633KP MIN	OPA633KP TYP	OPA633KP MAX	UNITS
FREQUENCY RESPONSE					
Small Signal Bandwidth			260		MHz
Full Power Bandwidth	V_O = 1Vrms, R_L = 1kΩ		40		MHz
Slew Rate	V_O = 10V, V_S = ±15V, R_L = 1kΩ	1000	2500		V/µs
Rise Time, 10% to 90%	V_O = 500mV		2.5		ns
Propagation Delay			1		ns
Overshoot			10		%
Settling Time, 0.1%			50		ns
Differential Phase Error [1]			0.1		Degrees
Differential Gain Error [1]			0.1		%
Total Harmonic Distortion	V_O = 1Vrms, R_L = 1kΩ, f = 100kHz		0.005		%
	V_O = 1Vrms, R_L = 100Ω, f = 100kHz		0.02		%
OUTPUT CHARACTERISTICS					
Voltage	$T_A = T_{MIN}$ to T_{MAX}	±8	±10		V
	R_L = 1kΩ, V_S = ±15V	±11	±13		V
Current		±80	±100		mA
Resistance			5		Ω
TRANSFER CHARACTERISTICS					
Gain		0.93	0.95		V/V
	R_L = 1kΩ		0.99		V/V
	$T_A = T_{MIN}$ to T_{MAX}	0.92	0.95		V/V
INPUT					
Offset Voltage	T_A = +25°C		±5	±15	mV
	$T_A = T_{MIN}$ to T_{MAX}		±6	±25	mV
vs Temperature			±33		µV/°C
vs Supply	$T_A = T_{MIN}$ to T_{MAX}	54	72		dB
Bias Current	T_A = +25°C		±15	±35	µA
	$T_A = T_{MIN}$ to T_{MAX}		±20	±50	µA
Noise Voltage	10Hz to 1MHz		20		µVp-p
Resistance			1.5		MΩ
Capacitance			1.6		pF
POWER SUPPLY					
Rated Supply Voltage	Specified Performance		±12		V
Operating Supply Voltage	Derated Performance	±5		±16	V
Current, Quiescent	I_O = 0		21	25	mA
	I_O = 0, $T_A = T_{MIN}$ to T_{MAX}		21	30	mA
TEMPERATURE RANGE					
Specification, Ambient		0		+75	°C
Operating, Ambient		–25		+85	°C
θ Junction, Ambient			90		°C/W

NOTE: (1) Differential phase error in video transmission systems is the change in phase of a color subcarrier resulting from a change in picture signal from blanked to white. Differential gain error is the change in amplitude at the color subcarrier frequency resulting from a change in picture signal from blanked to white.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply, ±V_S	±20V
Input Voltage V_{IN}	+V_S + 2V to –V_S – 2V
Output Current (peak)	±200mA
Internal Power Dissipation (25°C)	1.95W
Junction Temperature	200°C
Storage Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	300°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA633KP	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

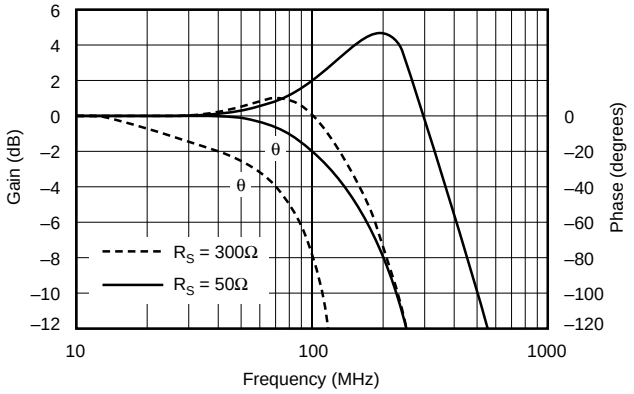
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA633KP	8-Pin Plastic DIP	0°C to +75°C

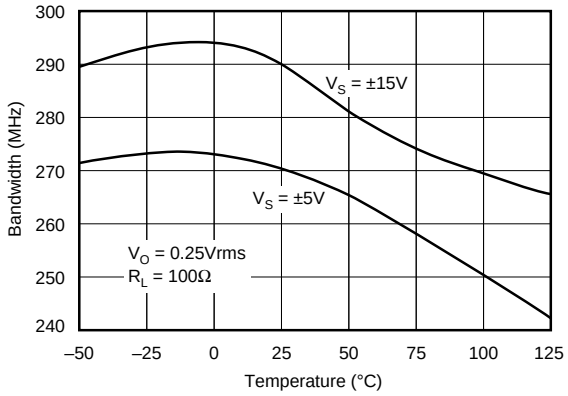
TYPICAL PERFORMANCE CURVES

At +25°C, V_S = ±12V, R_S = 50Ω, R_L = 100Ω, and C_L = 10pF, unless otherwise specified.

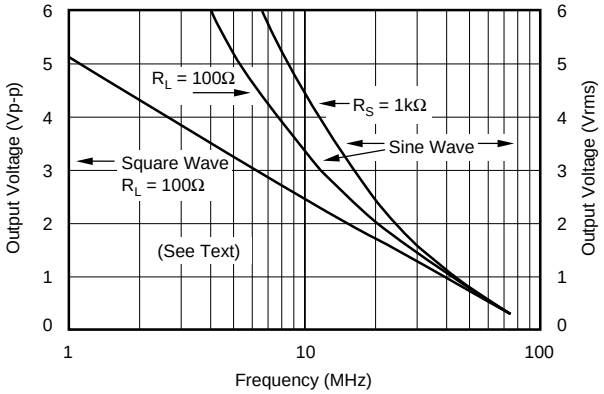
GAIN/PHASE vs FREQUENCY



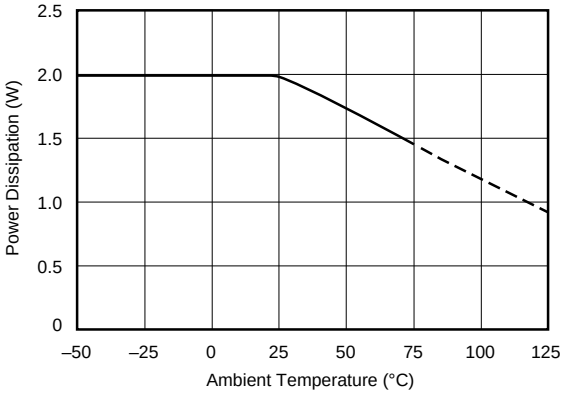
SMALL SIGNAL BANDWIDTH vs TEMPERATURE



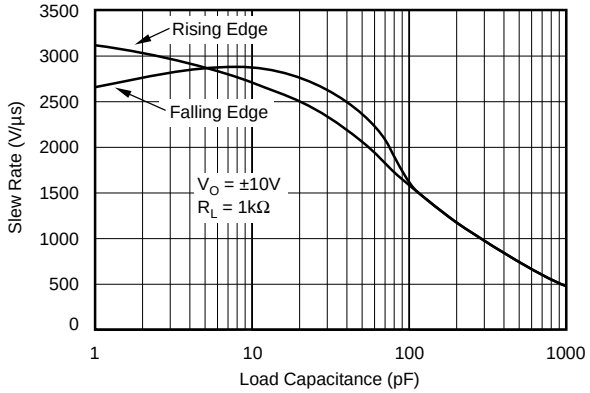
SAFE INPUT VOLTAGE vs FREQUENCY



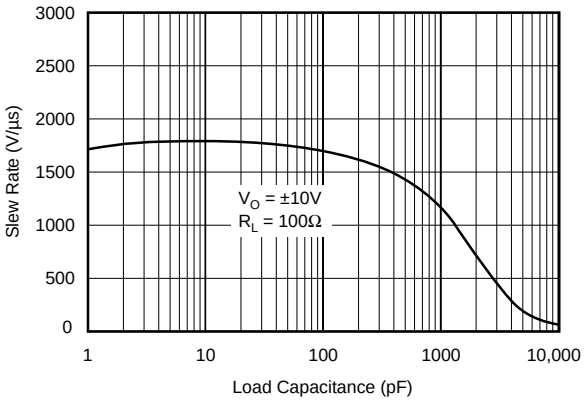
MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



SLEW RATE vs LOAD CAPACITANCE



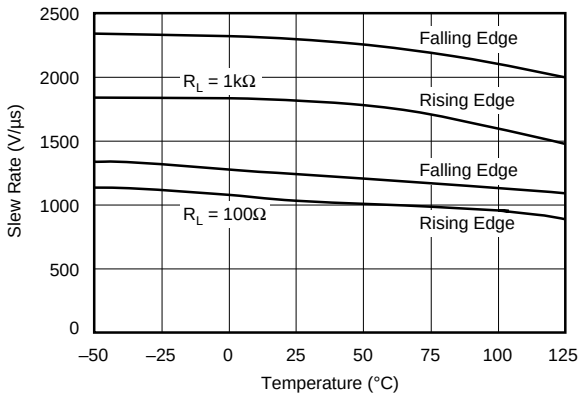
SLEW RATE vs LOAD CAPACITANCE



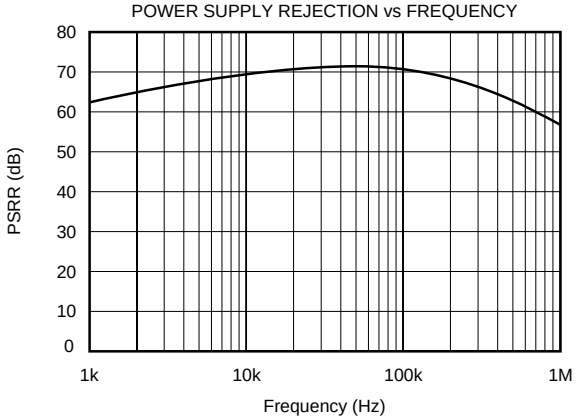
TYPICAL PERFORMANCE CURVES (CONT)

At +25°C, V_S = ±12V, R_S = 50Ω, R_L = 100Ω, and C_L = 10pF, unless otherwise specified.

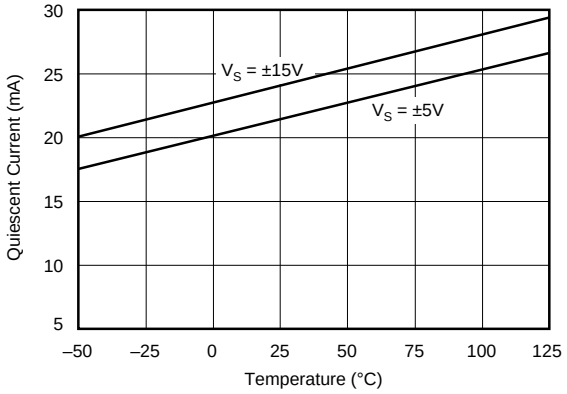
SLEW RATE vs TEMPERATURE



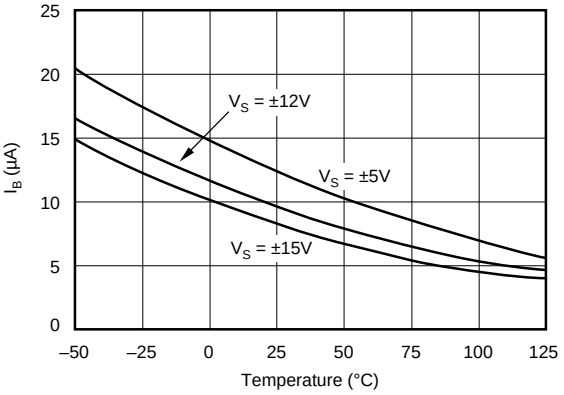
POWER SUPPLY REJECTION vs FREQUENCY



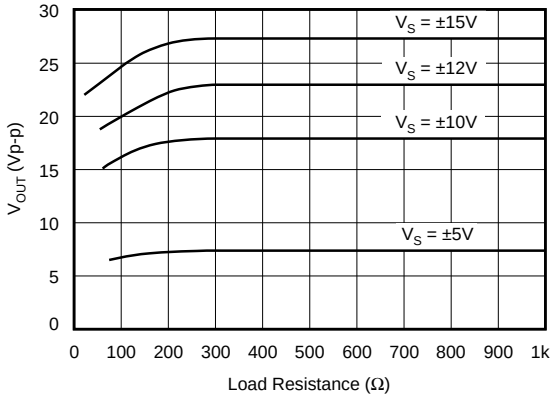
QUIESCENT CURRENT vs TEMPERATURE



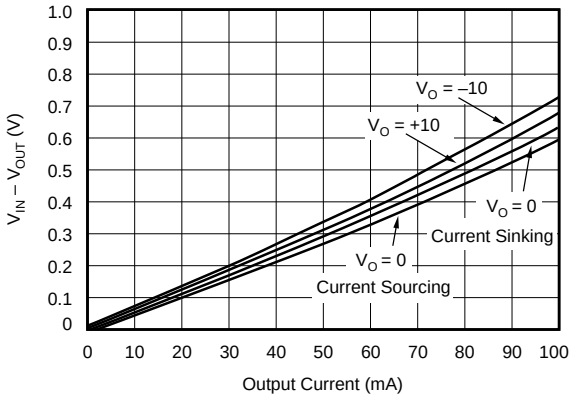
INPUT BIAS CURRENT vs TEMPERATURE



OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



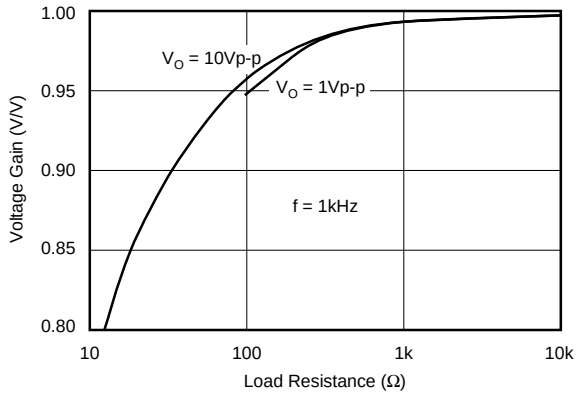
$V_{IN} – V_{OUT}$ vs OUTPUT CURRENT



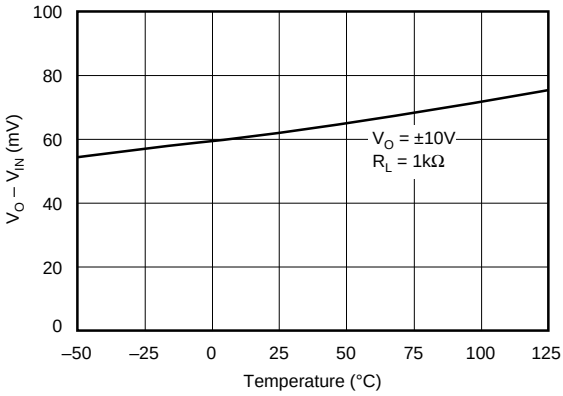
TYPICAL PERFORMANCE CURVES (CONT)

At +25°C, V_S = ±12V, R_S = 50Ω, R_L = 100Ω, and C_L = 10pF, unless otherwise specified.

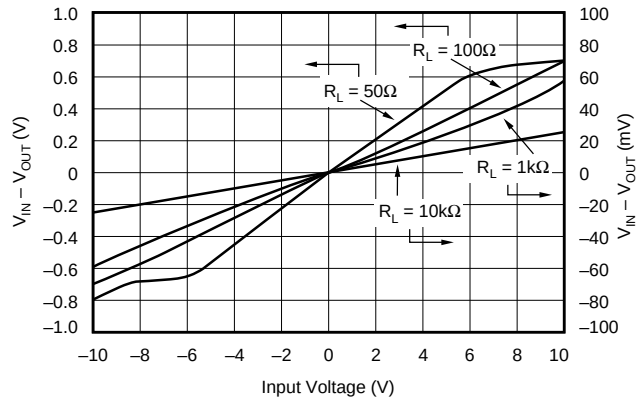
VOLTAGE GAIN vs LOAD RESISTANCE



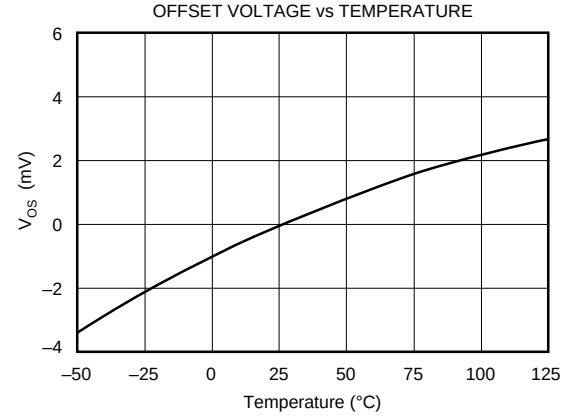
GAIN ERROR vs TEMPERATURE



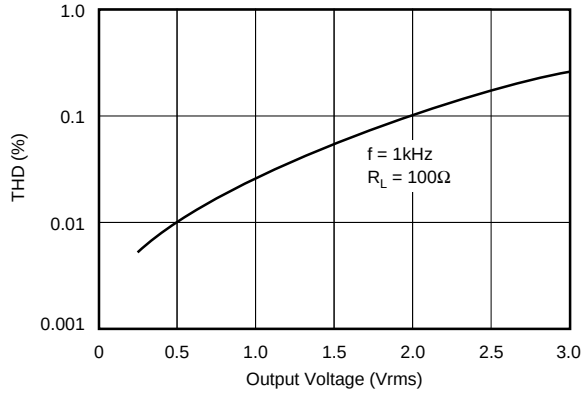
OUTPUT ERROR vs INPUT VOLTAGE



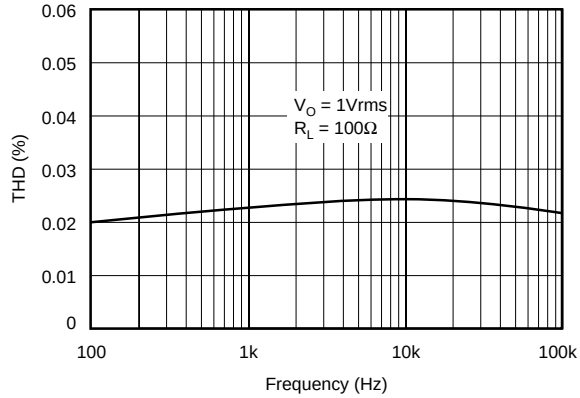
OFFSET VOLTAGE vs TEMPERATURE



TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGE



TOTAL HARMONIC DISTORTION vs FREQUENCY



APPLICATIONS INFORMATION

As with any high frequency circuitry, good circuit layout technique must be used to achieve optimum performance. Power supply connections must be bypassed with high frequency capacitors. Many applications benefit from the use of two capacitors on each power supply—a ceramic capacitor for good high frequency decoupling and a tantalum type for lower frequencies. They should be located as close as possible to the buffer's power supply pins. A large ground plane is used to minimize high frequency ground drops and stray coupling.

Pin 6 connects to the substrate of the integrated circuit and should be connected to ground. In principle it could also be connected to $+V_S$ or $-V_S$, but ground is preferable. The additional lead length and capacitance associated with sockets may cause problems in applications requiring the highest fidelity of high speed pulses.

Depending on the nature of the input source impedance, a series input resistor may be required for best stability. This behavior is influenced somewhat by the load impedance (including any reactive effects). A value of 50Ω to 200Ω is typical. This resistor should be located close to the OPA633's input pin to avoid stray capacitance at the input which could reduce bandwidth (see Gain and Phase versus Frequency curve).

OVERLOAD CONDITIONS

The input and output circuitry of the OPA633 are not protected from overload. When the input signal and load characteristics are within the devices's capabilities, no protection circuitry is required. Exceeding device limits can result in permanent damage.

The OPA633's small package and high output current capability can lead to overheating. The internal junction temperature should not be allowed to exceed 150°C. Although failure is unlikely to occur until junction temperature exceeds 200°C, reliability of the part will be degraded significantly at such high temperatures. Since significant heat transfer takes place through the package leads, wide printed circuit traces to all leads will improve heat sinking. Sockets reduce heat transfer significantly and are not recommended.

Junction temperature rise is proportional to internal power dissipation. This can be reduced by using the minimum supply voltage necessary to produce the required output voltage swing. For instance, 1V video signals can be easily handled with ±5V power supplies thus minimizing the internal power dissipation.

Output overloads or short circuits can result in permanent damage by causing excessive output current. The 50Ω or 75Ω series output resistor used to match line impedance will, in most cases, provide adequate protection. When this resistor is not used, the device can be protected by limiting the power supply current. See "Protection Circuits."

Excessive input levels at high frequency can cause increased internal dissipation and permanent damage. See the safe input voltage versus frequency curves. When used to buffer an op amp's output, the input to the OPA633 is limited, in most cases, by the op amp. When high frequency inputs can exceed safe levels, the device must be protected by limiting the power supply current.

PROTECTION CIRCUITS

The OPA633 can be protected from damage due to excessive currents by the simple addition of resistors in series with the power supply pins (Figure 5a). While this limits output current, it also limits voltage swing with low impedance loads. This reduction in voltage swing is minimal for AC or high crest factor signals since only the average current from the power supply causes a voltage drop across the series resistor. Short duration load-current peaks are supplied by the bypass capacitors.

The circuit of Figure 5b overcomes the limitations of the previous circuit with DC loads. It allows nearly full output voltage swing up to its current limit of approximately 140mA. Both circuits require good high frequency capacitors (e.g., tantalum) to bypass the buffer's power supply connections.

CAPACITIVE LOADS

The OPA633 is designed to safely drive capacitive loads up to 0.01µF. It must be understood, however, that rapidly changing voltages demand large output load currents:

$$I_{LOAD} = C_{LOAD} \frac{dV}{dt}$$

Thus, a signal slew rate of 1000V/µs and load capacitance of 0.01µF demands a load current of 10A. Clearly maximum slew rates cannot be combined with large capacitive loads. Load current should be kept less than 100mA continuous (200mA peak) by limiting the rate of change of the input signal or reducing the load capacitance.

USE INSIDE A FEEDBACK LOOP

The OPA633 may be used inside the feedback path of an op amp such as the OPA602. Higher output current is achieved without degradation in accuracy. This approach may actually improve performance in precision applications by removing load-dependent dissipation from a precision op amp. All vestiges of load-dependent offset voltage and temperature drift can be eliminated with this technique. Since the buffer is placed within the feedback loop of the op amp, its DC errors will have a negligible effect on overall accuracy. Any DC errors contributed by the buffer are divided by the loop gain of the op amp.

The low phase shift of the OPA633 allows its use inside the feedback loop of a wide variety of op amps. To assure stability, the buffer must not add significant phase shift to the loop at the gain crossing frequency of the circuit—the frequency at which the open loop gain of the op amp is equal to the closed loop gain of the application. The OPA633 has a typical phase shift of less than 10° up to 70MHz, thus making it useful even with wideband op amps.

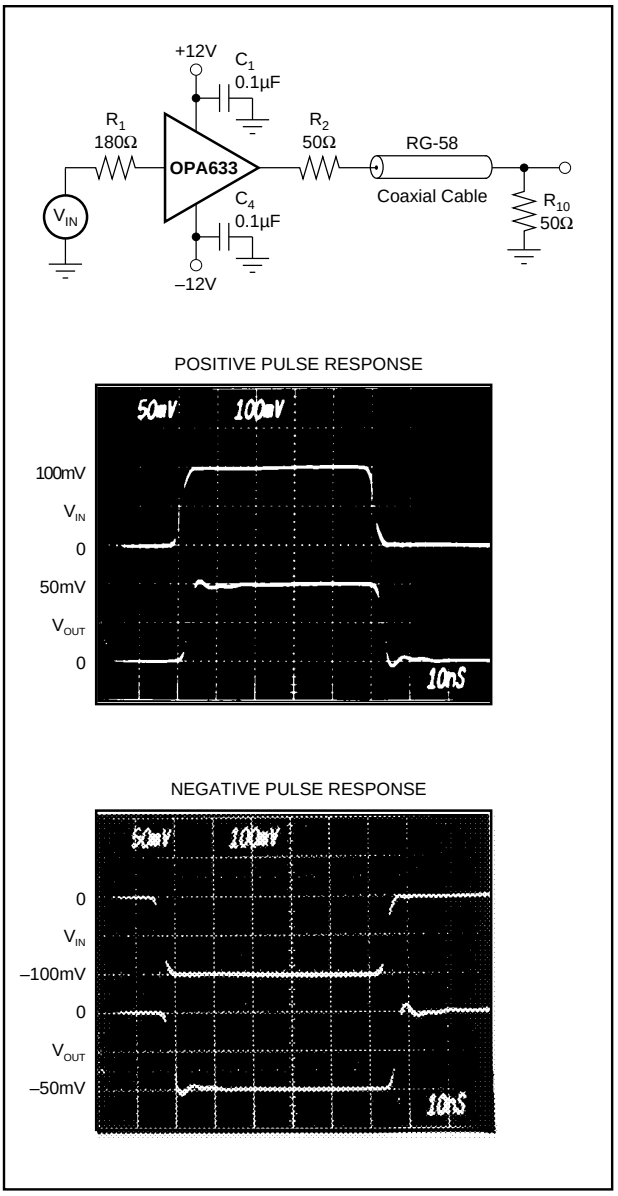


FIGURE 1. Coaxial Cable Driver Circuit.

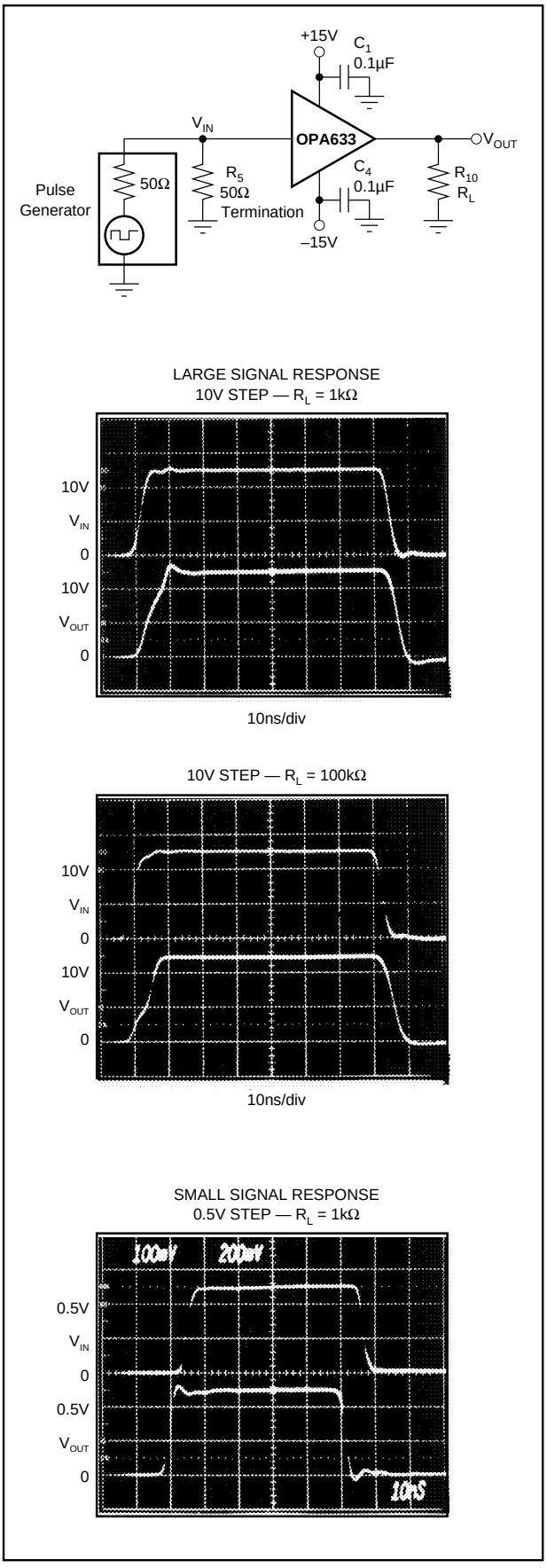


FIGURE 2. Dynamic Response Test Circuit.

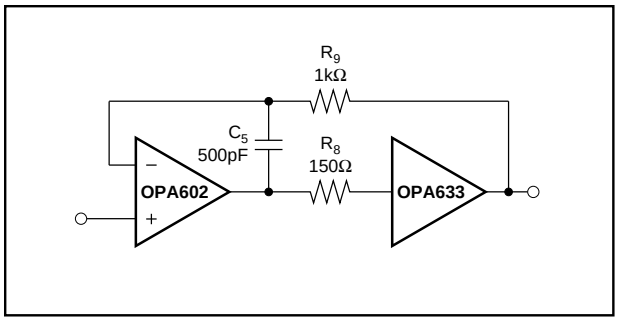


FIGURE 3. Precision High Current Buffer.

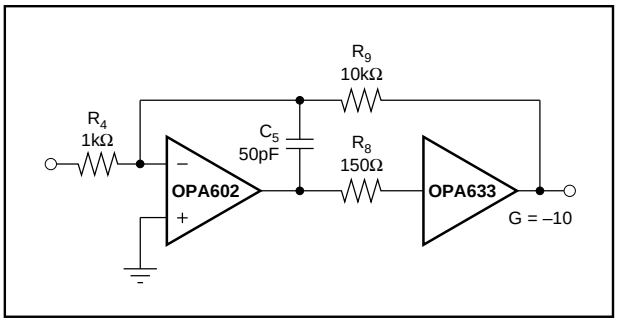


FIGURE 4. Buffered Inverting Amplifier.

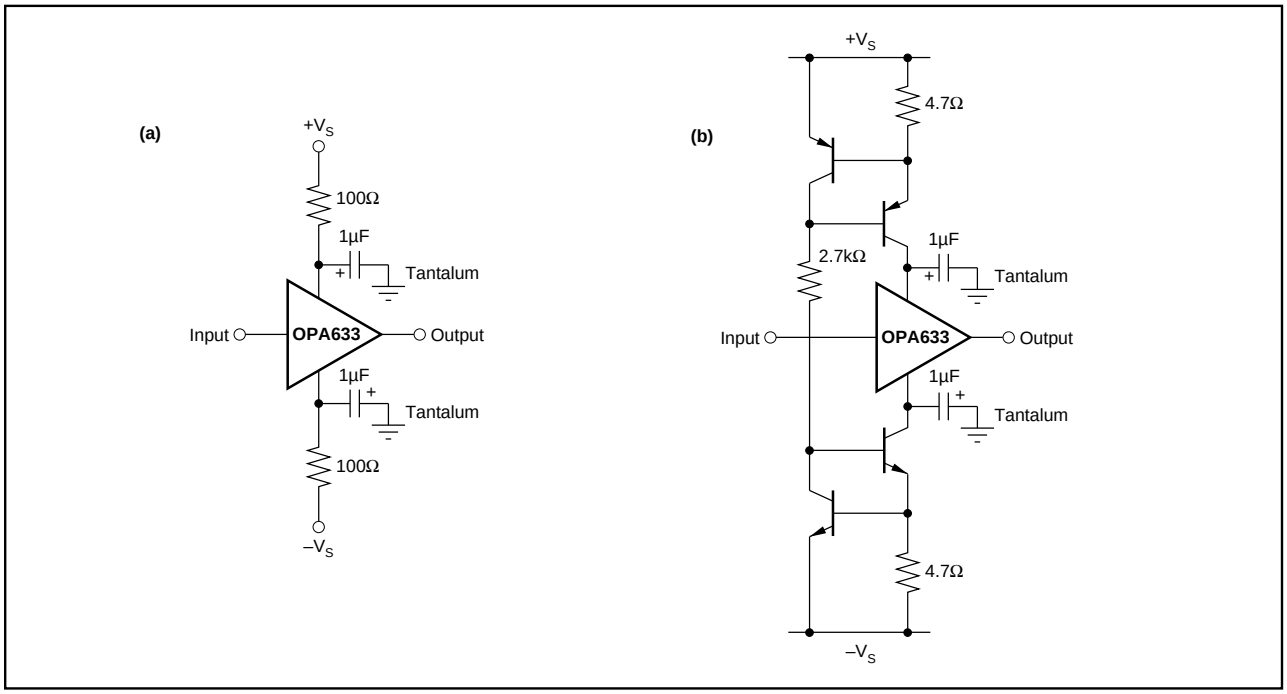


FIGURE 5. Output Protection Circuits.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.