# 8-Bit Addressable Latch 1-of-8 Decoder with LSTTL Inputs

# **High-Performance Silicon-Gate CMOS**

The MC74HCT259A is identical in pinout to the LS259. The device inputs are compatible with standard CMOS and LSTTL outputs.

The HCT259A has four modes of operation as shown in the mode selection table. In the addressable latch mode, the data on Data In is written into the addressed latch. The addressed latch follows the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one-of-eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode all outputs are LOW and unaffected by the address and data inputs. When operating the HCT259A as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

#### **Features**

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- These are Pb-Free Devices



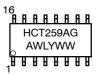
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## MARKING DIAGRAMS



SOIC-16 D SUFFIX CASE 751B





TSSOP-16 DT SUFFIX CASE 948F

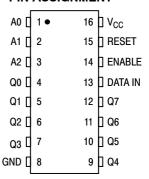


A = Assembly Location

WL, L = Wafer Lot YY, Y = Year WW, W = Work Week G or = Pb-Free Package

(Note: Microdot may be in either location)

#### **PIN ASSIGNMENT**



#### **MODE SELECTION TABLE**

Enable	Reset	Mode
L	Н	Addressable Latch
Н	Н	Memory
L	L	8-Line Demultiplexer
Н	L	Reset

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

#### 4 Q0 5 Q1 **ADDRESS INPUTS** 6 Q2 7 Q3 **NONINVERTING** 9 Q4 **OUTPUTS** 10 <sub>Q5</sub> DATA IN 13 11 Q6 12 Q7 RESET PIN 16 = V<sub>CC</sub> ENABLE 14 PIN 8 = GND

Figure 1. Logic Diagram

#### **LATCH SELECTION TABLE**

Address Inputs					
С	В	Α	Latch Addressed		
L	L	L	Q0		
L	LLHH		Q1		
L	L   H   L		Q2		
L	Н	Н	Q3		
Н	L	L	Q4		
Н	L	Н	Q5		
Н			Q6		
Н	Н	Н	Q7		

## **MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
l <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, SOIC Package TSSOP Package	500 450	mW
T <sub>stg</sub>	Storage Temperature	-65 to + 150	°C
V <sub>ESD</sub>	ESD Withstand Voltage Human Body Model (Note 1) Machine Model (Note 2)	>2000 >200	V
I <sub>Latchup</sub>	Latchup Performance Above V <sub>DD</sub> and Below GND at 125°C (Note 3)	±100	mA

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Tested to EIA / JESD22-A114-A.
- 2. Tested to EIA / JESD22-A115-A.
- 3. Tested to EIA / JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Symbol Parameter		Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)		5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 2)	0	500	ns

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Gu	aranteed Li	mit	
Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	– 55 to 25°C	≤ <b>85</b> °C	≤ 125°C	Unit
V <sub>IH</sub>	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20  \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \le 20  \mu\text{A}$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IH} \text{ or } V_{IL} \qquad  I_{out}  \le 5.2 \text{ mA}$	4.5	3.98	3.84	3.70	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL} $ $ I_{out}  \le 5.2 \text{ mA}$	4.5	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5	± 0.1	± 1.0	± 1.0	μΑ
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	5.5	4	40	160	μΑ
$\Delta I_{CC}$	Additional Quiescent Supply	V <sub>in</sub> = 2.4V, Any One Input		≥ <b>-55°C</b>	25 to	125°C	
	Ourient	$V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0\mu A$	5.5	2.9	2	.4	mA

# AC ELECTRICAL CHARACTERISTICS (V $_{CC}$ = 4.5 to 5.5 V, $C_L$ = 50 pF, Input $t_r$ = $t_f$ = 6 ns)

		Guaranteed Limit			
Symbol	Parameter	–55 to 25°C	≤ <b>85</b> °C	≤ 125°C	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Data to Output (Figures 2 and 7)	32	32	42	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Address Select to Output (Figures 3 and 7)	32	40	45	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Enable to Output (Figures 4 and 7)	32	40	45	ns
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Output (Figures 5 and 7)	22	26	32	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 2 and 7)	15	19	22	ns
C <sub>in</sub>	Maximum Input Capacitance	10	10	10	pF

		Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
$C_{PD}$	Power Dissipation Capacitance (Per Package)	30	pF

## TIMING REQUIREMENTS (V<sub>CC</sub> = 4.5 to 5.5 V, Input $t_r$ = $t_f$ = 6 ns)

		Gu	Guaranteed Limit			
Symbol	Parameter	–55 to 25°C	≤ <b>85</b> °C	≤ 125°C	Unit	
t <sub>su</sub>	Minimum Setup Time, Address or Data to Enable (Figure 6)	15	19	22	ns	
t <sub>h</sub>	Minimum Hold Time, Enable to Address or Data (Figure 6)	1	1	1	ns	
t <sub>w</sub>	Minimum Pulse Width, Reset or Enable (Figure 4 or 5)	15	19	22	ns	

## **SWITCHING WAVEFORMS**

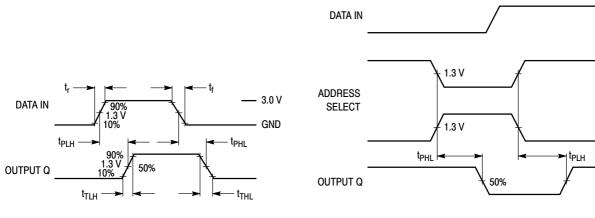


Figure 2.

Figure 3.

\_ 3.0V

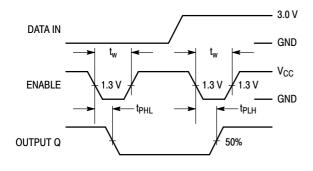
— GND

- 3.0V

— GND

— 3.0V

- GND





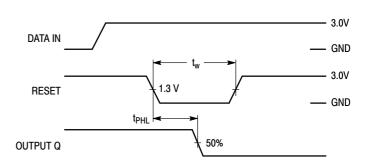


Figure 5.

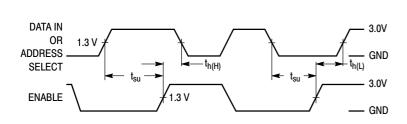
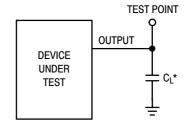


Figure 6.



\*Includes all probe and jig capacitance

Figure 7. Test Circuit

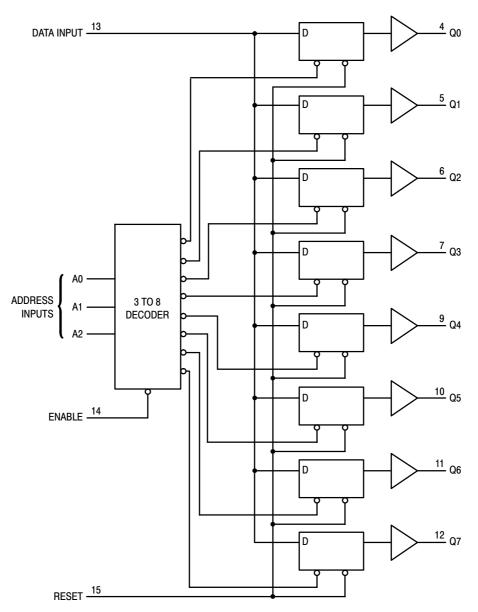


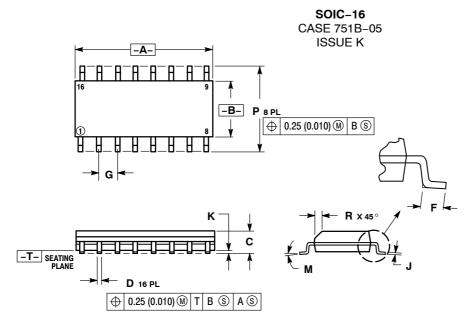
Figure 8. Expanded Logic Diagram

## **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC74HCT259ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HCT259ADR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74HCT259ADTR2G	TSSOP-16*	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
\*This package is inherently Pb-Free.

## **PACKAGE DIMENSIONS**



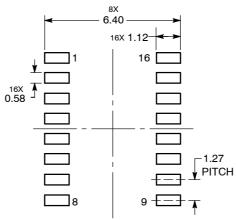
- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTECTION OF THE PROTECTION OF THE PROTECTION OF THE PROTECTION OF THE PROT

- DIMENSIONS A MAID B DO NOT INCLUDE MOLD PROTRUSION.

  MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	9.80	10.00	0.386	0.393	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	BSC	0.050 BSC		
J	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
M	0°	7°	0°	7°	
P	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.019	

## **SOLDERING FOOTPRINT\***

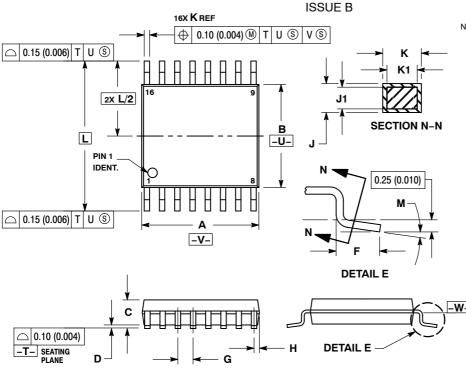


DIMENSIONS: MILLIMETERS

<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### PACKAGE DIMENSIONS

## TSSOP-16 **DT SUFFIX** CASE 948F-01

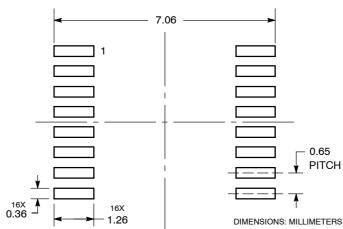


- NOTES:
  1. DIMENSIONING AND TOLERANCING PER

  - ANSI Y14.5M, 1982.
    2. CONTROLLING DIMENSION: MILLIMETER.
    3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS.
  - FLASH. PROTRUSIONS OR GATE BURRS.
    MOLD FLASH OR GATE BURRS SHALL NOT
    EXCEED 0.15 (0.006) PER SIDE.
    4. DIMENSION B DOES NOT INCLUDE
    INTERLEAD FLASH OR PROTRUSION.
    INTERLEAD FLASH OR PROTRUSION SHALL
    NOT EXCEED 0.25 (0.010) PER SIDE.
    5. DIMENSION K DOES NOT INCLUDE
    DAMBAR BROTTUSION ALL OWARLE
  - DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
    6. TERMINAL NUMBERS ARE SHOWN FOR
  - REFERENCE ONLY.
    7. DIMENSION A AND B ARE TO BE

	MILLIN	IETERS		HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026	BSC
Н	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40		0.252 BSC	
М	0 °	8°	0° 8°	

## **SOLDERING FOOTPRINT\***



\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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