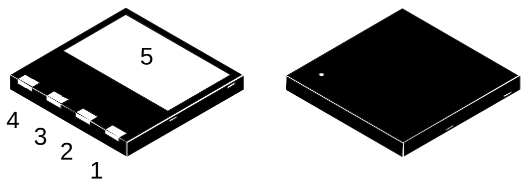
STL45N65M5

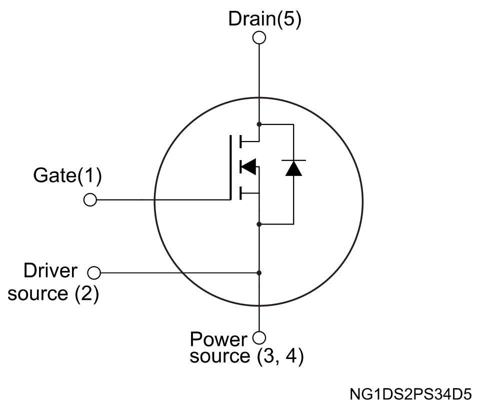
N-channel 650 V, 0.075 Ω typ., 22.5 A MDmesh™ M5 Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data



PowerFLAT™ 8x8 HV

Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ $T_{Jmax.}$	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL45N65M5	710 V	0.086 Ω	22.5 A	160 W

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STL45N65M5	45N65M5	PowerFLAT™ 8x8 HV	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	±25	V
I_D (1)	Drain current (continuous) at T_{case} = 25 °C	22.5	A
	Drain current (continuous) at T_{case} = 100 °C	18	
I_{DM} (1)(2)	Drain current (pulsed)	90	A
P_{TOT} (1)	Total dissipation at T_{case} = 25 °C	160	W
I_D (3)	Drain current (continuous) at T_{amb} = 25 °C	3.8	A
	Drain current (continuous) at T_{amb} = 100 °C	2.4	
P_{TOT} (3)	Total dissipation at T_{amb} = 25 °C	2.8	W
dv/dt (4)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Operating junction temperature		

Notes:

(1) The value is rated according to $R_{thj-case}$ and limited by package.

(2) Pulse width limited by safe operating area.

(3) When mounted on a 1-inch² FR-4, 2oz Cu board.

(4) I_{SD} ≤ 22.5 A, di/dt ≤ 400 A/µs, V_{DD} = 400 V, $V_{DS(peak)}$ < $V_{(BR)DSS}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.78	°C/W
$R_{thj-amb}$ (1)	Thermal resistance junction-ambient	45	

Notes:

(1) When mounted on a 1-inch² FR-4, 2oz Cu board.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} (1)	Avalanche current, repetitive or not repetitive	8	A
E_{AS} (2)	Single pulse avalanche energy	810	mJ

Notes:

(1) Pulse width limited by T_{jmax}.

(2) starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_{case} = 125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 14.5 A		0.075	0.086	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	3470	-	pF
C_{oss}	Output capacitance		-	82	-	
C_{rss}	Reverse transfer capacitance		-	7	-	
$C_{o(er)}$ (1)	Equivalent output capacitance energy related	V_{GS} = 0 V, V_{DS} = 0 to 520 V	-	79	-	pF
$C_{o(tr)}$ (2)	Equivalent output capacitance time related		-	280	-	
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	2	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 17.5 A, V_{GS} = 10 V (see *Figure 16: "Gate charge test circuit"*)	-	82	-	nC
Q_{gs}	Gate-source charge		-	18.5	-	
Q_{gd}	Gate-drain charge		-	35	-	

Notes:

(1) Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

(2) Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 22.5 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 20: "Switching time waveform"*)	-	79.5	-	ns
$t_{r(v)}$	Voltage rise time		-	11	-	
$t_{f(i)}$	Current fall time		-	9.3	-	
$t_{c(off)}$	Crossing time		-	16	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}[(1)]	Source-drain current		-		22.5	A
I_{SDM}[(1)(2)]	Source-drain current (pulsed)		-		90	A
V_{SD}[(3)]	Forward on voltage	V_{GS} = 0 V, I_{SD} = 22.5 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 22.5 A, di/dt = 100 A/µs, V_{DD} = 100 V (see *Figure 17: " Test circuit for inductive load switching and diode recovery times"*)	-	346		ns
Q_{rr}	Reverse recovery charge		-	6		µC
I_{RRM}	Reverse recovery current		-	35		A
t_{rr}	Reverse recovery time	I_{SD} = 22.5 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_J = 150 °C (see *Figure 17: " Test circuit for inductive load switching and diode recovery times"*)	-	432		ns
Q_{rr}	Reverse recovery charge		-	8.4		µC
I_{RRM}	Reverse recovery current		-	39		A

Notes:

(1) The value is rated according to $R_{thj\text{-}case}$ and limited by package.

(2) Pulse width is limited by safe operating area.

(3) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

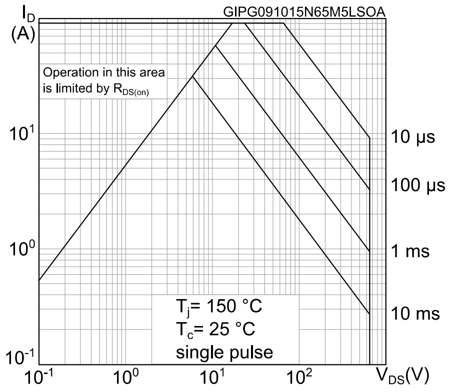


Figure 3: Thermal impedance

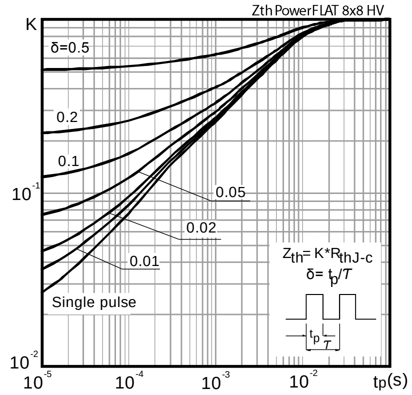


Figure 4: Output characteristics

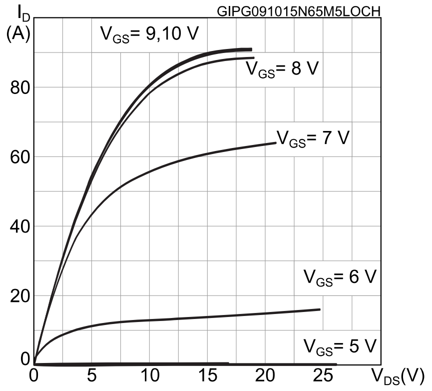


Figure 5: Transfer characteristics

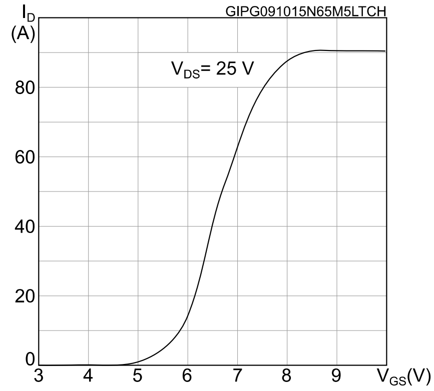


Figure 6: Gate charge vs gate-source voltage

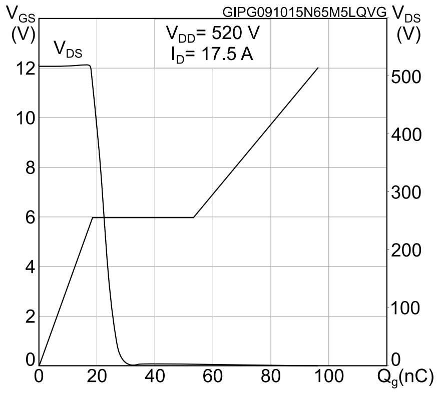


Figure 7: Static drain-source on-resistance

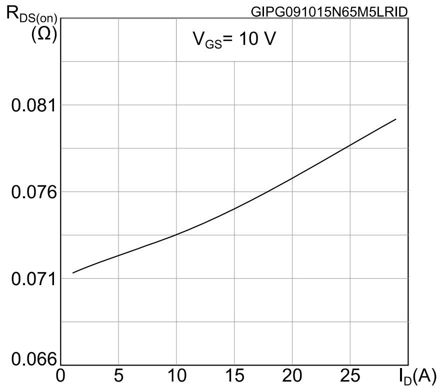


Figure 8: Capacitance variations

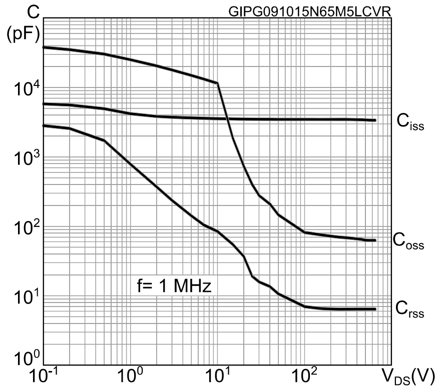


Figure 9: Output capacitance stored energy

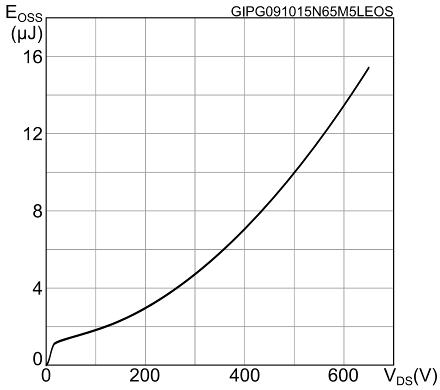


Figure 10: Normalized gate threshold voltage vs temperature

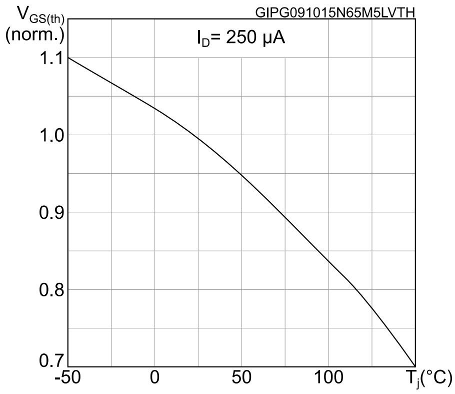


Figure 11: Normalized on-resistance vs. temperature

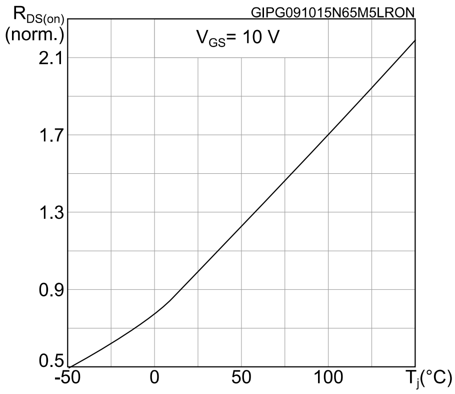


Figure 12: Drain-source diode forward characteristics

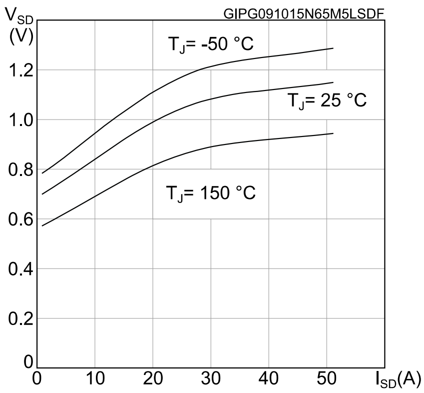


Figure 13: Normalized V(BR)DSS vs temperature

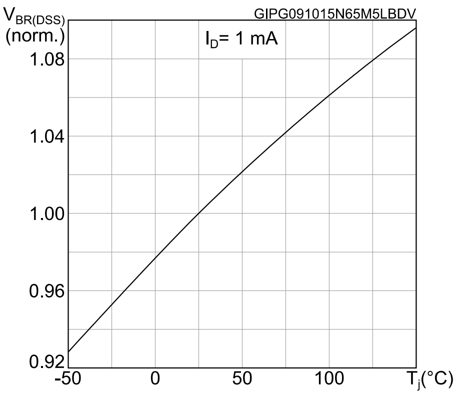
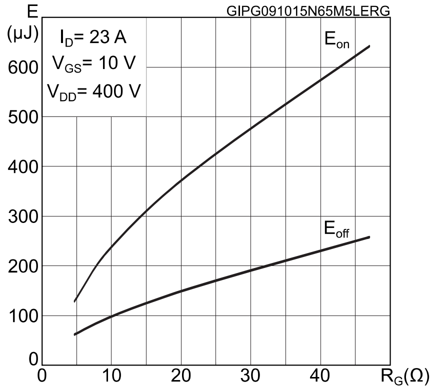


Figure 14: Switching loss vs. gate resistance[(1)]



Notes:

[(1)]E_{on} including reverse recovery of a SiC diode

3 Test circuits

Figure 15: Switching times test circuit for resistive load

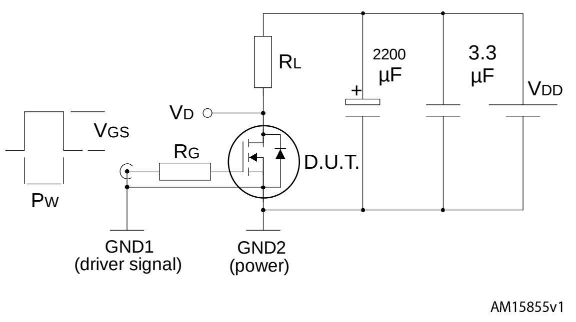


Figure 16: Gate charge test circuit

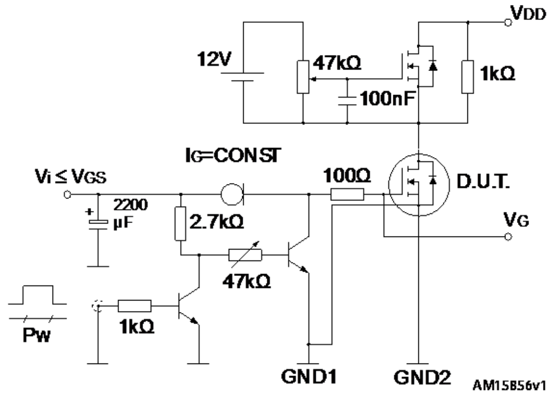


Figure 17: Test circuit for inductive load switching and diode recovery times

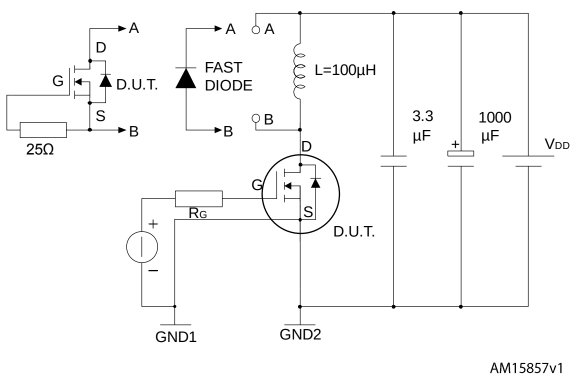


Figure 18: Unclamped inductive load test circuit

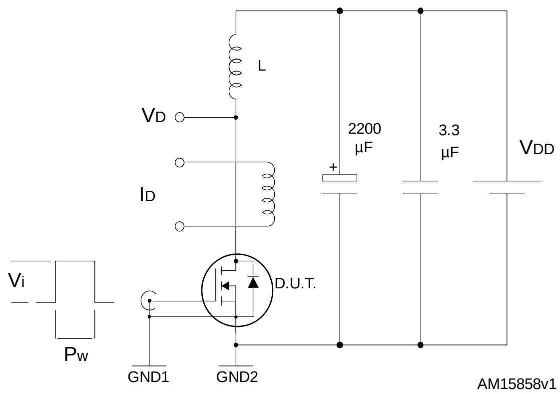


Figure 19: Unclamped inductive waveform

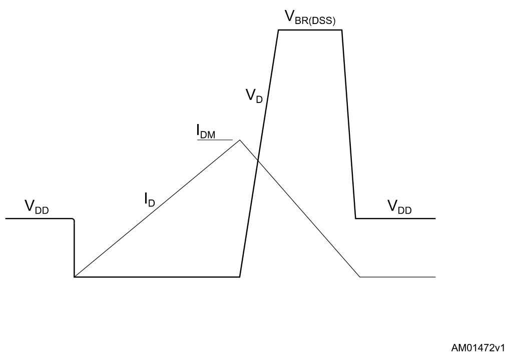
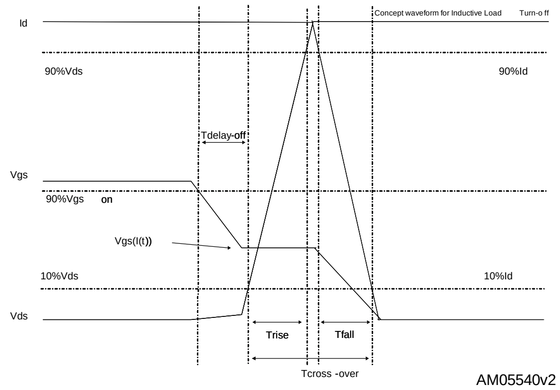


Figure 20: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT 8x8 HV package information

Figure 21: PowerFLAT™ 8x8 HV package outline

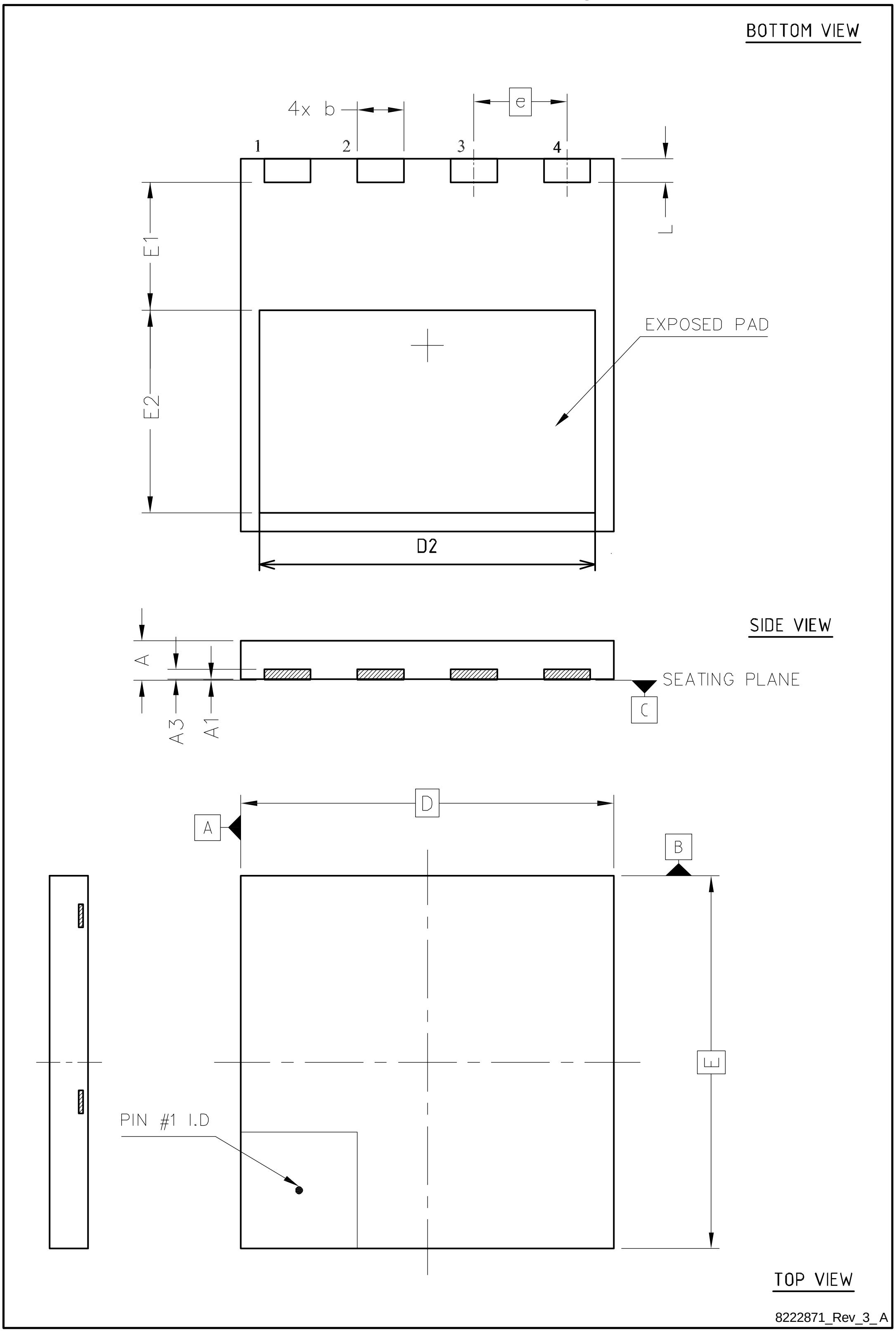
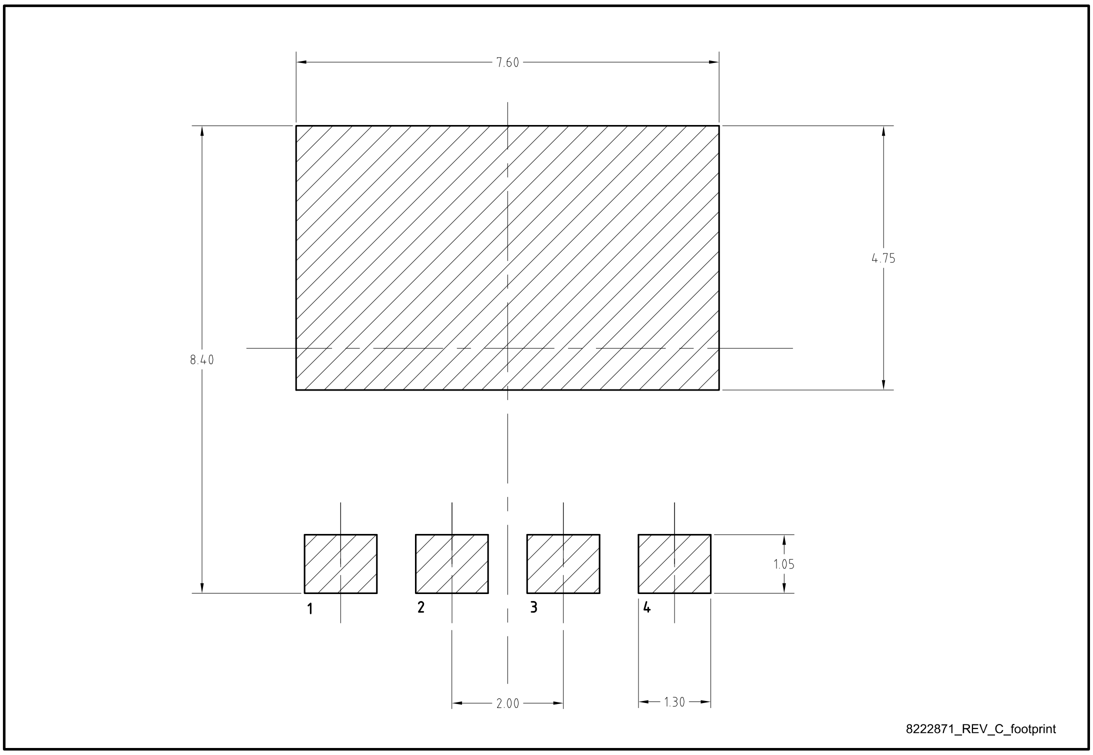


Table 9: PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00	
L	0.40	0.50	0.60

Figure 22: PowerFLAT™ 8x8 HV footprint



All dimensions are in millimeters.

4.2 PowerFLAT 8x8 HV packing information

Figure 23: PowerFLAT™ 8x8 HV tape

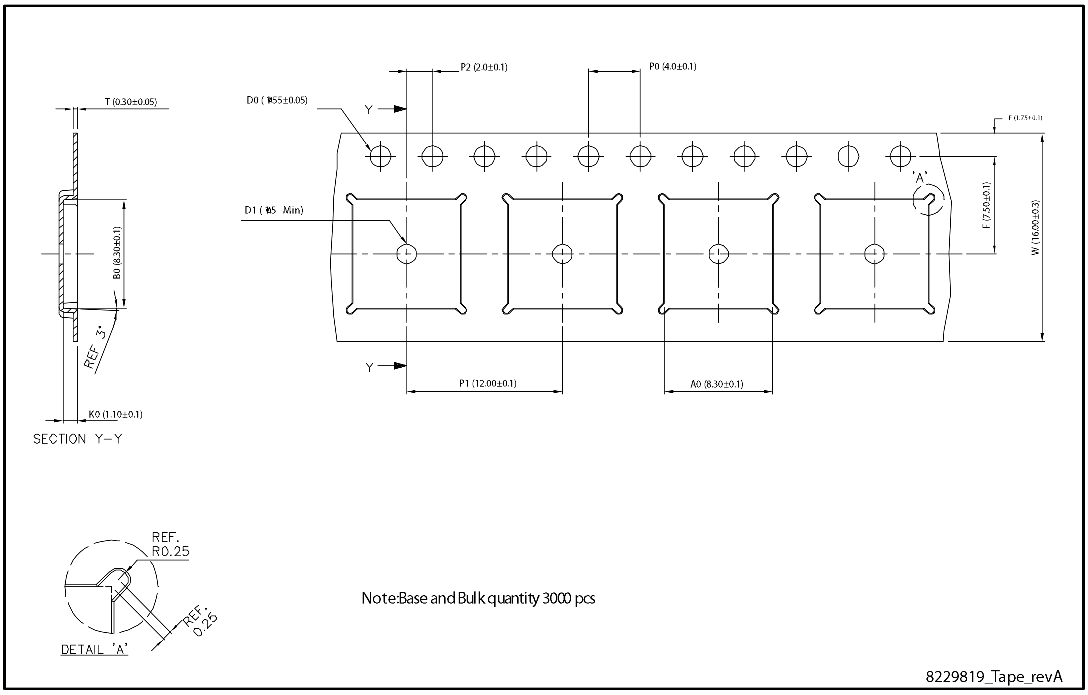


Figure 24: PowerFLAT™ 8x8 HV package orientation in carrier tape

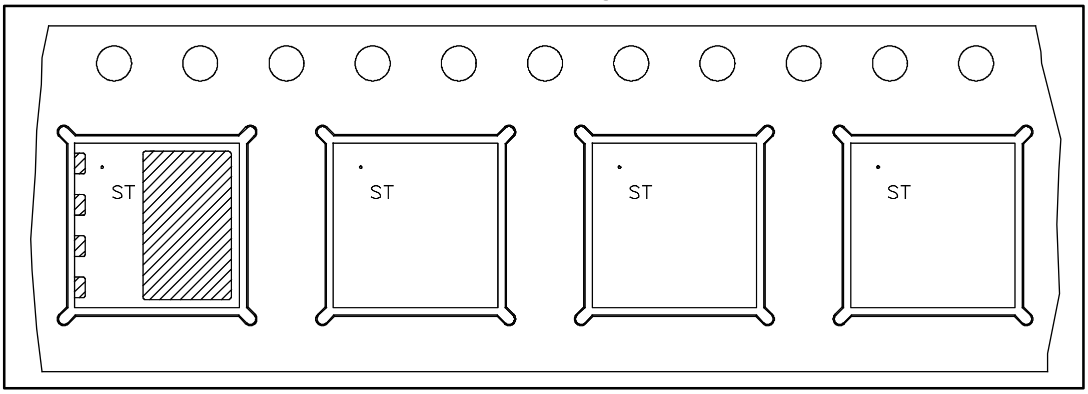
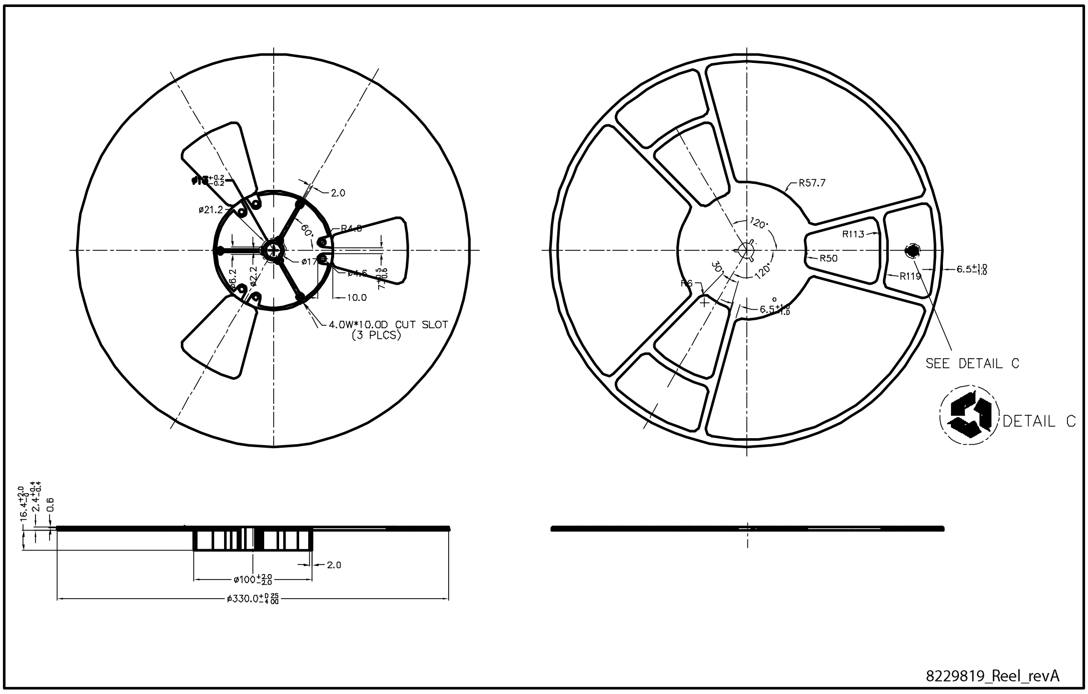


Figure 25: PowerFLAT™ 8x8 HV reel



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
20-Sep-2012	1	First release.
09-Oct-2015	2	Text and formatting changes throughout document Datasheet status changed from preliminary to production data In section Electrical ratings: - added table Avalanche characteristics In section Electrical characteristics: - renamed table Static (was On /off states) Updated section Test circuits Updated and renamed section Package information (was Package mechanical data)