LP2980-N Micropower 50-mA Ultra-Low-Dropout Regulator in SOT-23 Package

1 Features

- 2.1-V to 16-V Input Voltage Range
- 5-V, 4.7-V, 3.3-V, 3-V, and 2.5-V Output Versions
- Ultra-Low-Dropout Voltage
- Output Voltage Accuracy 0.5% (A Grade)
- Ensured 50-mA Output Current
- Requires Only 1-μF External Capacitance
- < 1-μA Quiescent Current When Shutdown
- Low Ground Pin Current at All Load Currents
- High Peak Current Capability (150 mA Typical)
- Wide Supply Voltage Range (16 V Maximum)
- Fast Dynamic Response to Line and Load
- Low Z_{OUT} Over Wide Frequency Range
- Overtemperature and Overcurrent Protection
- −40°C to 125°C Junction Temperature Range

2 Applications

- Cellular Phone
- Palmtop/Laptop Computer
- Personal Digital Assistant (PDA)
- Camcorder, Personal Stereo, Camera

3 Description

The LP2980-N is a 50-mA, fixed-output voltage regulator designed specifically to meet the requirements of battery-powered applications.

Using an optimized VIP (Vertically Integrated PNP) process, the LP2980-N delivers unequaled performance in all specifications critical to battery-powered designs:

Dropout voltage: Typically 120 mV at 50-mA load, and 7 mV at 1-mA load.

Ground pin current: Typically 375 μA at 50-mA load, and 80 μA at 1-mA load.

Sleep mode: Less than 1-μA quiescent current when ON/$\overline{\text{OFF}}$ pin is pulled to less than 0.18 V.

Minimum part count: Requires only a 1-μF capacitor on the regulator output.

Precision output: Initial output voltage tolerance of ±0.5% (A grade).

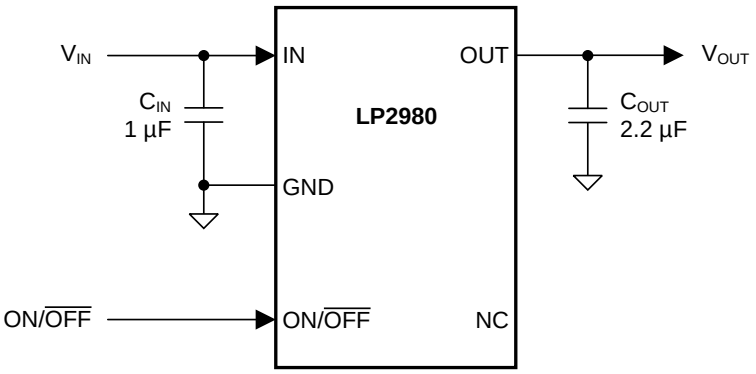
5-V, 4.7-V, 3.3-V, 3-V, and 2.5-V versions available as standard products.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2980-N	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (June 2015) to Revision P — **Page**

- Changed minor wording in *Description* for clarity ... 1
- Deleted input supply voltage (operating) row; deleted "(survival)" from rows of *Abs Max* table ... 4
- Deleted lead temperature from *Abs Max* per new format rules ... 4
- Added "(operating") from ROC table; add second row for "Shutdown input voltage" to ROC ... 4
- Added "High K" and footnote 2 to *Thermal Information* ... 4
- Changed "...an output tolerance of %..." to "...an initial output voltage tolerance of ±0.5%..." ... 12
- Deleted "Very high accuracy 1.23-V reference" ... 12
- Changed "150 mA" to "50 mA" to correct typo from reformat (2 places) ... 12
- Changed "...only 1 µA" to "...less than 1 µA" ... 12
- Changed "... pulled low" to "...pulled to less than 0.18 V" ... 12

Changes from Revision N (December 2014) to Revision O — **Page**

- Changed pin names VOUT to OUT and VIN to IN per TI nomenclature; correct typos ... 1
- Changed format of *ESD Ratings* table ... 4
- Deleted (the TO-220 package alone will safely dissipate this) - no TO-220 package for this part ... 20

Changes from Revision M (April 2013) to Revision N — **Page**

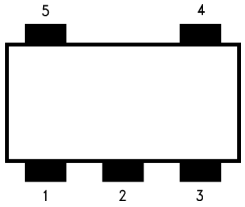
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section; add updated *Thermal Information* ... 1

Changes from Revision L (April 2013) to Revision M **Page**

- Changed layout of National Semiconductor data sheet to TI format..... 22

5 Pin Configuration and Functions

DBV Package
5 Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Input voltage
2	GND	—	Common ground (device substrate)
3	ON/$\overline{\text{OFF}}$	I	Logic high enable input
4	N/C	—	DO NOT CONNECT. Device pin 4 is reserved for post packaging test and calibration of the LP2980-N V_{OUT} accuracy. Device pin 4 must be left floating. Do not connect to any potential. Do not connect to ground. Any attempt to do pin continuity testing on device pin 4 is discouraged. Continuity test results will be variable depending on the actions of the factory calibration. Aggressive pin continuity testing (high voltage, or high current) on device pin 4 may activate the trim circuitry forcing VOUT to move out of tolerance.
5	OUT	O	Regulated output voltage

6 Specifications

6.1 Absolute Maximum Ratings (1)(2)

	MIN	MAX	UNIT
Operating junction temperature	−40	125	°C
Power dissipation (3)	Internally Limited		
Input supply voltage	−0.3	16	V
Shutdown input voltage	−0.3	16	V
Output voltage (4)	−0.3	9	V
I_{OUT}	Short-circuit protected		
Input-output voltage (5)	−0.3	16	V
Storage temperature, T_{stg}	–65	150	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
(2) If Military/Aerospace-specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using $P_{(MAX)} = ((T_{J(MAX)} – T_A) / R_{\theta JA})$.
The value of $R_{\theta JA}$ for the SOT-23 package is 175.7°C/W. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(4) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2980-N output must be diode-clamped to ground.
(5) The output PNP structure contains a diode between the IN and OUT pins that is normally reverse-biased. Reversing the polarity from V_{IN} to V_{OUT} turns on this diode (see *Reverse Current Path*).

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	All pins except 3 and 4	±2000	V
			Pins 3 and 4	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating junction temperature	−40	125	°C
Input supply voltage	2.1	16	V
Shutdown input voltage	0	V_{IN}	

6.4 Thermal Information

THERMAL METRIC (1)		LP2980-N DBV 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, High K (2)	175.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.3	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by *JESD51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.*

6.5 Electrical Characteristics

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, I_L = 1 mA, C_{OUT} = 1 µF, $V_{ON/\overline{OFF}}$ = 2 V.(1)

PARAMETER		TEST CONDITIONS	LP2980AI-XX(2)			LP2980I-XX(2)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_O	Output voltage tolerance	I_L = 1 mA	−0.5		0.5	−1		1	%V_{NOM}
		1 mA < I_L < 50 mA	−0.75		0.75	−1.5		1.5	
		1 mA < I_L < 50 mA –40°C ≤ T_J ≤ 125°C	−2.5		2.5	−3.5		3.5	
$\frac{\Delta V_O}{\Delta V_{IN}}$	Output voltage line regulation	$V_{O(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V		0.007	0.014		0.007	0.014	%/V
		$V_{O(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V –40°C ≤ T_J ≤ 125°C		0.007	0.032		0.007	0.032	
$V_{IN} – V_O$	Dropout voltage(3)	I_L = 0 mA		1	3		1	3	mV
		I_L = 0 mA, –40°C ≤ T_J ≤ 125°C		1	5		1	5	
		I_L = 1 mA		7	10		7	10	
		I_L = 1 mA, –40°C ≤ T_J ≤ 125°C		7	15		7	15	
		I_L = 10 mA		40	60		40	60	
		I_L = 10 mA, –40°C ≤ T_J ≤ 125°C		40	90		40	90	
		I_L = 50 mA		120	150		120	150	
		I_L = 50 mA, –40°C ≤ T_J ≤ 125°C		120	225		120	225	
I_{GND}	Ground pin current	I_L = 0 mA		65	95		65	95	µA
		I_L = 0 mA, –40°C ≤ T_J ≤ 125°C		65	125		65	125	
		I_L = 1 mA		80	110		80	110	
		I_L = 1 mA, –40°C ≤ T_J ≤ 125°C		80	170		80	170	
		I_L = 10 mA		140	220		140	220	
		I_L = 10 mA, –40°C ≤ T_J ≤ 125°C		140	460		140	460	
		I_L = 50 mA		375	600		375	600	
		I_L = 50 mA, –40°C ≤ T_J ≤ 125°C		375	1200		375	1200	
		$V_{ON/\overline{OFF}}$ < 0.18 V –40°C ≤ T_J ≤ 125°C		0	1		0	1	
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage(4)	High = O/P ON –40°C ≤ T_J ≤ 125°C	1.6	1.4		1.6	1.4		V
		Low = O/P OFF –40°C ≤ T_J ≤ 125°C		0.55	0.18		0.55	0.18	
$I_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input current	$V_{ON/\overline{OFF}}$ = 0 V		0	−1		0	−1	µA
		$V_{ON/\overline{OFF}}$ = 5 V –40°C ≤ T_J ≤ 125°C		5	15		5	15	
$I_{O(PK)}$	Peak output current	V_{OUT} ≥ $V_{O(NOM)}$ − 5%	100	150		100	150		mA
e_n	Output noise voltage (RMS)	BW = 300 Hz to 50 kHz C_{OUT} = 10 µF		160			160		µV
ΔV_{OUT} / ΔV_{IN}	Ripple rejection	f = 1 kHz C_{OUT} = 10 µF		63			63		dB

(1) Minimum and maximum limits are ensured through test, design, or statistical correlation over the junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using statistical quality control (SQC) methods. The limits are used to calculate average outgoing quality level (AOQL).
(3) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1-V differential.
(4) The ON/$\overline{OFF}$ inputs must be properly driven to prevent misoperation. For details, see *ON/$\overline{OFF}$ Input Operation*.

Electrical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, I_L = 1 mA, C_{OUT} = 1 µF, $V_{ON/\overline{OFF}}$ = 2 V.(1)

PARAMETER		TEST CONDITIONS	LP2980AI-XX(2)			LP2980I-XX(2)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$I_{O(MAX)}$	Short-circuit current	R_L = 0 Ω (steady state)(5)		150			150		mA

(5) See related curve(s) in *Typical Characteristics* section.

6.6 Typical Characteristics

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 2.2 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

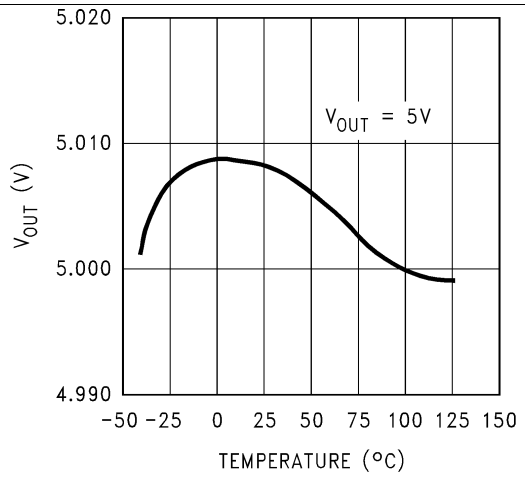


Figure 1. Output Voltage vs Temperature

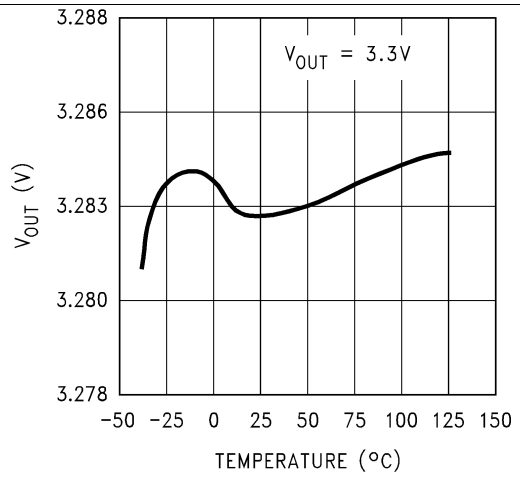


Figure 2. Output Voltage vs Temperature

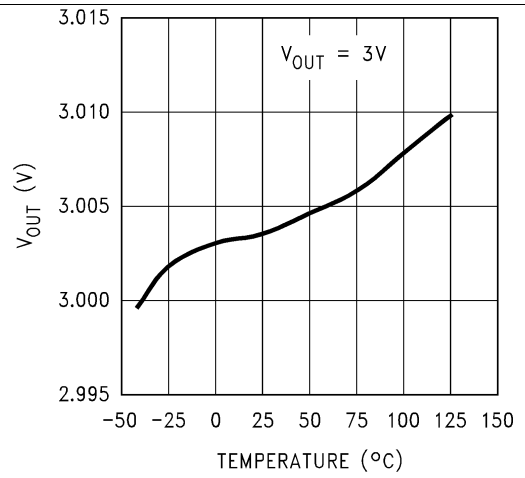


Figure 3. Output Voltage vs Temperature

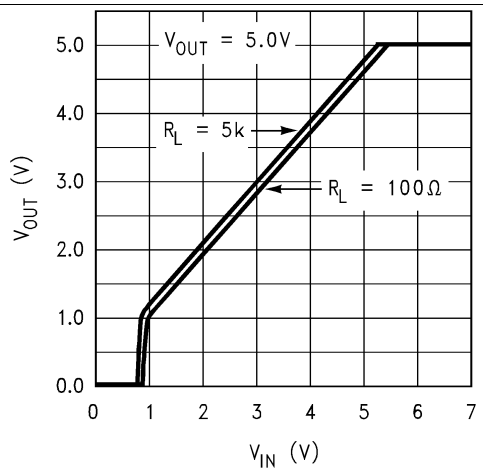


Figure 4. Dropout Characteristics

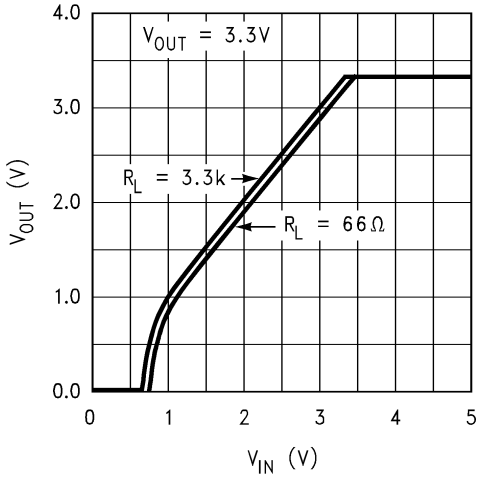


Figure 5. Dropout Characteristics

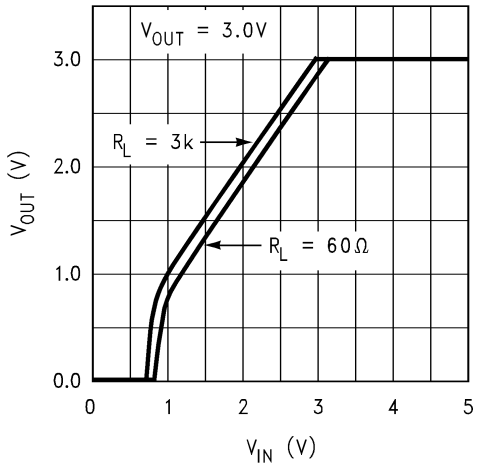


Figure 6. Dropout Characteristics

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 2.2 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

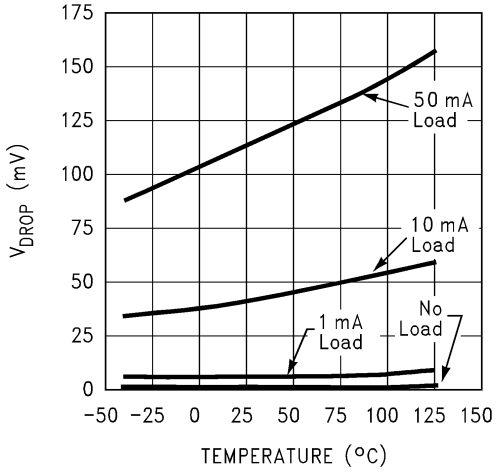


Figure 7. Dropout Voltage vs Temperature

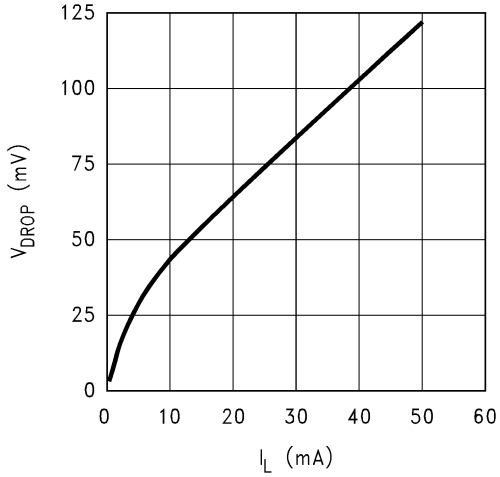


Figure 8. Dropout Voltage vs Load Current

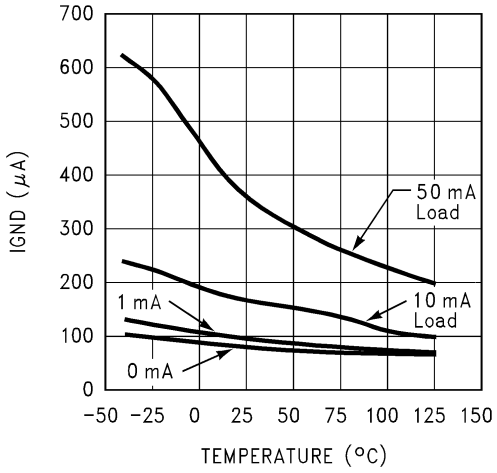


Figure 9. Ground Pin Current vs Temperature

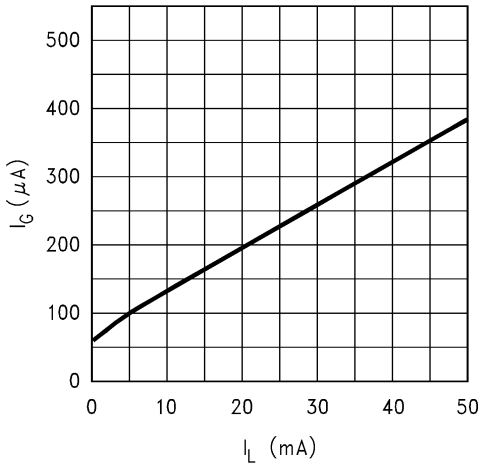


Figure 10. Ground Pin Current vs Load Current

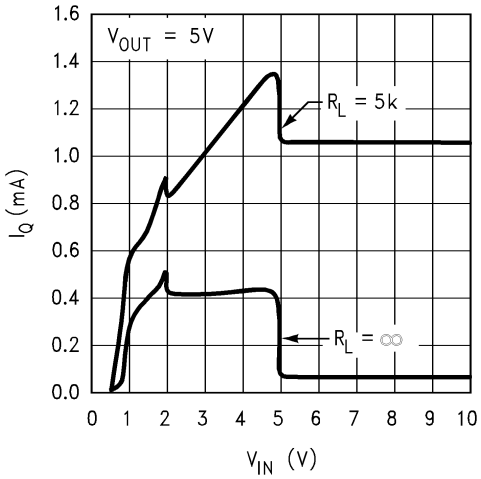


Figure 11. Input Current vs V_{IN}

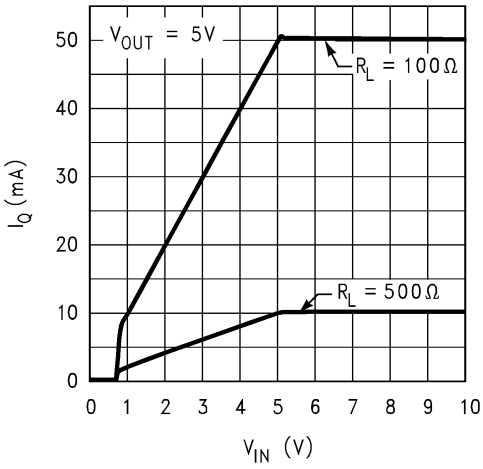


Figure 12. Input Current vs V_{IN}

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 2.2 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

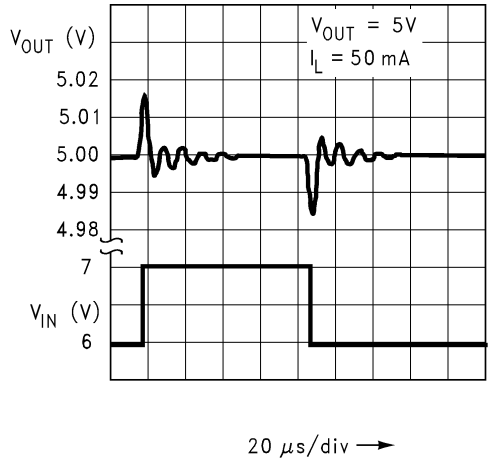


Figure 13. Line Transient Response

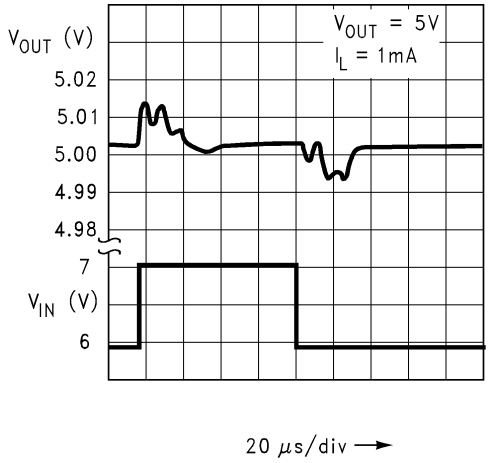


Figure 14. Line Transient Response

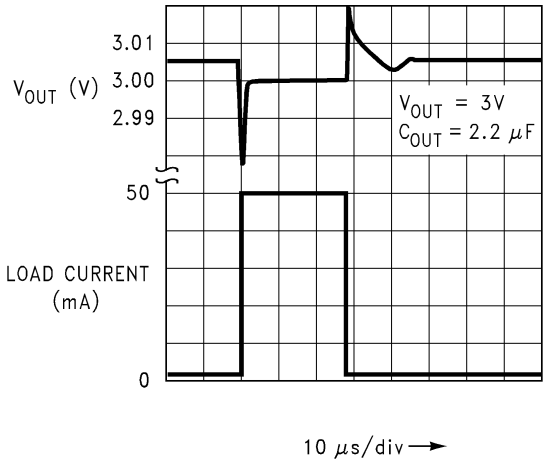


Figure 15. Load Transient Response

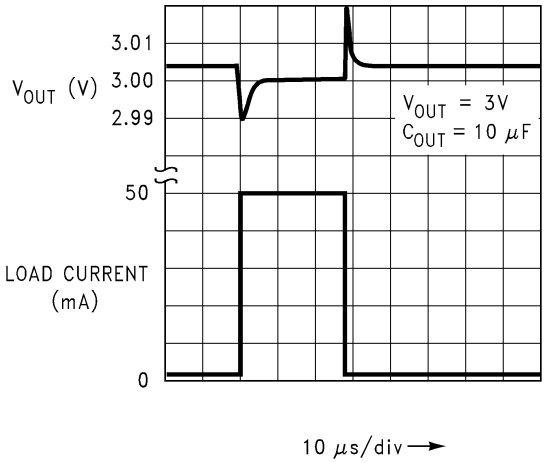


Figure 16. Load Transient Response

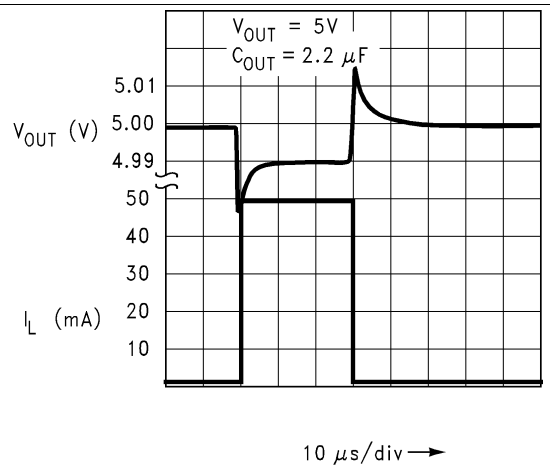


Figure 17. Load Transient Response

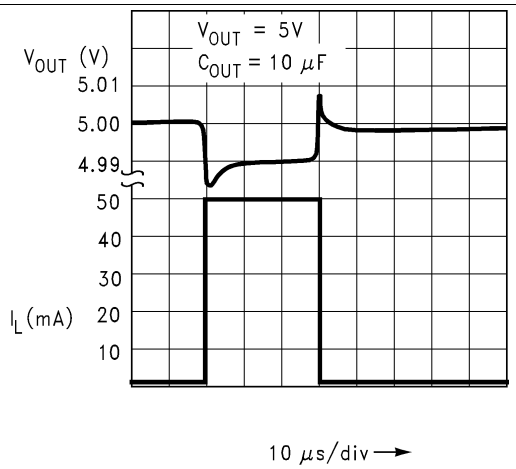


Figure 18. Load Transient Response

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 2.2 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

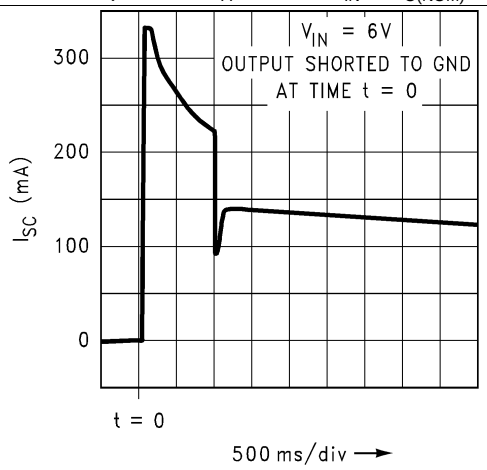


Figure 19. Short Circuit Current

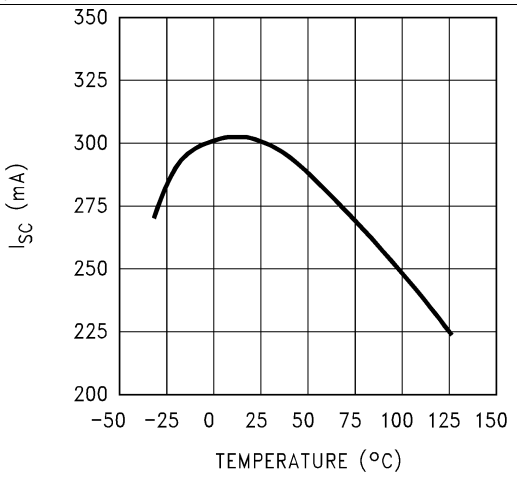


Figure 20. Instantaneous Short Circuit Current vs Temperature

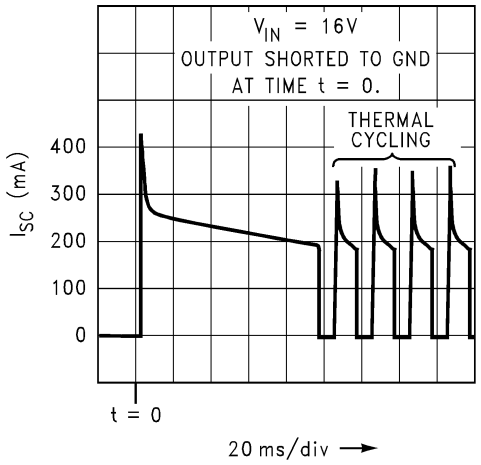


Figure 21. Short Circuit Current

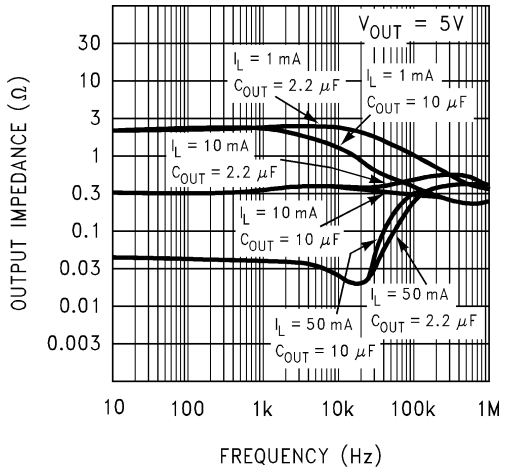


Figure 22. Output Impedance vs Frequency

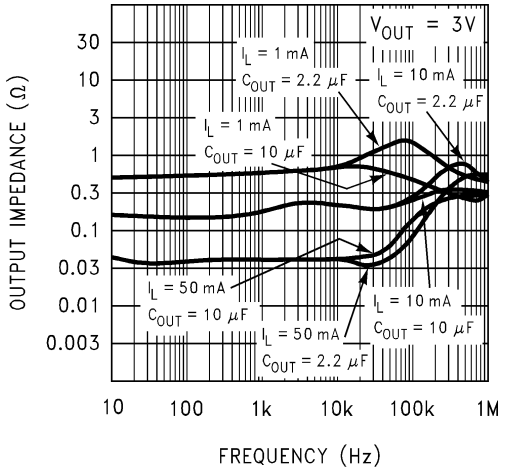


Figure 23. Output Impedance vs Frequency

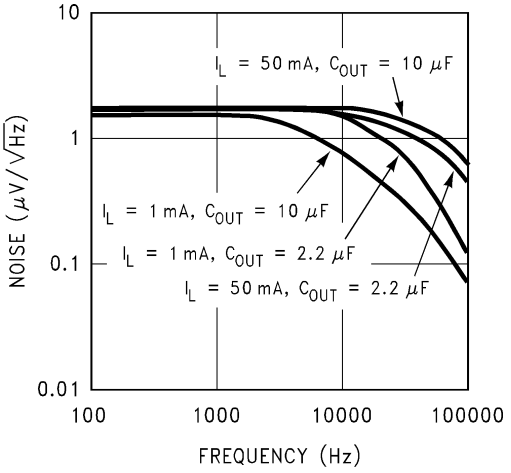


Figure 24. Output Noise Density

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 2.2 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

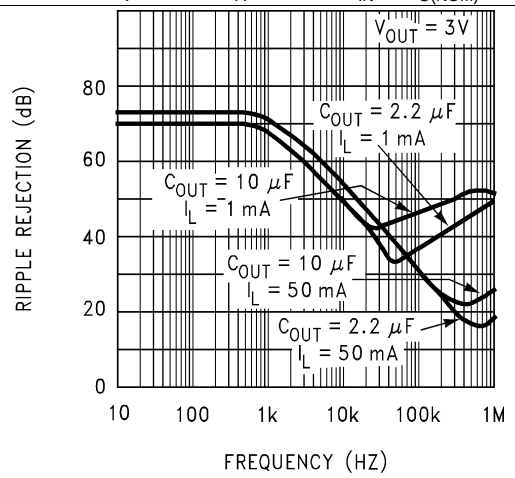


Figure 25. Ripple Rejection

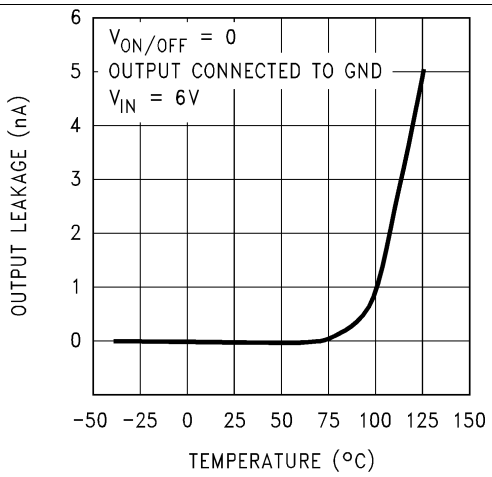


Figure 26. Input to Output Leakage vs Temperature

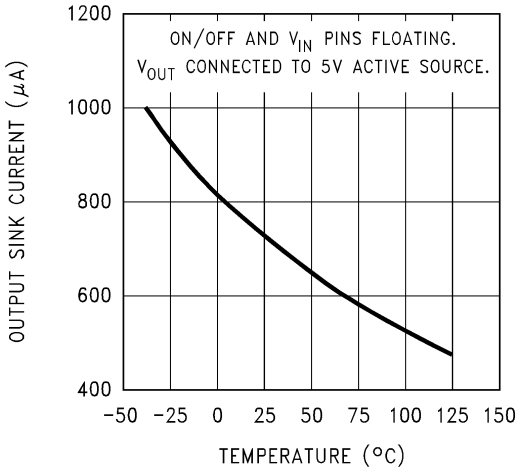


Figure 27. Output Reverse Leakage vs Temperature

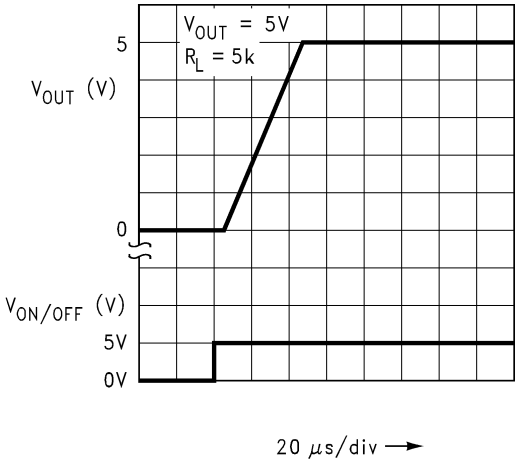


Figure 28. Turnon Waveform

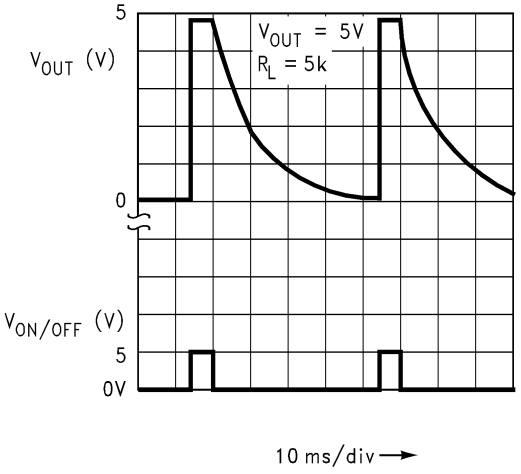


Figure 29. Turnoff Waveform

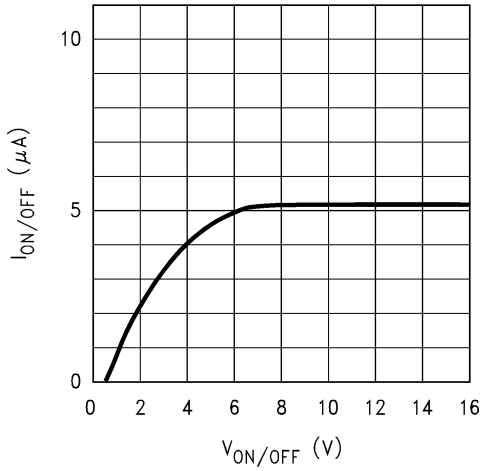


Figure 30. ON/$\overline{OFF}$ Pin Current vs $V_{ON/\overline{OFF}}$

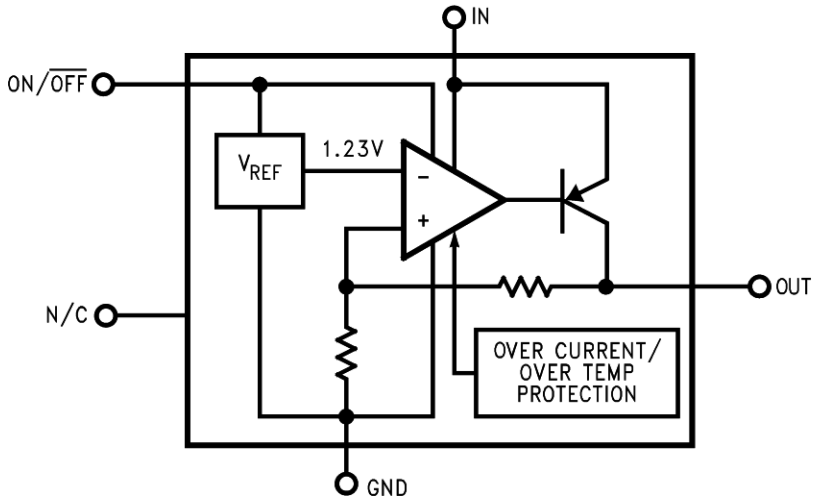
7 Detailed Description

7.1 Overview

The LP2980-N is a 50-mA, fixed-output voltage regulator designed specifically to meet the requirements of battery-powered applications. Available in output voltages from 2.5 V to 5 V, the device has an initial output voltage tolerance of ±0.5% for the A grade (1% for the non-A version). Using an optimized vertically integrated PNP (VIP) process, the LP2980-N contains these features to facilitate battery-powered designs:

- Fixed 5-V, 4.7-V, 3.3-V, 3-V, and 2.5-V output versions
- Low-dropout voltage, typical dropout of 120 mV at 50-mA load current and 7 mV at 1-mA load
- Low ground current, typically 370 μA at 50-mA load and 80 μA at 1-mA load
- A sleep mode feature is available, allowing the regulator to consume less than 1 μA typically when the ON/$\overline{\text{OFF}}$ pin is pulled to less than 0.18 V.
- Overtemperature protection and overcurrent protection circuitry is designed to safeguard the device during unexpected conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Multiple Voltage Options

To meet the different application requirements, the LP2980-N provides multiple fixed output options from 2.5 V to 5 V.

7.3.2 High-Accuracy Output Voltage

With special careful design to minimize all contributions to the output voltage error, the LP2980-N distinguishes itself as a very high-accuracy output voltage micropower LDO. This includes a tight initial tolerance (0.5% typical), extremely good line regulation (0.007%/V typical), and a very low output voltage temperature coefficient, making the part an ideal low-power voltage reference.

7.3.3 Ultra-Low-Dropout Voltage

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage (VDO = $V_{IN} – V_{OUT}$), where the main current pass-FET is fully on in the ohmic region of operation and is characterized by the classic $R_{DS(ON)}$ of the FET. VDO indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain within its accuracy boundary.

Feature Description (continued)

7.3.4 Low Ground Current

LP2980-N uses a vertical PNP process which allows for quiescent currents that are considerably lower than those associated with traditional lateral PNP regulators, typically 370 μA at 150-mA load and 80 μA at 1-mA load.

7.3.5 Sleep Mode

When pulling the ON/$\overline{\text{OFF}}$ pin to low level, LP2980-N enters sleep mode, and less than 1-μA quiescent current is consumed. This function is designed for the application which needs a sleep mode to effectively enhance battery life cycle.

7.3.6 Short-Circuit Protection (Current Limit)

The internal current-limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. If a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO resulting in a thermal shutdown of the output. A foldback feature limits the short-circuit current to protect the regulator from damage under all load conditions. If OUT is forced below 0 V before EN goes high and the load current required exceeds the foldback current limit, the device may not start up correctly.

7.3.7 Thermal Protection

The LP2980-N contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. The thermal time-constant of the semiconductor die is fairly short, and thus the output cycles on and off at a high rate when thermal shutdown is reached until the power dissipation is reduced. The internal protection circuitry of the LM2980-N is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown degrades its reliability.

7.4 Device Functional Modes

7.4.1 Operation with $V_{OUT(TARGET)}$ + 1 V ≤ V_{IN} < 16 V

The device operates if the input voltage is equal to, or exceeds, $V_{OUT(TARGET)}$ + 0.6 V. At input voltages below the minimum V_{IN} requirement, the device does not operate correctly and output voltage may not reach target value.

7.4.2 Operation With ON/$\overline{\text{OFF}}$ Control

If the voltage on the ON/$\overline{\text{OFF}}$ pin is less than 0.18 V, the device is disabled, and the shutdown current does not exceed 1 μA. Raising ON/$\overline{\text{OFF}}$ above 1.6 V initiates the start-up sequence of the device.

8 Application and Implementation

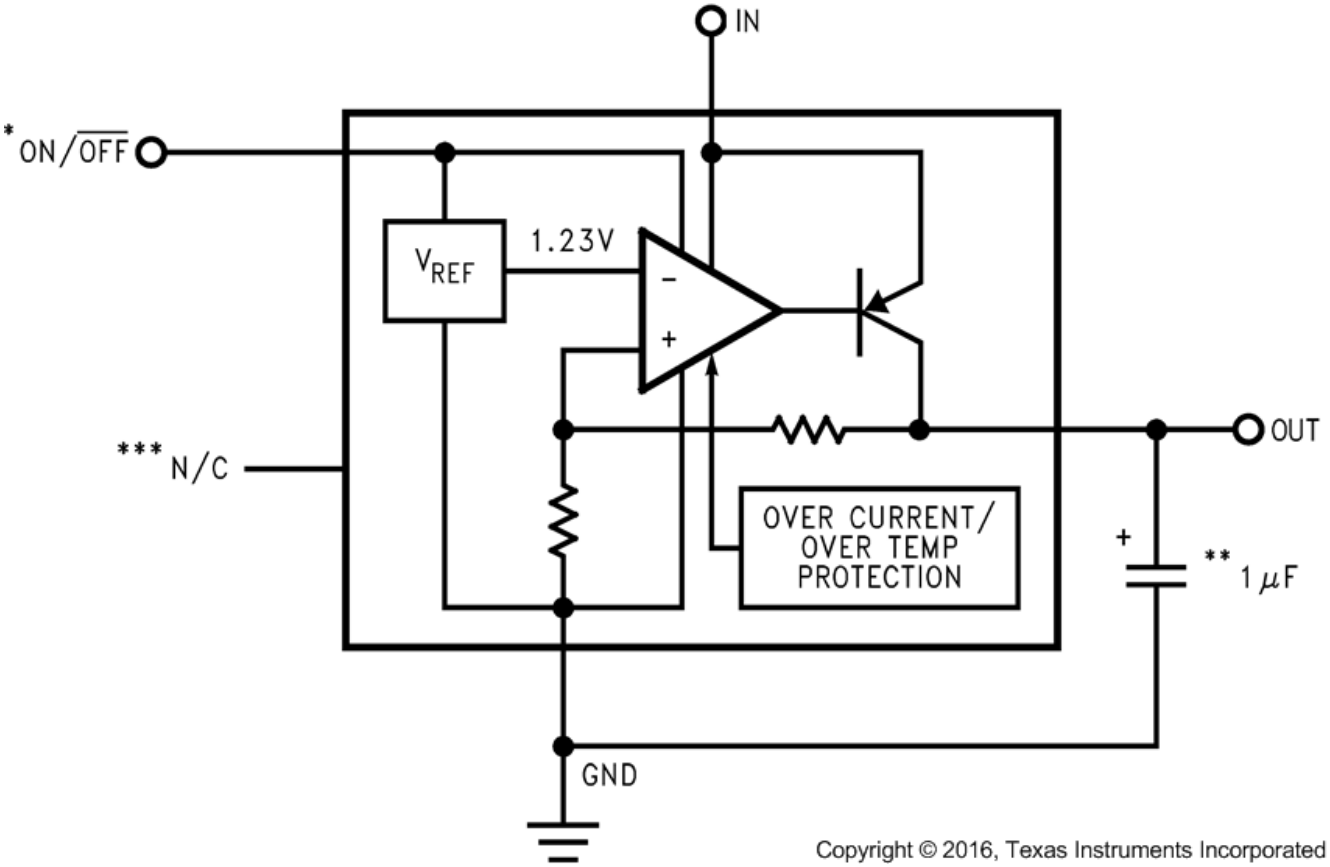
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP2980-N is a linear voltage regulator operating from 2.1 V to 16 V on the input and regulates voltages between 2.5 V to 5 V with 0.5% accuracy and 50-mA maximum output current. Efficiency is defined by the ratio of output voltage to input voltage because the LP2980-N is a linear voltage regulator. To achieve high efficiency, the dropout voltage (V_{IN} – V_{OUT}) must be as small as possible, thus requiring a very-low-dropout LDO. Successfully implementing an LDO in an application depends on the application requirements. If the requirements are simply input voltage and output voltage, compliance specifications (such as internal power dissipation or stability) must be verified to ensure a solid design. If timing, startup, noise, power supply rejection ratio (PSRR), or any other transient specification is required, then the design becomes more challenging. This section discusses the implementation and behavior of the LP2980-N LDO.

8.2 Typical Application



*ON/$\overline{\text{OFF}}$ input must be actively terminated. Tie to IN if this function is not to be used.
**Minimum output capacitance is 1 μF to ensure stability over full load current range. More capacitance provides superior dynamic performance and additional stability margin (see *Output Capacitor Recommendation*).
***Do not make connections to this pin.

Typical Application (continued)

8.2.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT
Input voltage	5 V ±10%, provided by the DC-DC converter switching at 1 MHz
Output voltage	3.3 V ±5%
Output current	50 mA (maximum), 1 mA (minimum)
RMS noise, 300 Hz to 50 kHz	< 1 mV_{RMS}
PSRR at 1 kHz	> 40 dB

8.2.2 Detailed Design Procedure

At 50-mA loading, the dropout of the LP2980-N has 225-mV maximum dropout over temperature, thus an 1700-mV headroom is sufficient for operation over both input and output voltage accuracy. The efficiency of the LP2980-N in this configuration is V_{OUT} / V_{IN} = 66.7%. To achieve the smallest form factor, the SOT-23 package is selected. Input and output capacitors are selected in accordance with the *Output Capacitor Recommendation* section. With an efficiency of 66.7% and a 50-mA maximum load, the internal power dissipation is 85 mW, which corresponds to a 14.9°C junction temperature rise for the SOT-23 package. With an 85°C maximum ambient temperature, the junction temperature is at 99.9°C.

8.2.2.1 Output Capacitor Recommendation

Like any low-dropout regulator, the LP2980-N requires an output capacitor to maintain regulator loop stability. This capacitor must be selected to meet the requirements of minimum capacitance and equivalent series resistance (ESR) range. It is not difficult to find capacitors which meet the criteria of the LP2980-N, as the acceptable capacitance and ESR ranges are wider than for most other LDOs.

In general, the capacitor value must be at least 1 μF (over the actual ambient operating temperature), and the ESR must be within the range indicated in Figure 31, Figure 32, and Figure 33. It should be noted that, although a maximum ESR is shown in these figures, it is very unlikely to find a capacitor with an ESR that high.

8.2.2.1.1 Tantalum Capacitors

Surface-mountable solid tantalum capacitors offer a good combination of small physical size for the capacitance value, and an ESR in the range needed by the LP2980-N.

The results of testing the LP2980-N stability with surface-mount solid tantalum capacitors show good stability with values of at least 1 μF. The value can be increased to 2.2 μF (or more) for even better performance, including transient response and noise.

Small value tantalum capacitors that have been verified as suitable for use with the LP2980-N are shown in Table 1. Capacitance values can be increased without limit.

8.2.2.1.2 Aluminum Electrolytic Capacitors

Although probably not a good choice for a production design, because of relatively large physical size, an aluminum electrolytic capacitor can be used in the design prototype for an LP2980-N regulator. A value of at least 1 μF should be used, and the ESR must meet the conditions of Figure 31, Figure 32, and Figure 33. If the operating temperature drops below 0°C, the regulator may not remain stable, as the ESR of the aluminum electrolytic capacitor will increase and may exceed the limits indicated in Figure 31, Figure 32, and Figure 33.

Table 1. Surface-Mount Tantalum Capacitor Selection Guide

1-μF SURFACE-MOUNT TANTALUM CAPACITORS	
MANUFACTURER	PART NUMBER
Kemet	T491A105M010AS
NEC	NRU105M10
Siemens	B45196-E3105-K
Nichicon	F931C105MA
Sprague	293D105X0016A2T

2.2-µF SURFACE-MOUNT TANTALUM CAPACITORS	
MANUFACTURER	**PART NUMBER**
Kemet	T491A225M010AS
NEC	NRU225M06
Siemens	B45196/2.2/10/10
Nichicon	F930J225MA
Sprague	293D225X0010A2T

8.2.2.1.3 Multilayer Ceramic Capacitors

Surface-mountable multilayer ceramic capacitors may be an attractive choice because of their relatively small physical size and excellent RF characteristics. However, they sometimes have ESR values lower than the minimum required by the LP2980-N, and relatively large capacitance change with temperature. The manufacturer's data sheet for the capacitor should be consulted before selecting a value.

Test results of LP2980-N stability using multilayer ceramic capacitors show that a minimum value of 2.2 µF is usually needed for the 5-V regulator. For the lower output voltages, or for better performance, a higher value should be used, such as 4.7 µF.

Multilayer ceramic capacitors that have been verified as suitable for use with the LP2980-N are shown in Table 2.

Table 2. Surface-Mount Multilayer Ceramic Capacitor Selection Guide

2.2-µF SURFACE-MOUNT CERAMIC	
MANUFACTURER	**PART NUMBER**
Tokin	1E225ZY5U-C203
Murata	GRM42-6Y5V225Z16

4.7-µF SURFACE-MOUNT CERAMIC	
MANUFACTURER	**PART NUMBER**
Tokin	1E475ZY5U-C304

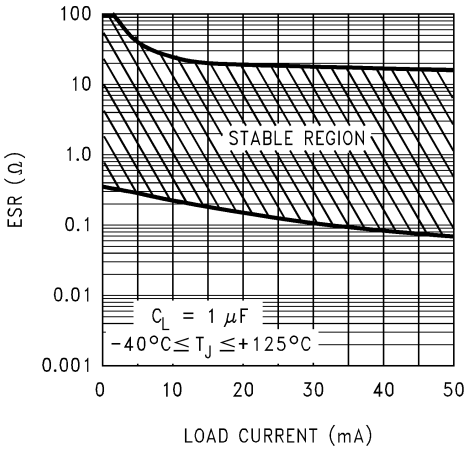


Figure 31. 1-µF ESR Range

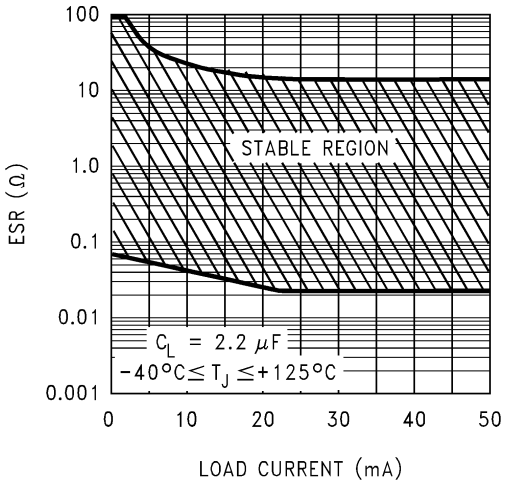


Figure 32. 2.2-µF ESR Range

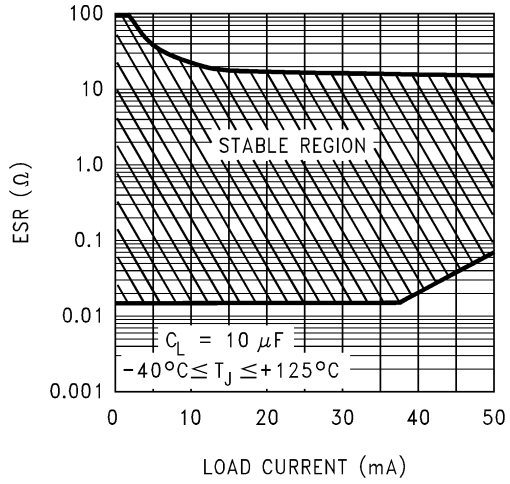


Figure 33. 10-µF ESR Range

8.2.2.2 Reverse Current Path

The internal PNP power transistor used as the pass element in the LP2980-N has an inherent diode connected between the regulator output and input. During normal operation (where the input voltage is higher than the output) this diode is reverse biased (see Figure 34).

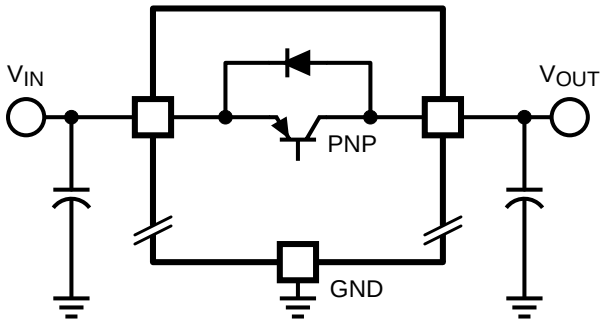


Figure 34. LP2980-N Reverse Current Path

However, if the input voltage is more than a V_{BE} below the output voltage, this diode will turn on and current will flow into the regulator output. In such cases, a parasitic SCR can latch which will allow a high current to flow into the V_{IN} pin and out the ground pin, which can damage the part.

The internal diode can also be turned on if the input voltage is abruptly stepped down to a voltage which is a V_{BE} below the output voltage.

In any application where the output voltage may be higher than the input voltage, an external Schottky diode must be connected from V_{IN} to V_{OUT} (cathode on V_{IN}, anode on V_{OUT}, see Figure 35), to limit the reverse voltage across the LP2980-N to 0.3 V (see *Absolute Maximum Ratings*).

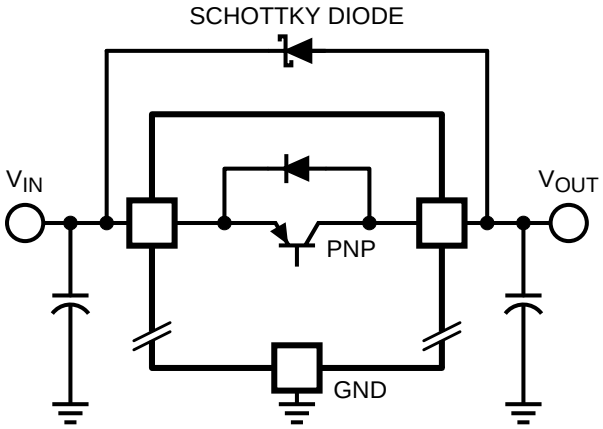


Figure 35. Adding External Schottky Diode Protection

8.2.2.3 ON/$\overline{\text{OFF}}$ Input Operation

The LP2980-N is shut off by pulling the ON/$\overline{\text{OFF}}$ input low, and turned on by driving the input high. If this feature is not to be used, the ON/$\overline{\text{OFF}}$ input must be tied to IN to keep the regulator on at all times (the ON/$\overline{\text{OFF}}$ input must not be left floating).

To ensure proper operation, the signal source used to drive the ON/$\overline{\text{OFF}}$ input must be able to swing above and below the specified turn-on and turn-off voltage thresholds which ensure an ON or OFF state (see *Electrical Characteristics*).

The ON/$\overline{\text{OFF}}$ signal may come from either a totem-pole output, or an open-collector output with a pull-up resistor to the LP2980-N input voltage or another logic supply. The high-level voltage may exceed the LP2980-N input voltage, but must remain within the absolute maximum ratings for the ON/$\overline{\text{OFF}}$ pin.

It is also important that the turn-on and turn-off voltage signals applied to the ON/$\overline{\text{OFF}}$ input have a slew rate that is greater than 40 mV/μs.

NOTE

The regulator shutdown function will not operate correctly if a slow-moving signal is used to drive the ON/$\overline{\text{OFF}}$ input.

8.2.2.4 Increasing Output Current

The LP2980-N can be used to control higher-current regulators, by adding an external PNP pass transistor. With the PNP transistors shown in Figure 36, the output current can be as high as 400 mA, as long as the input voltage is held within the Safe Operation Boundary Curves shown below in Figure 37.

To ensure regulation, the minimum input voltage of this regulator is 6 V. This headroom is the sum of the V_{BE} of the external transistor and the dropout voltage of the LP2980-N.

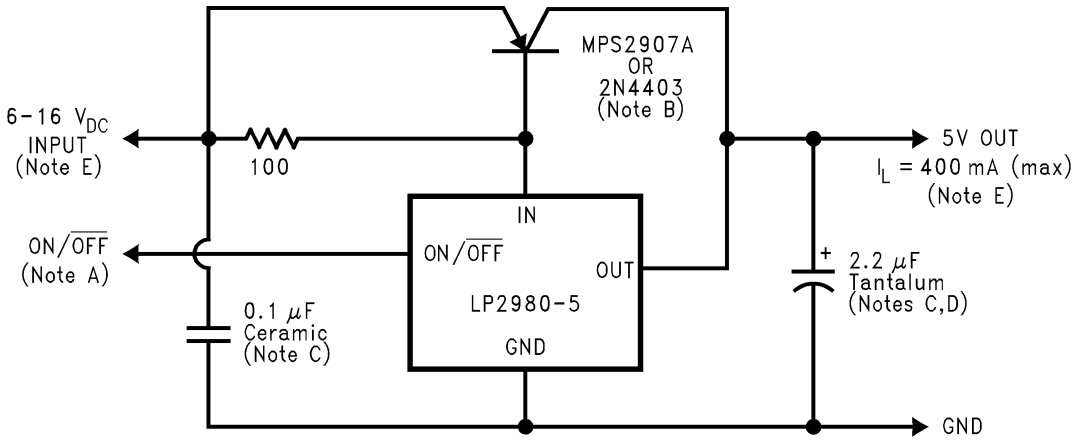


Figure 36. 5-V and 400-mA Regulator

Notes:

Note A: Drive this input with a logic signal (see *ON/OFF Input Operation*). If the shutdown function is not to be used, tie the ON/OFF pin directly to the IN pin.

Note B: Recommended devices (other PNP transistors can be used if the current gain and voltage ratings are similar).

Note C: Capacitor is required for regulator stability. Minimum size is shown, and may be increased without limit.

Note D: Increasing the output capacitance improves transient response and increases phase margin.

Note E: Maximum safe input voltage and load current are limited by power dissipation in the PNP pass transistor and the maximum ambient temperature for the specific application. If a TO-92 transistor such as the MPS2907A is used, the thermal resistance from junction-to-ambient is 180°C/W in still air.

Assuming a maximum allowable junction temperature of 150°C for the MPS2907A device, the following curves show the maximum V_{IN} and I_L values that may be safely used for several ambient temperatures.

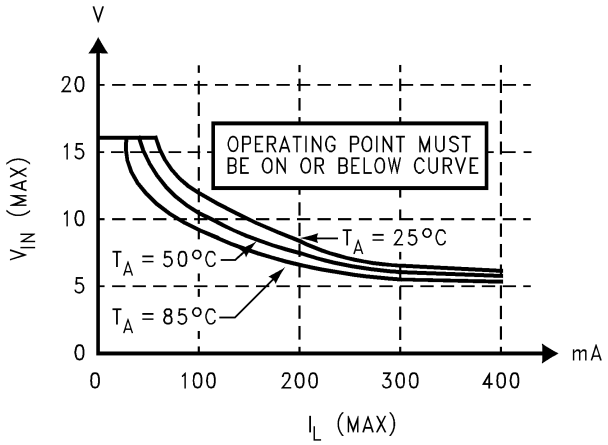


Figure 37. Safe Operation Boundary Curves for Figure 36

With limited input voltage range, the LP2980-N can control a 3.3-V, 3-A regulator with the use of a high current-gain external PNP pass transistor as shown in Figure 38. If the regulator is to be loaded with the full 3 A, heat sinking will be required on the pass transistor to keep it within its rated temperature range. See Figure 39. For best load regulation at the high load current, the LP2980-N output voltage connection should be made as close to the load as possible.

Although this regulator can handle a much higher load current than can the LP2980-N alone, it can be shut down in the same manner as the LP2980-N. When the ON/$\overline{\text{OFF}}$ control is brought low, the converter will be in shutdown, and will draw less than 1 μA from the source.

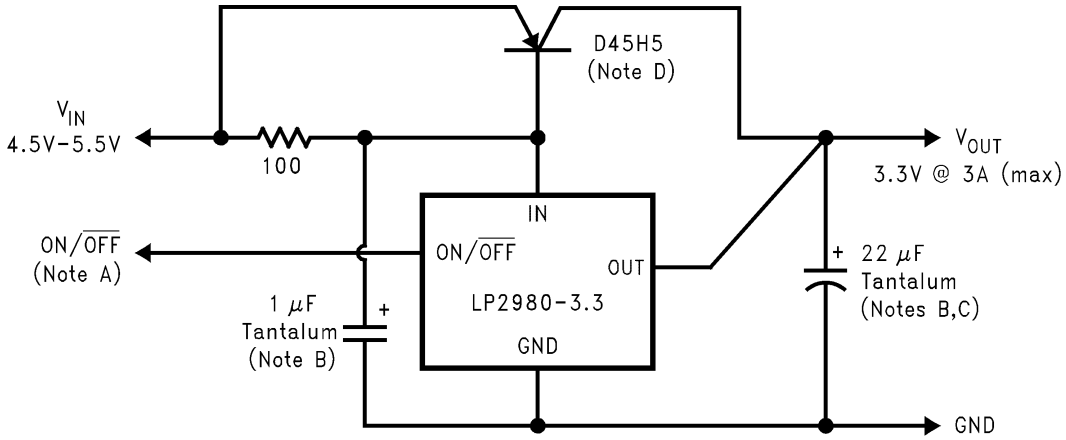


Figure 38. 5 V to 3.3 V at 3-A Converter

NOTES:

Note A: Drive this input with a logic signal (see *ON/$\overline{\text{OFF}}$ Input Operation*). If the shutdown function is not to be used, tie the ON/$\overline{\text{OFF}}$ pin directly to the IN pin.

Note B: Capacitor is required for regulator stability. Minimum size is shown, and may be increased without limit.

Note C: Increasing the output capacitance improves transient response and increases phase margin.

Note D: A heatsink may be required for this transistor. The maximum allowable value for thermal resistance of the heatsink is dependent on ambient temperature and load current (see curves in Figure 39). Once the value is obtained from the graph, a heatsink must be selected which has a thermal resistance equal to or lower than this value. If the value is above 60°C/W, no heatsink is required.

For these curves, a maximum junction temperature of 150°C is assumed for the pass transistor. The case-to-heatsink attachment thermal resistance is assumed to be 1.5°C/W. All calculations are for 5.5-V input voltage (which is worst-case for power dissipation).

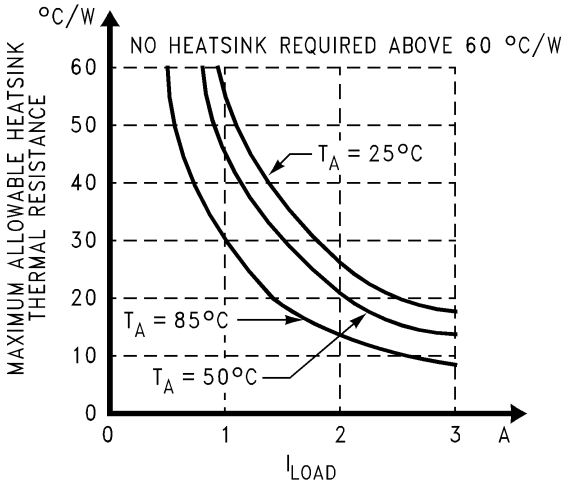


Figure 39. Heatsink Thermal Resistance Requirements for Figure 38

8.2.3 Application Curve

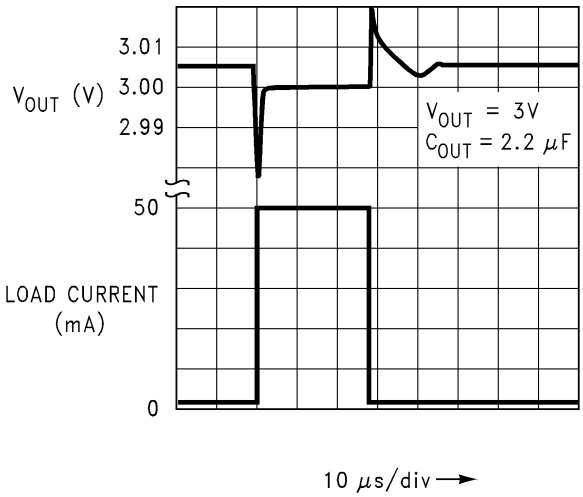


Figure 40. Load Transient Response

9 Power Supply Recommendations

The LP2980-N is designed to operate from an input voltage supply range between 2.1 V and 16 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

10.2 Layout Example

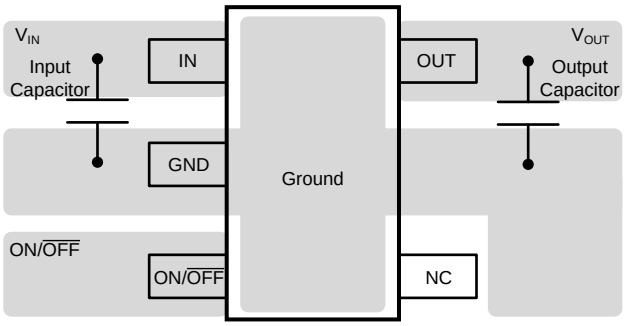


Figure 41. LP2980-N Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Receiving Notification of Documentation Updates

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The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2980AIM5-2.5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L0NA	
LP2980AIM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0NA	Samples
LP2980AIM5-3.0	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L02A	
LP2980AIM5-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L02A	Samples
LP2980AIM5-3.3	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L00A	
LP2980AIM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L00A	Samples
LP2980AIM5-4.7/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L37A	Samples
LP2980AIM5-5.0	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L01A	
LP2980AIM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L01A	Samples
LP2980AIM5X-2.5	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	L0NA	
LP2980AIM5X-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0NA	Samples
LP2980AIM5X-3.0	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	L02A	
LP2980AIM5X-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L02A	Samples
LP2980AIM5X-3.3	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	L00A	
LP2980AIM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L00A	Samples
LP2980AIM5X-4.7/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L37A	Samples
LP2980AIM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L01A	Samples
LP2980IM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0NB	Samples
LP2980IM5-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L02B	Samples
LP2980IM5-3.3	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L00B	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2980IM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L00B	Samples
LP2980IM5-3.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L21B	Samples
LP2980IM5-4.7/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L37B	Samples
LP2980IM5-5.0	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L01B	
LP2980IM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L01B	Samples
LP2980IM5X-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0NB	Samples
LP2980IM5X-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L02B	Samples
LP2980IM5X-3.3	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	L00B	
LP2980IM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L00B	Samples
LP2980IM5X-5.0	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	L01B	
LP2980IM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L01B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

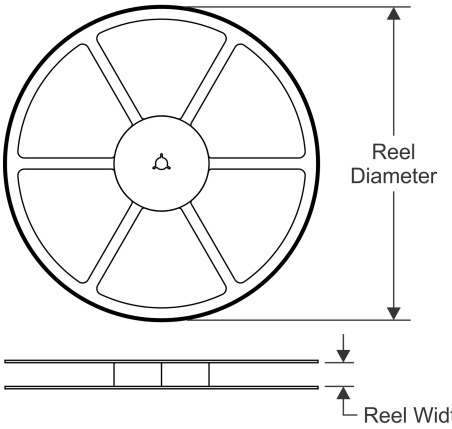
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

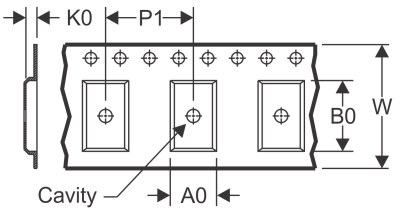
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

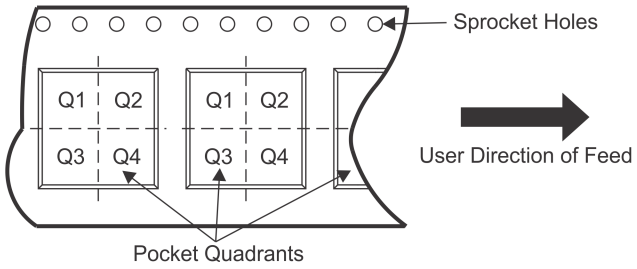


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

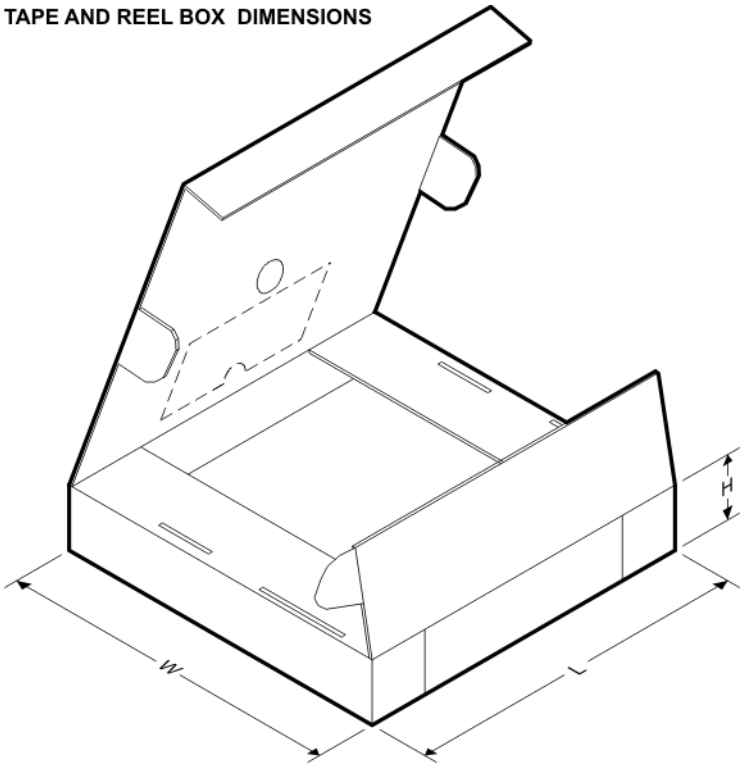


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2980AIM5-2.5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980AIM5-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980AIM5-3.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980AIM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980AIM5-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980AIM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980AIM5-4.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980AIM5-5.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980AIM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980AIM5X-2.5	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980AIM5X-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980AIM5X-3.0	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980AIM5X-3.3	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980AIM5X-4.7/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2980IM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5-3.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5-4.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5-5.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5X-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5X-3.3	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5X-5.0	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2980IM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2980AIM5-2.5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980AIM5-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980AIM5-3.0	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980AIM5-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0

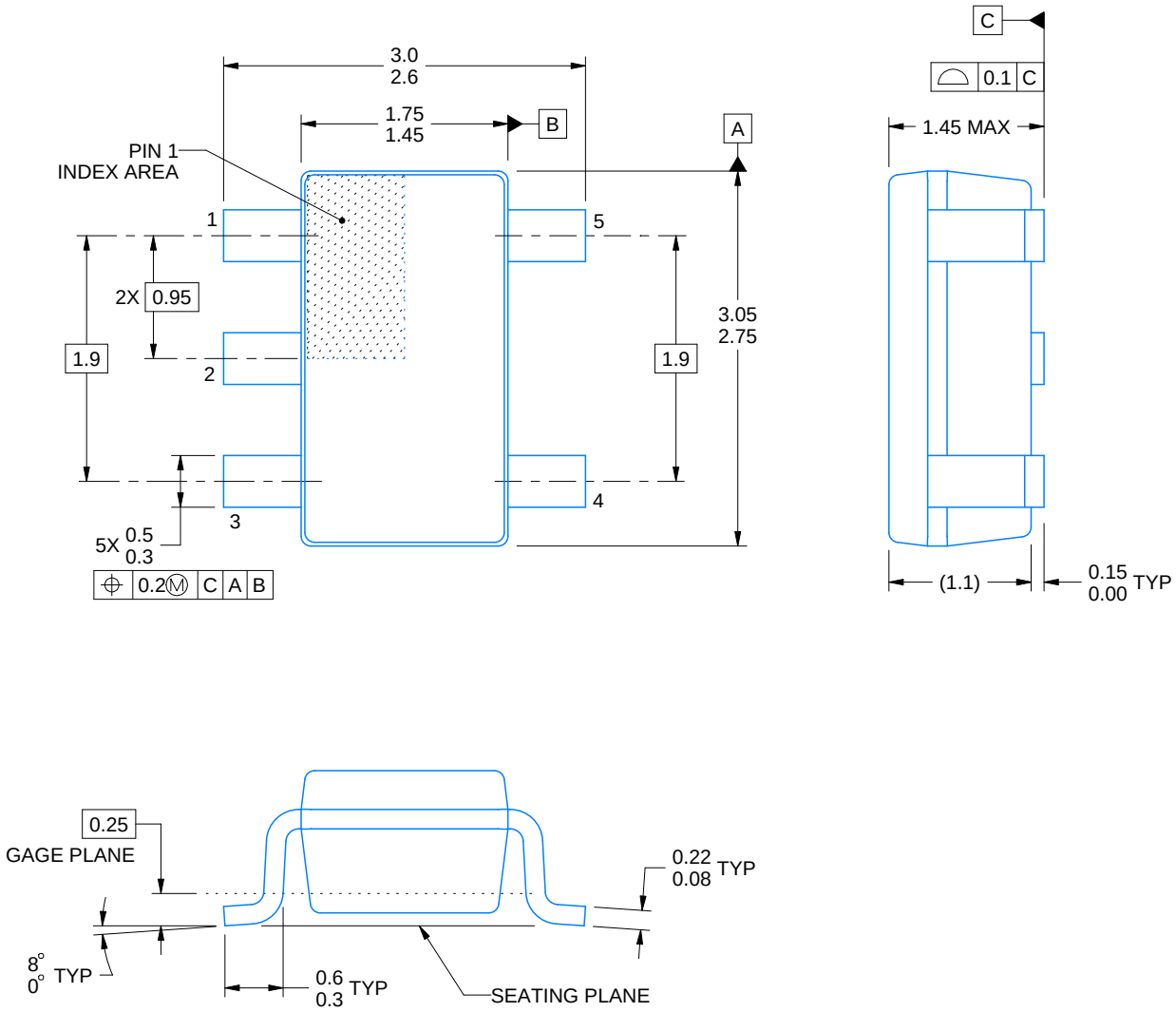
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2980AIM5-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980AIM5-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980AIM5-4.7/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980AIM5-5.0	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980AIM5-5.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980AIM5X-2.5	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2980AIM5X-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2980AIM5X-3.0	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2980AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2980AIM5X-3.3	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2980AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2980AIM5X-4.7/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2980AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2980IM5-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980IM5-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980IM5-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980IM5-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980IM5-3.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980IM5-4.7/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980IM5-5.0	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980IM5-5.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2980IM5X-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2980IM5X-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2980IM5X-3.3	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2980IM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2980IM5X-5.0	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2980IM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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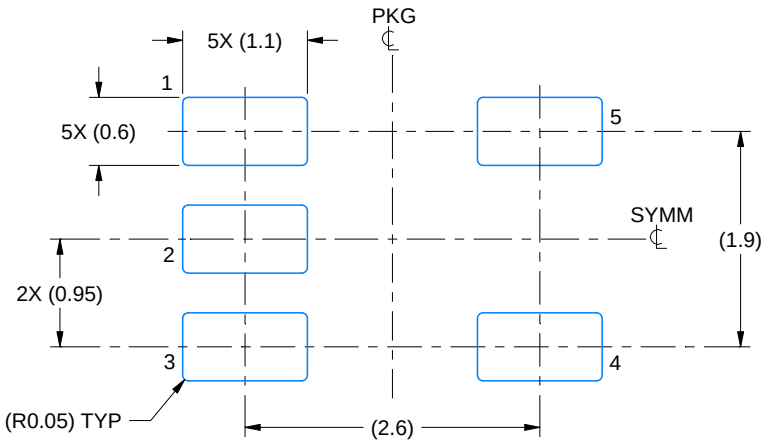
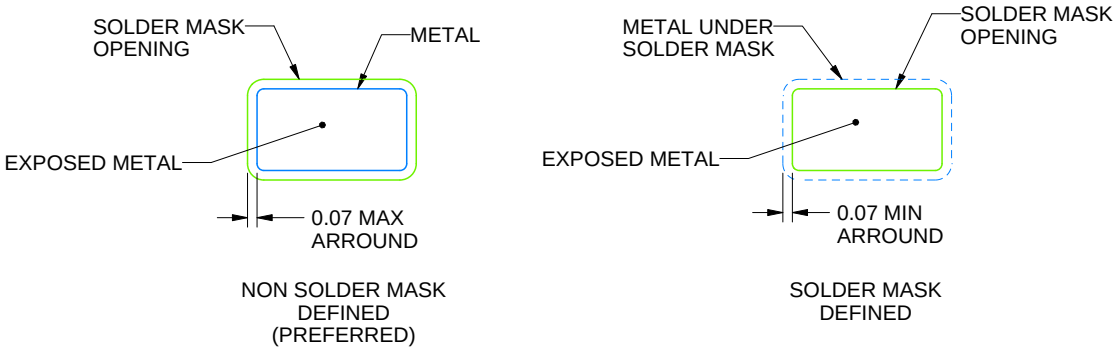
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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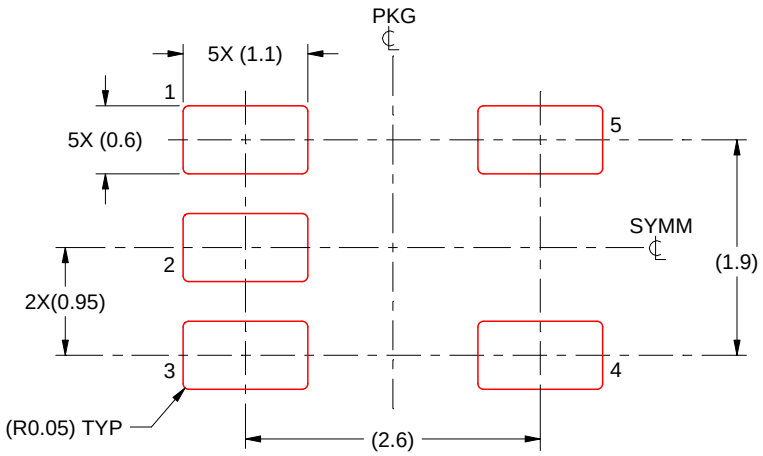
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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