# LM2682 Switched Capacitor Voltage Doubling Inverter

**Check for Samples: LM2682**

## FEATURES

- **Inverts Then Doubles Input Supply Voltage**
- **Small VSSOP Package and SOIC Package**
- **90Ω Typical Output Impedance**
- **94% Typical Power Efficiency at 10 mA**

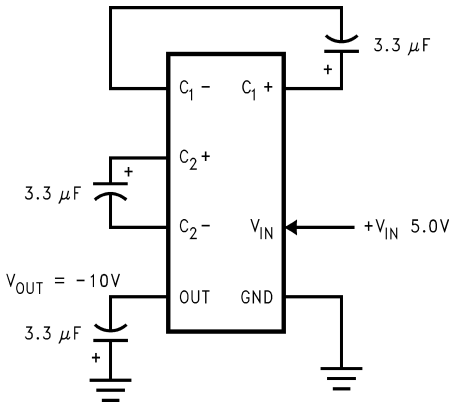
## APPLICATIONS

- **LCD Contrast Biasing**
- **GaAs Power Amplifier Biasing**
- **Interface Power Supplies**
- **Handheld Instrumentation**
- **Laptop Computers and PDAs**

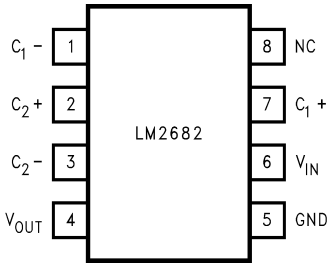
## DESCRIPTION

The LM2682 is a CMOS charge-pump voltage inverter capable of converting positive voltage in the range of +2.0V to +5.5V to the corresponding doubled negative voltage of −4.0V to −11.0V respectively. The LM2682 uses three low cost capacitors to provide 10 mA of output current without the cost, size, and EMI related to inductor based circuits. With an operating current of only 150 µA and an operating efficiency greater than 90% with most loads, the LM2682 provides ideal performance for battery powered systems. The LM2682 offers a switching frequency of 6 kHz.

### Typical Operating Circuit and Pin Configuration




**8-Pin VSSOP or 8-Pin SOIC**




These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

## Absolute Maximum Ratings(1)

| | | |
|---|---|---|
| Input Voltage ($V_{IN}$) | | +5.8V |
| $V_{IN}$ dV/dT | | 1V/µsec |
| $V_{OUT}$ | | −11.6V |
| $V_{OUT}$ Short-Circuit Duration | | Continuous |
| Storage Temperature | | −65°C to +150°C |
| Lead Temperature Soldering | | +300°C |
| Power Dissipation(2) | VSSOP | 300 mW |
| | SOIC | 470 mW |
| $T_{JMAX}$ | | +150°C |

(1) Absolute Maximum Ratings are those values beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.

(2) The maximum power dissipation must be de-rated at elevated temperatures (only needed for $T_A$>85°C) and is limited by $T_{JMAX}$ (maximum junction temperature), $\theta_{J-A}$ (junction to ambient thermal resistance) and $T_A$ (ambient temperature). $\theta_{J-A}$ is 140°C/W for the SOIC-8 package and 220°C/W for the VSSOP-8 package. The maximum power dissipation at any temperature is:$PDiss_{MAX} = (T_{JMAX} - T_A)/\theta_{J-A}$ up to the value listed in the Absolute Maximum Ratings.

## Operating Ratings

| | | |
|---|---|---|
| ESD Susceptibility(1) | Human Body Model | 2 kV |
| | Machine Model | 200V |
| Ambient Temp. Range | | −40°C to +85°C |
| Junction Temp. Range | | −40°C to +125°C |

(1) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

## LM2682 Electrical Characteristics

$V_{IN}$ = 5V and $C_1 = C_2 = C_3$ = 3.3µF unless otherwise specified. Limits with **bold typeface** apply over the full operating ambient temperature range, −40°C to +85°C, limits with standard typeface apply for $T_A$ = 25°C.

| Symbol | Parameter | Conditions | Min | Typical(1) | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Supply Voltage Range | $R_L$ = 2 kΩ | **2.0** | | **5.5** | V |
| $I_{IN}$ | Supply Current | Open Circuit, No Load | | 150 | 300<br>**400** | µA |
| $R_{OUT}$ | $V_{OUT}$ Source Resistance | $I_L$ = 10 mA | | 90 | 150<br>**200** | Ω |
| | | $I_L$=5 mA, $V_{IN}$=2 V | | 110 | **250** | Ω |
| $f_{OSC}$ | Oscillator Frequency | See(2) | | 12 | **30** | kHz |
| $f_{SW}$ | Switching Frequency | See(2) | | 6 | **15** | kHz |
| $\eta_{POWER}$ | Power Efficiency | $R_L$ = 2k(3) | 90 | 93 | | % |
| $\eta_{VOLTAGE}$ | Voltage Conversion Efficiency | | | 99.9 | | % |

(1) Typical numbers are at 25°C and represent the most likely norm.
(2) The output switches operate at one half of the oscillator frequency, $f_{OSC} = 2f_{SW}$.
(3) The minimum specification is specified by design and is not tested.

**Table 1. PIN DESCRIPTIONS**

| Pin Number | Symbol | Description |
|---|---|---|
| 1 | $C_1-$ | Capacitor $C_1$ negative terminal |
| 2 | $C_2+$ | Capacitor $C_2$ positive terminal |
| 3 | $C_2-$ | Capacitor $C_2$ negative terminal |
| 4 | $V_{OUT}$ | Negative output voltage ($-2V_{IN}$) |
| 5 | GND | Device ground |
| 6 | $V_{IN}$ | Power supply voltage |
| 7 | $C_1+$ | Capacitor $C_1$ positive terminal |
| 8 | NC | No Connection |

## Typical Performance Characteristics

$V_{IN}$ = 5V and $T_A$ = 25°C unless otherwise noted.

**Output Resistance vs Input Voltage**

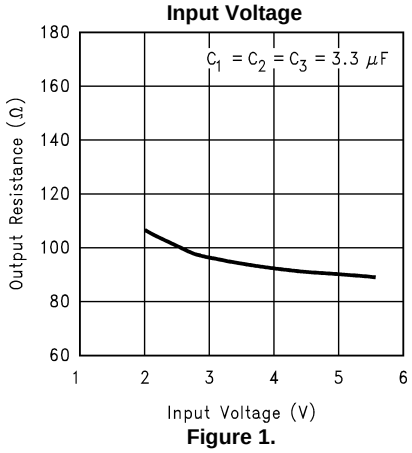



**Figure 1.**

**Output Voltage vs Load Current**

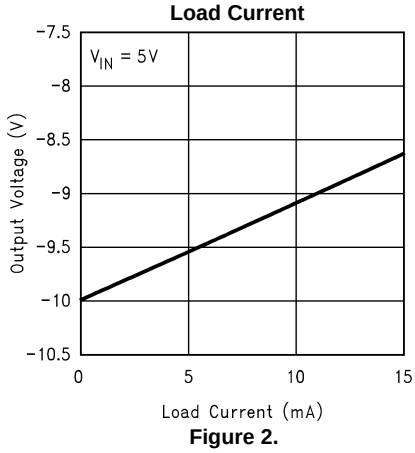



**Figure 2.**

**Supply Current vs Input Voltage**

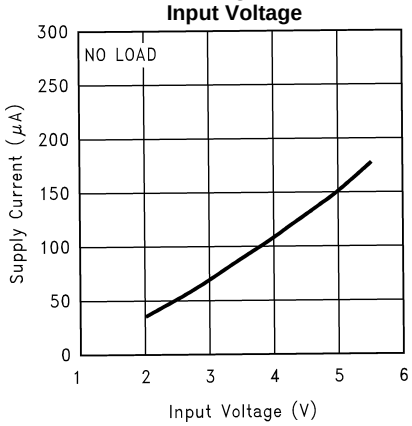



**Figure 3.**

**Output Resistance vs Temperature**

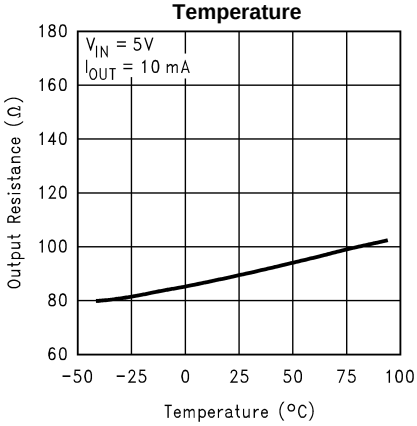



**Figure 4.**

**Output Voltage Ripple vs Load Current**

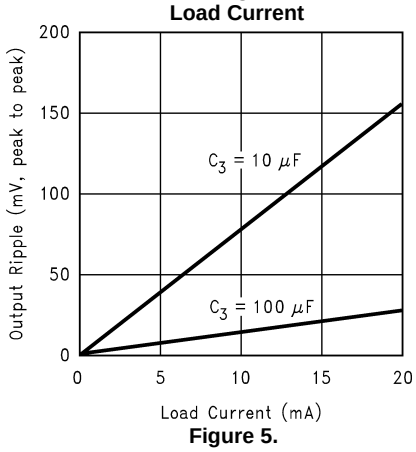



**Figure 5.**

## BASIC APPLICATION CIRCUITS

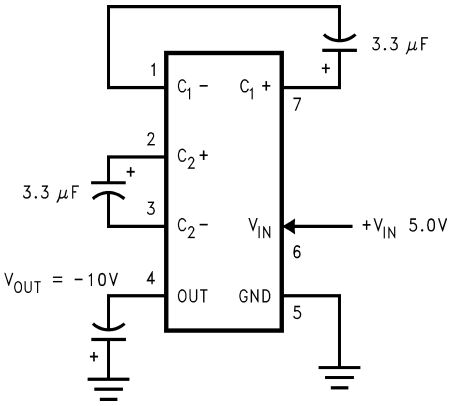



**Figure 6. Doubling Voltage Inverter**

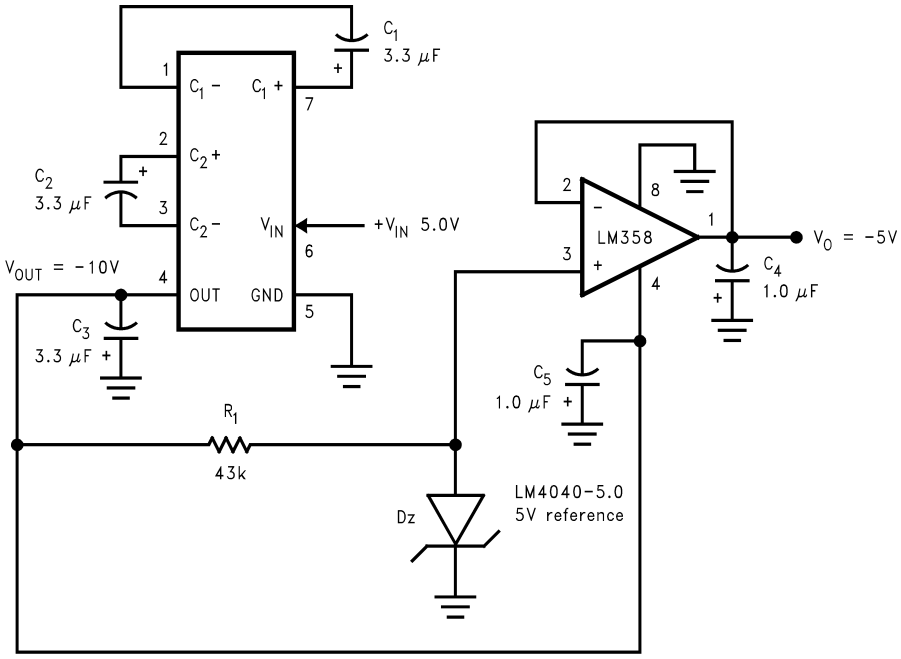



**Figure 7. +5V to −5V Regulated Voltage Converter**

## APPLICATION INFORMATION

### VOLTAGE DOUBLING INVERTER

The main application of the LM2682 is to generate a negative voltage that is twice the positive input voltage. This circuit requires only three external capacitors and is connected as shown in Figure 6. It is important to keep in mind that the efficiency of the circuit is determined by the output resistance. A derivation of the output resistance is shown below:

$R_{OUT} = 2(R_{SW1}+R_{SW2}+ESR_{C1}+R_{SW3}+R_{SW4}+ESR_{C2}) +2(R_{SW1}+R_{SW2}+ESR_{C1}+R_{SW3}+R_{SW4}+ESR_{C2}) + 1/(f_{OSC}\times C1) + 1/(f_{OSC}\times C2) + ESR_{C3}$

Using the assumption that all four switches have the same ON resistance our equation becomes:

$R_{OUT} = 16R_{SW} + 4ESR_{C1} + 4ESR_{C2} + ESR_{C3} + 1/(f_{OSC}\times C1) + 1/(f_{OSC}\times C2)$

Output resistance is typically 90Ω with an input voltage of +5V, an operating temperature of 25°C, and using low ESR 3.3 µF capacitors. This equation shows the importance of capacitor selection. Large value, low ESR capacitors will reduce the output resistance significantly but will also require a larger overall circuit. Smaller capacitors will take up less space but can lower efficiency greatly if the ESR is large. Also to be considered is that C1 must be rated at 6 VDC or greater while C2 and C3 must be rated at 12 VDC or greater.

The amount of output voltage ripple is determined by the output capacitor C3 and the output current as shown in this equation:

$V_{RIPPLE\ P-P} = I_{OUT} \times (2\times ESR_{C3} + 1/[2\times(f_{OSC}\times C3)])$

Once again a larger capacitor with smaller ESR will give better results.

### +5V TO −5V REGULATED VOLTAGE CONVERTER

Another application in which the LM2682 can be used is for generating a −5V regulated supply from a +5V unregulated supply. This involves using an op-amp and a reference and is connected as shown in Figure 7. The LM358 op-amp was chosen for its low cost and versatility and the LM4040-5.0 reference was chosen for its low bias current requirement. Of course other combinations may be used at the designer's discretion to fit accuracy, efficiency, and cost requirements. With this configuration the circuit is well regulated and is still capable of providing nearly 10 mA of output current. With a 9 mA load the circuit can typically maintain 5% regulation on the output voltage with the input varying anywhere from 4.5V to the maximum of 5.5V. With less load the results are even better. Voltage ripple concerns are reduced in this case since the ripple at the output of the LM2682 is reduced at the output by the PSRR of the op-amp used.

## PARALLELING DEVICES

Any number of devices can be paralleled to reduce the output resistance. As shown in Figure 8, each device must have its own pumping capacitors, C1 and C2, but only one shared output capacitor is required. The effective output resistance is the output resistance of one device divided by the number of devices used in parallel. Paralleling devices also gives the capability of increasing the maximum output current. The maximum output current now becomes the maximum output current for one device multiplied by the number of devices used in parallel. For example, if you parallel two devices you can get 20 mA of output current and have half the output resistance of one device supplying 10 mA.

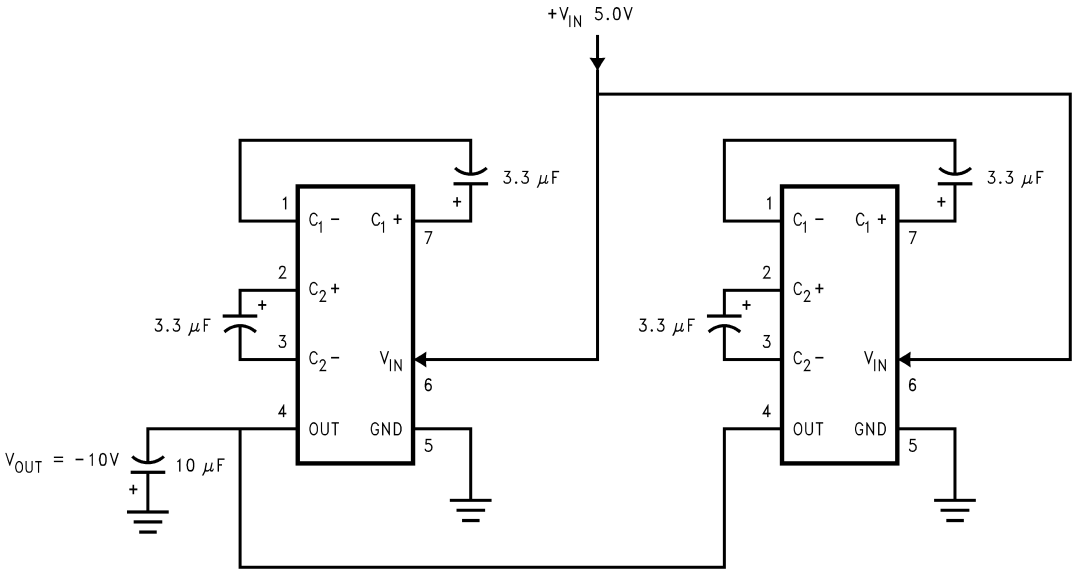



**Figure 8. Paralleling Devices**

## REVISION HISTORY

| Changes from Revision A (May 2013) to Revision B | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 7 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM2682MM/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | S11A | Samples |
| LM2682MMX/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | S11A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

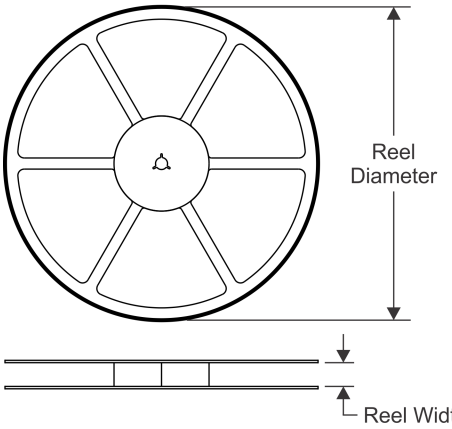
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

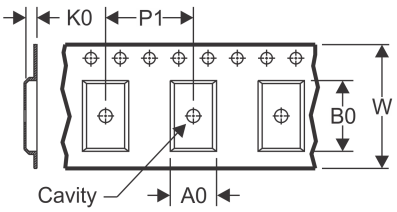
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

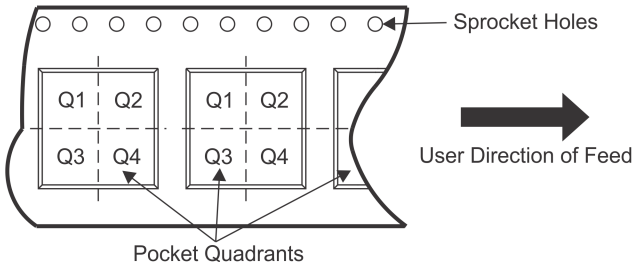



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

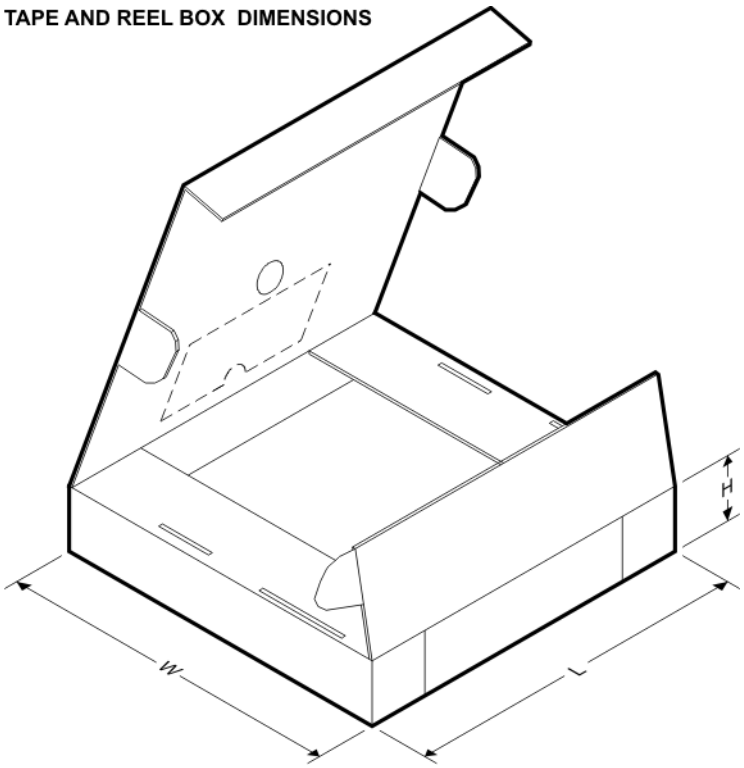
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM2682MM/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LM2682MMX/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

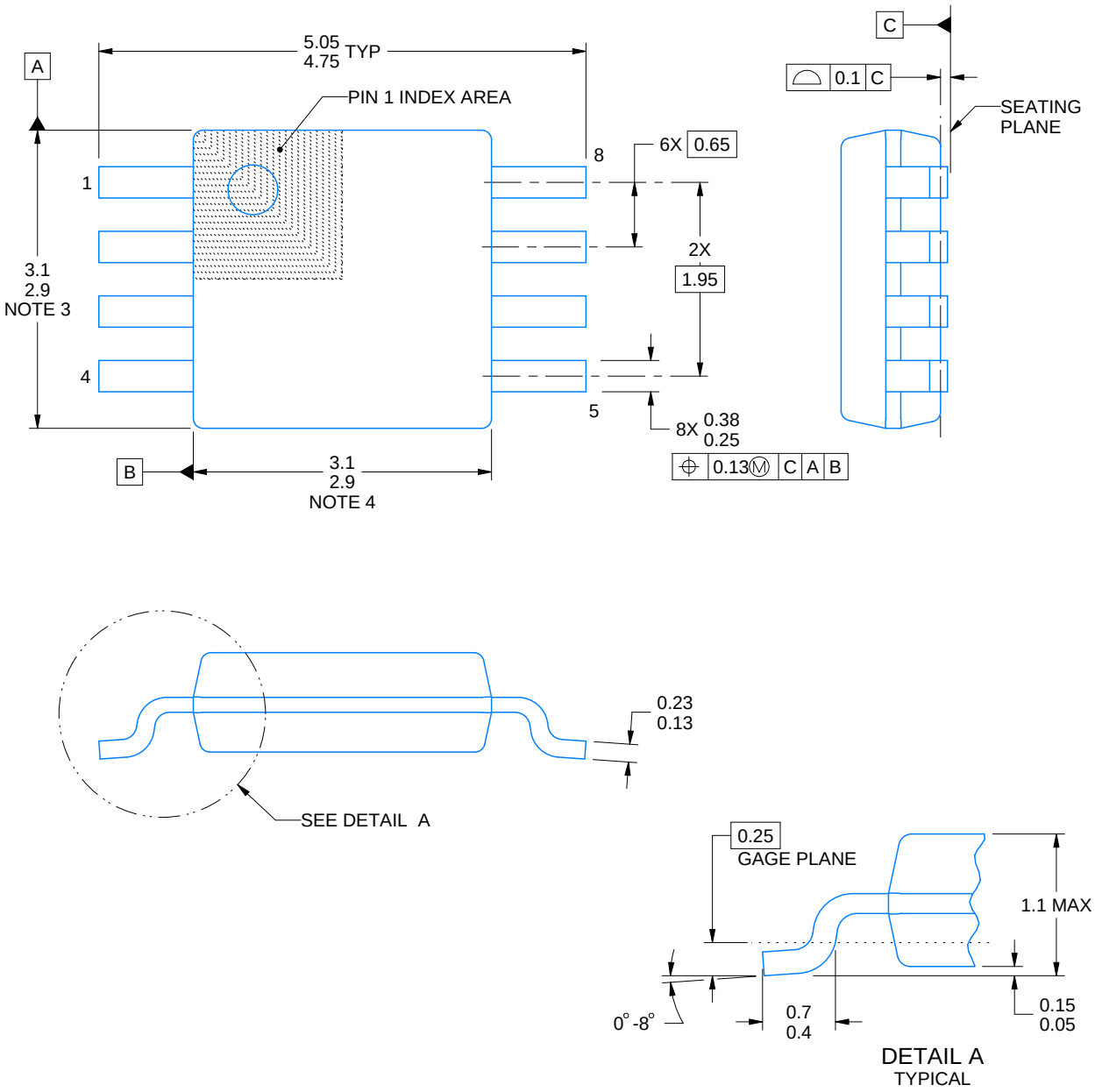
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM2682MM/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LM2682MMX/NOPB | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

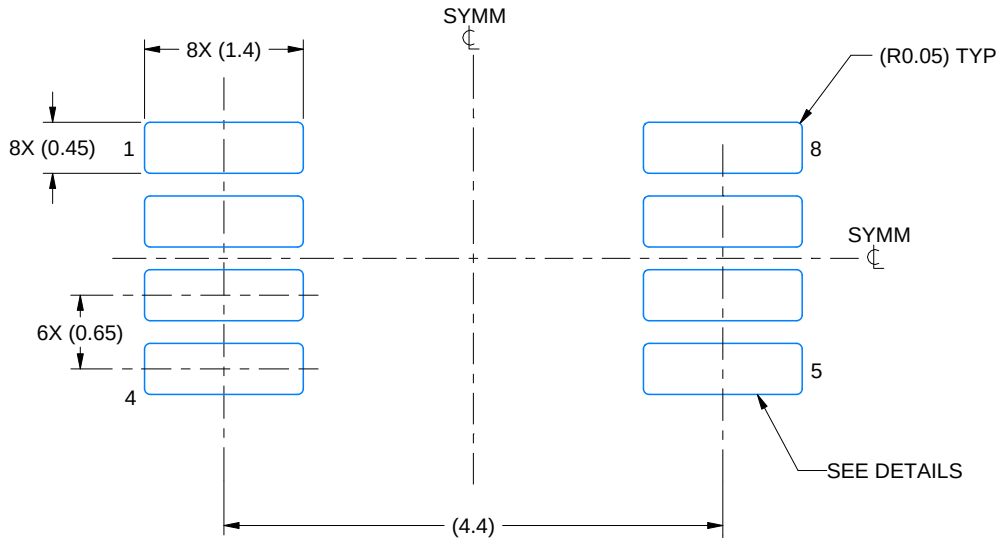
SMALL OUTLINE PACKAGE



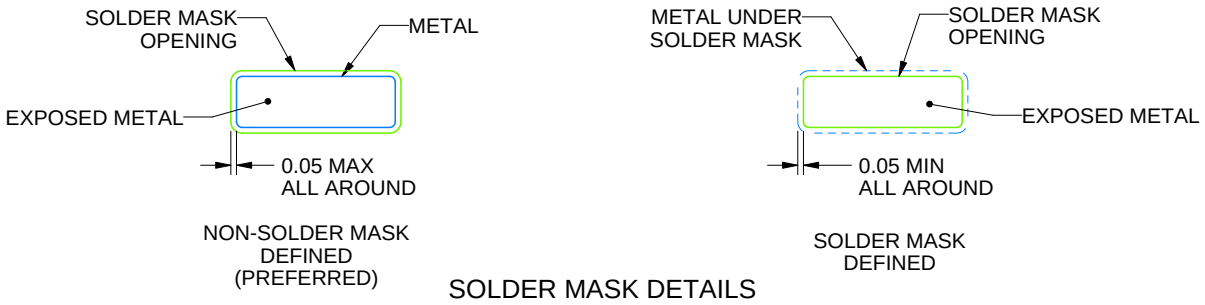

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

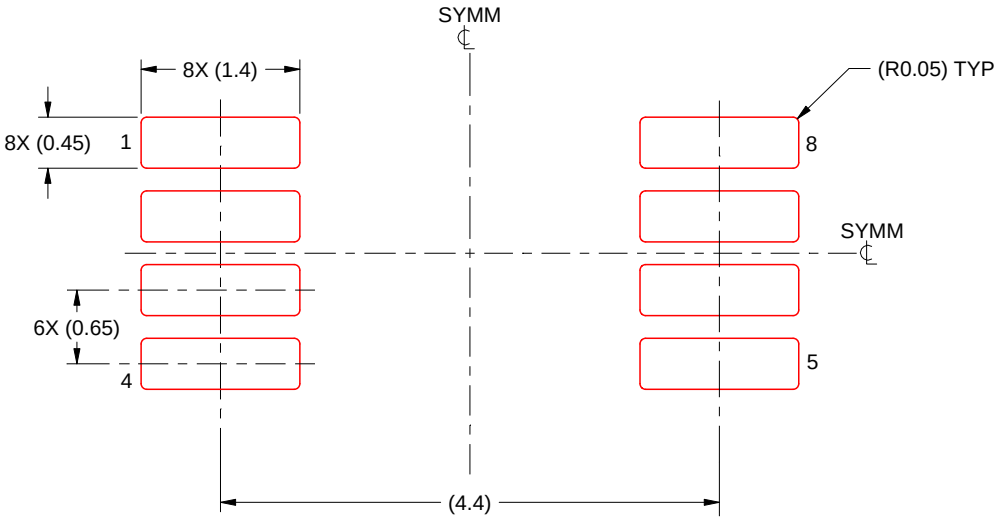



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265