Peregrine Semiconductor

SPDT UltraCMOS™ RF Switch
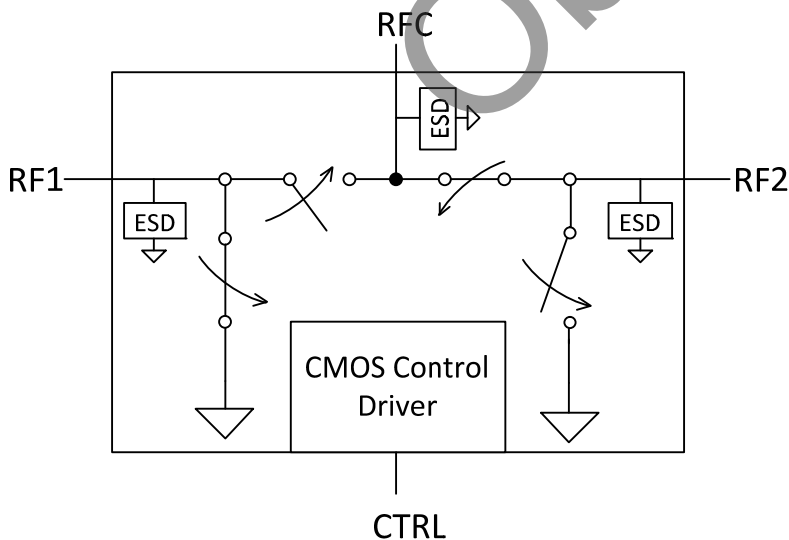**10 MHz - 3 GHz**

Features

- Single 3-volt power supply

- Low Insertion loss: 0.30 dB at 1000 MHz, 0.45 dB at 2000 MHz

- High isolation of 35 dB at 1000 MHz, 25 dB at 2000 MHz

- Typical input 1 dB compression point of +14.5 dBm

- Single-pin CMOS or TTL logic control

- Packaged in a small 8-lead MSOP

Product Description

The PE4210 UltraCMOS™ RF Switch is designed to cover a broad range of applications from 10 MHz to 3 GHz. This single-supply switch integrates on-board CMOS control logic driven by a simple, single-pin CMOS or TTL compatible control input. Using a nominal +3-volt power supply, a typical input 1 dB compression point of +14 dBm can be achieved. The PE4210 also exhibits input-output isolation of better than 35 dB at 1000 MHz and is offered in a small 8-lead MSOP package.

The PE4210 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

71-0014-01

Figure 2. Package Type
8-lead MSOP

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Table 1. Electrical Specifications @ +25 °C, V_{DD} = 3 V ($Z_S = Z_L = 50\ \Omega$)

Parameter	Conditions	Min	Typ	Max	Units
Operating Frequency[1]		10		3000	MHz
Insertion Loss	1000 MHz 2000 MHz		0.30 0.45	0.40 0.60	dB dB
Isolation – RFC to RF1/RF2	1000 MHz 2000 MHz	34.5 24.5	35.5 25		dB dB
Isolation – RF1 to RF2	1000 MHz 2000 MHz	36.5 25.5	37.5 26.5		dB dB
Return Loss	1000 MHz 2000 MHz	22.5 15	24.5 16		dB dB
'ON' Switching Time	CTRL to 0.1 dB final value, 2 GHz		200		ns
'OFF' Switching Time	CTRL to 25 dB isolation, 2 GHz		90		ns
Video Feedthrough[2]			2.5		mV_{pp}
Input 1 dB Compression	2000 MHz	13	14.5		dBm
Input IP3	2000 MHz, 5 dBm	30	33.5		dBm

Notes: 1. Device linearity will begin to degrade below 10 MHz.
2. The DC transient at the output of any port of the switch when the control voltage is switched from Low to High or High to Low in a 50 Ω test set-up, measured with 1 ns risetime pulses and 500 MHz bandwidth.

Table 2. DC Electrical Specifications

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	2.7	3.0	3.3	V
I_{DD} Power Supply Current (V_{DD} = 3 V, V_{CNTL} = 3)		250	500	nA
Control Voltage High	0.7x V_{DD}			V
Control Voltage Low			0.3x V_{DD}	V

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Figure 3. Pin Configuration (Top View)
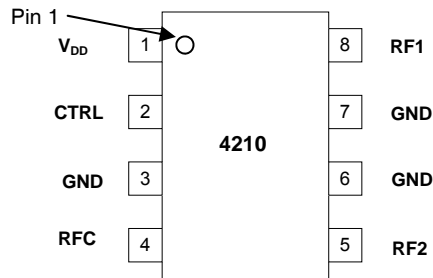
Table 3. Pin Descriptions

Pin No.	Pin Name	Description
1	V_{DD}	Nominal 3 V supply connection. A bypass capacitor (100 pF) to the ground plane should be placed as close as possible to the pin
2	CTRL	CMOS or TTL logic level: High = RFC to RF1 signal path Low = RFC to RF2 signal path
3	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
4	RFC	Common RF port for switch[1]
5	RF2	RF2 port[1]
6	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
7	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
8	RF1[1]	RF1 port

Note 1. All RF pins must be DC blocked with an external series capacitor or held at 0 V_{DC}.

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power Supply Voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	$V_{DD} + 0.3$	V
T_{ST}	Storage temperature range	-65	+150	°C
T_{OP}	Operating temperature range	-40	+85	°C
P_{IN}	Input power (50 Ω)		18	dBm
V_{ESD}[1]	HBM ESD Voltage	200		V

Note: 1. Human Body Model ESD Voltage (HBM, MIL_STD 883 Method 3015.7)

Exceeding absolute maximum ratings may cause permanent damage. Functional operation should be restricted to the limits in the DC Electrical Specifications table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 5. Control Logic Truth Table

Control Voltage	Signal Path
CTRL = CMOS or TTL High	RFC to RF1
CTRL = CMOS or TTL Low	RFC to RF2

Control Logic

The control logic input pin (CTRL) is typically driven by a 3-volt CMOS logic level signal, and has a threshold of 50% of V_{DD}. For flexibility to support systems that have 5-volt control logic drivers, the control logic input has been designed to handle a 5-volt logic HIGH signal. (A minimal current will be sourced out of the V_{DD} pin when the control logic input voltage level exceeds V_{DD}.)

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE4210 in the 8-lead 3 x 3 mm MSOP package is MSL1.

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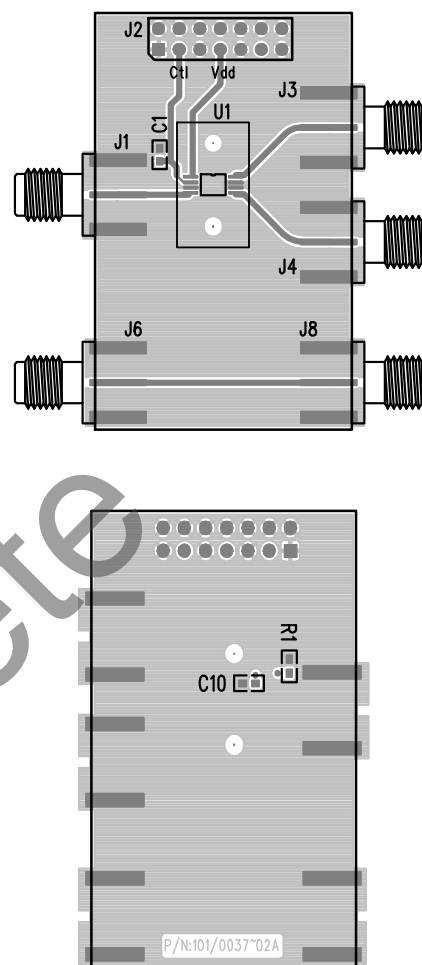
Evaluation Kit

The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE4210 SPDT switch. The RF common port is connected through a 50 Ω transmission line to the top left SMA connector, J1. Port 1 and Port 2 are connected through 50 Ω transmission lines to the top two SMA connectors on the right side of the board, J3 and J4. A through transmission line connects SMA connectors J6 and J8. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide model with a trace width of 0.030", trace gaps of 0.007", dielectric thickness of 0.028", metal thickness of 0.0014" and ε_r of 4.4. Note that the predominate mode for these transmission lines is coplanar waveguide with a ground plane.

J2 provides a means for controlling DC and digital inputs to the device. Starting from the lower left pin, the second pin to the right (J2-3) is connected to the device CTRL input. The fourth pin to the right (J2-7) is connected to the device V_{DD} input. A decoupling capacitor (100 pF) is provided on both CTRL and V_{DD} traces. It is the responsibility of the customer to determine proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

Figure 4. Evaluation Board Layout

101-0037

Figure 5. Evaluation Board Schematic

102-0035

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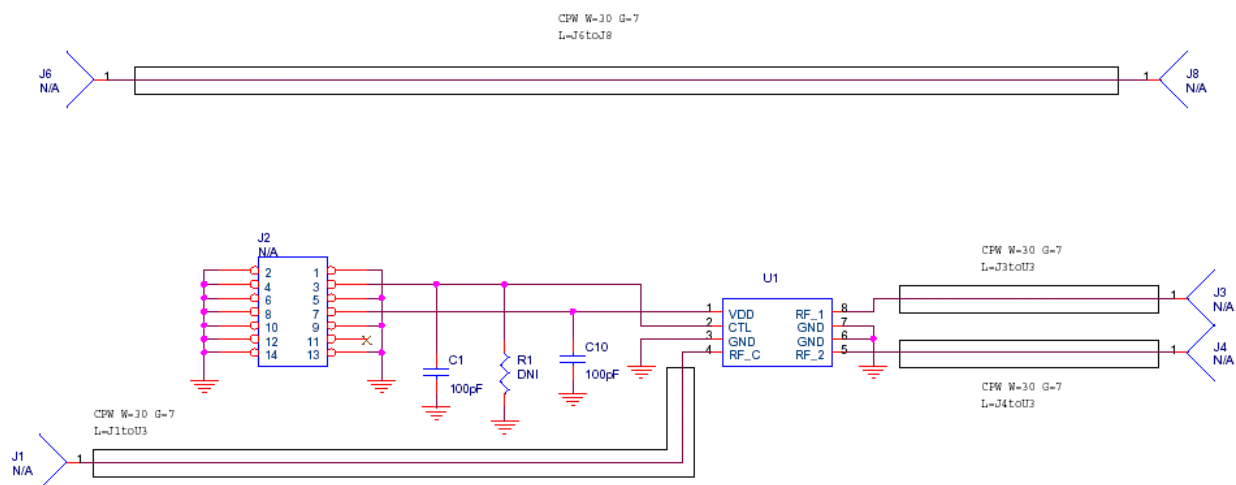
Typical Performance Data @ -40 °C to 85 °C (unless otherwise noted)

Figure 6. Insertion Loss – RFC to RF1
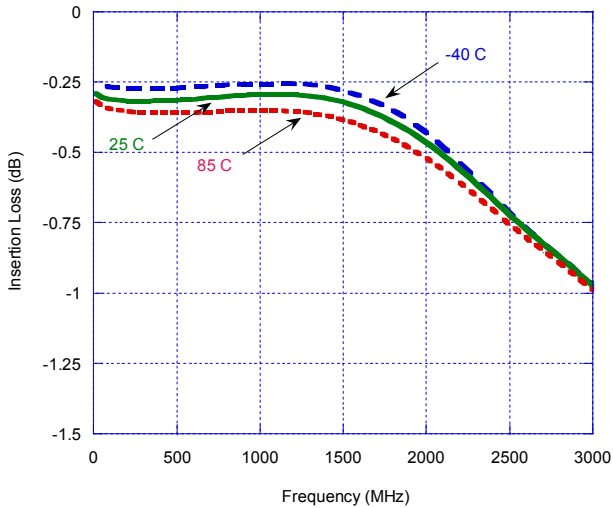
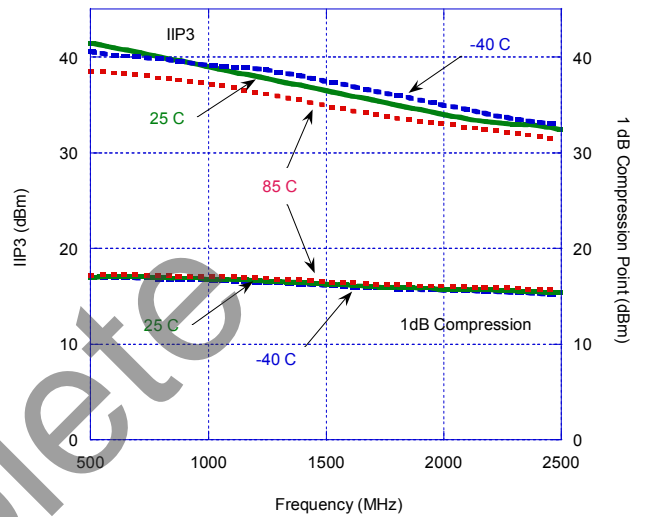### Figure 7. Input 1 dB Compression Point & IIP3
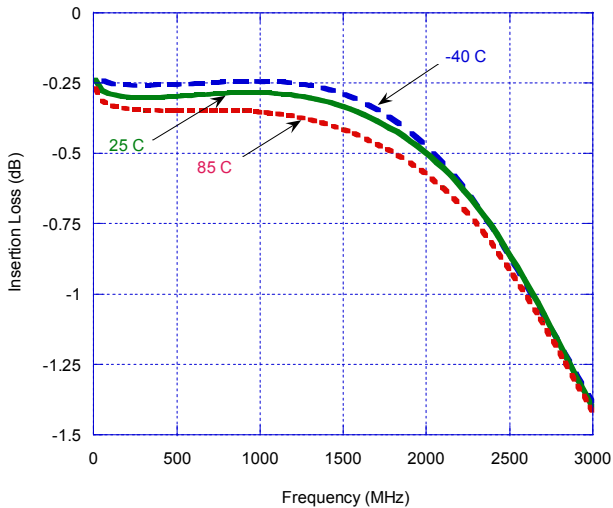

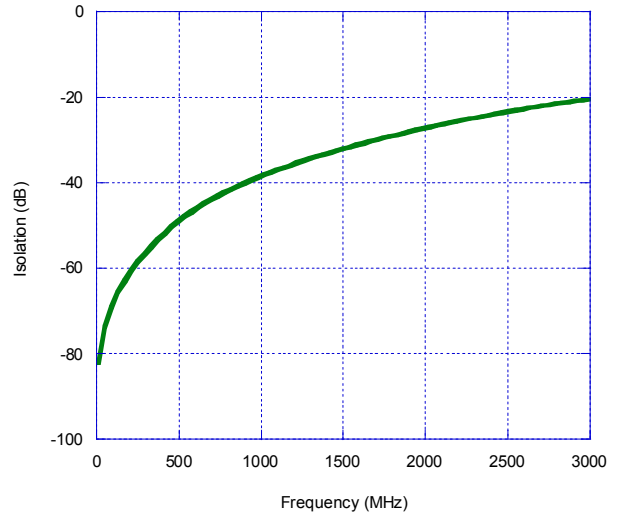### Figure 8. Insertion Loss – RFC to RF2

Figure 9. Isolation – RFC to RF1
T = 25 °C

Typical Performance Data @ 25 °C
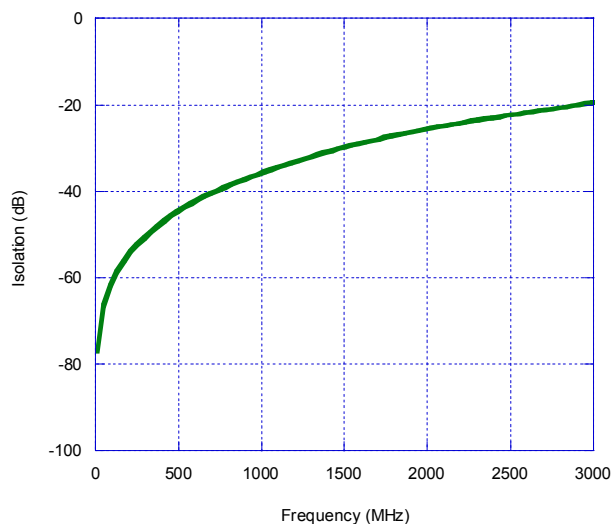
Figure 10. Isolation – RFC to RF2
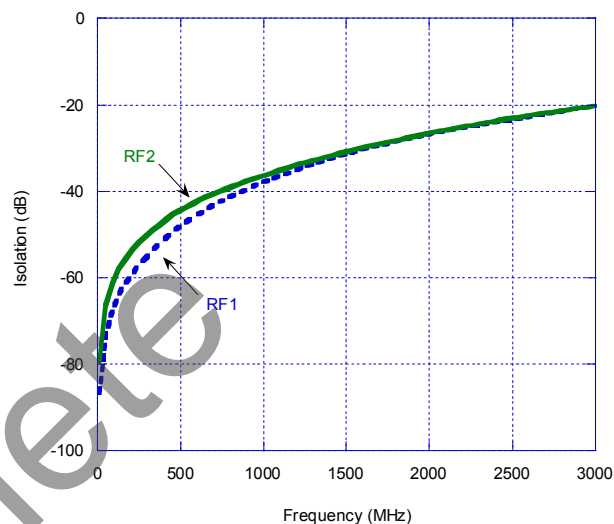

Figure 11. Isolation – RF1 to RF2, RF2 to RF1
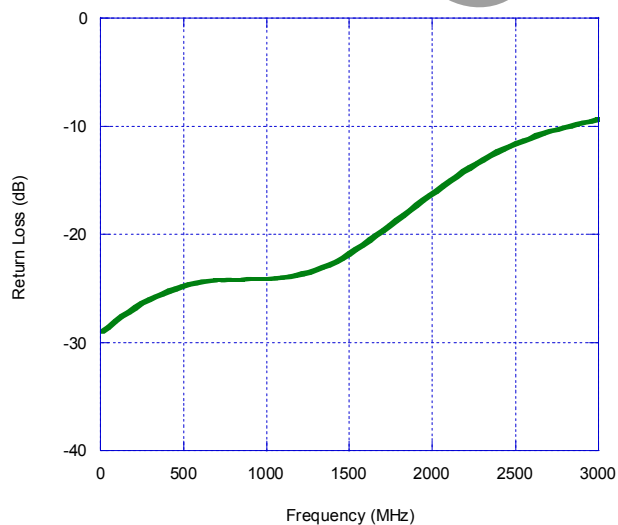

Figure 12. Return Loss – RFC to RF1, RF2

Figure 13. Return Loss – RF1, RF2

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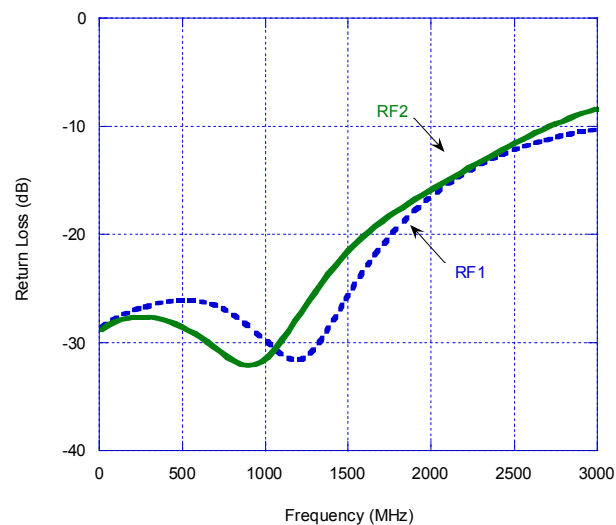
Figure 14. Package Drawing
8-lead MSOP
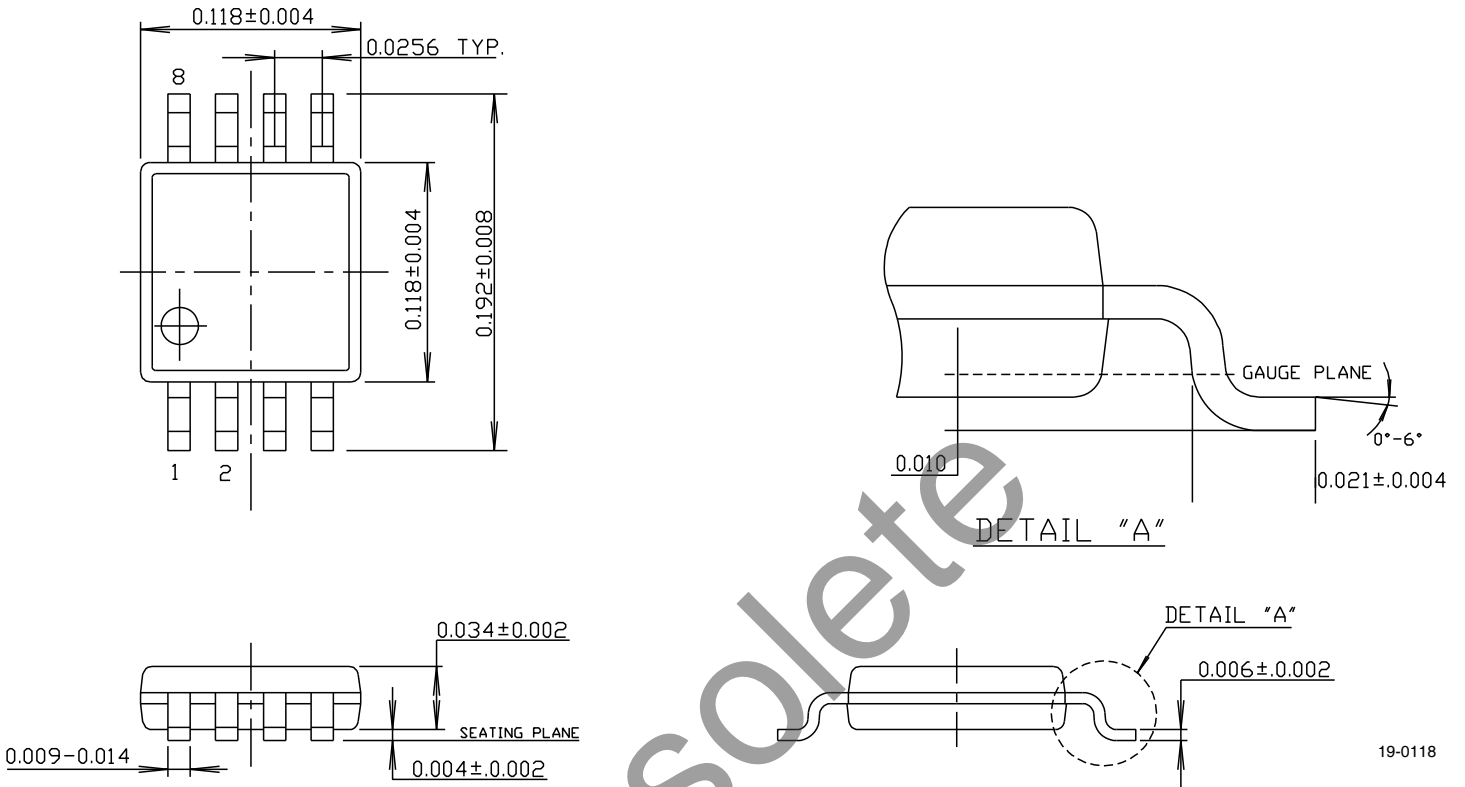
Figure 15. Marking Specifications

LLLL = Last four digits of the Assembly lot number
YWW = Date Code, last digit of the year and work week

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Figure 16. Tape and Reel Drawing

	Nominal	Tolerance
Ao	5.3	±0.10
Bo	3.4	±0.10
Ko	1.4	±0.10

Notes: Units are millimeters
Drawings not drawn to scale

Device Orientation in Tape
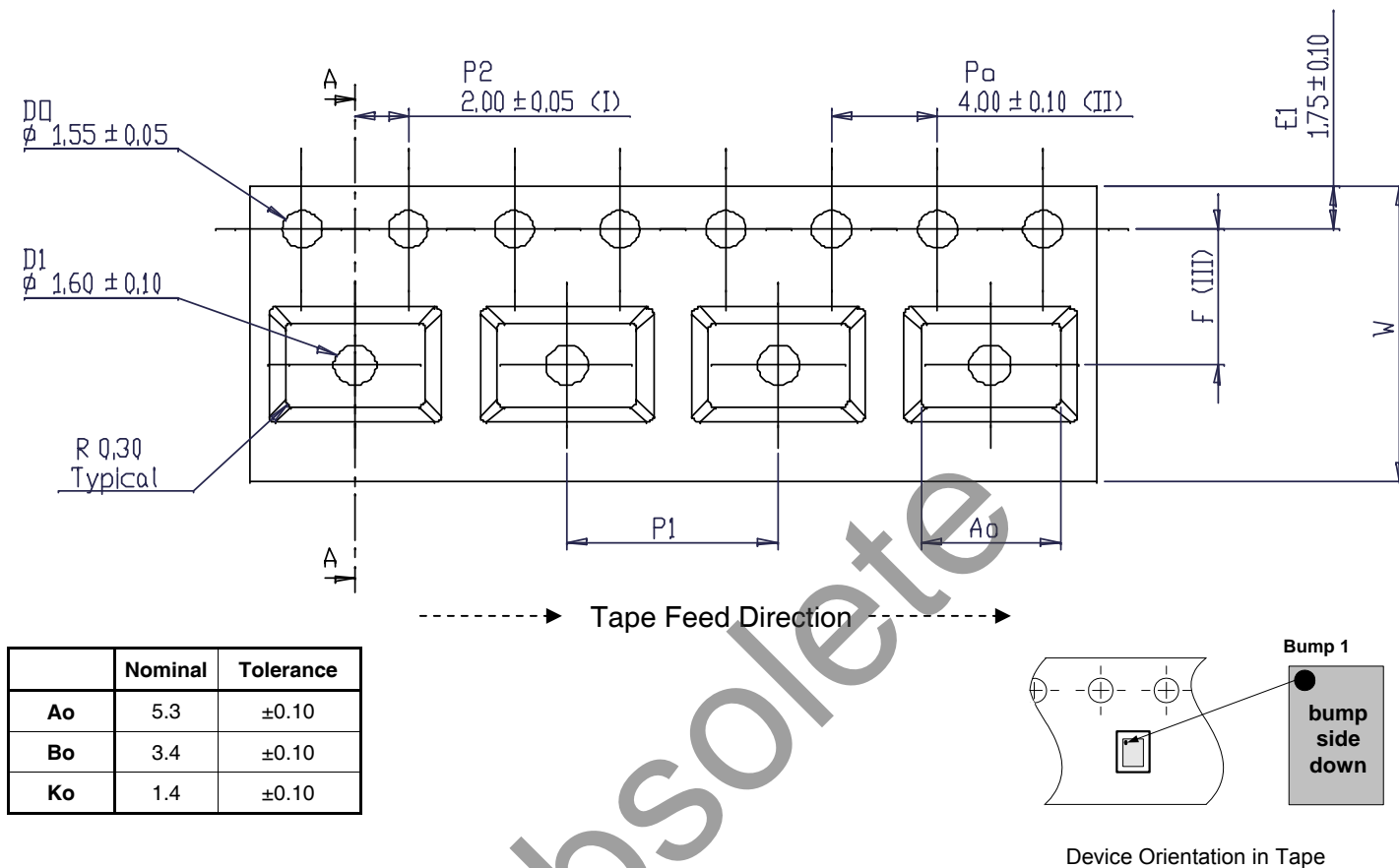
Table 6. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4210-00	PE4210-EK	PE4210-08MSOP-EK	Evaluation Kit	1 / Box
4210-52	4210	PE4210G-08MSOP-2000C	Green 8-lead MSOP	2000 units / T&R

Sales Contact and Information

For sales and contact information please visit www.psemi.com.