

## N-Channel 100 V (D-S) 175 °C MOSFET

### PRODUCT SUMMARY

V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
100	0.0165 at V <sub>GS</sub> = 10 V	60
	0.0190 at V <sub>GS</sub> = 6 V	56

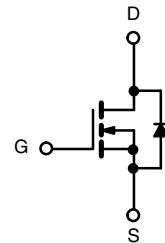
### FEATURES

- TrenchFET® Power MOSFETS
- 175 °C Junction Temperature
- Low Thermal Resistance Package
- PWM Optimized for Fast Switching
- 100 % R<sub>g</sub> and UIS Tested
- Compliant to RoHS Directive 2002/95/EC


**RoHS**  
COMPLIANT

### APPLICATIONS

- Isolated DC/DC converters
  - Primary-Side Switch


**Ordering Information:** SUM60N10-17-E3 (Lead (Pb)-free)


N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	100	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 175 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	60 <sup>a</sup>	A
		T <sub>C</sub> = 125 °C	34 <sup>a</sup>	
Pulsed Drain Current	I <sub>DM</sub>	100		
Avalanche Current	I <sub>AS</sub>	40		
Single Pulse Avalanche Energy <sup>b</sup>	L = 0.1 mH	E <sub>AS</sub>	80	mJ
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	P <sub>D</sub>	150 <sup>c</sup>	W
	T <sub>A</sub> = 25 °C <sup>d</sup>		3.75	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C	

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient	R <sub>thJA</sub>	40	°C/W
Junction-to-Case (Drain)	R <sub>thJC</sub>	1.0	

Notes:

- Package limited.
- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).

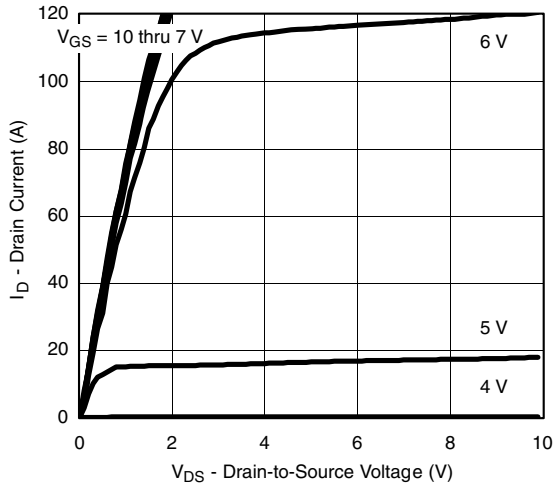
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{DS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2		4	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^\circ\text{C}$			250	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	100			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		0.013	0.0165	$\Omega$
		$V_{GS} = 6\text{ V}, I_D = 20\text{ A}$		0.015	0.019	
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 125\text{ }^\circ\text{C}$			0.031	
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 175\text{ }^\circ\text{C}$			0.041	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 30\text{ A}$	25			S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		4300		$\text{pF}$
Output Capacitance	$C_{oss}$			450		
Reverse Transfer Capacitance	$C_{rss}$			175		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_D = 60\text{ A}$		65	100	$\text{nC}$
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			25		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			19		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	0.3	1.5	3	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 60\text{ A}, V_{GEN} = 10\text{ V}, R_G = 2.5\text{ }\Omega$		15		$\text{ns}$
Rise Time <sup>c</sup>	$t_r$			12	20	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			30	45	
Fall Time <sup>c</sup>	$t_f$			10	15	
<b>Source-Drain Diode Ratings and Characteristics</b> ( $T_C = 25\text{ }^\circ\text{C}$ ) <sup>b</sup>						
Continuous Current	$I_S$				60	A
Pulsed Current	$I_{SM}$				100	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = 30\text{ A}, V_{GS} = 0\text{ V}$		1.0	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = 50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		125	200	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			8	12	A
Reverse Recovery Charge	$Q_{rr}$			0.5	1.2	$\mu\text{C}$

**Notes:**

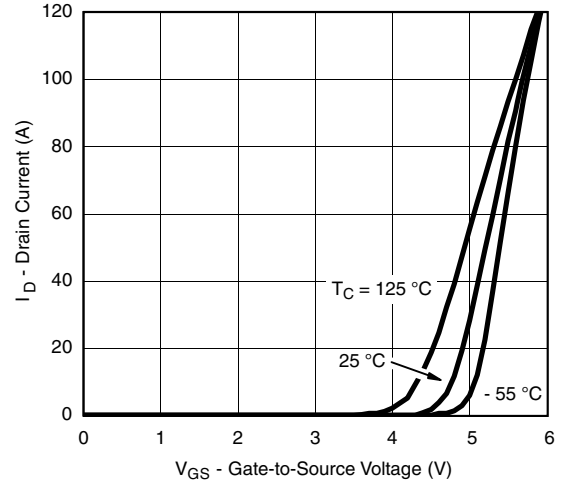
- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

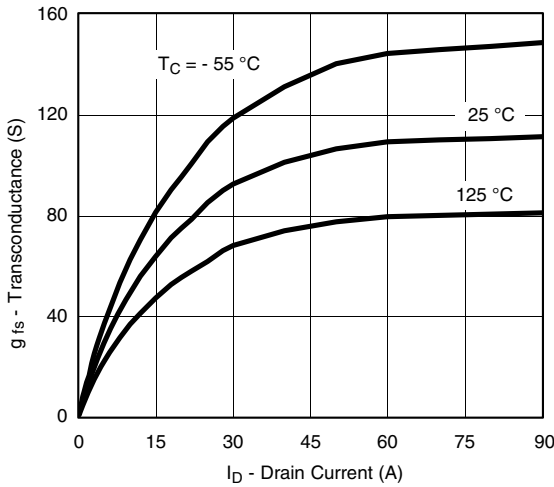
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



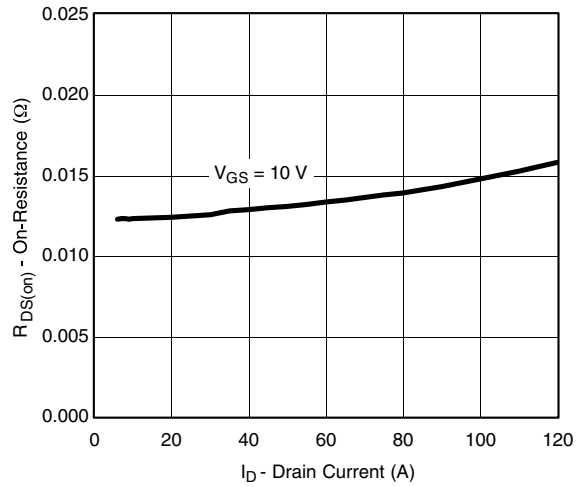
**Output Characteristics**



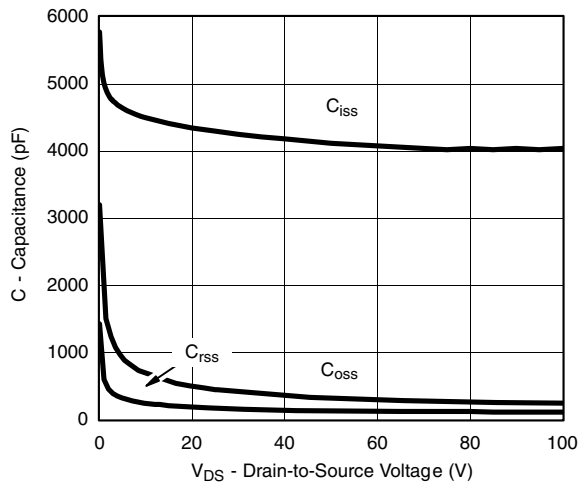
**Transfer Characteristics**



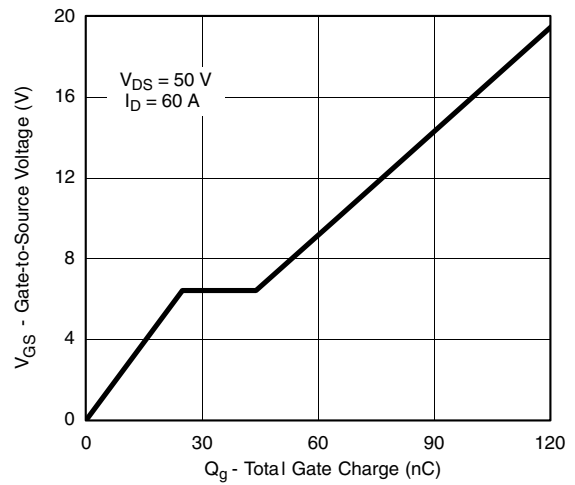
**Transconductance**



**On-Resistance vs. Drain Current**

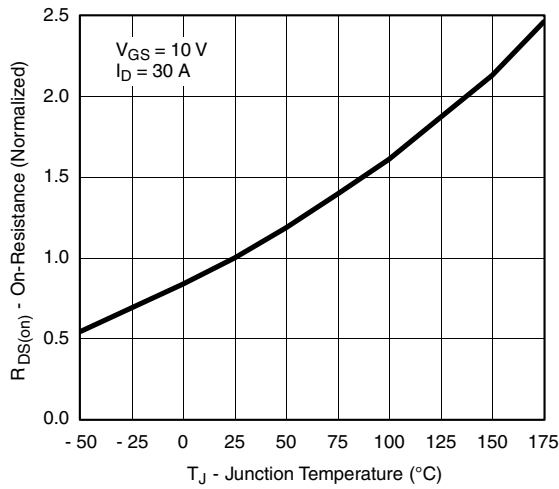


**Capacitance**

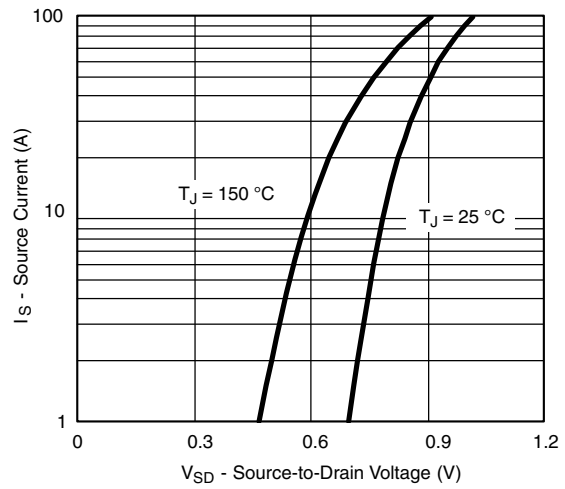


**Gate Charge**

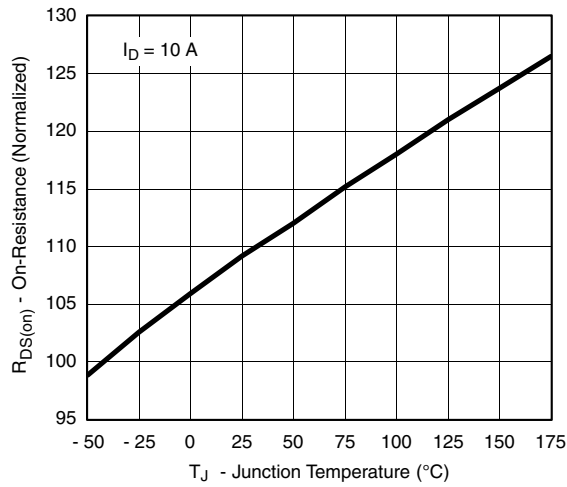
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



**On-Resistance vs. Junction Temperature**

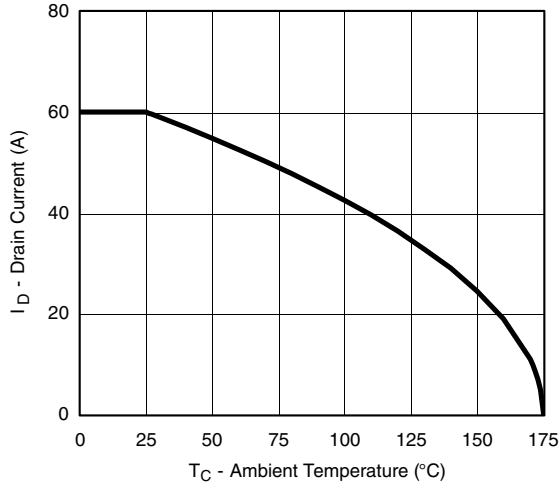


**Source-Drain Diode Forward Voltage**

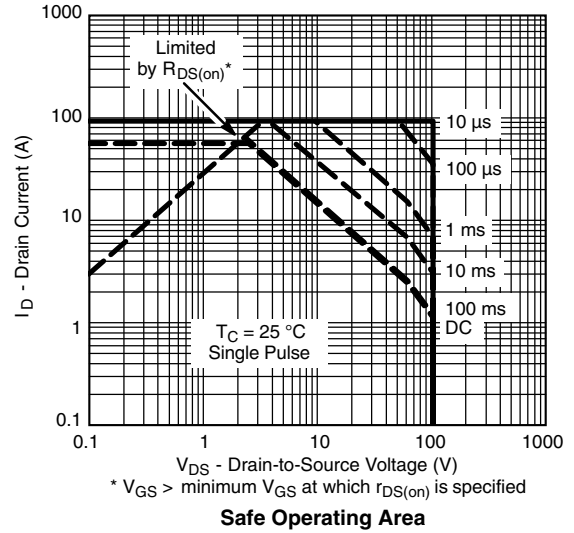


**On-Resistance vs. Junction Temperature**

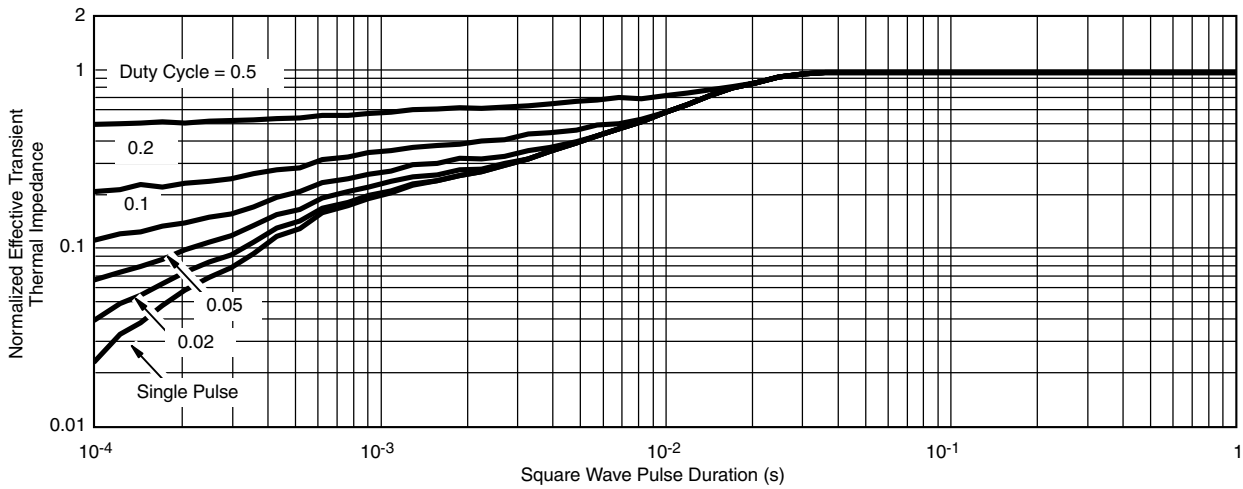
**THERMAL RATINGS**



**Maximum Avalanche and Drain Current vs. Case Temperature**



**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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# TO-263 (D<sup>2</sup>PAK): 3-LEAD



DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

**Notes**

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- \*: Thin lead is for SUB, SYB.  
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- This feature is for thick lead.

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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