# SN74LV4040A 12-Bit Asynchronous Binary Counters

## 1 Features

- 2-V to 5.5-V $V_{CC}$ Operation
- Typical $V_{OLP}$ (Output Ground Bounce) <0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Typical $V_{OHV}$ (Output VOH Undershoot) 2.3 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Individual Switch Controls
- Extremely Low Input Current
- $I_{off}$ Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

## 2 Description

The ’LV4040A devices are 12-bit asynchronous binary counters with the outputs of all stages available externally.

**Package Information**

| PART NUMBER | PACKAGE[1] | PACKAGE SIZE[2] |
|---|---|---|
| SN74LV4040A | N (PDIP, 16) | 19.3 mm x 9.4 mm |
| | D (SOIC, 16) | 9.9 mm x 6 mm |
| | NS (SOP, 16) | 10.2 mm x 7.8 mm |
| | DB (SSOP, 16) | 6.2 mm x 7.8 mm |
| | PW (TSSOP, 16) | 5 mm x 6.4 mm |
| | DGV (TVSOP, 16) | 3.6 mm x 6.4 mm |
| | RGY (VQFN, 16) | 4 mm x 3.5 mm |

1. For all available packages, see the orderable addendum at the end of the data sheet.
2. The package size (length × width) is a nominal value and includes pins, where applicable.

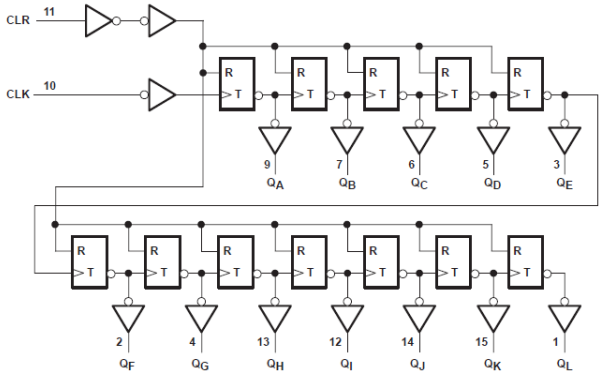



**Figure 2-1. Logic Diagram (Positive Logic)**

## Table of Contents



## 3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision I (May 2005) to Revision J (July 2023) | Page |
|---|---|
| • Added *Package Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |
| • Updated thermal values for RθJA: D = 73 to 99.5, PW = 108 to 122.3, all values in °C/W | 5 |

## 4 Pin Configuration and Functions

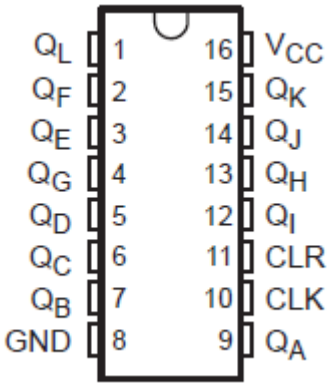
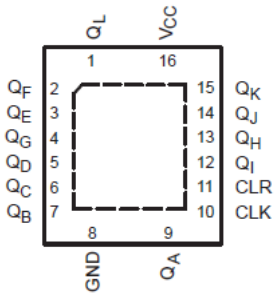



**Figure 4-1. SN74LV4040A D, DB, DGV, N, NS, or PW Package (Top View)**




A. NC - no internal connection

**Figure 4-2. SN74LV4040A RGY Package (Top View)**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $Q_L$ | 1 | O | $Q_L$ output |
| $Q_F$ | 2 | O | $Q_F$ output |
| $Q_E$ | 3 | O | $Q_E$ output |
| $Q_G$ | 4 | O | $Q_G$ output |
| $Q_D$ | 5 | O | $Q_D$ output |
| $Q_C$ | 6 | O | $Q_C$ output |
| $Q_B$ | 7 | O | $Q_B$ output |
| GND | 8 | - | Ground |
| $V_{CC}$ | 9 | - | Positive supply |
| $Q_K$ | 10 | O | $Q_K$ output |
| $Q_J$ | 11 | O | $Q_J$ output |
| $Q_H$ | 12 | O | $Q_H$ output |
| $Q_I$ | 13 | O | $Q_I$ output |
| CLR | 14 | I | Clear, active high |
| CLK | 15 | I | Clock, falling edge triggered |
| $Q_A$ | 16 | O | $Q_A$ output |

1. I = input, O = output

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | -0.5 | 7 | V |
| $V_I$ | Input voltage range | | -0.5 | 7 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state | | -0.5 | 7 | V |
| $V_O$ | Output voltage range | | −0.5 V to $V_{CC}$ | 0.5 | V |
| $I_{IK}$ | Input clamp current(2) | ($V_I$ < 0) | | −20 | mA |
| $I_{OK}$ | Output clamp current(2) | ($V_O$ < 0) | | ±50 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_{stg}$ | Storage temperature range | | -65 | 150 | ℃ |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101[2] | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC}$ × 0.7 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $V_{CC}$ × 0.3 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | − 50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | − 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | − 6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | − 12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 12 | |
| Δt/Δv | Input transition rise/fall time | $V_{CC}$ = 2.3 V to 2.7 V | | 200 | ns |
| | | $V_{CC}$ = 3 V to 3.6 V | | 100 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | -40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 5.4 Thermal Information

| THERMAL METRIC[1] | | D (SOIC) | DB (SSOP) | DGV (TVSOP) | N (PDIP) | NS (SOP) | PW (TSSOP) | RGY (VQFN) | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 99.5 | 82 | 120 | 67 | 64 | 122.3 | 39 | °C/W |

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics.*

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | SN74LV4040A | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $V_{OH}$ | $I_{OH}$ = −50 µA | 2 V to 5.5 V | $V_{CC}$ − 0.1 | | | V |
| | $I_{OH}$ = −2 mA | 2.3 V | 2 | | | |
| | $I_{OH}$ = −6 mA | 3 V | 2.48 | | | |
| | $I_{OH}$ = −12 mA | 4.5 V | 3.8 | | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 2 V to 5.5 V | | | 0.1 | V |
| | $I_{OL}$ = 2 mA | 2.3 V | | | 0.4 | |
| | $I_{OL}$ = 6 mA | 3 V | | | 0.44 | |
| | $I_{OL}$ = 12 mA | 4.5 V | | | 0.55 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 20 | µA |
| $I_{off}$ | $V_I$ or $V_O$ = 0 to 5.5 V | 0 | | | 5 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 1.9 | | pF |

## 5.6 Timing Requirements, $V_{CC}$ = 2.5 V ± 0.2 V

timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted)

| | | | $T_A$ = 25°C | | SN74LV4040A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | CLK high or low | 7 | | 7 | | ns |
| | | CLR high | 6.5 | | 6.5 | | |
| $t_{su}$ | Setup time | CLR inactive before CLK↓ | 6.5 | | 6.5 | | |

## 5.7 Timing Requirements, $V_{CC}$ = 3.3 V ± 0.3 V

timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted)

| | | | $T_A$ = 25°C | | SN74LV4040A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | CLK high or low | 5 | | 5 | | ns |
| | | CLR high | 5 | | 5 | | |
| $t_{su}$ | Setup time | CLR inactive before CLK↓ | 5 | | 5 | | |

## 5.8 Timing Requirements, $V_{CC}$ = 5 V ± 0.5 V

timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted)

| | | | $T_A$ = 25°C | | SN74LV4040A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | CLK high or low | 5 | | 5 | | ns |
| | | CLR high | 5 | | 5 | | |
| $t_{su}$ | Setup time | CLR inactive before CLK↓ | 5 | | 5 | | |

## 5.9 Switching Characteristics, $V_{CC}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted) (Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN74LV4040A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 50[1] | 115[1] | | 40[1] | | MHz |
| | | | $C_L$ = 50 pF | 40 | 95 | | 35 | | |
| $t_{PLH}$ | CLK | $Q_A$ | $C_L$ = 15 pF | | 8.7[1] | 19.4[1] | 1[1] | 23[1] | ns |
| $t_{PHL}$ | | | | | 8.7[1] | 19.4[1] | 1[1] | 23[1] | |
| $t_{PHL}$ | CLR | Any Q | $C_L$ = 15 pF | | 9.3[1] | 19.9[1] | 1[1] | 24[1] | |
| $t_{PLH}$ | $\overline{CLK}$ | $Q_A$ | $C_L$ = 50 pF | | 10.5 | 24.1 | 1 | 28 | |
| $t_{PHL}$ | | | | | 10.5 | 24.1 | 1 | 28 | |
| $t_{PHL}$ | CLR | Any Q | $C_L$ = 50 pF | | 11.7 | 24.5 | 1 | 28 | ns |
| $\Delta t_{pd}$ | $Q_n$ | $Q_{n+1}$ | $C_L$ = 50 pF | | 1.7 | 5.9 | | 7 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 5.10 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 (unless otherwise noted) (Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN74LV4040A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 75[1] | 160[1] | | 75 | | MHz |
| | | | $C_L$ = 50 pF | 55 | 130 | | 50 | | |
| $t_{PLH}$ | CLK | $Q_A$ | $C_L$ = 15 pF | | 6.1[1] | 11.9[1] | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 6.1[1] | 11.9[1] | 1 | 14 | ns |
| $t_{PHL}$ | CLR | Any Q | $C_L$ = 15 pF | | 7.1[1] | 12.8[1] | 1 | 15 | ns |
| $t_{PLH}$ | $\overline{CLK}$ | $Q_A$ | $C_L$ = 50 pF | | 7.5 | 15.4 | 1 | 17.5 | ns |
| $t_{PHL}$ | | | | | 7.5 | 15.4 | 1 | 17.5 | ns |
| $t_{PHL}$ | CLR | Any Q | $C_L$ = 50 pF | | 9 | 16.3 | 1 | 18.5 | ns |
| $\Delta t_{pd}$ | $Q_n$ | $Q_{n+1}$ | $C_L$ = 50 pF | | 1.2 | 4.4 | | 5 | ns |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 5.11 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN74LV4040A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 150[1] | 235[1] | | 125 | | MHz |
| | | | $C_L$ = 50 pF | 95 | 185 | | 80 | | |
| $t_{PLH}$ | CLK | $Q_A$ | $C_L$ = 15 pF | | 4.2[1] | 7.3[1] | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 4.2[1] | 7.3[1] | 1 | 8.5 | ns |
| $t_{PHL}$ | CLR | Any Q | $C_L$ = 15 pF | | 5.3[1] | 8.6[1] | 1 | 10 | ns |
| $t_{PLH}$ | $\overline{CLK}$ | $Q_A$ | $C_L$ = 50 pF | | 5.3 | 9.3 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 9.3 | 1 | 10.5 | ns |
| $t_{PHL}$ | CLR | Any Q | $C_L$ = 50 pF | | 6.8 | 10.6 | 1 | 12 | ns |
| $\Delta t_{pd}$ | $Q_n$ | $Q_{n+1}$ | $C_L$ = 50 pF | | 0.8 | 3.1 | | 3.5 | ns |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 5.12 Noise Characteristics

$V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C

| PARAMETER[(1)] | | SN74LV4040A | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.5 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | − 0.5 | − 0.8 | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | V |

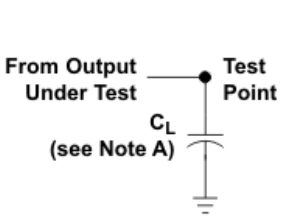
(1) Characteristics for surface-mount packages only.

## 5.13 Operating Characteristics

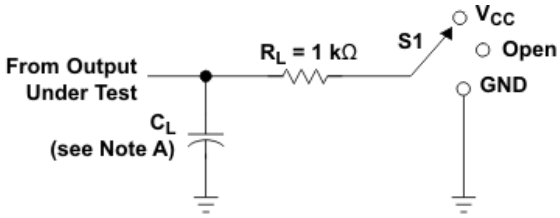
$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, | f = 10 MHz | 3.3 V | 11.9 | pF |
| | | | | 5 V | 13.1 | |

## 6 Parameter Measurement Information

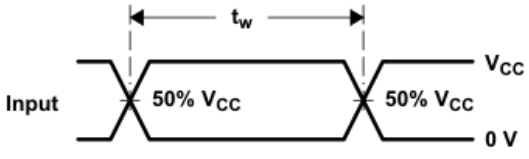



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

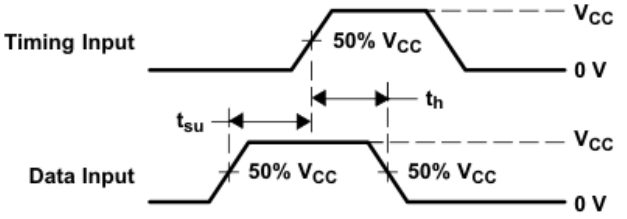



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |

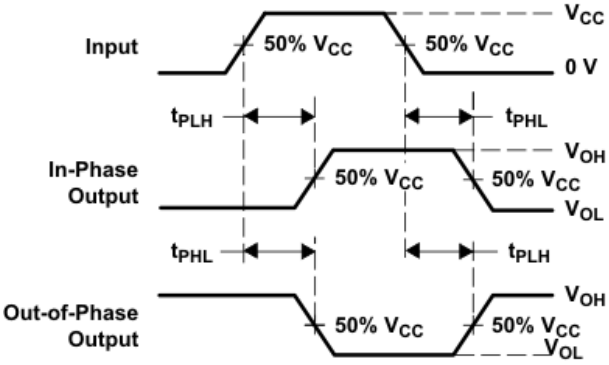
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



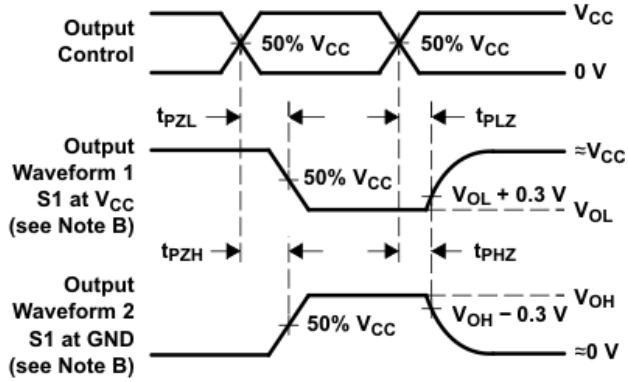

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, and $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 6-1. Load Circuit and Voltage Waveforms**

# 7 Detailed Description

## 7.1 Overview

The ’LV4040A devices are 12-bit asynchronous binary counters with the outputs of all stages available externally. A high level at the clear (CLR) input asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at the clock (CLK) input. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

These devices are fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

## 7.2 Functional Block Diagram

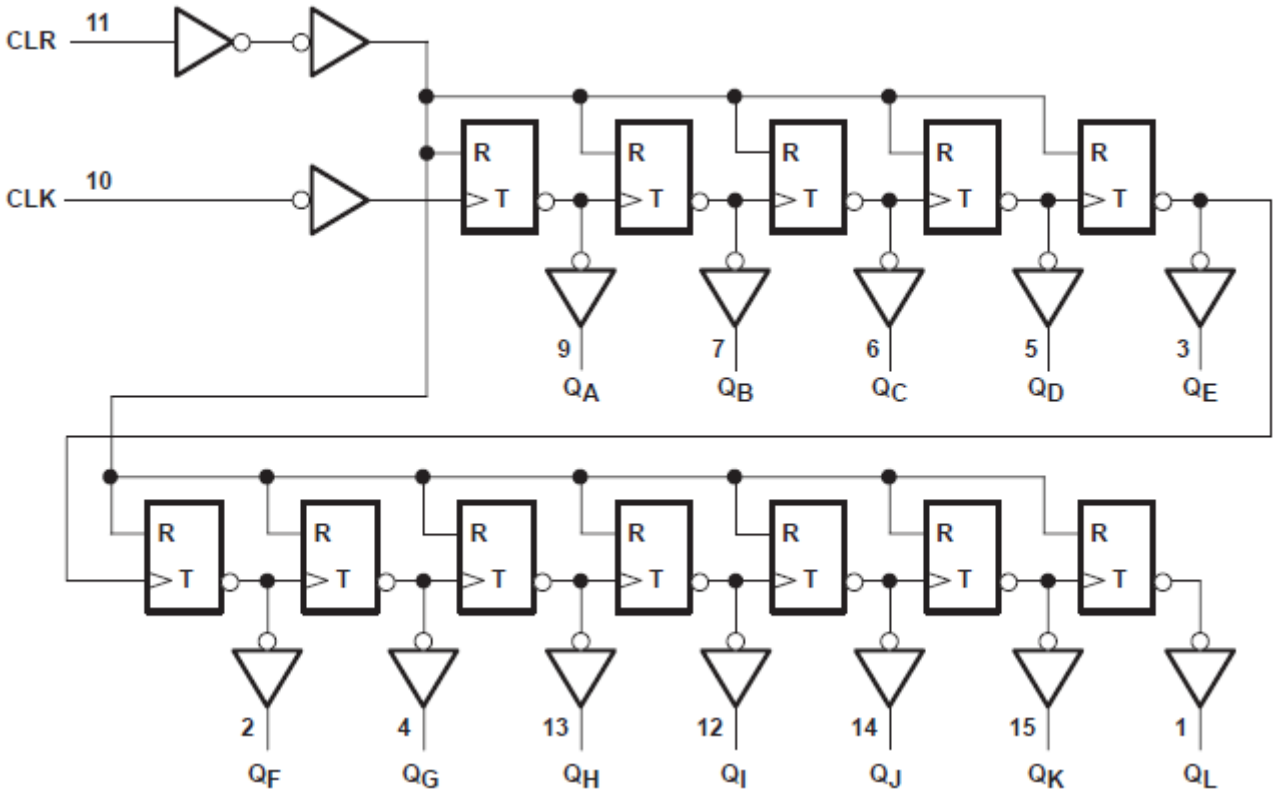



**Figure 7-1. Logic Diagram (Positive Logic)**

## 7.3 Device Functional Modes

**Table 7-1. Function Table (Each Buffer)**

| INPUTS | | FUNCTION |
|---|---|---|
| CLK | CLR | |
| ↑ | L | No change |
| ↓ | L | Advance to next stage |
| X | H | All outputs L |

# 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 8.1 Documentation Support (Analog)

### 8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 8-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN74LV4040A | Click here | Click here | Click here | Click here | Click here |

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV4040ADBR | ACTIVE | SSOP | DB | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LW040A | Samples |
| SN74LV4040ADGVR | ACTIVE | TVSOP | DGV | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LW040A | Samples |
| SN74LV4040ADR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV4040A | Samples |
| SN74LV4040AN | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74LV4040AN | Samples |
| SN74LV4040ANSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV4040A | Samples |
| SN74LV4040APWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | LW040A | Samples |
| SN74LV4040ARGYR | ACTIVE | VQFN | RGY | 16 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LW040A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

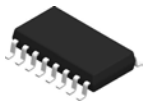


**OTHER QUALIFIED VERSIONS OF SN74LV4040A :**

- Enhanced Product : SN74LV4040A-EP

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

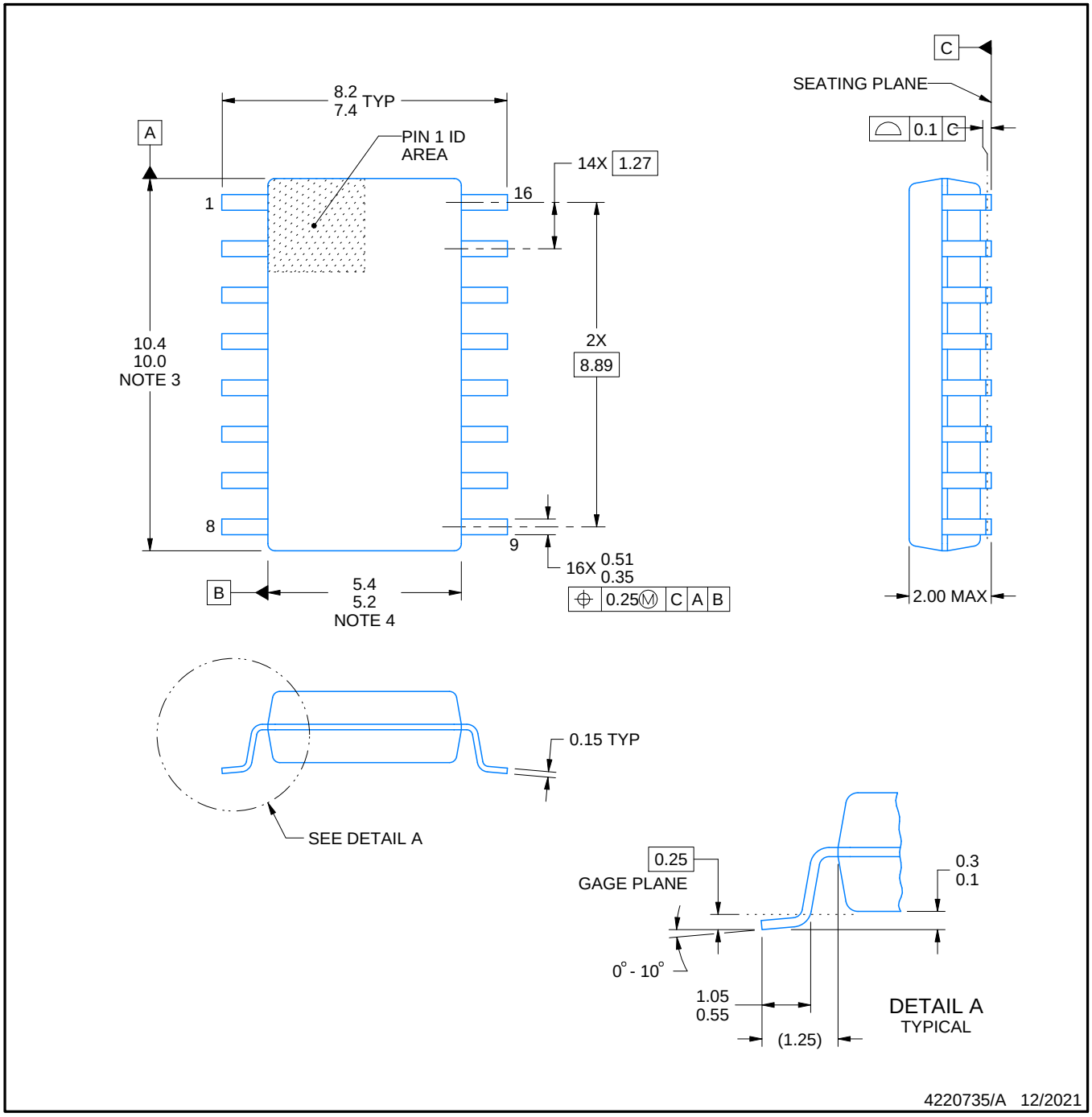


# PACKAGE OUTLINE

## NS0016A

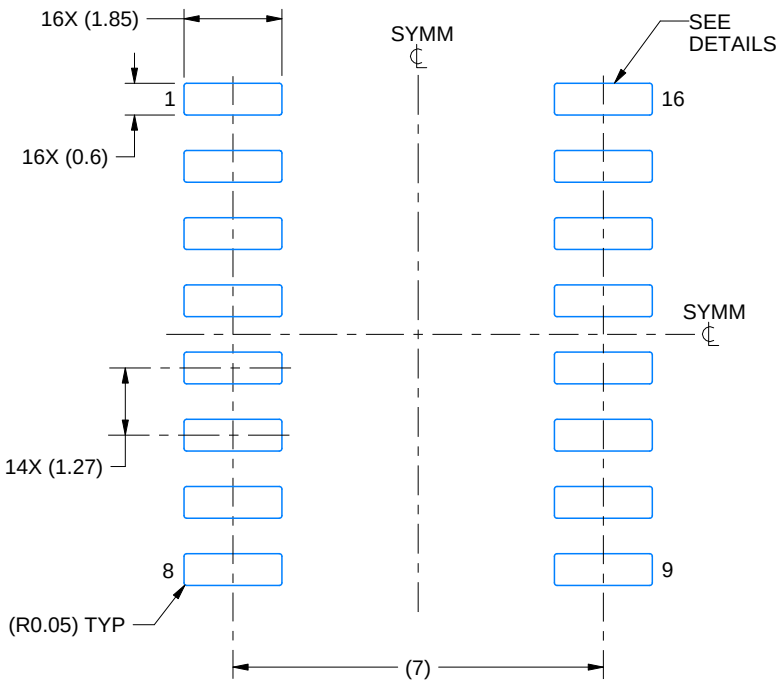
## SOP - 2.00 mm max height

SOP

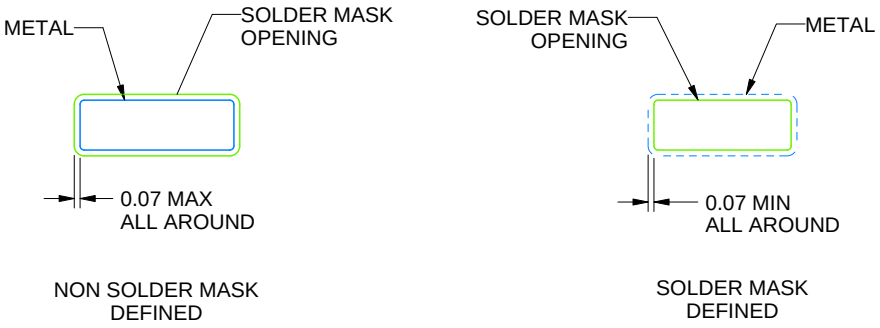



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
SCALE:7X




NON SOLDER MASK
DEFINED

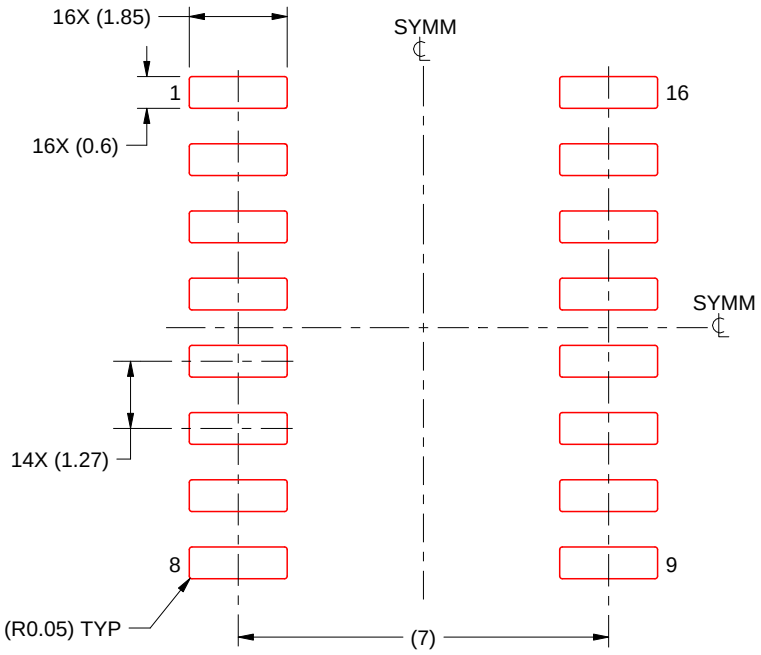
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

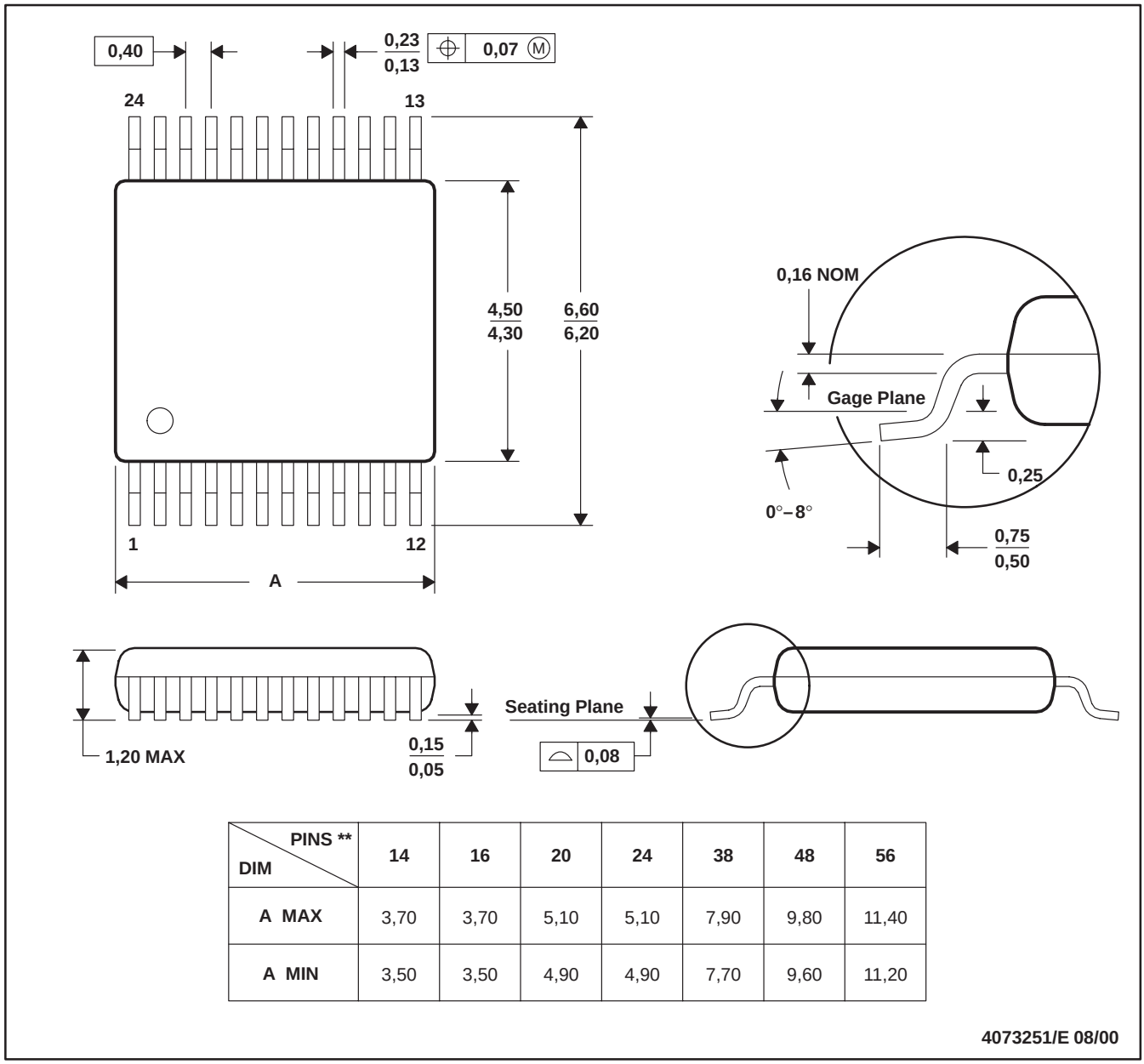
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

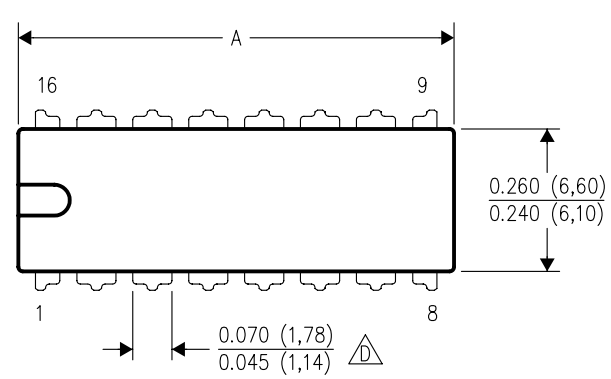
**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

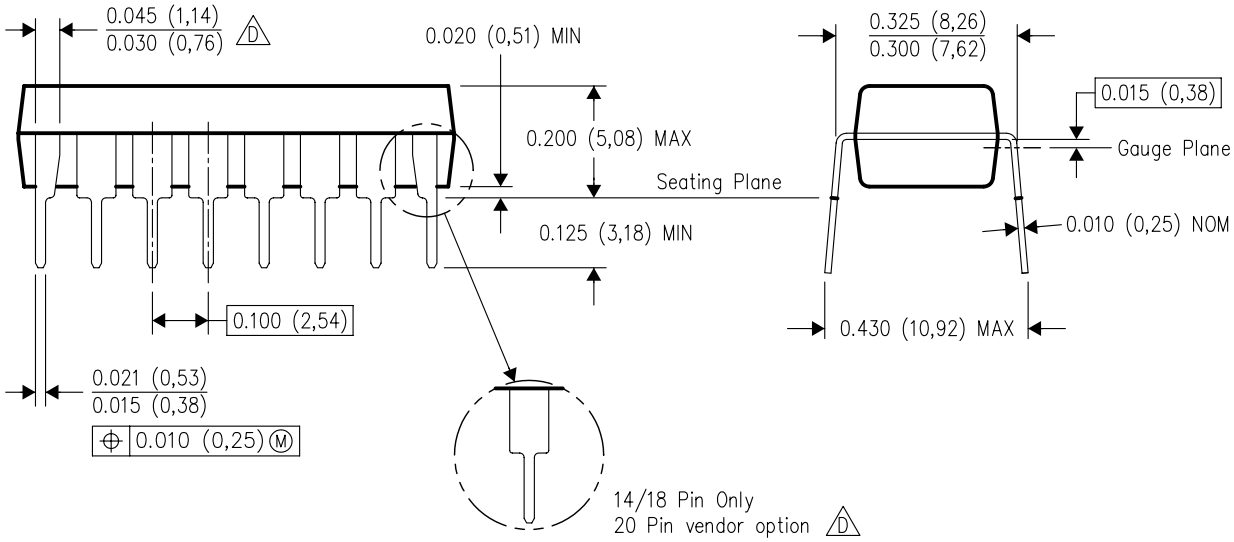
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



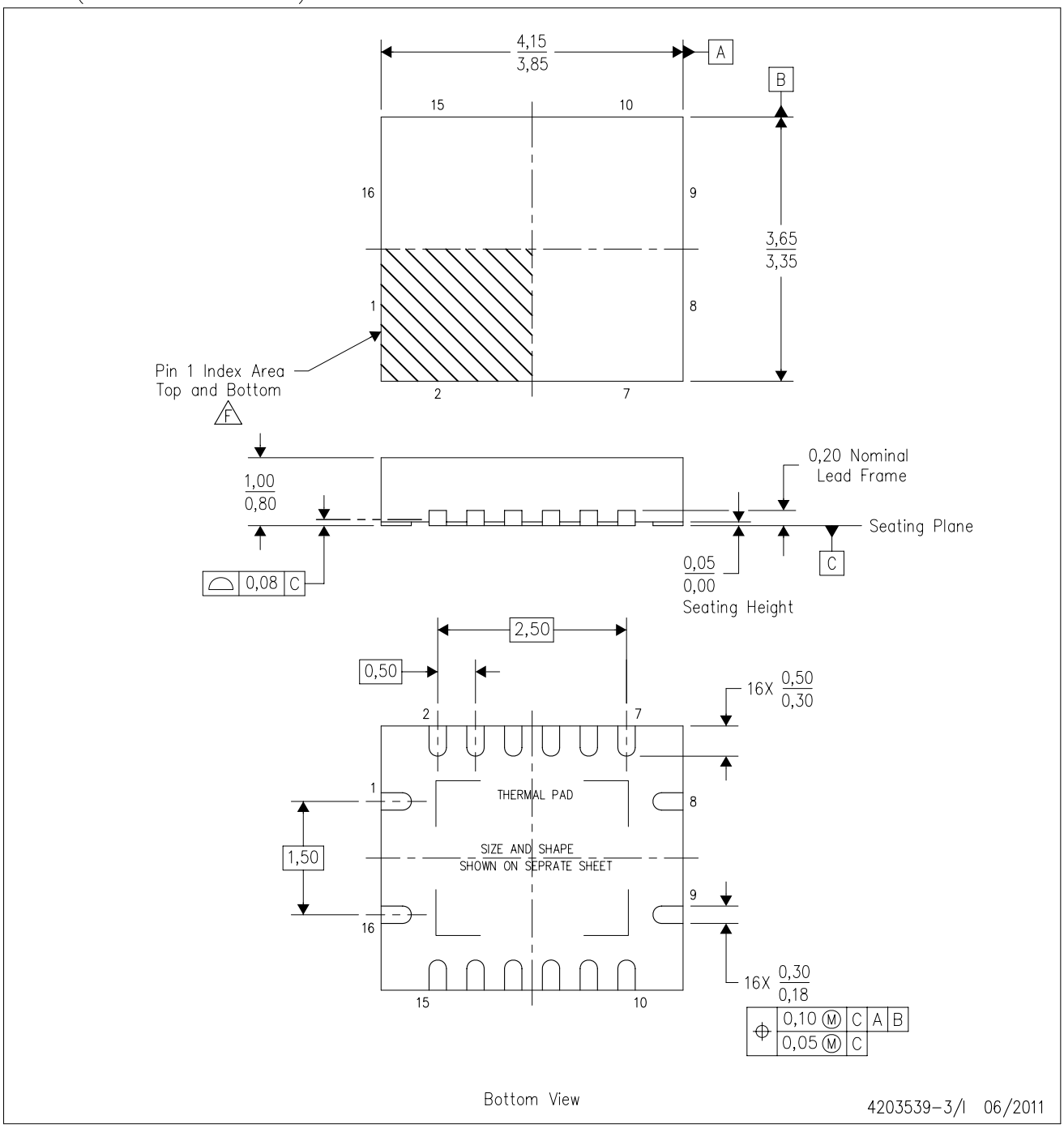

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

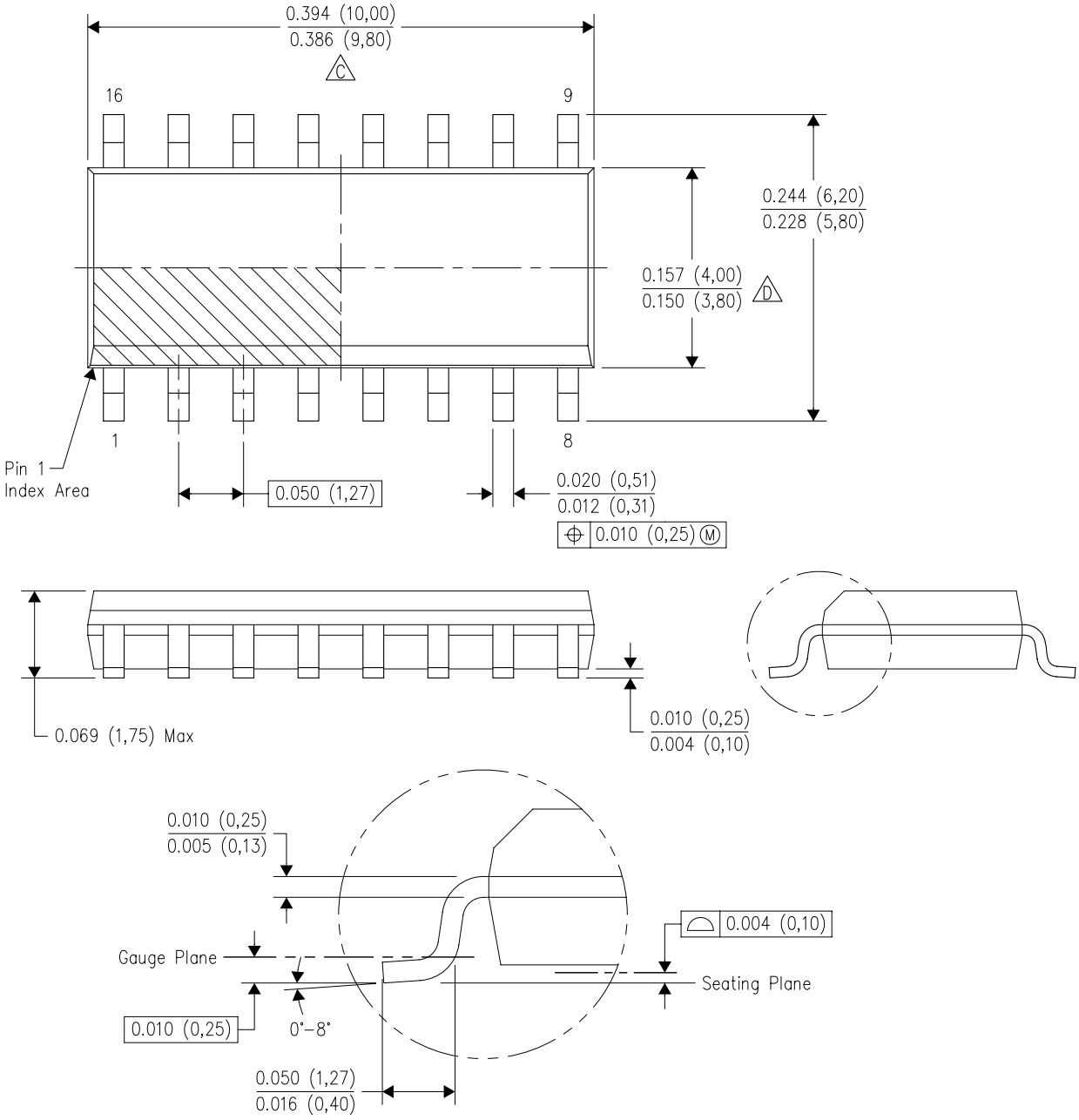
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



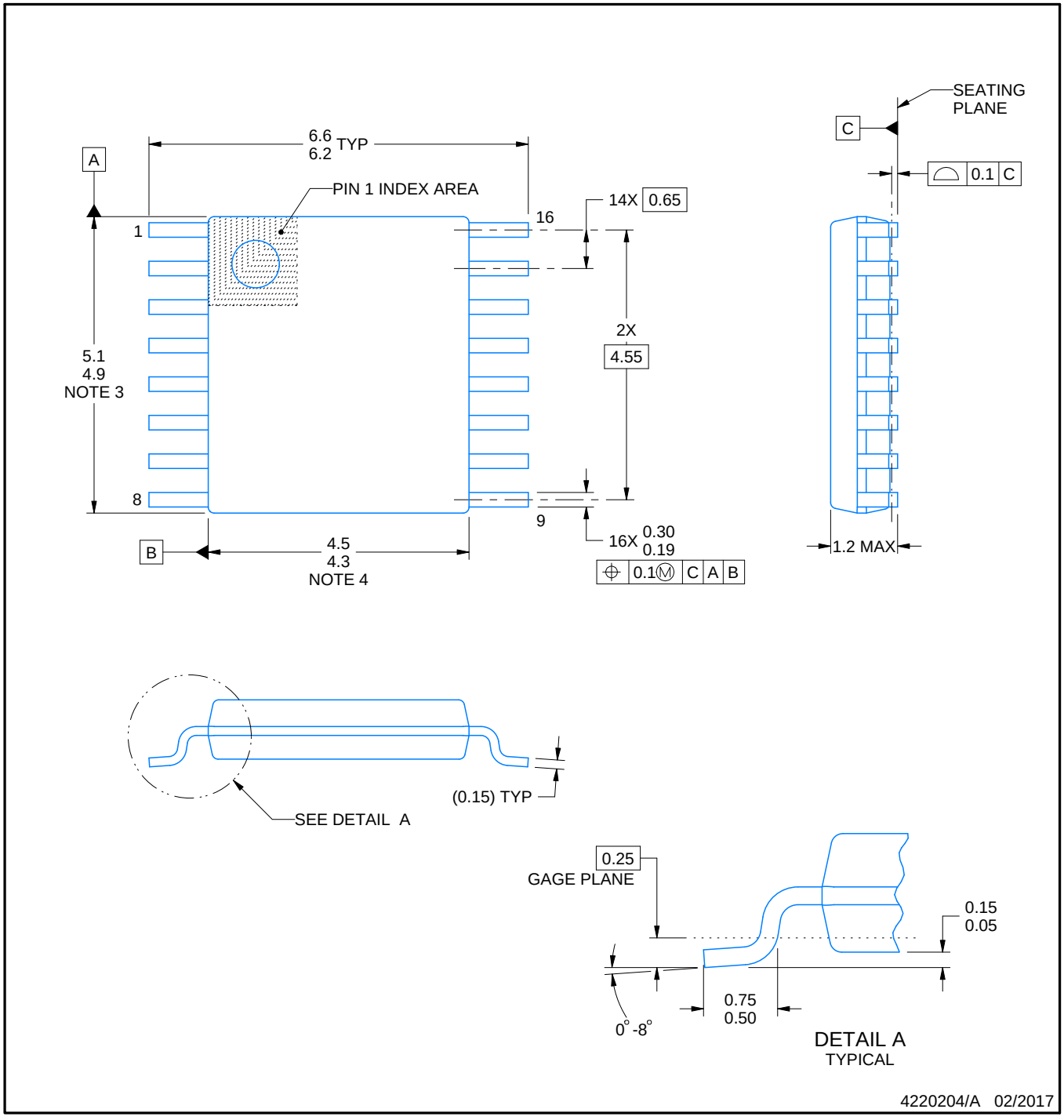

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

# PACKAGE OUTLINE

## PW0016A

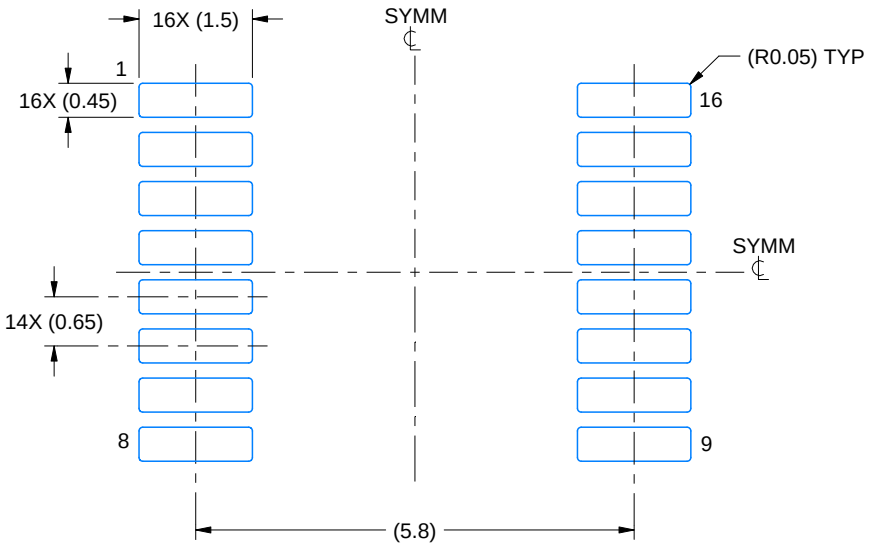
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

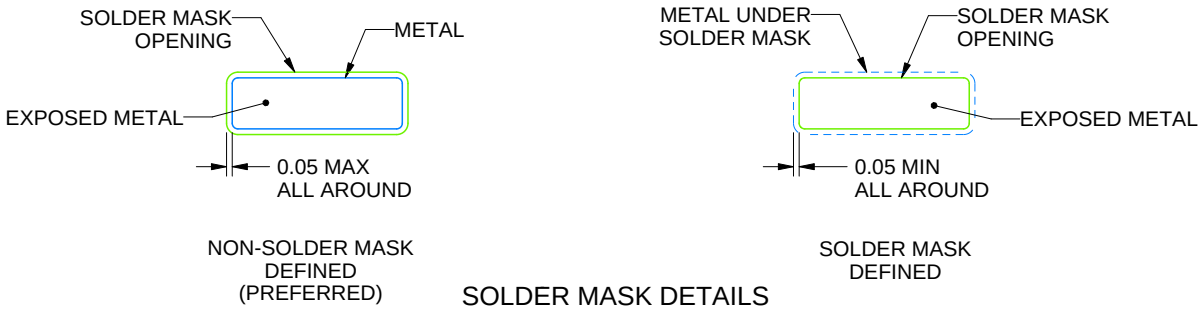



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

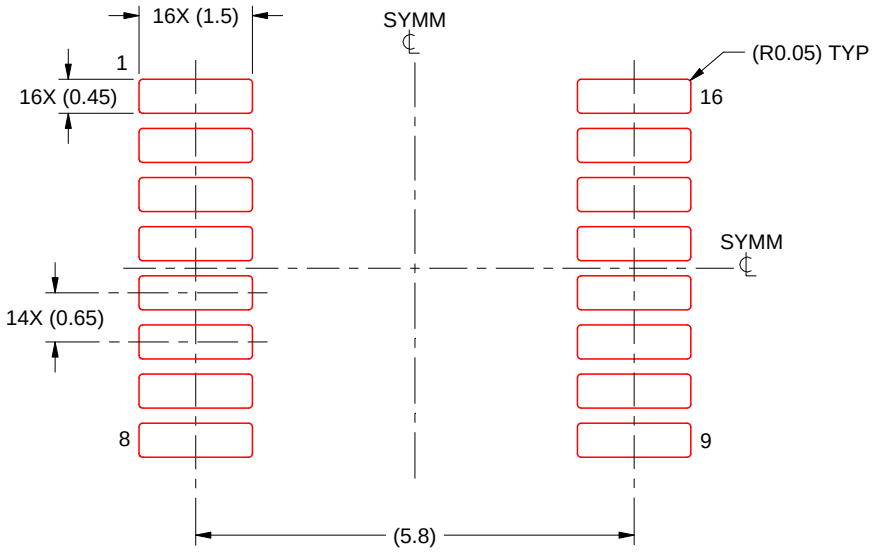



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

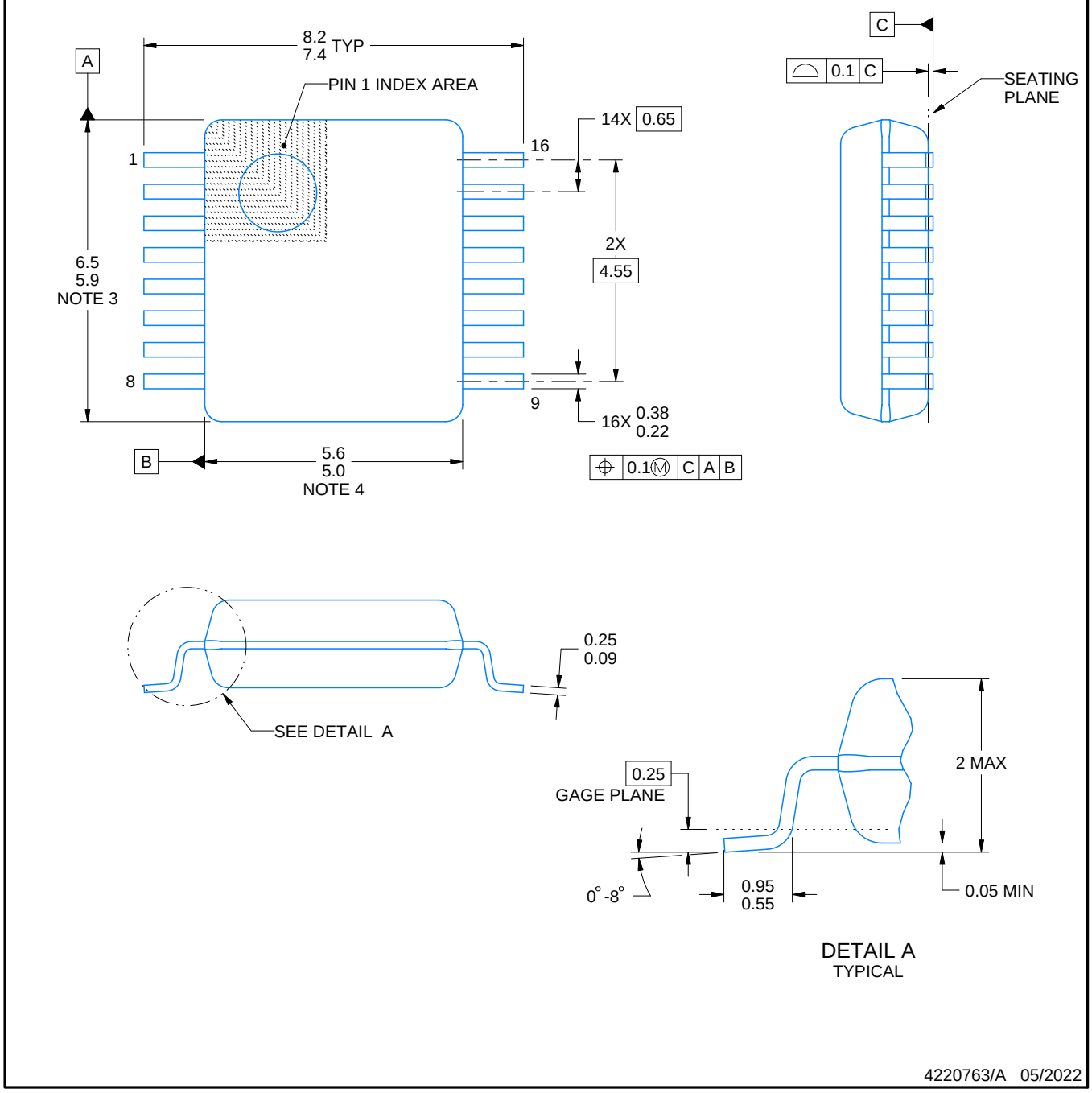
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DB0016A

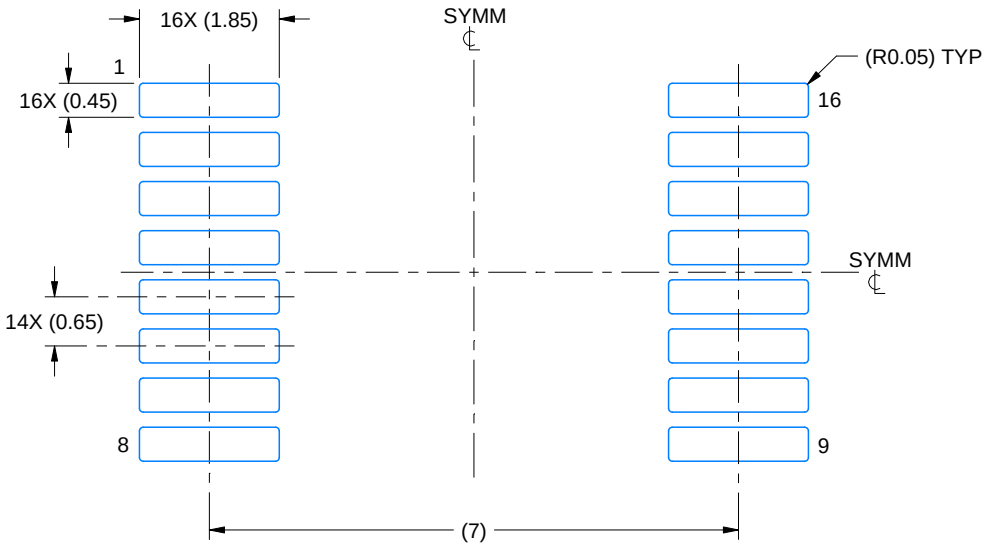
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

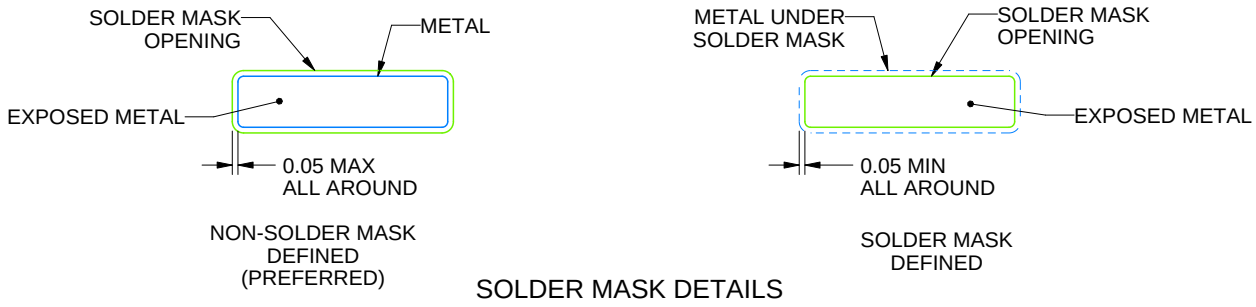



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

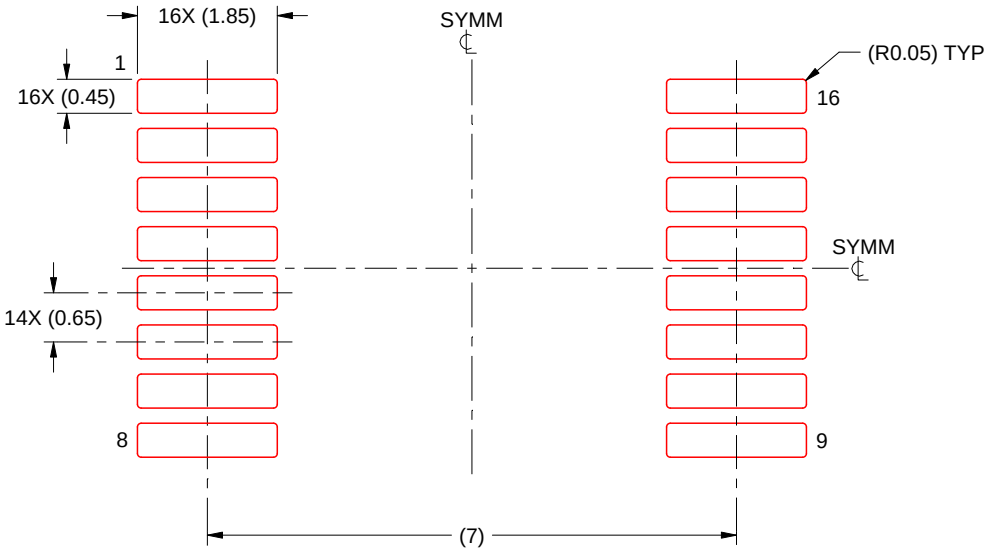



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

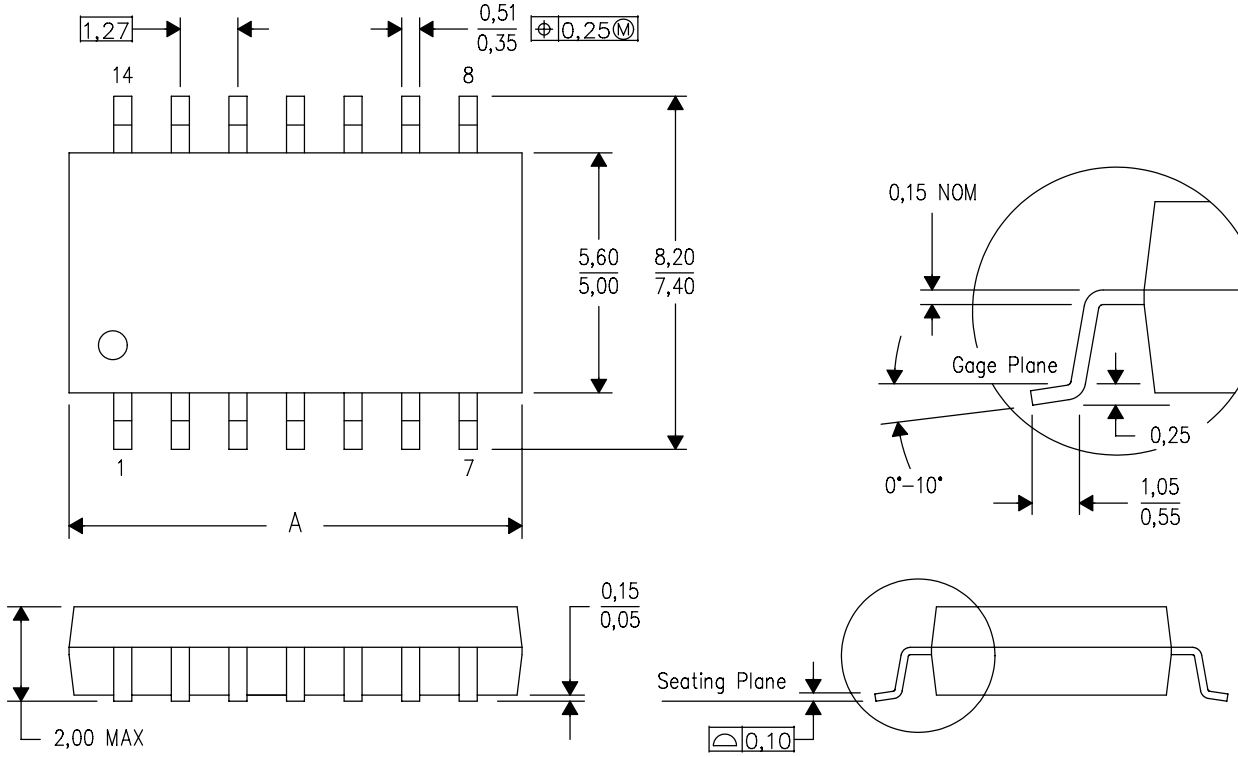
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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