

# NSTB1005DXV5T1G

## Dual Common Base-Collector Bias Resistor Transistors

### NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. The NSTB1005DXV5T1 contains two complementary BRT devices are housed in the SOT-553 package which is ideal for low power surface mount applications where board space is at a premium.

#### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch Tape and Reel
- This is a Pb-Free Device

**MAXIMUM RATINGS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted, common for  $Q_1$  and  $Q_2$ , – minus sign for  $Q_1$  (PNP) omitted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{CBO}$	50	Vdc
Collector-Emitter Voltage	$V_{CEO}$	50	Vdc
Collector Current	$I_C$	100	mAdc

#### THERMAL CHARACTERISTICS

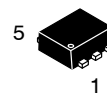
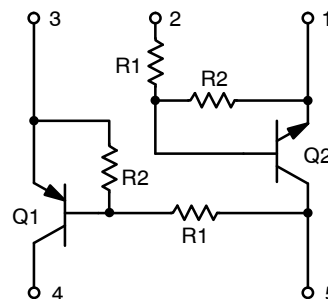
Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 1) Derate above $25^\circ\text{C}$ (Note 1)	$P_D$	357 2.9	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient (Note 1)	$R_{\theta JA}$	350	$^\circ\text{C}/\text{W}$
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 1) Derate above $25^\circ\text{C}$ (Note 1)	$P_D$	500 4.0	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient (Note 1)	$R_{\theta JA}$	250	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad



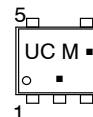
ON Semiconductor®

<http://onsemi.com>



SOT-553  
CASE 463B

#### MARKING DIAGRAM



UC = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

Device	Package	Shipping†
NSTB1005DXV5T1G	SOT-553 (Pb-Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NSTB1005DXV5T1G

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Q1 TRANSISTOR: PNP – OFF CHARACTERISTICS</b>					
Collector–Base Cutoff Current ( $V_{CB} = 50\text{ V}, I_E = 0$ )	$I_{CBO}$	–	–	100	nAdc
Collector–Emitter Cutoff Current ( $V_{CE} = 50\text{ V}, I_B = 0$ )	$I_{CEO}$	–	–	500	nAdc
Emitter–Base Cutoff Current ( $V_{EB} = 6.0\text{ V}, I_C = 0$ )	$I_{EBO}$	–	–	0.1	mAdc
Collector–Base Breakdown Voltage ( $I_C = 10\ \mu\text{A}, I_E = 0$ )	$V_{(BR)CBO}$	50	–	–	Vdc
Collector–Emitter Breakdown Voltage ( $I_C = 2.0\text{ mA}, I_B = 0$ )	$V_{(BR)CEO}$	50	–	–	Vdc

### ON CHARACTERISTICS

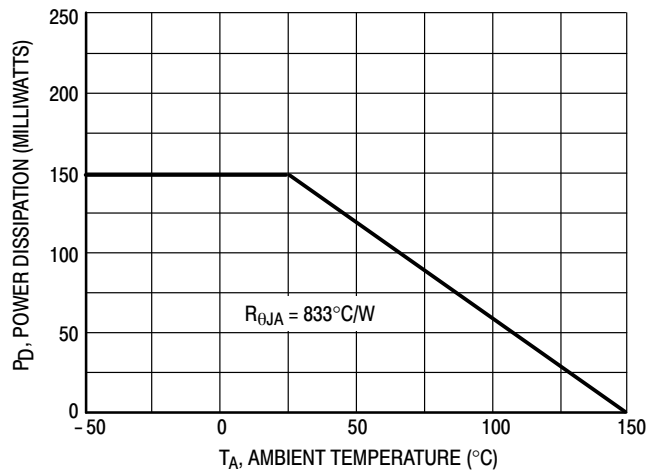
DC Current Gain	$h_{FE}$	80	140	–	
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ mA}, I_E = 0.3\text{ mA}$ )	$V_{CE(sat)}$	–	–	0.25	Vdc
Output Voltage (on) ( $V_{CC} = 5.0\text{ V}, V_B = 3.5\text{ V}, R_L = 1.0\text{ k}\Omega$ )	$V_{OL}$	–	–	0.2	Vdc
Output Voltage (off) ( $V_{CC} = 5.0\text{ V}, V_B = 0.5\text{ V}, R_L = 1.0\text{ k}\Omega$ )	$V_{OH}$	4.9	–	–	Vdc
Input Resistor	R1	32.9	47	61.1	k $\Omega$
Resistor Ratio	$R_1/R_2$	0.8	1.0	1.2	

### Q2 TRANSISTOR: NPN – OFF CHARACTERISTICS

Collector–Base Cutoff Current ( $V_{CB} = 50\text{ V}, I_E = 0$ )	$I_{CBO}$	–	–	100	nAdc
Collector–Emitter Cutoff Current ( $V_{CB} = 50\text{ V}, I_B = 0$ )	$I_{CEO}$	–	–	500	nAdc
Emitter–Base Cutoff Current ( $V_{EB} = 6.0, I_C = 0$ )	$I_{EBO}$	–	–	0.1	mAdc

### ON CHARACTERISTICS

Collector–Base Breakdown Voltage ( $I_C = 10\ \mu\text{A}, I_E = 0$ )	$V_{(BR)CBO}$	50	–	–	Vdc
Collector–Emitter Breakdown Voltage ( $I_C = 2.0\text{ mA}, I_B = 0$ )	$V_{(BR)CEO}$	50	–	–	Vdc
DC Current Gain ( $V_{CE} = 10\text{ V}, I_C = 5.0\text{ mA}$ )	$h_{FE}$	80	140	–	
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ mA}, I_B = 0.3\text{ mA}$ )	$V_{CE(SAT)}$	–	–	0.25	Vdc
Output Voltage (on) ( $V_{CC} = 5.0\text{ V}, V_B = 2.5\text{ V}, R_L = 1.0\text{ k}\Omega$ )	$V_{OL}$	–	–	0.2	Vdc
Output Voltage (off) ( $V_{CC} = 5.0\text{ V}, V_B = 0.5\text{ V}, R_L = 1.0\text{ k}\Omega$ )	$V_{OH}$	4.9	–	–	Vdc
Input Resistor	R1	33	47	61	k $\Omega$
Resistor Ratio	$R_1/R_2$	0.8	1.0	1.2	



**Figure 1. Derating Curve**

# NSTB1005DXV5T1G

## TYPICAL ELECTRICAL CHARACTERISTICS – PNP TRANSISTOR

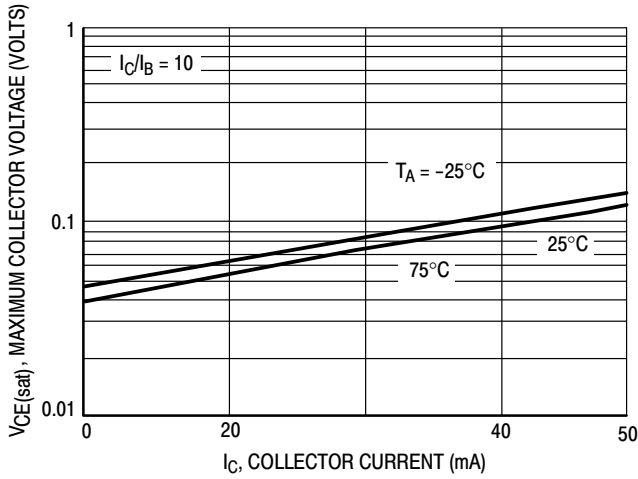


Figure 2.  $V_{CE(sat)}$  versus  $I_C$

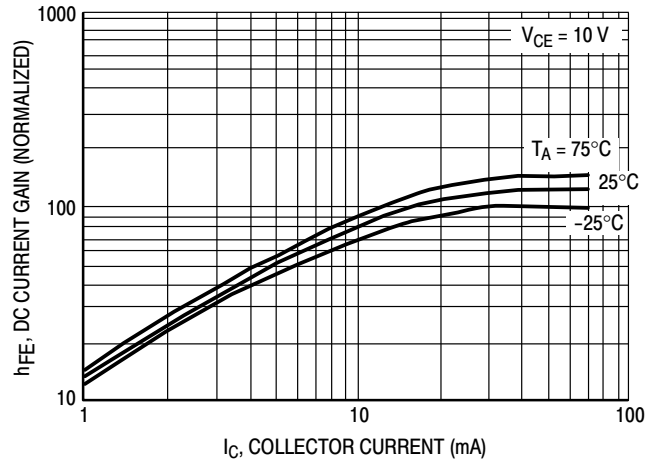


Figure 3. DC Current Gain

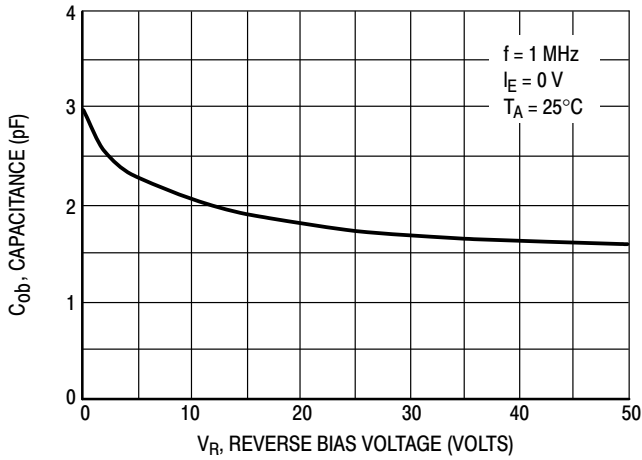


Figure 4. Output Capacitance

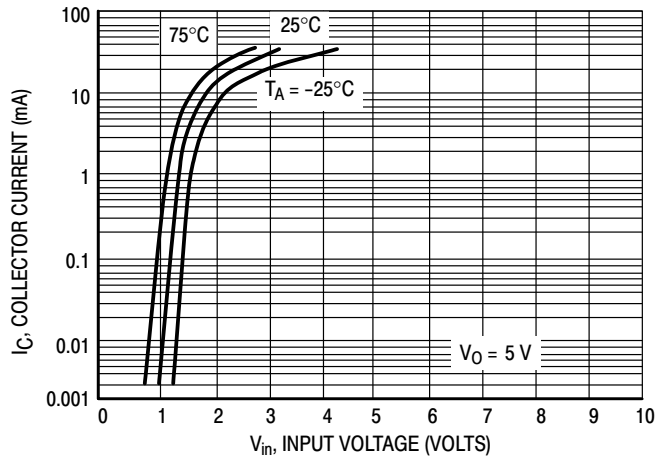


Figure 5. Output Current versus Input Voltage

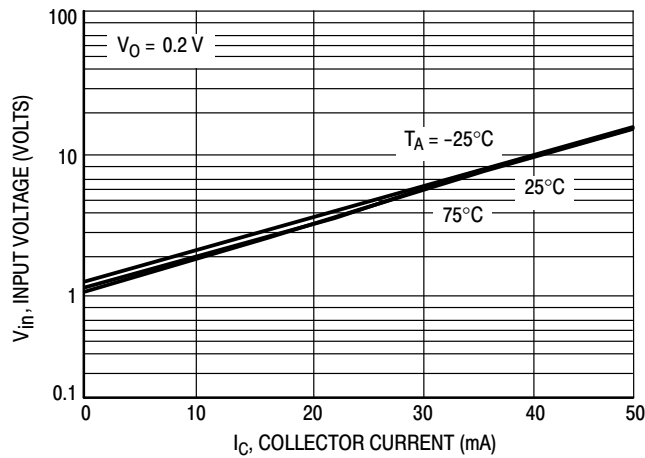


Figure 6. Input Voltage versus Output Current

# NSTB1005DXV5T1G

## TYPICAL ELECTRICAL CHARACTERISTICS — NPN TRANSISTOR

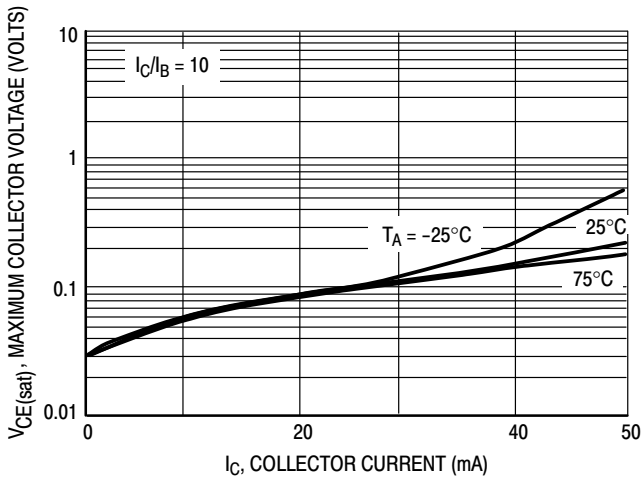


Figure 7.  $V_{CE(sat)}$  versus  $I_C$

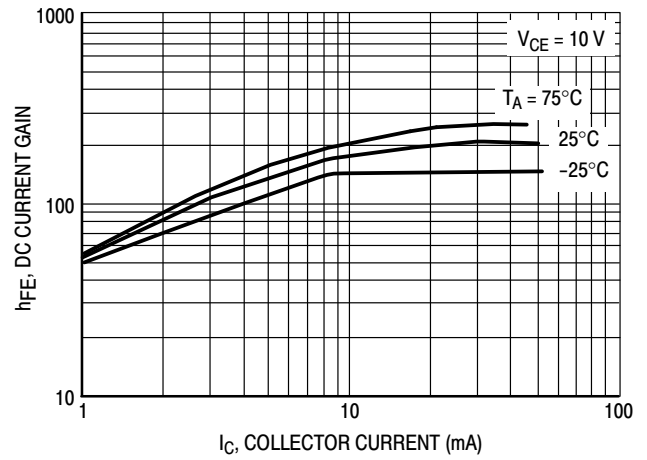


Figure 8. DC Current Gain

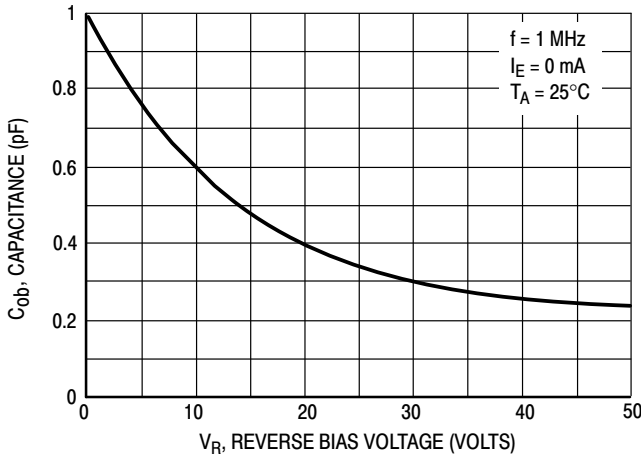


Figure 9. Output Capacitance

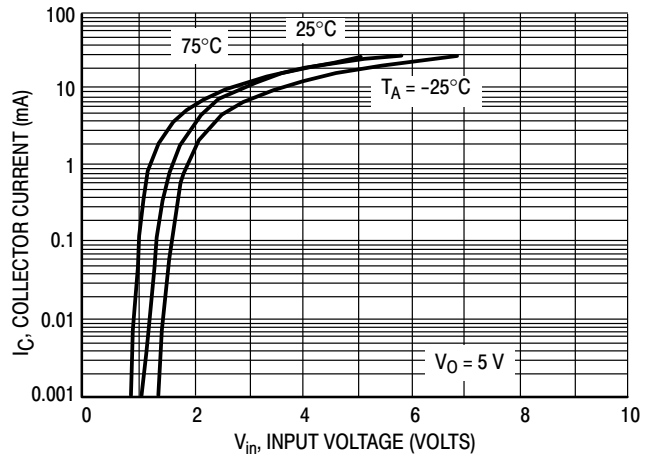


Figure 10. Output Current versus Input Voltage

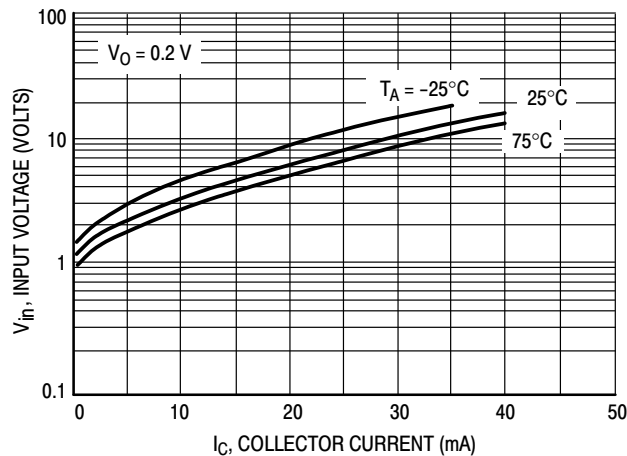
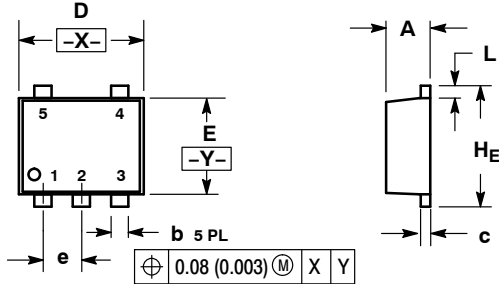


Figure 11. Input Voltage versus Output Current

# NSTB1005DXV5T1G

## PACKAGE DIMENSIONS

**SOT-553**  
**XV5 SUFFIX**  
**CASE 463B-01**  
**ISSUE B**

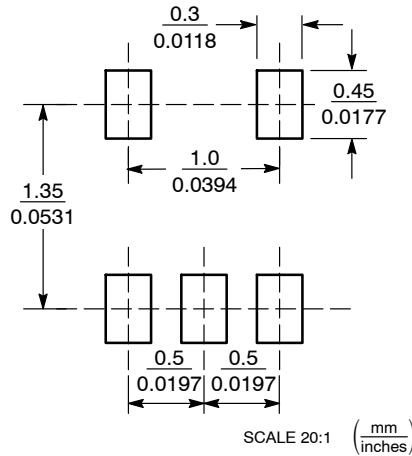


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.063	0.067
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	1.50	1.60	1.70	0.059	0.063	0.067

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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