THC63LVD1024

135MHz 67Bits LVDS Receiver

General Description

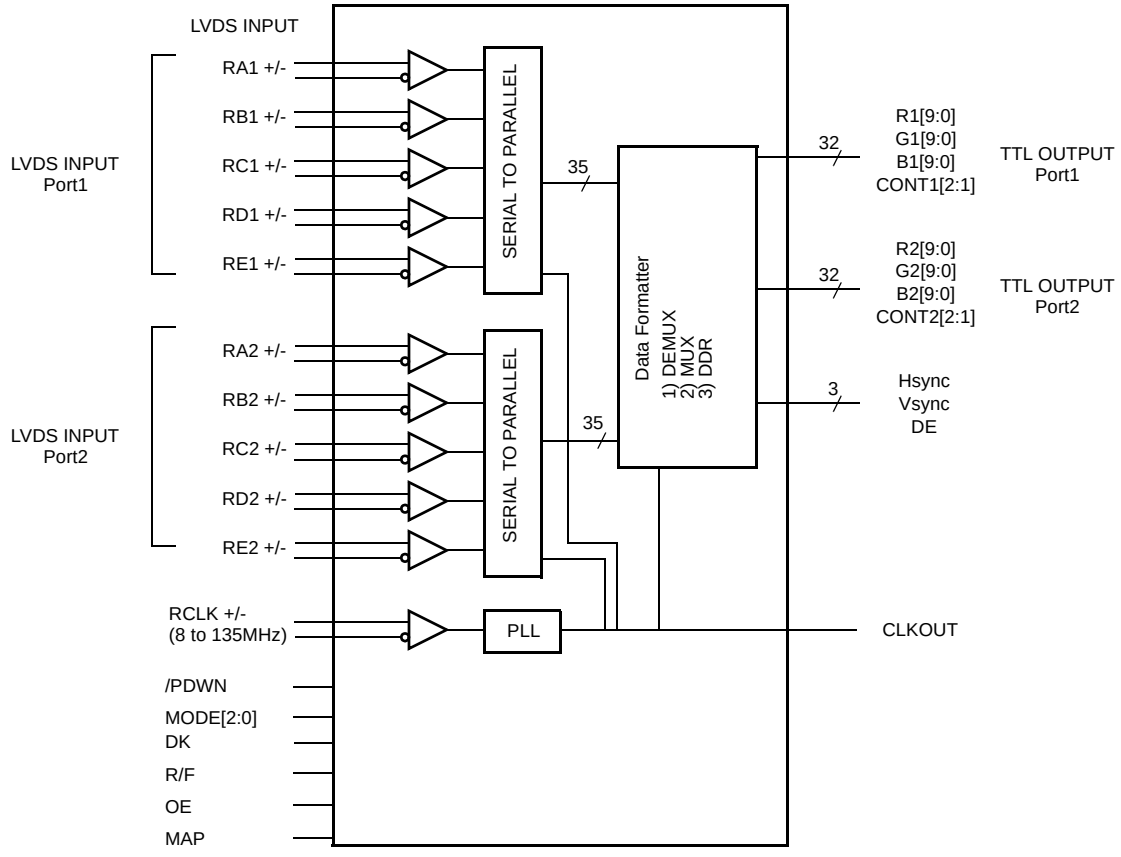
The THC63LVD1024 receiver is designed to support Dual Link transmission between Host and Flat Panel Display up to 1080p/QXGA resolutions. The THC63LVD1024 converts the LVDS data streams back into 67bits of CMOS/TTL data with falling edge or rising edge clock for convenient with a variety of LCD panel controllers.

In Dual Link, data transmit clock frequency of 135MHz, 67bits of RGB data are transmitted at an effective rate of 945Mbps per LVDS channel. Using a 135MHz clock, the data throughput is 1.1Gbytes per second.

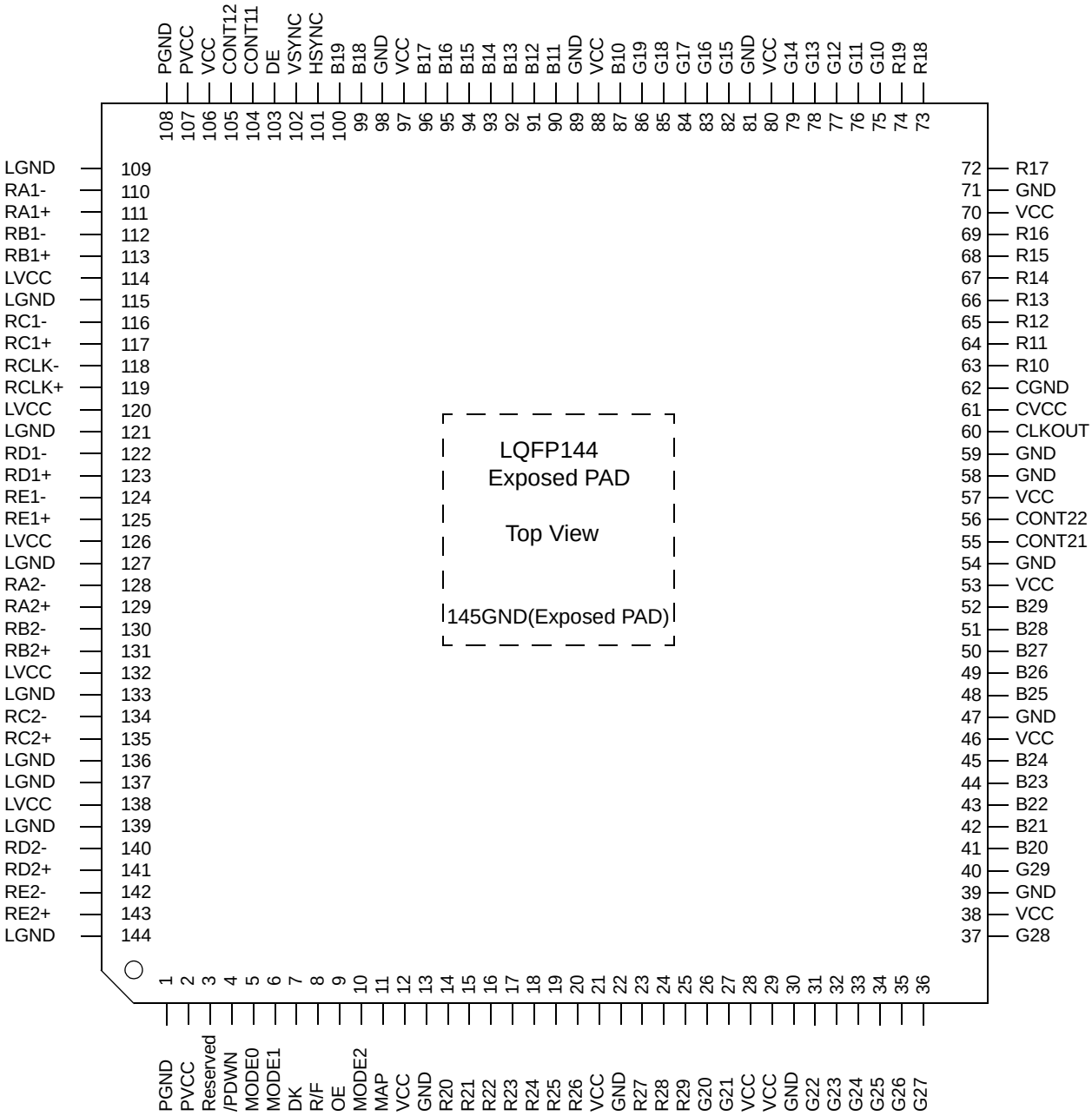
Features

- Wide dot clock range suited for TV Signal(480i-1080p), PC Signal(VGA-QXGA)
  Dual LVDS port IN/Dual TTL port Out Mode:
  8 - 135MHz(CLKOUT)
  Dual LVDS port IN/Single TTL port Out Mode:
  40 - 150MHz(CLKOUT)
- PLL requires No external components
- Flexible Input/Output mode
  1. Single/Dual LVDS port IN /Single/Dual TTL port OUT
  2. Double Edge output
- 50% output clock duty cycle
- TTL clock edge selectable
- TTL clock output timing programmable(3 step)
- 2 Output data mapping for simplifying PCB layout.
- Power down mode
- 144pin LQFP Exposed PAD
- EU RoHS Compliant

Block Diagram



Pin Diagram


LQFP144
Exposed PAD
Top View
145GND(Exposed PAD)
1 PGND
2 PVCC
3 Reserved
4 /PDWN
5 MODE0
6 MODE1
7 DK
8 R/F
9 OE
10 MODE2
11 MAP
12 VCC
13 GND
14 R20
15 R21
16 R22
17 R23
18 R24
19 R25
20 R26
21 VCC
22 GND
23 R27
24 R28
25 R29
26 G20
27 G21
28 VCC
29 VCC
30 GND
31 G22
32 G23
33 G24
34 G25
35 G26
36 G27
37 G28
38 VCC
39 GND
40 G29
41 B20
42 B21
43 B22
44 B23
45 B24
46 VCC
47 GND
48 B25
49 B26
50 B27
51 B28
52 B29
53 VCC
54 GND
55 CONT21
56 CONT22
57 VCC
58 GND
59 GND
60 CLKOUT
61 CVCC
62 CGND
63 R10
64 R11
65 R12
66 R13
67 R14
68 R15
69 R16
70 VCC
71 GND
72 R17
73 R18
74 R19
75 G10
76 G11
77 G12
78 G13
79 G14
80 VCC
81 GND
82 G15
83 G16
84 G17
85 G18
86 G19
87 B10
88 VCC
89 GND
90 B11
91 B12
92 B13
93 B14
94 B15
95 B16
96 B17
97 VCC
98 GND
99 B18
100 B19
101 HSYNC
102 VSYNC
103 DE
104 CONT11
105 CONT12
106 VCC
107 PVCC
108 PGND
109 LGND
110 RA1-
111 RA1+
112 RB1-
113 RB1+
114 LVCC
115 LGND
116 RC1-
117 RC1+
118 RCLK-
119 RCLK+
120 LVCC
121 LGND
122 RD1-
123 RD1+
124 RE1-
125 RE1+
126 LVCC
127 LGND
128 RA2-
129 RA2+
130 RB2-
131 RB2+
132 LVCC
133 LGND
134 RC2-
135 RC2+
136 LGND
137 LGND
138 LVCC
139 LGND
140 RD2-
141 RD2+
142 RE2-
143 RE2+
144 LGND

Pin Description

Pin Name	Pin #	Type	Description
RA1+, RA1-	111, 110	LVDS IN	The 1st Link. The 1st pixel input data when Dual Link.
RB1+, RB1-	113, 112	LVDS IN	
RC1+, RC1-	117, 116	LVDS IN	
RD1+, RD1-	123, 122	LVDS IN	
RE1+, RE1-	125, 124	LVDS IN	
RCLK+, RCLK-	119, 118	LVDS IN	LVDS Clock Input.
RA2+, RA2-	129, 128	LVDS IN	The 2nd Link. These pins are disabled when Single Link.
RB2+, RB2-	131, 130	LVDS IN	
RC2+, RC2-	135, 134	LVDS IN	
RD2+, RD2-	141, 140	LVDS IN	
RE2+, RE2-	143, 142	LVDS IN	
R19 ~ R10	74 - 72, 69 - 63	OUT	The 1st Pixel Data Outputs.
G19 ~ G10	86 - 82, 79 - 75	OUT	
B19 ~ B10	100, 99, 96-90, 87	OUT	
R29 ~ R20	25-23, 20-14	OUT	The 2nd Pixel Data Outputs.
G29 ~ G20	40, 37 - 31, 27, 26	OUT	
B29 ~ B20	52 - 48, 45 - 41	OUT	
CONT11,CONT12	104, 105	OUT	User defined data output
CONT21,CONT22	55, 56		
DE	103	OUT	Data Enable Output.
VSYNC	102	OUT	Vsync Output.
HSYNC	101	OUT	Hsync Output.
CLKOUT	60	OUT	Clock Output.
/PDWN	4	IN	Power down and Output Control.(Table1) H: Normal operation L: Power down
MODE1, MODE0	6, 5	IN	Pixel Data Mode.

MODE1	MODE0	Mode
H	H	Single Link (Single-in/Single-out)
H	L	Single Link (Single-in/Dual-out)
L	H	Dual Link (Dual-in/Single-out)
L	L	Dual Link (Dual-in/Dual-out)

Pin Description (Continued)

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>Type</th><th>Description</th></tr>
<tr><td>DK</td><td>7</td><td>IN</td><td>Output Clock Delay Timing Select.
t_{DOUT}=Output Data Cycle
<table>
<tr><th>MODE[1:0]</th><th>DK</th><th>Offset [ns]</th></tr>
<tr><td rowspan="3">LL
HH
HL</td><td>L</td><td>0</td></tr>
<tr><td>M</td><td>$-6\frac{t_{DOUT}}{28}$</td></tr>
<tr><td>H</td><td>$6\frac{t_{DOUT}}{28}$</td></tr>
<tr><td rowspan="3">LH</td><td>L</td><td>0</td></tr>
<tr><td>M</td><td>$-7\frac{t_{DOUT}}{28}$</td></tr>
<tr><td>H</td><td>$7\frac{t_{DOUT}}{28}$</td></tr>
</table></td></tr>
<tr><td>R/F</td><td>8</td><td>IN</td><td>Output Clock Triggering Edge Select.
H: Rising edge, L: Falling edge.</td></tr>
<tr><td>OE</td><td>9</td><td>IN</td><td>Output Enable.(Table1)
H: Output enable, L: Output disable</td></tr>
<tr><td>MODE2</td><td>10</td><td>IN</td><td>DDR function enable.
The use of this function depends on the setting of MODE<1:0>.
MODE<1:0>=LH(Dual-in/Single-out Mode)
H: DDR (Double Edge Output) function enable.
L: DDR (Double Edge Output) function disable.
MODE<1:0>=Other
Must be tied to GND</td></tr>
<tr><td>MAP</td><td>11</td><td>IN</td><td>LVDS mapping table select. See Fig9,10 and Table2 - 9.
H: Mapping Mode1
L: Mapping Mode2</td></tr>
<tr><td>Reserved</td><td>3</td><td>IN</td><td>Must be tied to VCC.</td></tr>
<tr><td>VCC</td><td>12, 21, 28, 29, 38, 46, 53, 57, 70, 80, 88, 97, 106</td><td>Power</td><td>Power Supply Pins for TTL outputs and digital circuitry.</td></tr>
<tr><td>GND</td><td>13, 22, 30, 39, 47, 54, 58, 59, 71, 81, 89, 98,145</td><td>Ground</td><td>Ground Pins for TTL outputs and digital circuitry.</td></tr>
<tr><td>LVCC</td><td>114, 120, 126, 132, 138</td><td>Power</td><td>Power Supply Pins for LVDS inputs.</td></tr>
<tr><td>LGND</td><td>109, 115, 121, 127, 133, 136, 137, 139, 144</td><td>Ground</td><td>Ground Pins for LVDS inputs.</td></tr>
<tr><td>PVCC</td><td>2, 107</td><td>Power</td><td>Power Supply Pin for PLL circuitry.</td></tr>
<tr><td>PGND</td><td>1, 108</td><td>Ground</td><td>Ground Pin for PLL circuitry.</td></tr>
<tr><td>CVCC</td><td>61</td><td>Power</td><td>Power Supply Pins for TTL output of CLKOUT.</td></tr>
<tr><td>CGND</td><td>62</td><td>Ground</td><td>Ground Pins for TTL output of CLKOUT</td></tr>
</table>

Pin Description (Continued)

Table 1. Output Control

/PDWN	OE	Data Outputs (Rxn)	CLKOUT
L	L	Hi-Z	Hi-Z
L	H	All Low	Fixed Low
H	L	Hi-Z	Hi-Z
H	H	Data Out	CLK Out

Absolute Maximum Ratings

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
Output Current	-30mA ~ 30mA
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +125°C
Reflow Peak Temperature / Time	+260°C / 10sec.
Maximum Power Dissipation @+25°C	4.4W

Recommended Operating Conditions

Parameter				Min.	Typ	Max	Unit
All Supply Voltage				3.0	3.3	3.6	V
Operating Ambient Temperature				-40	-	85	°C
CLK Frequency	MODE<1:0>=LL Dual-in/Dual-out Ta ≦ 70°C (Ta ≦ 85°C)*		LVDS Input	8	-	135 (80)*	MHz
			Output	8	-	135 (80)*	MHz
	MODE<1:0>=LH Dual-in/Single-out	Single Edge Output (MODE2=L)	LVDS Input	20	-	75	MHz
			Output	40	-	150	MHz
		Double Edge Output (MODE2=H)	LVDS Input	20	-	75	MHz
			Output	20	-	75	MHz
	MODE<1:0>=HL Single-in/Dual-out		LVDS Input	8	-	135	MHz
			Output	4	-	67.5	MHz
	MODE<1:0>=HH Single-in/Single-out		LVDS Input	8	-	135	MHz
			Output	8	-	135	MHz

Electrical Characteristics

CMOS/TTL DC Specifications

V_{CC}=VCC=PVCC=LVCC=CVCC

Symbol	Parameter	Conditions	Min.	Typ	Max	Unit
V_{IH}	High Level Input Voltage	/PDWN, MODE[2:0] R/F, OE, MAP Pin	2.0	-	V_{CC}	V
V_{IL}	Low Level Input Voltage		GND	-	0.8	V
V_{IH3}	High Level Input Voltage	3-Level Inputs (DK Pin)	$0.8V_{CC}$	-	V_{CC}	V
V_{IM3}	Middle Level Input Voltage		$0.6V_{CC}$	-	$0.4V_{CC}$	V
V_{IL3}	Low Level Input Voltage		GND	-	$0.2V_{CC}$	V
V_{OH}	High Level Output Voltage	I_{OH}= -8mA	2.4	-		V
V_{OL}	Low Level Output Voltage	I_{OL}= 8mA	-	-	0.4	V
I_{IL}	Input Leakage Current	/PDWN, MODE[2:0] R/F, OE, MAP Pin $0V \le V_{IN} \le V_{CC}$	-	-	±10	μA
I_{IL3}	3-Level Input Leakage Current	3-Level Inputs (DK Pin) $0V \le V_{IN} \le V_{CC}$	-	-	±10	μA

LVDS Receiver DC Specifications

V_{CC}=VCC=PVCC=LVCC=CVCC

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{TH}	Differential Input High Threshold	V_{IC}= 1.2V	-	-	100	mV
V_{TL}	Differential Input Low Threshold	V_{IC}= 1.2V	-100	-	-	mV
I_{ILD}	Differential Input Leakage Current	V_{IN}= 2.4V / 0V	-	-	30	μA

Electrical Characteristics (Continued)

Supply Current

V_{CC}=VCC=PVCC=LVCC=CVCC

Symbol	Parameter	Condition			Typ.	Max.	Unit
I_{RCCW}	Receiver Supply Current (Worst Case Pattern) Fig2.	CLKOUT=65MHz	CL=8pF	MODE<1:0>=HH Single-in/Single-out MODE2=L	-	201	mA
		CLKOUT=85MHz			-	248	mA
		CLKOUT=135MHz			-	364	mA
		CLKOUT=32.5MHz		MODE<1:0>=HL Single-in/ Dual-out	-	138	mA
		CLKOUT=42.5MHz			-	164	mA
		CLKOUT=67.5MHz			-	233	mA
		CLKOUT=65MHz		MODE<1:0>=LH Dual-in/Single-out MODE2=L DDR Output Off	-	146	mA
		CLKOUT=85MHz			-	165	mA
		CLKOUT=135MHz			-	210	mA
		CLKOUT=150MHz			-	223	mA
		CLKOUT=32.5MHz		MODE<1:0>=LH Dual-in/Single-out MODE2=H DDR Output On	-	147	mA
		CLKOUT=42.5MHz			-	165	mA
		CLKOUT=67.5MHz			-	205	mA
		CLKOUT=75MHz			-	217	mA
		CLKIN=65MHz		MODE<1:0>=LL Dual-in/Dual-out	-	366	mA
		CLKIN=85MHz			-	453	mA
		CLKIN=135MHz		MODE<1:0>=LL Dual-in/Dual-out Ta ≦ 70°C	-	671	mA
I_{RCCS}	Receiver Power Down Supply Current	/PDWN = L			-	50	μA

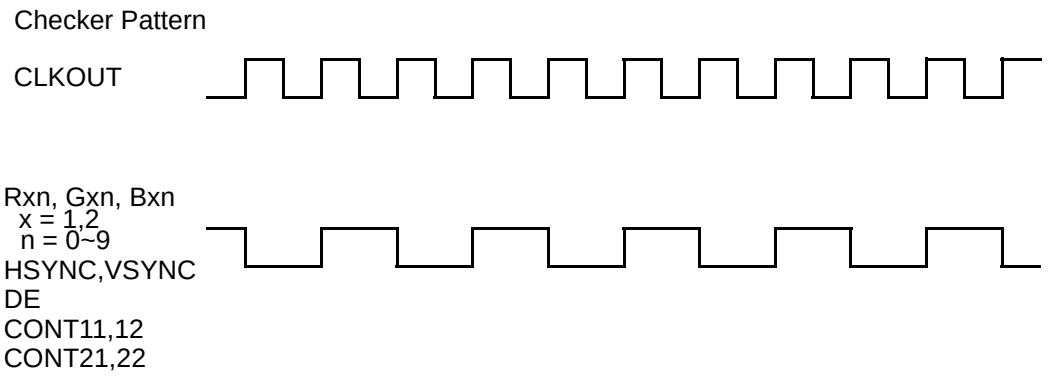


Fig1. Test Pattern

Electrical Characteristics (Continued)

Output load limitation

Output load is limited so that Junction temperature is not over 125°C

calculating formula

$Tj = Ta + \theta_{ja} * P$

$P = V_{CC} * (I_{OUTDT} + I_{OUTCK} + I_{CORE})$

$I_{OUTDT} = 1/2 * F_{CLK} * V_{CC} * C_{LOAD} * n$

$I_{OUTCK} = F_{CLK} * V_{CC} * C_{LOAD}$

Tj : Junction temperature ≦ 125°C

Ta : Ambient temperature ≦ 70°C

θ_{ja} : Package thermal resistance = 22 [°C /W]

I_{CORE}: Supply Current except all output buffers = 520mA

I_{OUTDT}: Supply Current only output buffers of data output.
(R1,G1,B1,R2,G2,B2,HSYNC,VSYNC,DE,CONT11,CONT12,CONT21,CONT22)

I_{OUTCK}: Supply Current only output buffer of CLKOUT.

F_{CLK} : CLKOUT Frequency

n : 67 (Number of data output pin)

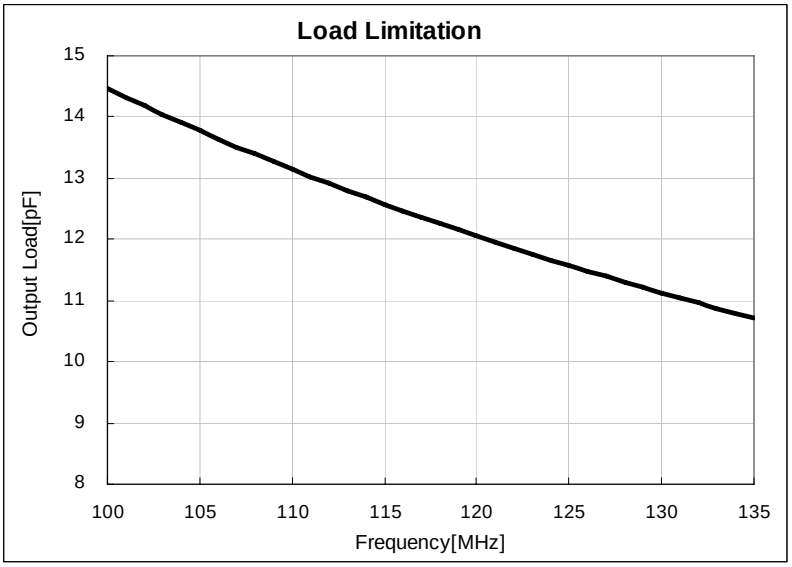


Fig2. CMOS/TTL Output Load Limitation

Switching Characteristics

VCC=VCC=PVCC=LVCC=CVCC

Symbol	Parameter		Min.	Typ.	Max.	Unit
t_{RCP}	CLKOUT Period (Fig4)		6.67	T	250	ns
t_{RCH}	CLKOUT High Time(Fig4)		-	$\frac{T}{2}$	-	ns
t_{RCL}	CLKOUT Low Time(Fig4)		-	$\frac{T}{2}$	-	ns
t_{DOUT}	TTL Data OUT Period (Fig5,6)		6.67	T	250	ns
t_{RS}	TTL Data Setup to CLKOUT(Fig5,6)		$0.45t_{DOUT}$ -0.45	-	-	ns
t_{RH}	TTL Data Hold to CLKOUT(Fig5,6)		$0.45t_{DOUT}$ -0.45	-	-	ns
t_{TLH}	TTL Low to High Transition Time(Fig3)		-	0.7	1.0	ns
t_{THL}	TTL High to Low Transition Time(Fig3)		-	0.7	1.0	ns
t_{SK}	Receiver Skew Margin (Fig7)	t_{RCIP}=65MHz	-650	0	650	ps
		t_{RCIP}=85MHz	-450	0	450	ps
		t_{RCIP}=108MHz	-250	0	250	ps
		t_{RCIP}=135MHz	-170	0	170	ps
t_{RIP1}	Input Data Position0 (Fig7)		$-t_{SK}$	0	$+t_{SK}$	ns
t_{RIP0}	Input Data Position1 (Fig7)		$\frac{t_{RCIP}}{7} - t_{SK}$	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RIP6}	Input Data Position2 (Fig7)		$2\frac{t_{RCIP}}{7} - t_{SK}$	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RIP5}	Input Data Position3 (Fig7)		$3\frac{t_{RCIP}}{7} - t_{SK}$	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RIP4}	Input Data Position4 (Fig7)		$4\frac{t_{RCIP}}{7} - t_{SK}$	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RIP3}	Input Data Position5 (Fig7)		$5\frac{t_{RCIP}}{7} - t_{SK}$	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RIP2}	Input Data Position6 (Fig7)		$6\frac{t_{RCIP}}{7} - t_{SK}$	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RPLL}	Phase Lock Loop Set (Fig8)		-	-	10.0	ms
t_{RCD}	RCLK +/- to CLK OUT Delay (Fig9) MODE<1:0>=LL DK=L, 75MHz		89.7	-	94	ns
t_{RCIP}	CLKIN Period (Fig7)		7.4	-	125.0	ns
t_{RCIH}	Differential CLKIN High Time (Fig7)		$2\frac{t_{RCIP}}{7}$	-	$5\frac{t_{RCIP}}{7}$	ns
t_{RCIL}	Differential CLKIN Low Time (Fig7)		$2\frac{t_{RCIP}}{7}$	-	$5\frac{t_{RCIP}}{7}$	ns
t_{DEINT}	MODE<1:0>=HL (Single IN/ Dual OUT Mode) Only	DE input period (Fig9-1)	$4t_{RCIP}$	t_{RCIP}*(2n) n= integer	-	ns
t_{DEH}		DE input High time (Fig9-1)	$2t_{RCIP}$	-	-	ns
t_{DEL}		DE input Low time (Fig9-1)	$2t_{RCIP}$	-	-	ns

AC Timing Diagrams

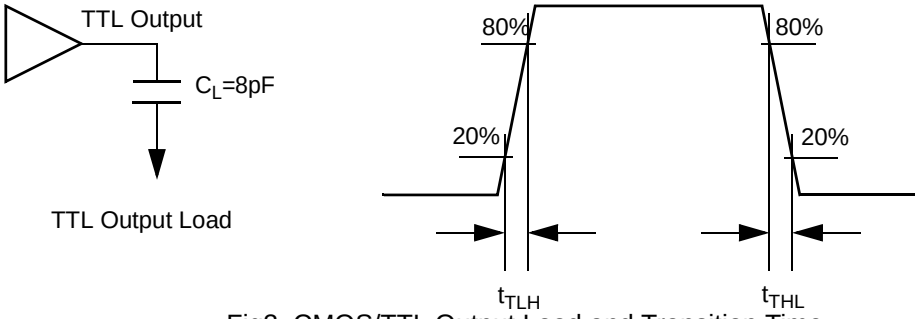


Fig3. CMOS/TTL Output Load and Transition Time

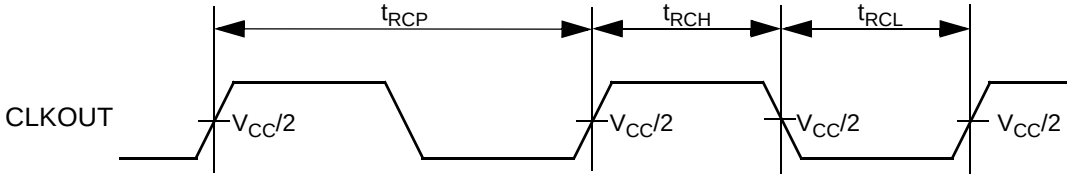


Fig4. CLKOUT Period and High/Low Time

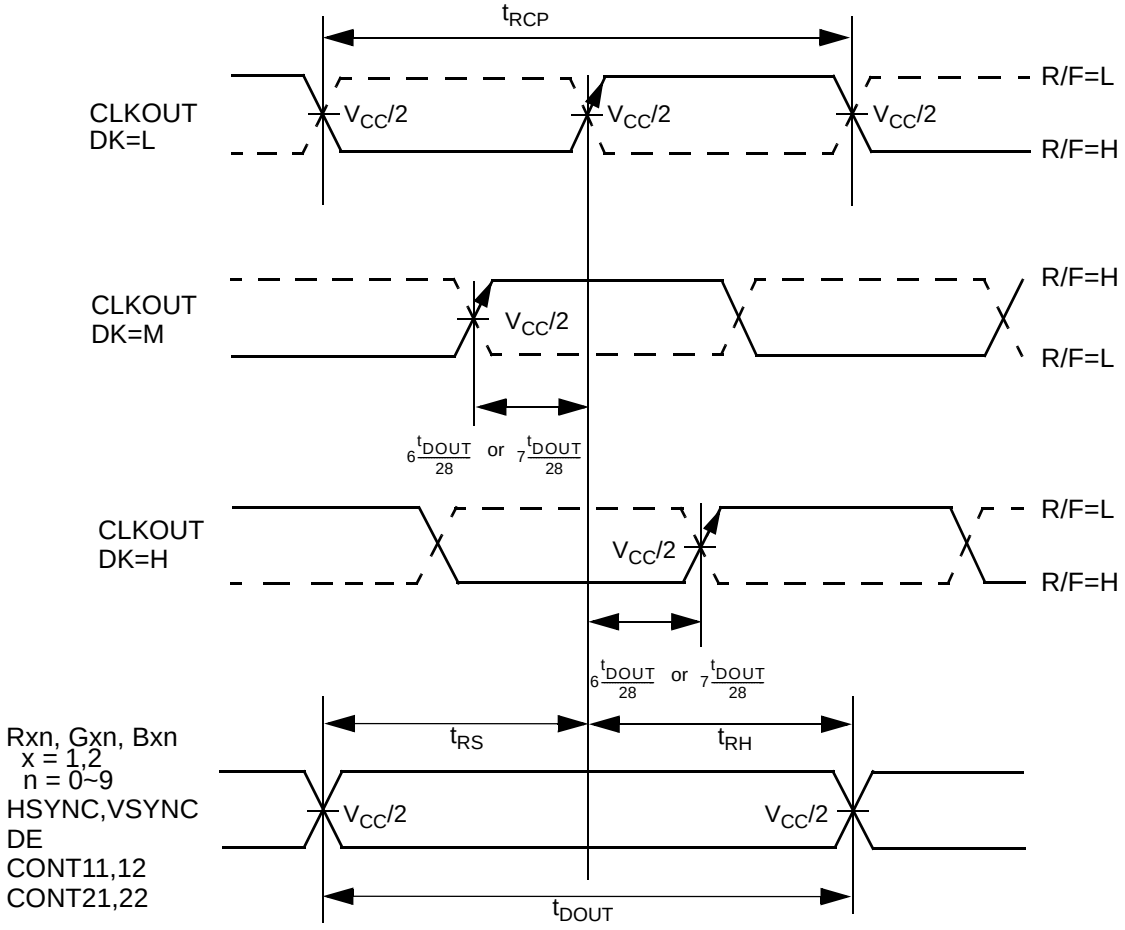


Fig5. CLKOUT Position and Setup/Hold Timing

AC Timing Diagrams (Continued)

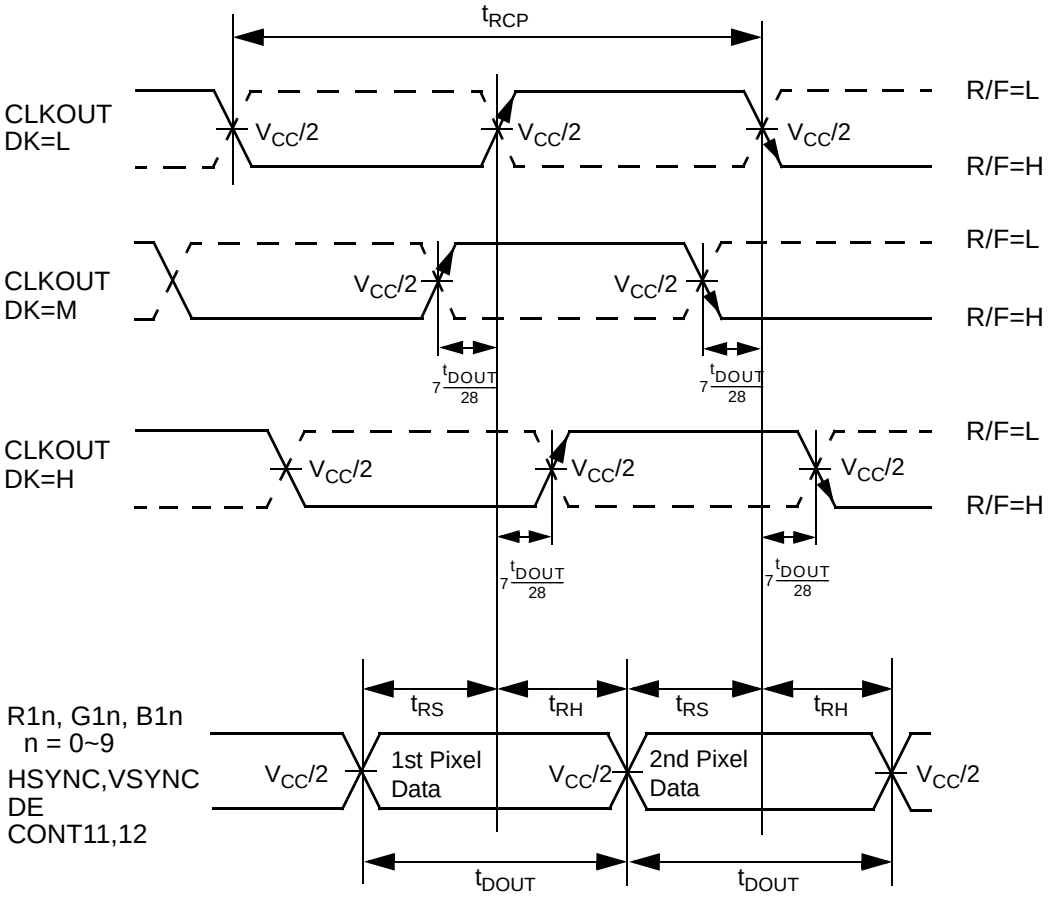


Fig6. CLKOUT Position and Setup/Hold Timing for Double Edge Output Mode
MODE<1:0>=LH, MODE2=H

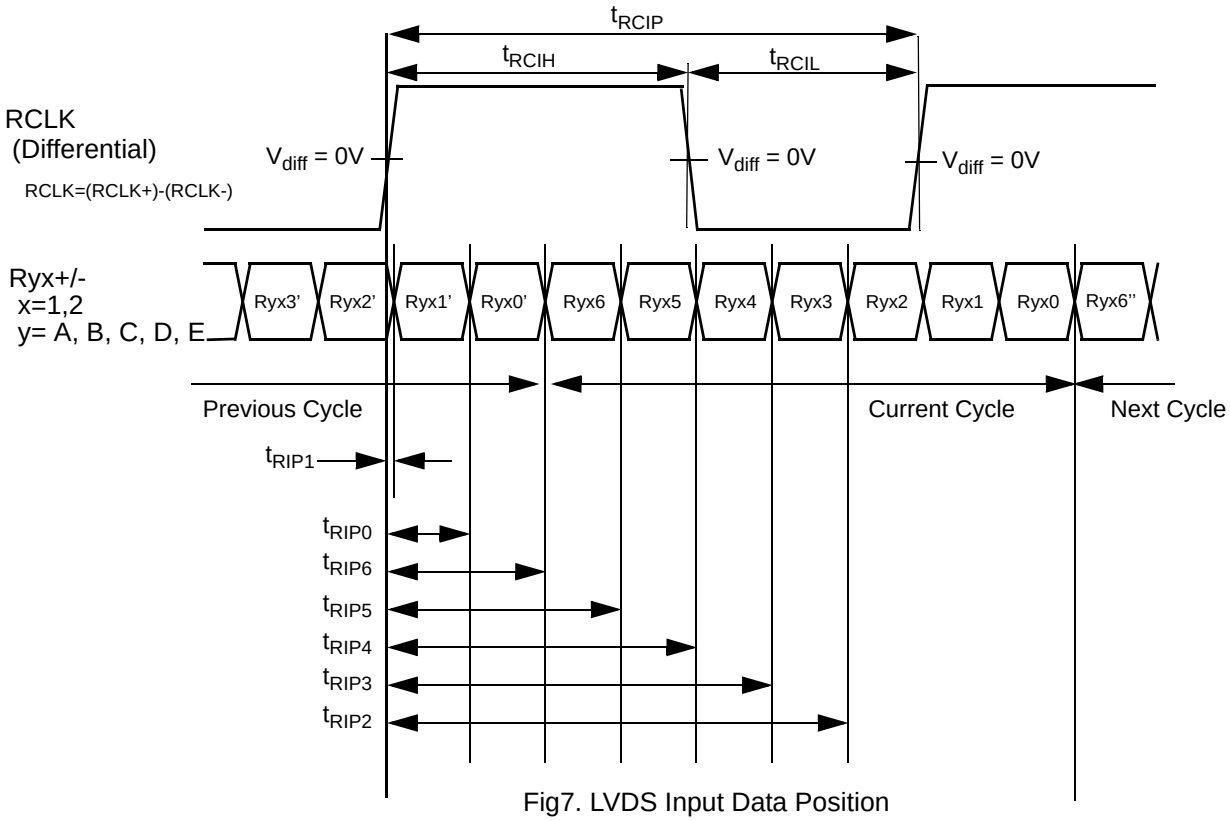


Fig7. LVDS Input Data Position

AC Timing Diagrams (Continued)

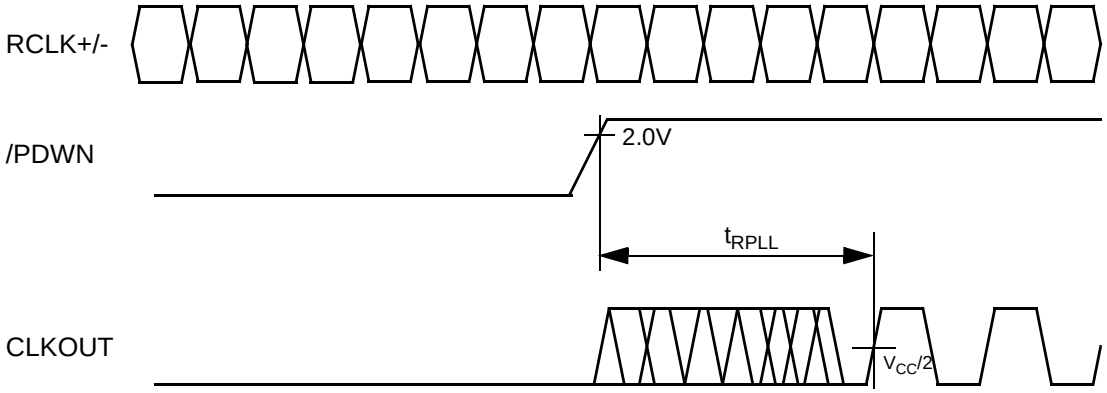


Fig8. PLL Lock Loop Set Time

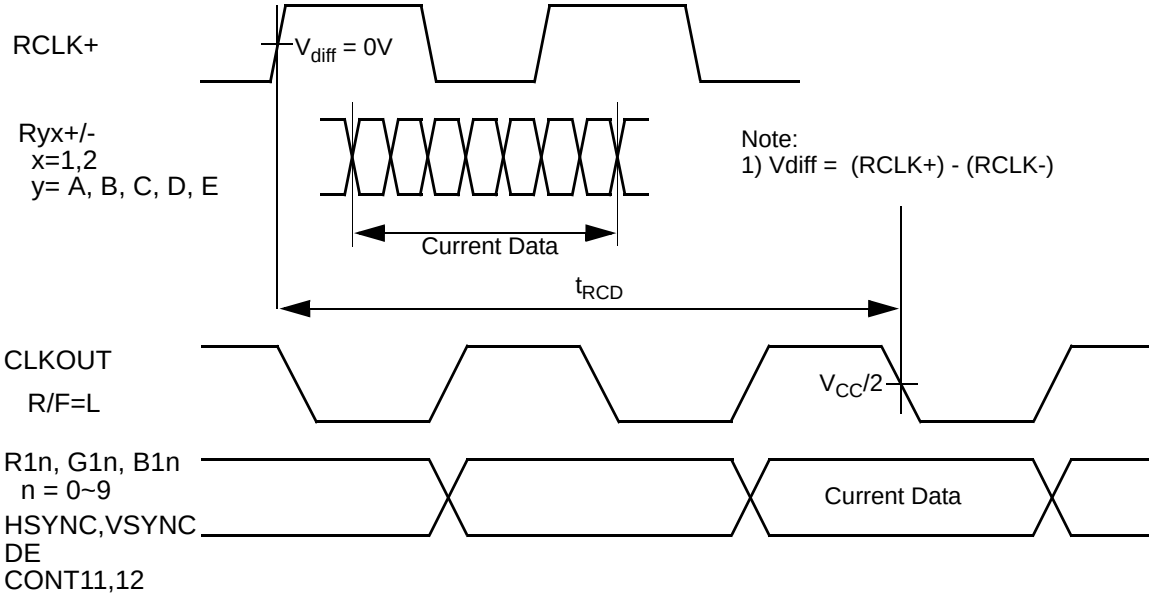


Fig9. RCLK +/- to CLKOUT Delay

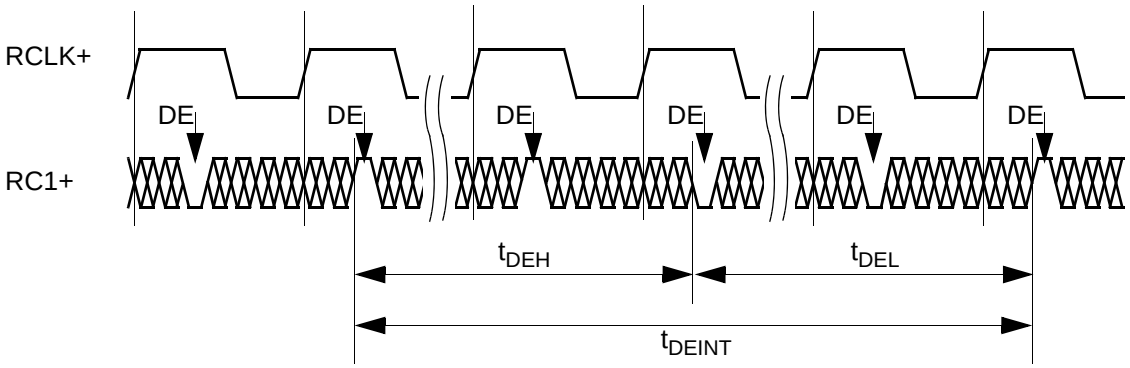


Fig9-1. Single IN / Dual OUT mode RC1(DE) input timing

Output Data Mapping

Table2. Output Color Data naming rule

X	Y	Z	Description	
X=R	-	-	Red Color Data	
X=G	-	-	Green Color Data	
X=B	-	-	Blue Color Data	
	Y= None	-	Single Pixel	
	Y=O	-	Dual Pixel	1st Pixel Data
	Y=E	-		2nd Pixel Data
		Z=0-9	Bit number 0: LSB (Least Significant Bit) 9: MSB (Most Significant Bit)	

Table3. TTL/CMOS Output Data Mapping (Single-out mode, MODE0=H)

Data Signal			Receiver Output Pin Name		
30-bit	24-bit	18-bit	30-bit	24-bit	18-bit
R0	-	-	R10	-	-
R1	-	-	R11	-	-
R2	R0	-	R12	R12	-
R3	R1	-	R13	R13	-
R4	R2	R0	R14	R14	R14
R5	R3	R1	R15	R15	R15
R6	R4	R2	R16	R16	R16
R7	R5	R3	R17	R17	R17
R8	R6	R4	R18	R18	R18
R9	R7	R5	R19	R19	R19
G0	-	-	G10	-	-
G1	-	-	G11	-	-
G2	G0	-	G12	G12	-
G3	G1	-	G13	G13	-
G4	G2	G0	G14	G14	G14
G5	G3	G1	G15	G15	G15
G6	G4	G2	G16	G16	G16
G7	G5	G3	G17	G17	G17
G8	G6	G4	G18	G18	G18
G9	G7	G5	G19	G19	G19
B0	-	-	B10	-	-
B1	-	-	B11	-	-
B2	B0	-	B12	B12	-
B3	B1	-	B13	B13	-
B4	B2	B0	B14	B14	B14
B5	B3	B1	B15	B15	B15
B6	B4	B2	B16	B16	B16
B7	B5	B3	B17	B17	B17
B8	B6	B4	B18	B18	B18
B9	B7	B5	B19	B19	B19

Output Data Mapping (Continued)

Table4. TTL/CMOS Output Data Mapping (Dual-out mode, MODE0=L)

1st Pixel Data						2nd Pixel Data					
Data Signal			Receiver Output Pin Name			Data Signal			Receiver Output Pin Name		
30-bit	24-bit	18-bit	30-bit	24-bit	18-bit	30-bit	24-bit	18-bit	30-bit	24-bit	18-bit
RE0	-	-	R10	-	-	RO0	-	-	R20	-	-
RE1	-	-	R11	-	-	RO1	-	-	R22	-	-
RE2	RE0	-	R12	R12	-	RO2	RO0	-	R22	R22	-
RE3	RE1	-	R13	R13	-	RO3	RO1	-	R23	R23	-
RE4	RE2	RE0	R14	R14	R14	RO4	RO2	RO0	R24	R24	R24
RE5	RE3	RE1	R15	R15	R15	RO5	RO3	RO1	R25	R25	R25
RE6	RE4	RE2	R16	R16	R16	RO6	RO4	RO2	R26	R26	R26
RE7	RE5	RE3	R17	R17	R17	RO7	RO5	RO3	R27	R27	R27
RE8	RE6	RE4	R18	R18	R18	RO8	RO6	RO4	R28	R28	R28
RE9	RE7	RE5	R19	R19	R19	RO9	RO7	RO5	R29	R29	R29
GE0	-	-	G10	-	-	GO0	-	-	G20	-	-
GE1	-	-	G11	-	-	GO1	-	-	G22	-	-
GE2	GE0	-	G12	G12	-	GO2	GO0	-	G22	G22	-
GE3	GE1	-	G13	G13	-	GO3	GO1	-	G23	G23	-
GE4	GE2	GE0	G14	G14	G14	GO4	GO2	GO0	G24	G24	G24
GE5	GE3	GE1	G15	G15	G15	GO5	GO3	GO1	G25	G25	G25
GE6	GE4	GE2	G16	G16	G16	GO6	GO4	GO2	G26	G26	G26
GE7	GE5	GE3	G17	G17	G17	GO7	GO5	GO3	G27	G27	G27
GE8	GE6	GE4	G18	G18	G18	GO8	GO6	GO4	G28	G28	G28
GE9	GE7	GE5	G19	G19	G19	GO9	GO7	GO5	G29	G29	G29
BE0	-	-	B10	-	-	BO0	-	-	B20	-	-
BE1	-	-	B11	-	-	BO1	-	-	B22	-	-
BE2	BE0	-	B12	B12	-	BO2	BO0	-	B22	B22	-
BE3	BE1	-	B13	B13	-	BO3	BO1	-	B23	B23	-
BE4	BE2	BE0	B14	B14	B14	BO4	BO2	BO0	B24	B24	B24
BE5	BE3	BE1	B15	B15	B15	BO5	BO3	BO1	B25	B25	B25
BE6	BE4	BE2	B16	B16	B16	BO6	BO4	BO2	B26	B26	B26
BE7	BE5	BE3	B17	B17	B17	BO7	BO5	BO3	B27	B27	B27
BE8	BE6	BE4	B18	B18	B18	BO8	BO6	BO4	B28	B28	B28
BE9	BE7	BE5	B19	B19	B19	BO9	BO7	BO5	B29	B29	B29

LVDS Input Data Mapping

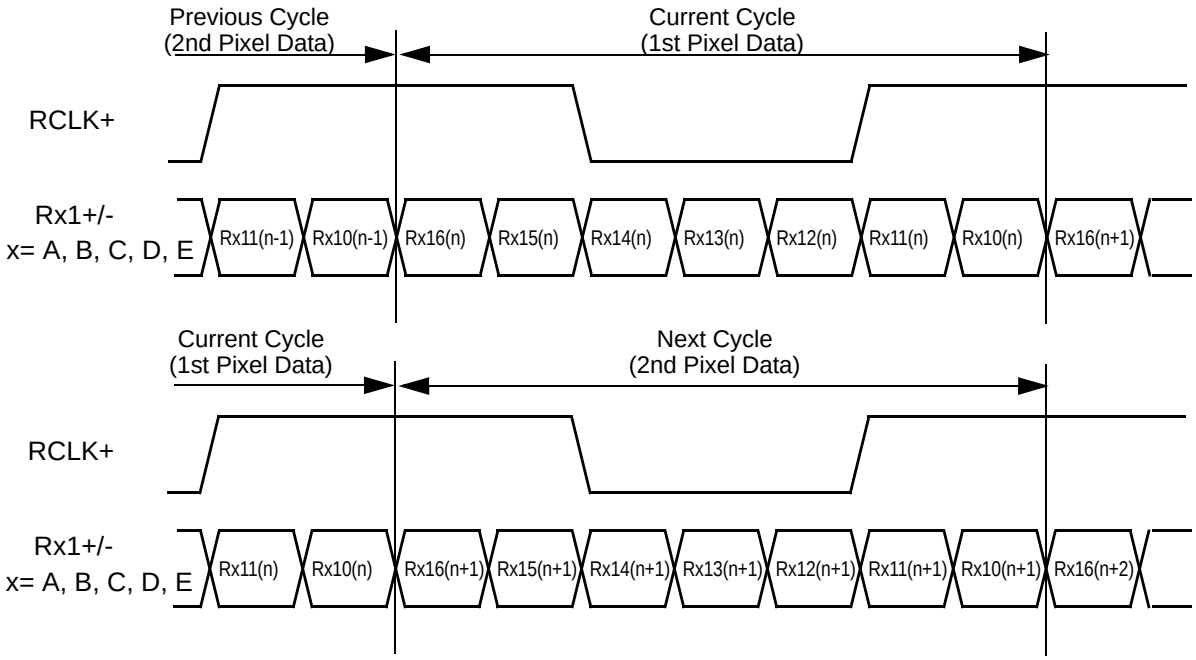


Fig10. LVDS Inputs Mapped to TTL Data Outputs
MODE1= H (Single-in Mode)

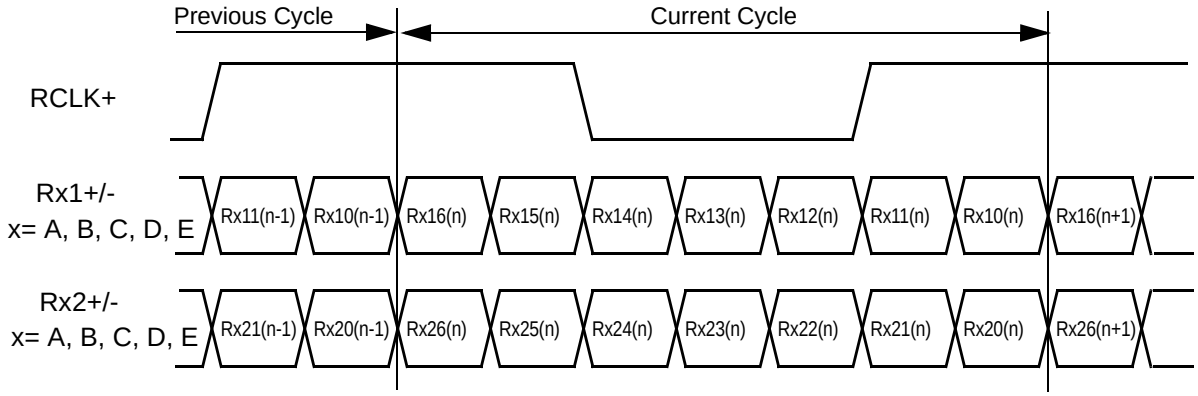


Fig11. LVDS Inputs Mapped to TTL Data Outputs
MODE1= L (Dual-in Mode)

LVDS Input Data Mapping (Continued)

Table5. LVDS Input Data Mapping (Single-in/Single-out, MODE<1:0>=HH)

LVDS Input Data	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)
RA10	R14	R12
RA11	R15	R13
RA12	R16	R14
RA13	R17	R15
RA14	R18	R16
RA15	R19	R17
RA16	G14	G12
RB10	G15	G13
RB11	G16	G14
RB12	G17	G15
RB13	G18	G16
RB14	G19	G17
RB15	B14	B12
RB16	B15	B13
RC10	B16	B14
RC11	B17	B15
RC12	B18	B16
RC13	B19	B17
RC14	HSYNC	HSYNC
RC15	VSYNC	VSYNC
RC16	DE	DE
RD10	R12	R18
RD11	R13	R19
RD12	G12	G18
RD13	G13	G19
RD14	B12	B18
RD15	B13	B19
RD16	CONT11	CONT11
RE10	R10	R10
RE11	R11	R11
RE12	G10	G10
RE13	G11	G11
RE14	B10	B10
RE15	B11	B11
RE16	CONT12	CONT12

LVDS Input Data Mapping (Continued)

Table6. LVDS Input Data Mapping (Single-in/Dual-out, MODE<1:0>=HL)

1st Pixel Data			2nd Pixel Data		
LVDS Input Data (1st Pixel Data)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)	LVDS Input Data (1st Pixel Data)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)
RA10(n)	R14	R12	RA10(n+1)	R24	R22
RA11(n)	R15	R13	RA11(n+1)	R25	R23
RA12(n)	R16	R14	RA12(n+1)	R26	R24
RA13(n)	R17	R15	RA13(n+1)	R27	R25
RA14(n)	R18	R16	RA14(n+1)	R28	R26
RA15(n)	R19	R17	RA15(n+1)	R29	R27
RA16(n)	G14	G12	RA16(n+1)	G24	G22
RB10(n)	G15	G13	RB10(n+1)	G25	G23
RB11(n)	G16	G14	RB11(n+1)	G26	G24
RB12(n)	G17	G15	RB12(n+1)	G27	G25
RB13(n)	G18	G16	RB13(n+1)	G28	G26
RB14(n)	G19	G17	RB14(n+1)	G29	G27
RB15(n)	B14	B12	RB15(n+1)	B24	B22
RB16(n)	B15	B13	RB16(n+1)	B25	B23
RC10(n)	B16	B14	RC10(n+1)	B26	B24
RC11(n)	B17	B15	RC11(n+1)	B27	B25
RC12(n)	B18	B16	RC12(n+1)	B28	B26
RC13(n)	B19	B17	RC13(n+1)	B29	B27
RC14(n)	HSYNC	HSYNC	RC14(n+1)	HSYNC	HSYNC
RC15(n)	VSYNC	VSYNC	RC15(n+1)	VSYNC	VSYNC
RC16(n)	DE	DE	RC16(n+1)	DE	DE
RD10(n)	R12	R18	RD10(n+1)	R22	R28
RD11(n)	R13	R19	RD11(n+1)	R23	R29
RD12(n)	G12	G18	RD12(n+1)	G22	G28
RD13(n)	G13	G19	RD13(n+1)	G23	G29
RD14(n)	B12	B18	RD14(n+1)	B22	B28
RD15(n)	B13	B19	RD15(n+1)	B23	B29
RD16(n)	CONT11	CONT11	RD16(n+1)	CONT21	CONT21
RE10(n)	R10	R10	RE10(n+1)	R20	R20
RE11(n)	R11	R11	RE11(n+1)	R21	R21
RE12(n)	G10	G10	RE12(n+1)	G20	G20
RE13(n)	G11	G11	RE13(n+1)	G21	G21
RE14(n)	B10	B10	RE14(n+1)	B20	B20
RE15(n)	B11	B11	RE15(n+1)	B21	B21
RE16(n)	CONT12	CONT12	RE16(n+1)	CONT22	CONT22

LVDS Input Data Mapping (Continued)

Table7. LVDS Input Data Mapping (Dual-in/Single-out DDR On or Off, MODE<1:0>=LH, MODE2=H or L)

1st Pixel Data			2nd Pixel Data		
LVDS Input Data (1st Pixel Data)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)	LVDS Input Data (2nd Pixel Data)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)
RA10	R14(n)	R12(n)	RA20	R14(n+1)	R12(n+1)
RA11	R15(n)	R13(n)	RA21	R15(n+1)	R13(n+1)
RA12	R16(n)	R14(n)	RA22	R16(n+1)	R14(n+1)
RA13	R17(n)	R15(n)	RA23	R17(n+1)	R15(n+1)
RA14	R18(n)	R16(n)	RA24	R18(n+1)	R16(n+1)
RA15	R19(n)	R17(n)	RA25	R19(n+1)	R17(n+1)
RA16	G14(n)	G12(n)	RA26	G14(n+1)	G12(n+1)
RB10	G15(n)	G13(n)	RB20	G15(n+1)	G13(n+1)
RB11	G16(n)	G14(n)	RB21	G16(n+1)	G14(n+1)
RB12	G17(n)	G15(n)	RB22	G17(n+1)	G15(n+1)
RB13	G18(n)	G16(n)	RB23	G18(n+1)	G16(n+1)
RB14	G19(n)	G17(n)	RB24	G19(n+1)	G17(n+1)
RB15	B14(n)	B12(n)	RB25	B14(n+1)	B12(n+1)
RB16	B15(n)	B13(n)	RB26	B15(n+1)	B13(n+1)
RC10	B16(n)	B14(n)	RC20	B16(n+1)	B14(n+1)
RC11	B17(n)	B15(n)	RC21	B17(n+1)	B15(n+1)
RC12	B18(n)	B16(n)	RC22	B18(n+1)	B16(n+1)
RC13	B19(n)	B17(n)	RC23	B19(n+1)	B17(n+1)
RC14	HSYNC(n)	HSYNC(n)	RC24	HSYNC(n+1)	HSYNC(n+1)
RC15	VSYNC(n)	VSYNC(n)	RC25	VSYNC(n+1)	VSYNC(n+1)
RC16	DE(n)	DE(n)	RC26	DE(n+1)	DE(n+1)
RD10	R12(n)	R18(n)	RD20	R12(n+1)	R18(n+1)
RD11	R13(n)	R19(n)	RD21	R13(n+1)	R19(n+1)
RD12	G12(n)	G18(n)	RD22	G12(n+1)	G18(n+1)
RD13	G13(n)	G19(n)	RD23	G13(n+1)	G19(n+1)
RD14	B12(n)	B18(n)	RD24	B12(n+1)	B18(n+1)
RD15	B13(n)	B19(n)	RD25	B13(n+1)	B19(n+1)
RD16	CONT11(n)	CONT11(n)	RD26	CONT11(n+1)	CONT11(n+1)
RE10	R10(n)	R10(n)	RE20	R10(n+1)	R10(n+1)
RE11	R11(n)	R11(n)	RE21	R11(n+1)	R11(n+1)
RE12	G10(n)	G10(n)	RE22	G10(n+1)	G10(n+1)
RE13	G11(n)	G11(n)	RE23	G11(n+1)	G11(n+1)
RE14	B10(n)	B10(n)	RE24	B10(n+1)	B10(n+1)
RE15	B11(n)	B11(n)	RE25	B11(n+1)	B11(n+1)
RE16	CONT12(n)	CONT12(n)	RE26	CONT12(n+1)	CONT12(n+1)

LVDS Input Data Mapping (Continued)

Table8. LVDS Input Data Mapping (Dual-in/Dual-out, MODE<1:0>=LL)

1st Pixel Data			2nd Pixel Data		
LVDS Input Data (1st Pixel Data)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)	LVDS Input Data (2nd Pixel Data)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)
RA10	R14	R12	RA20	R24	R22
RA11	R15	R13	RA21	R25	R23
RA12	R16	R14	RA22	R26	R24
RA13	R17	R15	RA23	R27	R25
RA14	R18	R16	RA24	R28	R26
RA15	R19	R17	RA25	R29	R27
RA16	G14	G12	RA26	G24	G22
RB10	G15	G13	RB20	G25	G23
RB11	G16	G14	RB21	G26	G24
RB12	G17	G15	RB22	G27	G25
RB13	G18	G16	RB23	G28	G26
RB14	G19	G17	RB24	G29	G27
RB15	B14	B12	RB25	B24	B22
RB16	B15	B13	RB26	B25	B23
RC10	B16	B14	RC20	B26	B24
RC11	B17	B15	RC21	B27	B25
RC12	B18	B16	RC22	B28	B26
RC13	B19	B17	RC23	B29	B27
RC14	HSYNC	HSYNC	RC24	N/A	
RC15	VSYNC	VSYNC	RC25		
RC16	DE	DE	RC26		
RD10	R12	R18	RD20	R22	R28
RD11	R13	R19	RD21	R23	R29
RD12	G12	G18	RD22	G22	G28
RD13	G13	G19	RD23	G23	G29
RD14	B12	B18	RD24	B22	B28
RD15	B13	B19	RD25	B23	B29
RD16	CONT11	CONT11	RD26	CONT21	CONT21
RE10	R10	R10	RE20	R20	R20
RE11	R11	R11	RE21	R21	R21
RE12	G10	G10	RE22	G20	G20
RE13	G11	G11	RE23	G21	G21
RE14	B10	B10	RE24	B20	B20
RE15	B11	B11	RE25	B21	B21
RE16	CONT12	CONT12	RE26	CONT22	CONT22

Note

1)Power On Sequence

Power on LVDS-Tx after THC63LVD1024.

2)Cable Connection and Disconnection

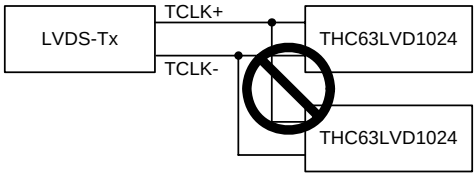
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

3)GND Connection

Connect the each GND of the PCB which LVDS-Tx and THC63LVD1024 on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

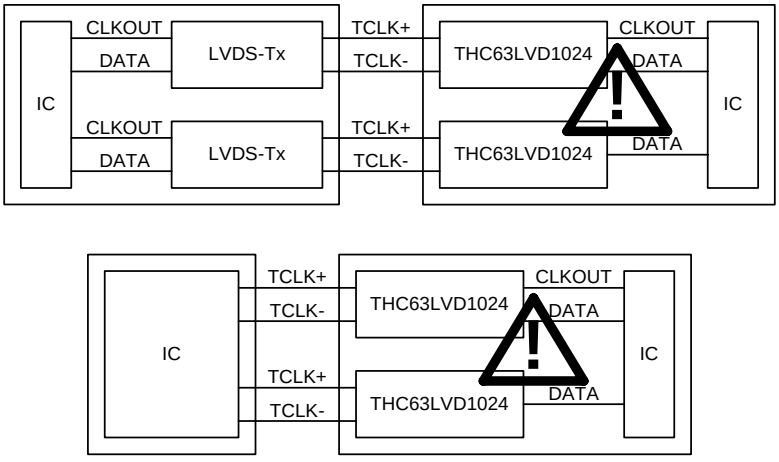
4)Multi Drop Connection

Multi drop connection is not recommended.



5)Asynchronous use

Asynchronous use such as following system is not recommended.



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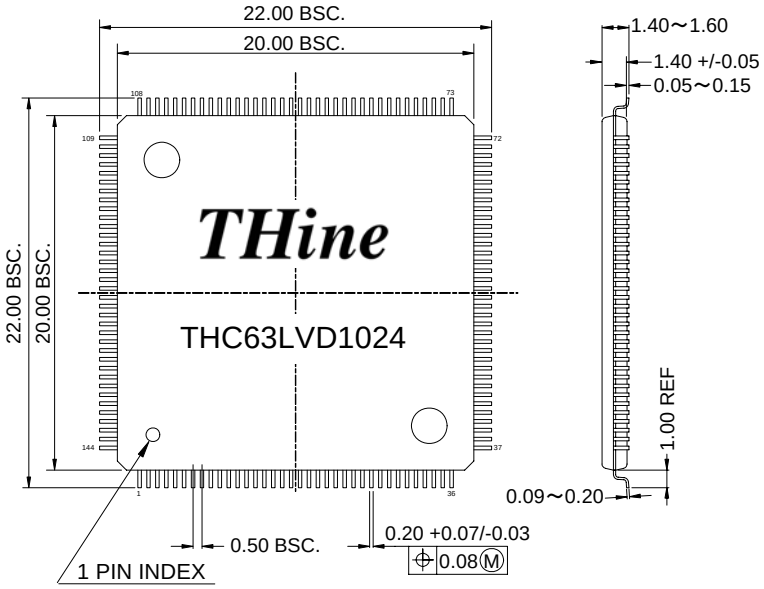
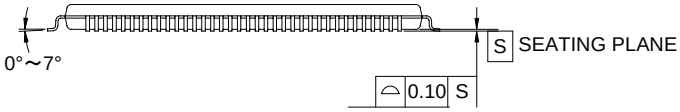
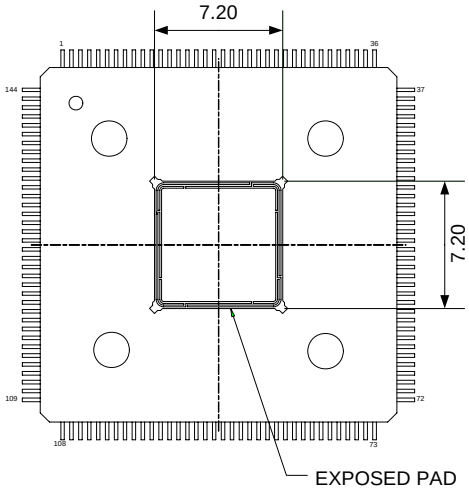
Package

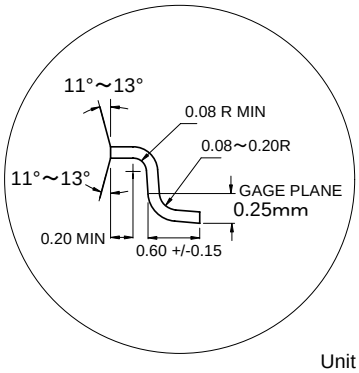


TOP VIEW





BOTTOM VIEW



Unit : mm

Exposed PAD is GND and must be soldered to PCB.

Notices and Requests

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