DUAL HIGH-SPEED DIFFERENTIAL LINE DRIVER

Check for Samples: uA9638C-EP

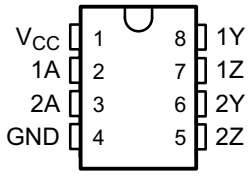
FEATURES

- **Meets or Exceeds ANSI Standard EIA/TIA-422-B**
- **Operates From a Single 5-V Power Supply**
- **Drives Loads as Low as 50 Ω up to 15 Mbps**
- **TTL- and CMOS-Input Compatibility**
- **Output Short-Circuit Protection**
- **Interchangeable With National Semiconductor™ DS9638**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Rated From –40°C to 85°C**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

D PACKAGE
(TOP VIEW)

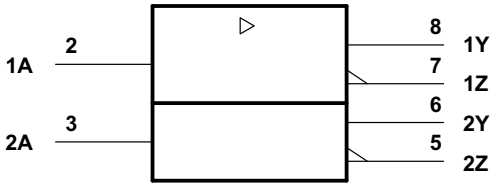


DESCRIPTION

The uA9638C is a dual high-speed differential line driver designed to meet ANSI Standard EIA/TIA-422-B. The inputs are TTL and CMOS compatible and have input clamp diodes. Schottky-diode-clamped transistors are used to minimize propagation delay time. This device operates from a single 5-V power supply and is supplied in an 8-pin package.

The uA9638 provides the current needed to drive low-impedance loads at high speeds. Typically used with twisted-pair cabling and differential receiver(s), base-band data transmission can be accomplished up to and exceeding 15 Mbps in properly designed systems. The uA9637A dual line receiver is commonly used as the receiver. For even faster switching speeds in the same pin configuration, see the SN75ALS191.

The uA9638C is characterized for operation from -40°C to 85°C.



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Figure 1. Logic Symbol

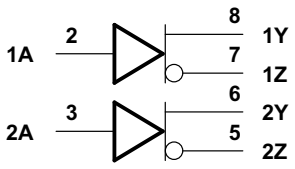


Figure 2. Logic Diagram

ORDERING INFORMATION(1)

$T_A = T_J$	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–40°C to 85°C	SOIC - D	Reel of 2500	UA9638CIDREP	9638I	V62/12606-10XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

SCHEMATICS OF INPUTS AND OUTPUTS

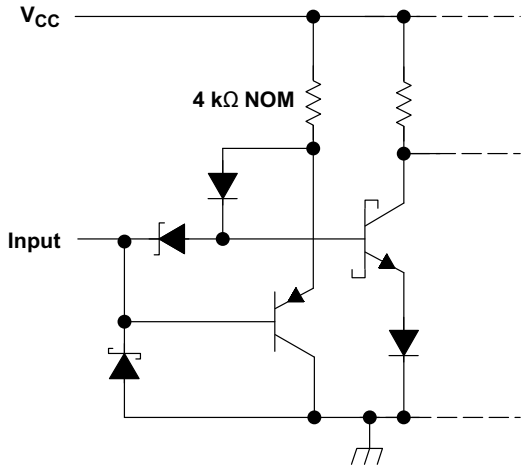


Figure 3. Equivalent of Each Input

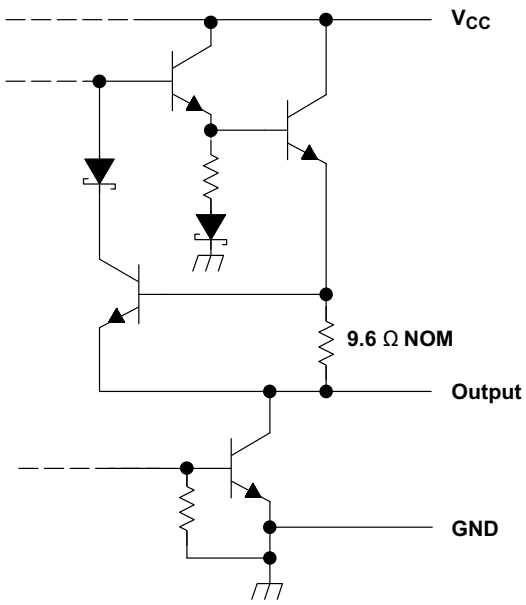


Figure 4. Typical of All Inputs

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage range(2)	–0.5 V to 7 V
V_I	Input voltage range	–0.5 V to 7 V
	Continuous total power dissipation	See Dissipation Ratings Table
	Lead temperature 1,6 mm (1/16 inch) from 10 seconds	260°C
T_A	Operating free-air temperature range	–40°C to 85°C
T_{stg}	Storage temperature range	–65°C to 150°C

(1) Voltage values except differential output voltages are with respect to network GND.
(2) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC[1]		uA9638C D 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	114.3	°C/W
θ_{JC}	Junction-to-case thermal resistance	59.1	
θ_{JB}	Junction-to-board thermal resistance[3]	55.3	
ψ_{JT}	Junction-to-top characterization parameter[4]	12.7	
ψ_{JB}	Junction-to-board characterization parameter[5]	54.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

DISSIPATION RATINGS

PACKAGE	POWER RATING T_A = 25°C (mW)	DERATING FACTOR T_A > 70°C (mW/°C)	POWER RATING T_A = 85°C (mW)
D	725	8.75	199

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-50	mA
I_{OL}	Low-level output current			50	mA
T_A	Operating free-air temperature	-40		85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −18 mA			-1	-1.2	V
V_{OH}	High level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −10 mA	2.5	3.5		V
			I_{OH} = −40 mA	2			
V_{OL}	Low level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 40 mA				0.5	V
$\lvert V_{OD1}\rvert$	Magnitude of differential output voltage	V_{CC} = 5.25 V, I_O = 0 A			1.25 x V_{OD2}		V
$\lvert V_{OD2}\rvert$	Magnitude of differential output voltage	V_{CC} = 4.75 V to 5.25 V, R_L = 100 Ω, See Figure 5		2			V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage[2]	V_{CC} = 4.75 V to 5.25 V, R_L = 100 Ω, See Figure 5				±0.4	V
V_{OC}	Common-mode output voltage[3]	V_{CC} = 4.75 V to 5.25 V, R_L = 100 Ω, See Figure 5				3	V

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level or vice versa.
(3) In Standard EIA-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage(2)	V_{CC} = 4.75 V to 5.25 V, R_L = 100 Ω, See Figure 5				±0.4	V
I_O	Output current with power off	V_{CC} = 0 V	V_O = 6 V		0.1	100	μA
			V_O = −0.25 V		-0.1	-100	
			V_O = −0.25 V to 6 V			±100	
I_I	Input current	V_{CC} = 5.25 V, V_I = 5.5 V				50	μA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.5 V				-200	μA
I_{OS}	Short-circuit output current(4)	V_{CC} = 5.25 V, V_O = 0 V		-50		-150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = 5.25 V, No load, All inputs at 0 V			45	65	mA

(4) Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

SWITCHING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	C_L = 15 pF, R_L = 100 Ω, See Figure 6		10		ns
$t_{t(OD)}$	Differential output transition time	C_L = 15 pF, R_L = 100 Ω, See Figure 6		10		ns
$t_{sk(o)}$	Output skew	See Figure 6		1		ns

PARAMETER MEASUREMENT INFORMATION

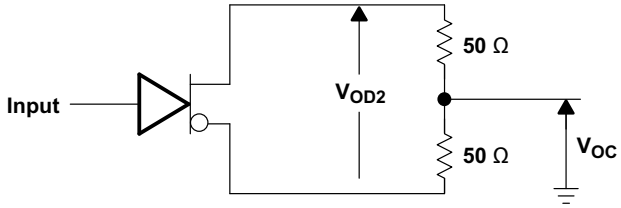
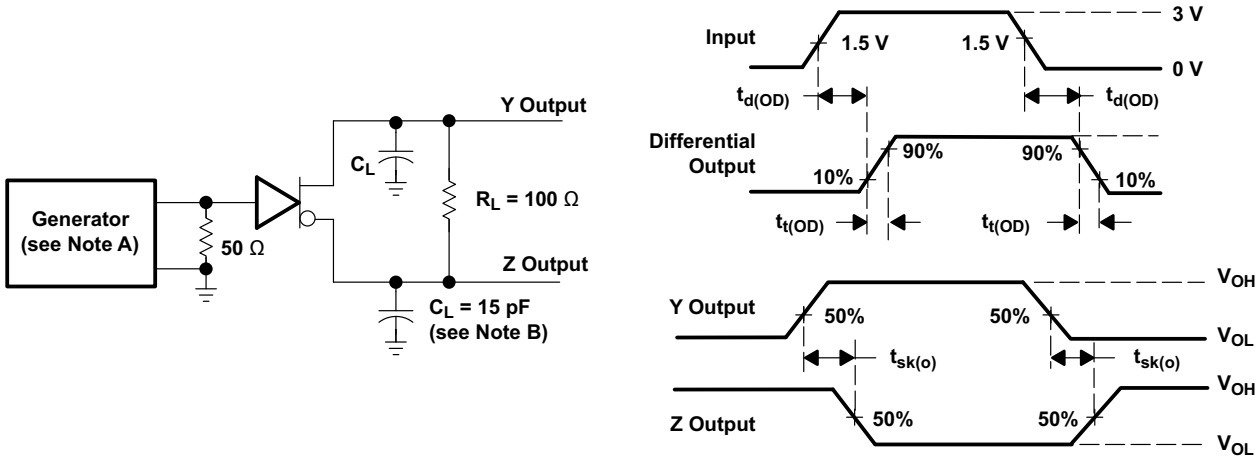


Figure 5. Differential and Common-Mode Output Voltages



TEST CIRCUIT **VOLTAGE WAVEFORMS**

A. The input pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_w = 100 ns, t_r = ≤ 5 ns.

B. C_L includes probe and jig capacitance.

Figure 6. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA9638CIDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	9638I	Samples
V62/12606-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	9638I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

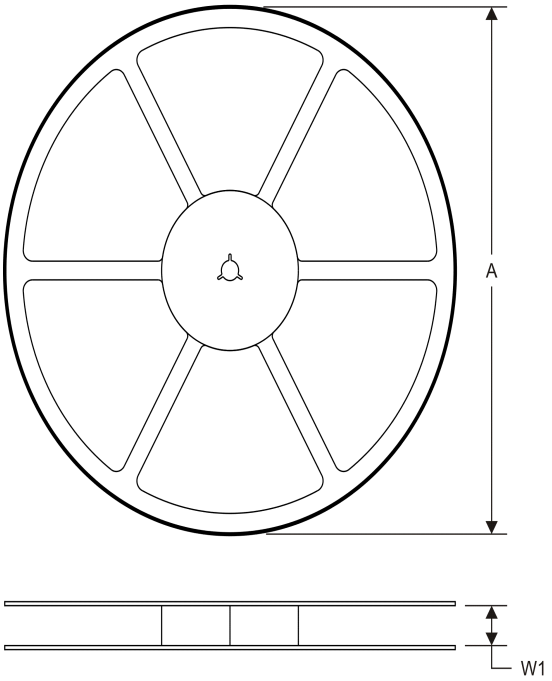
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

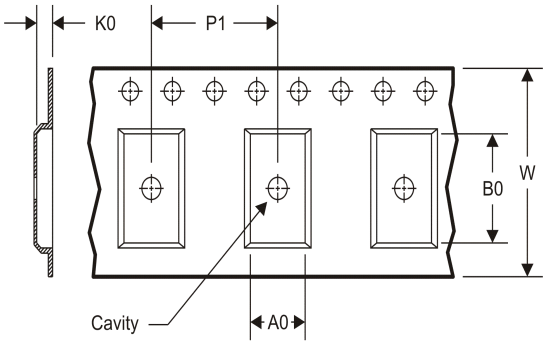
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



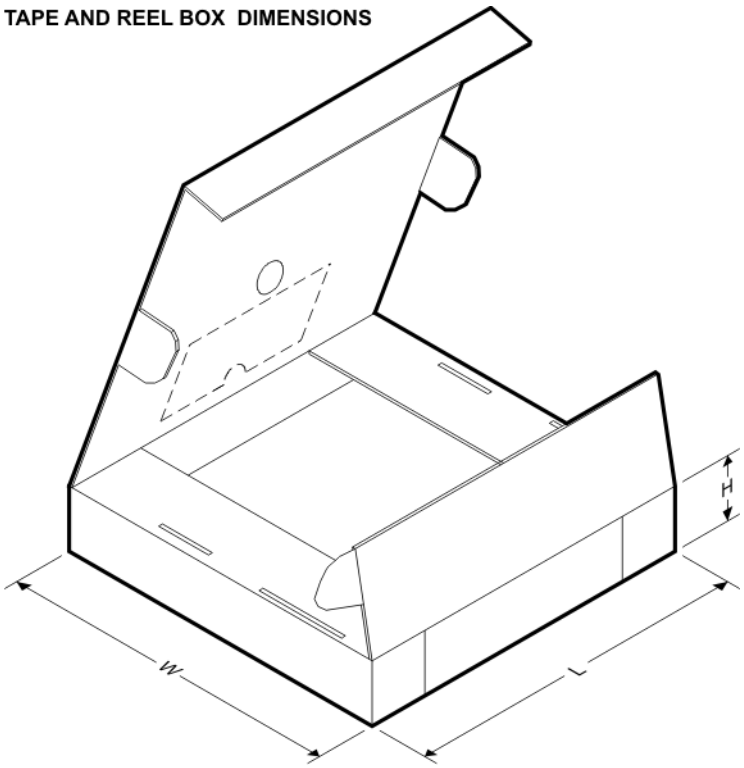
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

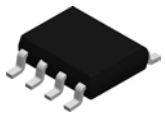
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA9638CIDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA9638CIDREP	SOIC	D	8	2500	340.5	338.1	20.6

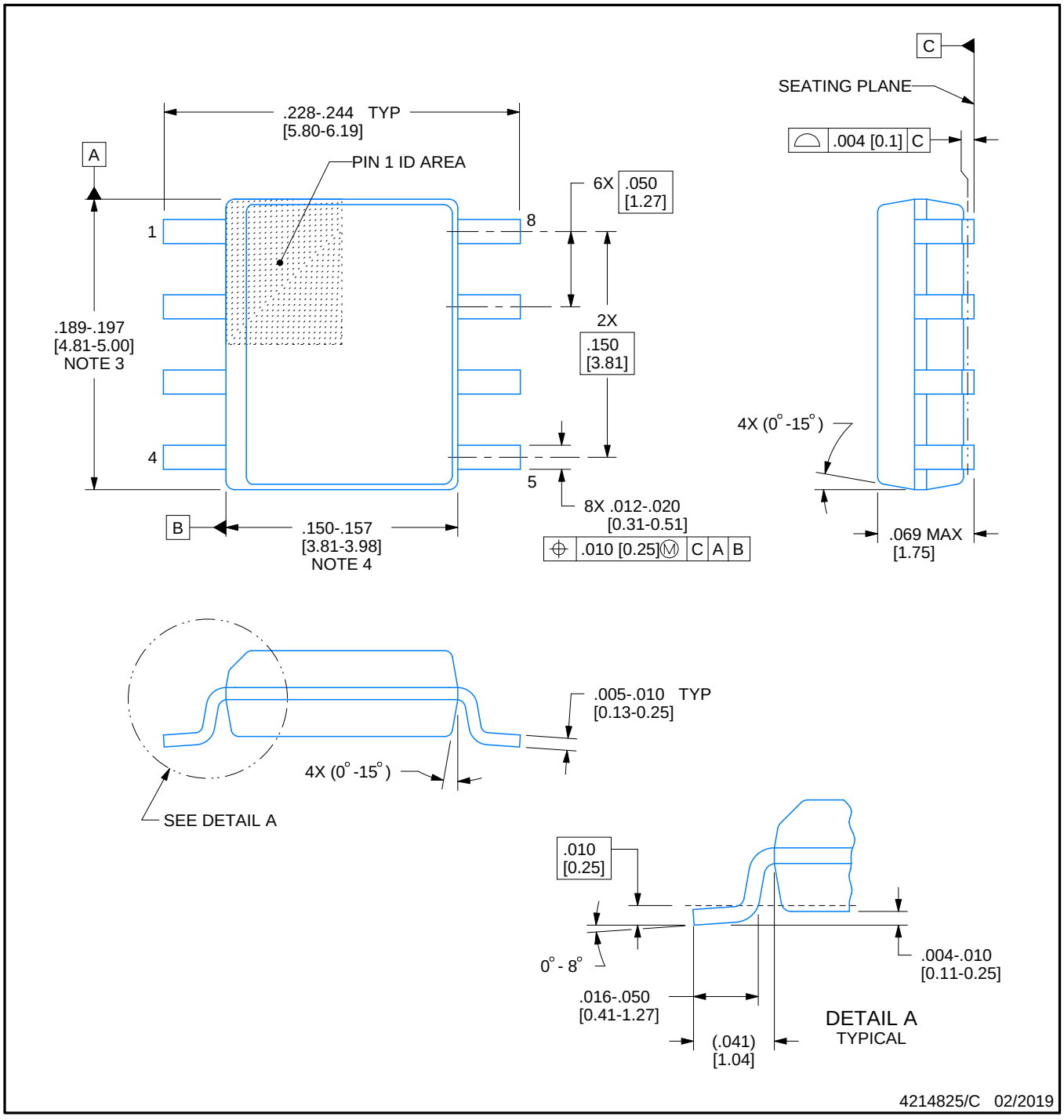


PACKAGE OUTLINE

D0008A

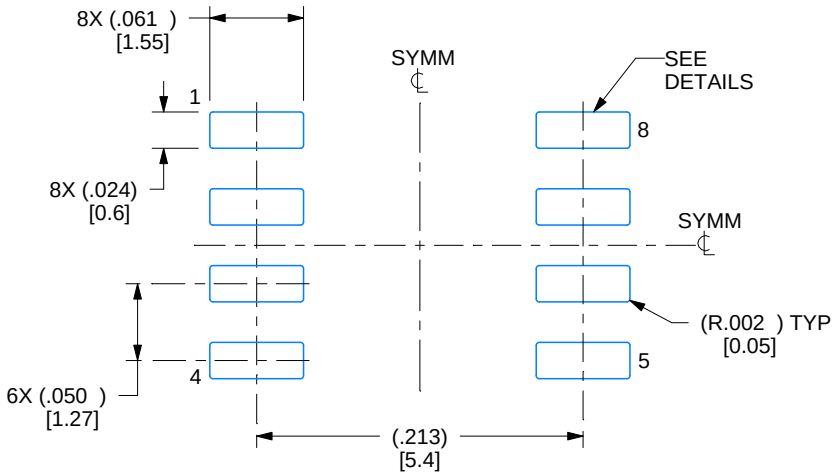
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

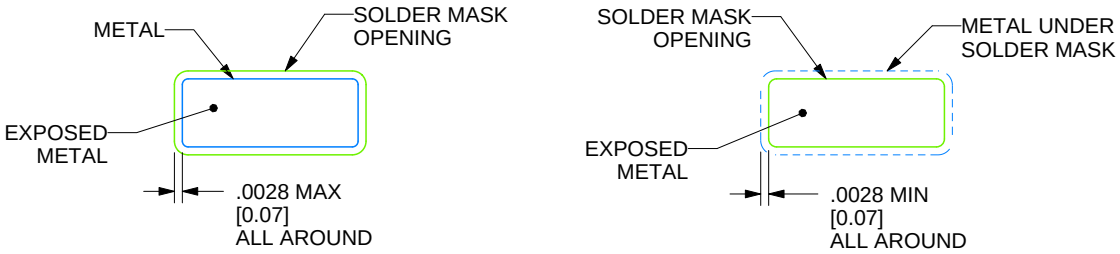


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

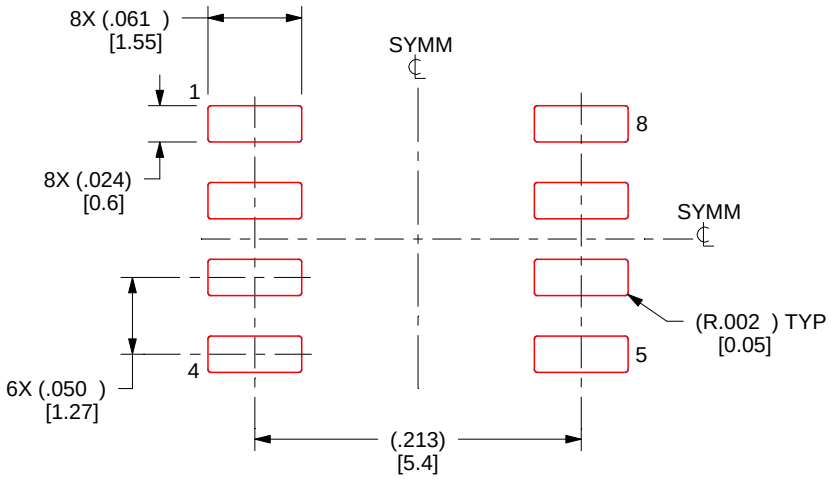
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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