

HCF4070

Quad exclusive OR gate

The HCF4070 is a monolithic integrated circuit fabricated in metal oxide semiconductor technology available in an SO14 package. The HCF4070 contains four independent

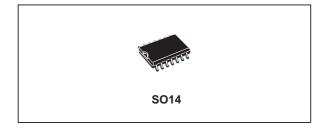
exclusive OR gates. This device provides the system designer with a means for direct implementation of the exclusive OR gate for

applications such as logical comparators, adders/subtractors, parity generators and

Description

checkers.

Datasheet - production data



Features

- Medium-speed operation
 t_{PHL} = t_{PLH} = 70 ns (typ) at C_L = 50 pF and
 V_{DD} = 10 V
- Quiescent current specified up to 20 V
- 5 V, 10 V and 15 V parametric ratings
- Input leakage current
 I₁ = 100 nA (max) at V_{DD} = 18 V, T_A = 25 °C
- 100% tested for quiescent current
- ESD performance
 - HBM: 2 kV
 - MM: 200 V
 - CDM: 1 kV

Applications

- Automotive
- Industrial
- Computer
- Consumer

Table 1. Device summary

Order code	Temperature range	Package	Packing	Marking
HCF4070M013TR	–55 °C to +125 °C	SO14	Tape and reel	HCF4070
HCF4070YM013TR ⁽¹⁾	–40 °C to +125 °C	SO14 (automotive grade)	Tape and reer	HCF4070Y

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

January 2014

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This is information on a product in full production.

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1 Device overview

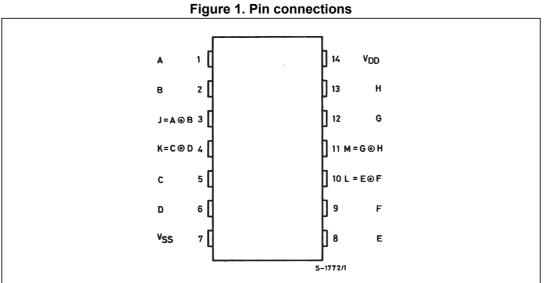
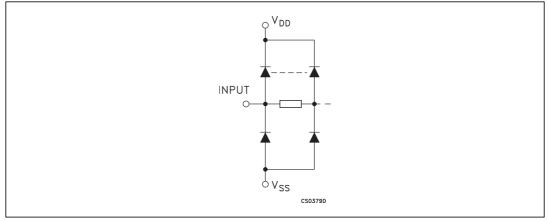


	Table 2. Pin description								
Pin number	Symbol/name	Function							
1, 5, 8, 12	A, C, E, G	Data inputs							
2, 6, 9, 13	B, D, F, H	Data inputs							
3, 4, 10, 11	J, K, L, M	Data outputs							
7	V _{SS}	Negative supply voltage							
14	V _{DD}	Positive supply voltage							

Figure 2. Input equivalent circuit





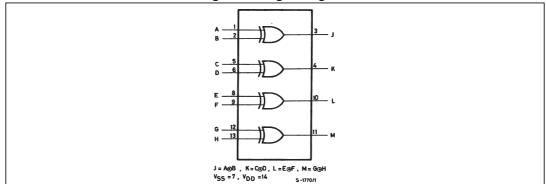


Table 3. Truth table

Inp	Output	
A, C, E, G	B, D, F, H	J, K, L, M
L	L	L
L	Н	н
Н	L	н
Н	Н	L

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DD}	Supply voltage	-0.5 to +22	V
VI	DC input voltage	-0.5 to V _{DD} + 0.5	V
l _l	DC input current	± 10	mA
Р	Power dissipation per package	200	mW
PD	Power dissipation per output transistor	100	mW
T _{op}	Operating temperature	-55 to +125	°C
T _{stg}	Storage temperature	-65 to +150	°C

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are relative to the V_{SS} pin voltage.

Symbol	Par	ameter	Value	Unit
V _{DD}	Supply voltage		3 to 20	V
VI	Input voltage		0 to V _{DD}	V
т		SO14	-55 to 125	°C
Гор	Operating temperature	SO14 (automotive grade)	-40 to 125	°C



			Test con	dition		Value							
Sym.	Parameter	v	vo	llol	VDD	т	م = 25°	С	-40 to	85°C	-55 to	125°C	Unit
		(V)	(V)	(μ A)	(μ Α) (V)	Min.	Тур.	Max.	Min.	Max.	Min.	Max.	
		0/5			5		0.02	1		30		30	
	Quieseent eurrent	0/10			10		0.02	2		60		60	
۱L	Quiescent current	0/15			15		0.02	4		120		120	μA
		0/20			20		0.04	20		600		600	
		0/5		<1	5	4.95			4.95		4.95		
V _{OH}	High-level output voltage	0/10		<1	10	9.95			9.95		9.95		V
		0/15		<1	15	14.95			14.95		14.95		
		5/0		<1	5		0.05			0.05		0.05	
V _{OL}	Low-level output voltage	10/0		<1	10		0.05			0.05		0.05	V
		15/0		<1	15		0.05			0.05		0.05	1
			0.5/4.5	<1	5	3.5			3.5		3.5		
$V_{\rm IH}$	High-level input voltage		1/9	<1	10	7			7		7		V
			1.5/13.5	<1	15	11			11		11		
			4.5/0.5	<1	5			1.5		1.5		1.5	
V_{IL}	Low-level input voltage		9/1	<1	10			3		3		3	V
	5		13.5/1.5	<1	15			4		4		4	
		0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		
I _{ОН}	Output drive current	0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		mA
ЮН		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
		0/5	0.4	<1	5	0.44	1		0.36		0.36		
I _{OL}	Output sink current	0/10	0.5	<1	10	1.1	2.6		0.9		0.9		mA
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
Ц	Input leakage current	0/18	Any In	put	18		±10 ⁻⁵	±0.1		±1		±1	μA
Cl	Input capacitance		Any In	put			5	7.5					pF

 Table 6. DC specifications

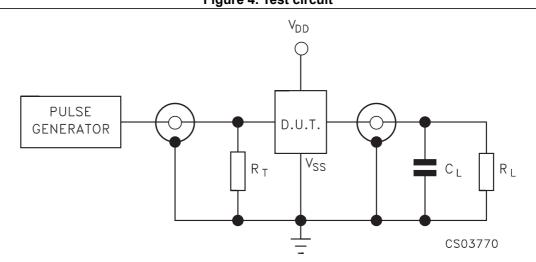
The noise margin for both the "1" and "0" level is: 1 V min. with V_{DD} = 5 V, 2 V min. with V_{DD} = 10 V, 2.5 V min. with V_{DD} = 15 V.



Symbol	Parameter	Test condition	est condition		Value ⁽¹⁾		
	Falameter	V _{DD} (V)	Min.	Тур.	Max.	Unit	
		5		140	280		
t _{PLH} t _{PHL}	Propagation delay time	10		70	130	ns	
		15		50	100		
		5		100	200		
t _{TLH} t _{THL}	Output transition time	10		50	100	ns	
		15		40	80		

Table 7. Dynamic electrical characteristics (T_{amb} = 25 °C, C₁ = 50 pF, R₁ = 200 k Ω_c t_r = t_f = 20 ns)

1. Typical temperature coefficient for all V_{DD} values is 0.3%/°C.





1. C_L = 50 pF or equivalent (includes jig and probe capacitance)

2. $R_L = 200 \text{ k}\Omega$

3. $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)



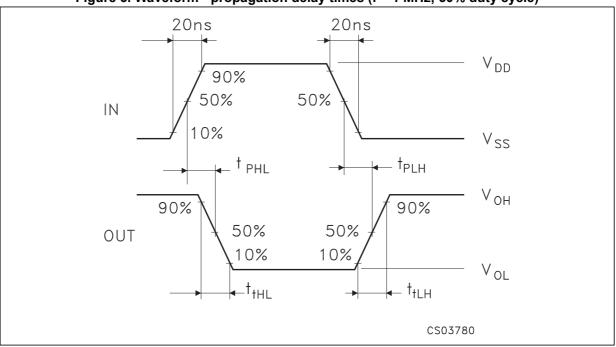


Figure 5. Waveform - propagation delay times (f = 1 MHz; 50% duty cycle)



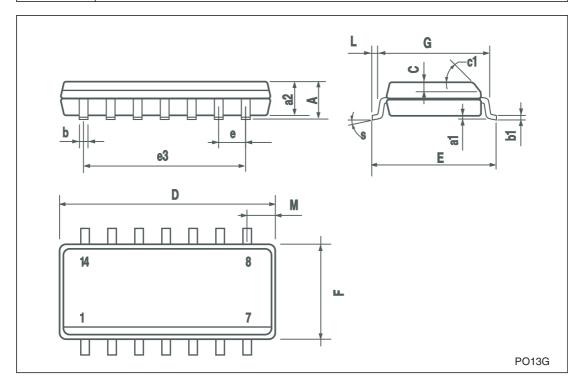
2 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK[®] is an ST trademark.



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	SO-14 MECHANICAL DATA							
DIM.	mm.				inch			
	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX.		
А			1.75			0.068		
a1	0.1		0.2	0.003		0.007		
a2			1.65			0.064		
b	0.35		0.46	0.013		0.018		
b1	0.19		0.25	0.007		0.010		
С		0.5			0.019			
c1			45°	(typ.)				
D	8.55		8.75	0.336		0.344		
E	5.8		6.2	0.228		0.244		
е		1.27			0.050			
e3		7.62			0.300			
F	3.8		4.0	0.149		0.157		
G	4.6		5.3	0.181		0.208		
L	0.5		1.27	0.019		0.050		
М			0.68			0.026		
S			8° (r	max.)	1			



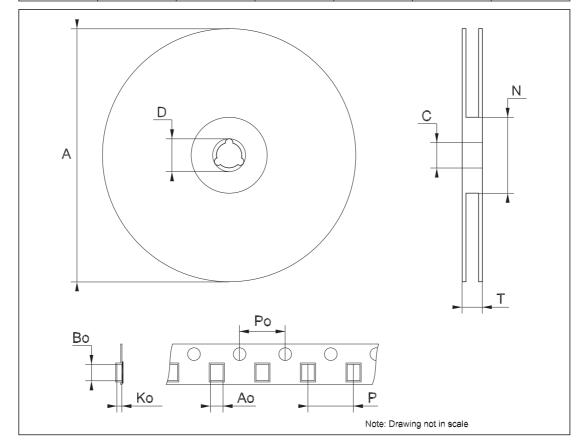
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Tape & Reel SO-14 MECHANICAL DATA								
DIM.		mm.			inch			
DIWI.	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX.		
А			330			12.992		
С	12.8		13.2	0.504		0.519		
D	20.2			0.795				
Ν	60			2.362				
Т			22.4			0.882		
Ao	6.4		6.6	0.252		0.260		
Во	9		9.2	0.354		0.362		
Ко	2.1		2.3	0.082		0.090		
Po	3.9		4.1	0.153		0.161		
Р	7.9		8.1	0.311		0.319		



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3 Revision history

Date	Revision	Changes
11-Jun-2012	3	Added Applications on page 1 Updated Table 1: Device summary Revised document presentation, minor textual updates
15-Jun-2012	4	Updated temperature range in <i>Table 1</i> Updated T _{op} in <i>Table 4</i> and 5
06-Jan-2014	5	Removed DIP package option Added ESD performance to <i>Features</i> Added packing and marking to <i>Table 1: Device summary</i> Updated footnote <i>1</i> of <i>Table 1: Device summary</i>

Table 8. Document revision history



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