Rail-to-Rail Output 215MHz, 1.1nV/√Hz Op Amp/SAR ADC Driver

FEATURES

- **Low Noise: 1.1nV/√Hz**
- **Low Supply Current: 3.5mA/Amp Max**
- **Low Offset Voltage: 350μV Max**
- Fast Settling Time: 570ns to 18-Bit, $2V_{P-P}$ Output
- Low Distortion: THD = –116.8dB at 2kHz
- Wide Supply Range: 3V to 12.6V
- Output Swings Rail-to-Rail
- 215MHz Gain-Bandwidth Product
- Specified Temperature Range: –40°C to 125°C
- LT6236 Shutdown to 10μA Max
- LT6236 in Low Profile (1mm) ThinSOT™ Package
- Dual LT6237 in 3mm × 3mm 8-Lead DFN and 8-Lead MSOP Packages
- LT6238 in 16-Lead SSOP Package

APPLICATIONS

- 16-Bit and 18-Bit SAR ADC Drivers
- Active Filters
- Low Noise, Low Power Signal Processing

DESCRIPTION

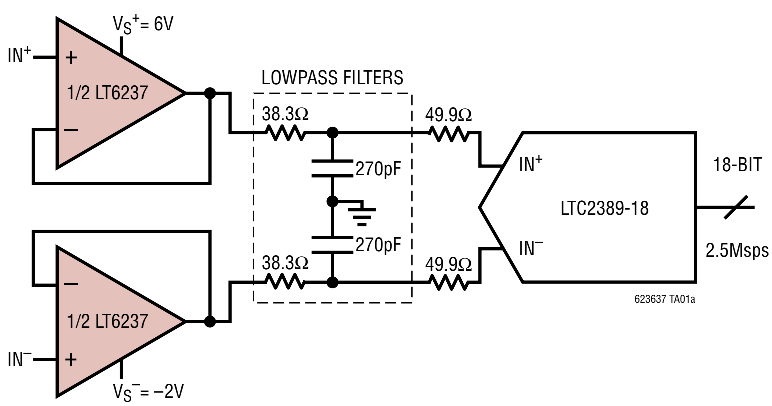
The LT®6236/LT6237/LT6238 are single/dual/quad low noise, rail-to-rail output op amps that feature 1.1nV/√Hz input referred noise voltage density and draw only 3.5mA of supply current per amplifier. These amplifiers combine very low noise and supply current with a 215MHz gain bandwidth product and a 70V/μs slew rate. Low noise, fast settling time and low offset voltage make this amplifier optimal to drive low noise, high speed SAR ADCs. The LT6236 includes a shutdown feature that can be used to reduce the supply current to less than 10μA.

This amplifier family has an output that swings within 50mV of either supply rail to maximize the signal dynamic range in low supply applications and is specified on 3.3V, 5V and ±5V supplies.

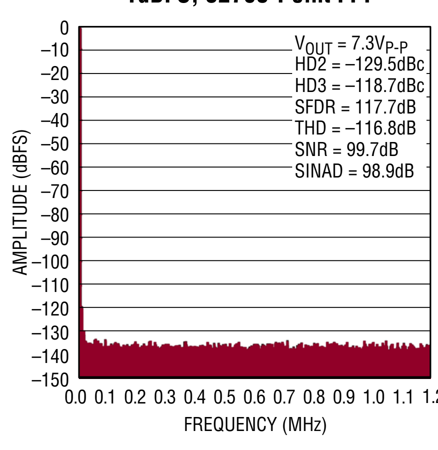
The LT6236/LT6237/LT6238 are upgrades to the LT6230/LT6231/LT6232, offering similar performance with reduced wideband noise beyond 100kHz.

TYPICAL APPLICATION

Differentially Driving a SAR ADC



LT6237 Driving LTC2389-18 f_{IN} = 2kHz, –1dBFS, 32768-Point FFT

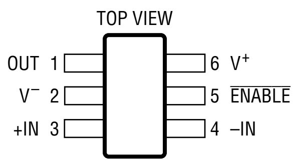


ABSOLUTE MAXIMUM RATINGS

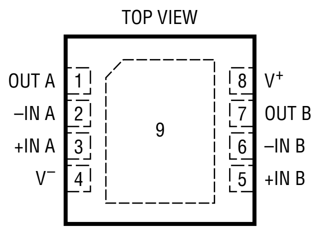
(Note 1)

Total Supply Voltage (V^+ to V^-) 12.6V
Input Current (Note 2) .... ±40mA
Output Short-Circuit Duration (Note 3) .... Indefinite
Operating Temperature Range (Note 4).. –40°C to 125°C
Specified Temperature Range (Note 5).....–40°C to125°C
Maximum Junction Temperature .... 150°C
Storage Temperature Range .... –65°C to 150°C

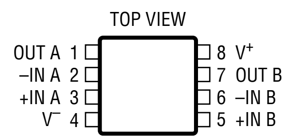
PIN CONFIGURATION



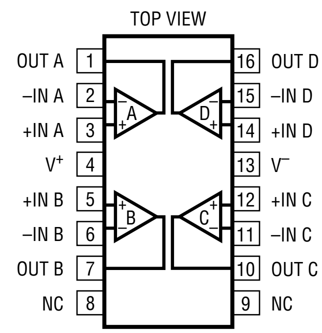
S6 PACKAGE
6-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 192°C/W



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
UNDERSIDE METAL CONNECTED TO V^-
(PCB CONNECTION OPTIONAL)



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 273°C/W



GN PACKAGE
16-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6236CS6#TRMPBF	LT6236CS6#TRPBF	LTGHM	6-Lead Plastic TSOT-23	0°C to 70°C
LT6236IS6#TRMPBF	LT6236IS6#TRPBF	LTGHM	6-Lead Plastic TSOT-23	–40°C to 85°C
LT6236HS6#TRMPBF	LT6236HS6#TRPBF	LTGHM	6-Lead Plastic TSOT-23	–40°C to 125°C
LT6237CDD#PBF	LT6237CDD#TRPBF	LGHN	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT6237IDD#PBF	LT6237IDD#TRPBF	LGHN	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT6237HDD#PBF	LT6237HDD#TRPBF	LGHN	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT6237CMS8#PBF	LT6237CMS8#TRPBF	LTGHP	8-Lead Plastic MSOP	0°C to 70°C
LT6237IMS8#PBF	LT6237IMS8#TRPBF	LTGHP	8-Lead Plastic MSOP	–40°C to 85°C
LT6237HMS8#PBF	LT6237HMS8#TRPBF	LTGHP	8-Lead Plastic MSOP	–40°C to 125°C
LT6238CGN#PBF	LT6238CGN#TRPBF	6238	16-Lead Narrow Plastic SSOP	0°C to 70°C
LT6238IGN#PBF	LT6238IGN#TRPBF	6238	16-Lead Narrow Plastic SSOP	–40°C to 85°C
LT6238HGN#PBF	LT6238HGN#TRPBF	6238	16-Lead Narrow Plastic SSOP	–40°C to 125°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 5V, 0V; V_S = 3.3V, 0V; V_{CM} = V_{OUT} = half supply, $\overline{ENABLE}$ = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	LT6236 LT6237MS8, LT6238GN LT6237DD8		100 50 75	500 350 450	µV µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)			100	600	µV
I_B	Input Bias Current			5	10	µA
	I_B Match (Channel-to-Channel) (Note 6)			0.1	0.9	µA
I_{OS}	Input Offset Current			0.1	0.6	µA
	Input Noise Voltage	0.1Hz to 10Hz		180		nV_{P-P}
e_n	Input Noise Voltage Density	f = 10kHz, V_S = 5V		1.1	1.7	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density, Balanced Source Input Noise Current Density, Unbalanced Source	f = 10kHz, V_S = 5V, R_S = 10k f = 10kHz, V_S = 5V, R_S = 10k		1 2.4		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
R_{IN}	Input Resistance	Common Mode Differential Mode		6.5 7.5		MΩ kΩ
C_{IN}	Input Capacitance	Common Mode Differential Mode		2.9 7.7		pF pF
A_{VOL}	Large-Signal Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 10k to V_S/2 V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to V_S/2 V_S = 5V, V_O = 1V to 4V, R_L = 100Ω to V_S/2	105 21 5.4	200 40 9		V/mV V/mV V/mV
		V_S = 3.3V, V_O = 0.65V to 2.65V, R_L = 10k to V_S/2 V_S = 3.3V, V_O = 0.65V to 2.65V, R_L = 1k to V_S/2	90 16.5	175 32		V/mV V/mV
V_{CM}	Input Voltage Range	Guaranteed by CMRR, V_S = 5V, 0V Guaranteed by CMRR, V_S = 3.3V, 0V	1.5 1.15		4 2.65	V V
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 1.5V to 4V V_S = 3.3V, V_{CM} = 1.15V to 2.65V	90 90	115 115		dB dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 10V	90	115		dB
	Minimum Supply Voltage (Note 7)		3			V
V_{OL}	Output Voltage Swing Low (Note 8)	No Load I_{SINK} = 5mA V_S = 5V, I_{SINK} = 20mA V_S = 3.3V, I_{SINK} = 15mA		4 85 240 185	40 190 460 350	mV mV mV mV
V_{OH}	Output Voltage Swing High (Note 8)	No Load I_{SOURCE} = 5mA V_S = 5V, I_{SOURCE} = 20mA V_S = 3.3V, I_{SOURCE} = 15mA		5 90 325 250	50 200 600 400	mV mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3.3V	±30 ±25	±45 ±40		mA mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	 $\overline{ENABLE}$ = V^+ – 0.35V		3.15 0.2	3.5 10	mA µA
$I_{\overline{ENABLE}}$	$\overline{ENABLE}$ Pin Current	$\overline{ENABLE}$ = 0.3V		–25	–75	µA

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 5V, 0V; V_S = 3.3V, 0V; V_{CM} = V_{OUT} = half supply, $\overline{ENABLE}$ = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_L	$\overline{ENABLE}$ Pin Input Voltage Low				0.3	V
V_H	$\overline{ENABLE}$ Pin Input Voltage High		V^+ – 0.35V			V
	Output Leakage Current	$\overline{ENABLE}$ = V^+ – 0.35V, V_O = 1.5V to 3.5V		0.2	10	µA
t_{ON}	Turn-On Time	$\overline{ENABLE}$ = 5V to 0V, R_L = 1k, V_S = 5V		800		ns
t_{OFF}	Turn-Off Time	$\overline{ENABLE}$ = 0V to 5V, R_L = 1k, V_S = 5V		41		µs
GBW	Gain-Bandwidth Product	Frequency = 1MHz, V_S = 5V		200		MHz
$f_{–3db}$	–3dB Bandwidth	V_S = 5V, R_L = 100Ω		90		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 1.5V to 3.5V	42	60		V/µs
FPBW	Full-Power Bandwidth	V_S = 5V, V_{OUT} = $3V_{P-P}$ (Note 9)	4.4	6.3		MHz
t_S	Settling Time	0.1%, V_S = 5V, V_{STEP} = 2V, A_V = 1 0.01% 0.0015% (16-Bit) 4ppm (18-Bit)		50 60 240 570		ns ns ns ns

The ● denotes the specifications which apply over the 0°C < T_A < 70°C temperature range. V_S = 5V, 0V; V_S = 3.3V, 0V; V_{CM} = V_{OUT} = half supply, $\overline{ENABLE}$ = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	LT6236 LT6237MS8, LT6238GN LT6237DD8	● ● ●			600 450 550	µV µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●			800	µV
V_{OS} TC	Input Offset Voltage Drift (Note 10)	LT6236 LT6237MS8 LT6237DD8 LT6238GN	● ● ● ●		0.5 0.3 0.4 0.5	2.0 1.4 2.2 2.2	µV/°C µV/°C µV/°C µV/°C
I_B	Input Bias Current		●			11	µA
	I_B Match (Channel-to-Channel) (Note 6)		●			1	µA
I_{OS}	Input Offset Current		●			0.7	µA
A_{VOL}	Large-Signal Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 10k to $V_S/2$ V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to $V_S/2$ V_S = 5V, V_O = 1V to 4V, R_L = 100Ω to $V_S/2$	● ● ●	78 17 4.1			V/mV V/mV V/mV
		V_S = 3.3V, V_O = 0.65V to 2.65V, R_L = 10k to $V_S/2$ V_S = 3.3V, V_O = 0.65V to 2.65V, R_L = 1k to $V_S/2$	● ●	66 13			V/mV V/mV
V_{CM}	Input Voltage Range	Guaranteed by CMRR V_S = 5V, 0V V_S = 3.3V, 0V	 ● ●	 1.5 1.15		 4 2.65	 V V
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 1.5V to 4V V_S = 3.3V, V_{CM} = 1.15V to 2.65V	● ●	90 85			dB dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 10V	●	85			dB
	Minimum Supply Voltage (Note 7)		●	3			V
V_{OL}	Output Voltage Swing Low (Note 8)	No Load I_{SINK} = 5mA V_S = 5V, I_{SINK} = 20mA V_S = 3.3V, I_{SINK} = 15mA	● ● ● ●			50 200 500 380	mV mV mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the 0°C < T_A < 70°C temperature range. V_S = 5V, 0V; V_S = 3.3V, 0V; V_{CM} = V_{OUT} = half supply, $\overline{ENABLE}$ = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	Output Voltage Swing High (Note 8)	No Load I_{SOURCE} = 5mA V_S = 5V, I_{SOURCE} = 20mA V_S = 3.3V, I_{SOURCE} = 15mA	● ● ● ●			60 215 650 430	mV mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3.3V	● ●	±25 ±20			mA mA
I_S	Supply Current per Amplifier		●			4.2	mA
	Disabled Supply Current per Amplifier	$\overline{ENABLE}$ = V^+ – 0.25V	●		1		µA
$I_{\overline{ENABLE}}$	$\overline{ENABLE}$ Pin Current	$\overline{ENABLE}$ = 0.3V	●			–85	µA
V_L	$\overline{ENABLE}$ Pin Input Voltage Low		●			0.3	V
V_H	$\overline{ENABLE}$ Pin Input Voltage High		●	V^+ – 0.25V			V
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 1.5V to 3.5V	●	35			V/µs
FPBW	Full-Power Bandwidth (Note 9)	V_S = 5V, V_{OUT} = $3V_{P-P}$	●	3.7			MHz

The ● denotes the specifications which apply over the –40°C < T_A < 85°C temperature range. V_S = 5V, 0V; V_S = 3.3V, 0V; V_{CM} = V_{OUT} = half supply, $\overline{ENABLE}$ = 0V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6236 LT6237MS8, LT6238GN LT6237DD8	● ● ●			700 550 650	µV µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●			1000	µV
V_{OS} TC	Input Offset Voltage Drift (Note 10)	LT6236 LT6237MS8 LT6237DD8 LT6238GN	● ● ● ●		0.5 0.3 0.4 0.5	2.0 1.4 2.2 2.2	µV/°C µV/°C µV/°C µV/°C
I_B	Input Bias Current		●			12	µA
	I_B Match (Channel-to-Channel) (Note 6)		●			1.1	µA
I_{OS}	Input Offset Current		●			0.8	µA
A_{VOL}	Large-Signal Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 10k to $V_S/2$ V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to $V_S/2$ V_S = 5V, V_O = 1V to 4V, R_L = 100Ω to $V_S/2$	● ● ●	72 16 3.6			V/mV V/mV V/mV
		V_S = 3.3V, V_O = 0.65V to 2.65V, R_L = 10k to $V_S/2$ V_S = 3.3V, V_O = 0.65V to 2.65V, R_L = 1k to $V_S/2$	● ●	60 12			V/mV V/mV
V_{CM}	Input Voltage Range	Guaranteed by CMRR V_S = 5V, 0V V_S = 3.3V, 0V	 ● ●	 1.5 1.15		 4 2.65	 V V
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 1.5V to 4V V_S = 3.3V, V_{CM} = 1.15V to 2.65V	● ●	90 85			dB dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 10V	●	85			dB
	Minimum Supply Voltage (Note 7)		●	3			V
V_{OL}	Output Voltage Swing Low (Note 8)	No Load I_{SINK} = 5mA V_S = 5V, I_{SINK} = 15mA V_S = 3.3V, I_{SINK} = 15mA	● ● ● ●			60 210 510 390	mV mV mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C < T_A < 85°C temperature range. V_S = 5V, 0V; V_S = 3.3V, 0V; V_{CM} = V_{OUT} = half supply, $\overline{ENABLE}$ = 0V, unless otherwise noted. (Note 5)

V_{OH}	Output Voltage Swing High (Note 6)	No Load I_{SOURCE} = 5mA V_S = 5V, I_{SOURCE} = 20mA V_S = 3.3V, I_{SOURCE} = 15mA	● ● ● ●			70 220 675 440	mV mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3.3V	● ●	±15 ±15			mA mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	 $\overline{ENABLE}$ = V⁺ – 0.2V	● ●		 1	4.4 	mA µA
$I_{\overline{ENABLE}}$	$\overline{ENABLE}$ Pin Current	$\overline{ENABLE}$ = 0.3V	●			–100	µA
V_L	$\overline{ENABLE}$ Pin Input Voltage Low		●			0.3	V
V_H	$\overline{ENABLE}$ Pin Input Voltage High		●	V^+ – 0.2V			V
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 1.5V to 3.5V	●	31			V/µs
FPBW	Full-Power Bandwidth (Note 9)	V_S = 5V, V_{OUT} = $3V_{P-P}$	●	3.3			MHz

The ● denotes the specifications which apply over the –40°C < T_A < 125°C temperature range. V_S = 5V, 0V; V_S = 3.3V, 0V; V_{CM} = V_{OUT} = half supply, $\overline{ENABLE}$ = 0V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6236 LT6237MS8,LT6238GN LT6237DD8	● ● ●			750 650 700	µV µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●			1000	µV
V_{OS} TC	Input Offset Voltage Drift (Note 10)	LT6236 LT6237MS8 LT6237DD8 LT6238GN	● ● ● ●		0.5 0.3 0.4 0.5	2.0 1.4 2.2 2.2	µV/°C µV/°C µV/°C µV/°C
I_B	Input Bias Current		●			12	µA
	I_B Match (Channel-to-Channel) (Note 6)		●			1.1	µA
I_{OS}	Input Offset Current		●			1.2	µA
A_{VOL}	Large-Signal Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 10k to V_S/2 V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to V_S/2 V_S = 5V, V_O = 1V to 4V, R_L = 100Ω to V_S/2	● ● ●	62 14 3			V/mV V/mV V/mV
		V_S = 3.3V, V_O = 0.65V to 2.65V, R_L = 10k to V_S/2 V_S = 3.3V, V_O = 0.65V to 2.65V, R_L = 1k to V_S/2	● ●	52 11			V/mV V/mV
V_{CM}	Input Voltage Range	Guaranteed by CMRR V_S = 5V, 0V V_S = 3.3V, 0V	 ● ●	 1.5 1.15		 4 2.65	 V V
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 1.5V to 4V V_S = 3.3V, V_{CM} = 1.15V to 2.65V	● ●	90 85			dB dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 10V	●	85			dB
	Minimum Supply Voltage (Note 7)		●	3			V
V_{OL}	Output Voltage Swing Low (Note 8)	No Load I_{SINK} = 5mA V_S = 5V, I_{SINK} = 15mA V_S = 3.3V, I_{SINK} = 15mA	● ● ● ●			60 225 550 425	mV mV mV mV
V_{OH}	Output Voltage Swing High (Note 8)	No Load I_{SOURCE} = 5mA V_S = 5V, I_{SOURCE} = 20mA V_S = 3.3V, I_{SOURCE} = 15mA	● ● ● ●			80 240 700 470	mV mV mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C < T_A < 125°C temperature range. V_S = 5V, 0V; V_S = 3.3V, 0V; V_{CM} = V_{OUT} = half supply, $\overline{ENABLE}$ = 0V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3.3V	● ●	±15 ±15			mA mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	 $\overline{ENABLE}$ = V^+ – 0.15V	● ●		 2	5 	mA µA
$I_{\overline{ENABLE}}$	$\overline{ENABLE}$ Pin Current	$\overline{ENABLE}$ = 0.3V	●			–100	µA
V_L	$\overline{ENABLE}$ Pin Input Voltage Low		●			0.3	V
V_H	$\overline{ENABLE}$ Pin Input Voltage High		●	V^+– 0.15V			V
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 1.5V to 3.5V	●	31			V/µs
FPBW	Full-Power Bandwidth (Note 9)	V_S = 5V, V_{OUT} = $3V_{P-P}$	●	3.3			MHz

T_A = 25°C, V_S = ±5V, V_{CM} = V_{OUT} = 0V, $\overline{ENABLE}$ = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6236 LT6237MS8, LT6238GN LT6237DD8		100 50 75	500 350 450	µV µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)			100	600	µV
I_B	Input Bias Current			5	10	µA
	I_B Match (Channel-to-Channel) (Note 6)			0.1	0.9	µA
I_{OS}	Input Offset Current			0.1	0.6	µA
	Input Noise Voltage	0.1Hz to 10Hz		180		nV_{P-P}
e_n	Input Noise Voltage Density	f = 10kHz		1.1	1.7	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density, Balanced Source Input Noise Current Density, Unbalanced source	f = 10kHz, R_S = 10k f = 10kHz, R_S = 10k		1 2.4		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
R_{IN}	Input Resistance	Common Mode Differential Mode		6.5 7.5		MΩ kΩ
C_{IN}	Input Capacitance	Common Mode Differential Mode		2.4 6.5		pF pF
A_{VOL}	Large-Signal Gain	V_O = ±4.5V, R_L = 10k V_O = ±4.5V, R_L = 1k V_O = ±2V, R_L = 100Ω	140 35 8.5	260 65 16		V/mV V/mV V/mV
V_{CM}	Input Voltage Range	Guaranteed by CMRR	–3		4	V
CMRR	Common Mode Rejection Ratio	V_{CM} = –3V to 4V	95	120		dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.5V to ±5V	90	115		dB
V_{OL}	Output Voltage Swing Low (Note 8)	No Load I_{SINK} = 5mA I_{SINK} = 20mA		4 85 240	40 190 460	mV mV mV
V_{OH}	Output Voltage Swing High (Note 8)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA		5 90 325	50 200 600	mV mV mV
I_{SC}	Short-Circuit Current		±30			mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	 $\overline{ENABLE}$ = 4.65V		3.3 0.2	3.9 	mA µA
$I_{\overline{ENABLE}}$	$\overline{ENABLE}$ Pin Current	$\overline{ENABLE}$ = 0.3V		–35	–85	µA
V_L	$\overline{ENABLE}$ Pin Input Voltage Low				0.3	V
V_H	$\overline{ENABLE}$ Pin Input Voltage High		4.65			V

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = ±5V$, $V_{CM} = V_{OUT} = 0V$, $\overline{ENABLE} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Output Leakage Current	$\overline{ENABLE}$ = V+ –0.35V, V_O = ±1V		0.2	10	µA
t_{ON}	Turn-On Time	$\overline{ENABLE}$ = 5V to 0V, R_L = 1k		800		ns
t_{OFF}	Turn-Off Time	$\overline{ENABLE}$ = 0V to 5V, R_L = 1k		62		µs
GBW	Gain-Bandwidth Product	Frequency = 1MHz	150	215		MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = –2V to 2V	50	70		V/µs
FPBW	Full-Power Bandwidth	V_{OUT} = $3V_{P-P}$ (Note 9)	5.3	7.4		MHz
t_S	Settling Time	0.1%, V_{STEP} = 4V, A_V = 1, 0.01% 0.0015% (16-Bit) 4ppm (18-Bit)		60 80 470 1200		ns ns ns ns

The ● denotes the specifications which apply over the 0°C < T_A < 70°C temperature range. $V_S = ±5V$, $V_{CM} = V_{OUT} = 0V$, $\overline{ENABLE} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6236 LT6237MS8, LT6238GN LT6237DD8	● ● ●			600 450 550	µV µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●			800	µV
V_{OS} TC	Input Offset Voltage Drift (Note 10)	LT6236 LT6237MS8 LT6237DD8 LT6238GN	● ● ● ●		0.7 0.5 0.4 0.5	2.2 1.8 2.2 2.2	µV/°C µV/°C µV/°C µV/°C
I_B	Input Bias Current		●			11	µA
	I_B Match (Channel-to-Channel) (Note 6)		●			1	µA
I_{OS}	Input Offset Current		●			0.7	µA
A_{VOL}	Large-Signal Gain	V_O = ±4.5V, R_L = 10k V_O = ±4.5V, R_L = 1k V_O = ±2V, R_L = 100Ω	● ● ●	100 27 6			V/mV V/mV V/mV
V_{CM}	Input Voltage Range	Guaranteed by CMRR	●	–3		4	V
CMRR	Common Mode Rejection Ratio	V_{CM} = –3V to 4V	●	95			dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.5V to ±5V	●	85			dB
V_{OL}	Output Voltage Swing Low (Note 8)	No Load I_{SINK} = 5mA I_{SINK} = 20mA	● ● ●			50 200 500	mV mV mV
V_{OH}	Output Voltage Swing High (Note 8)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA	● ● ●			60 215 650	mV mV mV
I_{SC}	Short-Circuit Current		●	±25			mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	 $\overline{ENABLE}$ = 4.75V	● ●		 1	4.6 	mA µA
$I_{\overline{ENABLE}}$	$\overline{ENABLE}$ Pin Current	$\overline{ENABLE}$ = 0.3V	●			–95	µA
V_L	$\overline{ENABLE}$ Pin Input Voltage Low		●			0.3	V
V_H	$\overline{ENABLE}$ Pin Input Voltage High		●	4.75			V
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = –2V to 2V	●	44			V/µs
FPBW	Full-Power Bandwidth	V_{OUT} = $3V_{P-P}$ (Note 9)	●	4.66			MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C < T_A < 85°C temperature range. V_S = ±5V, V_{CM} = V_{OUT} = 0V, $\overline{ENABLE}$ = 0V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6236 LT6237MS8, LT6238GN LT6237DD8	● ● ●			700 550 650	µV µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●			1000	µV
V_{OS} TC	Input Offset Voltage Drift (Note 10)	LT6236 LT6237MS8 LT6237DD8 LT6238GN	● ● ● ●		0.7 0.5 0.4 0.5	2.2 1.8 2.2 2.2	µV/°C µV/°C µV/°C µV/°C
I_B	Input Bias Current		●			12	µA
	I_B Match (Channel-to-Channel) (Note 6)		●			1.1	µA
I_{OS}	Input Offset Current		●			0.8	µA
A_{VOL}	Large-Signal Gain	V_O = ±4.5V, R_L = 10k V_O = ±4.5V, R_L = 1k V_O = ±1.5V, R_L = 100Ω	● ● ●	93 25 4.8			V/mV V/mV V/mV
V_{CM}	Input Voltage Range	Guaranteed by CMRR	●	–3		4	V
CMRR	Common Mode Rejection Ratio	V_{CM} = –3V to 4V	●	95			dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.5V to ±5V	●	85			dB
V_{OL}	Output Voltage Swing Low (Note 8)	No Load I_{SINK} = 5mA I_{SINK} = 15mA	● ● ●			60 210 510	mV mV mV
V_{OH}	Output Voltage Swing High (Note 8)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA	● ● ●			70 220 675	mV mV mV
I_{SC}	Short-Circuit Current		●	±15			mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	 $\overline{ENABLE}$ = 4.8V	● ●		 1	4.85	mA µA
$I_{\overline{ENABLE}}$	$\overline{ENABLE}$ Pin Current	$\overline{ENABLE}$ = 0.3V	●			–110	µA
V_L	$\overline{ENABLE}$ Pin Input Voltage Low		●			0.3	V
V_H	$\overline{ENABLE}$ Pin Input Voltage High		●	4.8			V
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = –2V to 2V	●	37			V/µs
FPBW	Full-Power Bandwidth	V_{OUT} = $3V_{P-P}$ (Note 9)	●	3.9			MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C < T_A < 125°C temperature range. V_S = ±5V, V_{CM} = V_{OUT} = 0V, $\overline{ENABLE}$ = 0V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6236 LT6237MS8, LT6238GN LT6237DD8	● ● ●			750 650 700	μV μV μV
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●			1000	μV
$V_{OS}TC$	Input Offset Voltage Drift (Note 10)	LT6236 LT6237MS8 LT6237DD8 LT6238GN	● ● ● ●		0.7 0.5 0.4 0.5	2.2 1.8 2.2 2.2	μV/°C μV/°C μV/°C μV/°C
I_B	Input Bias Current		●			12	μA
	I_B Match (Channel-to-Channel) (Note 6)		●			1.1	μA
I_{OS}	Input Offset Current		●			1.2	μA
A_{VOL}	Large-Signal Gain	V_O = ±4.5V, R_L = 10k V_O = ±4.5V, R_L = 1k V_O = ±1.5V, R_L = 100Ω	● ● ●	76 21 4.1			V/mV V/mV V/mV
V_{CM}	Input Voltage Range	Guaranteed by CMRR	●	–3		4	V
CMRR	Common Mode Rejection Ratio	V_{CM} = –3V to 4V	●	95			dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.5V to ±5V	●	85			dB
V_{OL}	Output Voltage Swing Low (Note 8)	No Load I_{SINK} = 5mA I_{SINK} = 15mA	● ● ●			70 230 550	mV mV mV
V_{OH}	Output Voltage Swing High (Note 8)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA	● ● ●			78 240 710	mV mV mV
I_{SC}	Short-Circuit Current		●	±15			mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	 $\overline{ENABLE}$ = 4.85V	● ●		 10	5.5 	mA μA
$I_{\overline{ENABLE}}$	$\overline{ENABLE}$ Pin Current	$\overline{ENABLE}$ = 0.3V	●			–110	μA
V_L	$\overline{ENABLE}$ Pin Input Voltage Low		●			0.3	V
V_H	$\overline{ENABLE}$ Pin Input Voltage High		●	4.85			V
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = –2V to 2V	●	37			V/μs
FPBW	Full-Power Bandwidth	V_{OUT} = $3V_{P-P}$ (Note 9)	●	3.9			MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Inputs are protected by back-to-back diodes. If the differential input voltage exceeds 0.7V, the input current must be limited to less than 40mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LT6236C/LT6236I/LT6236H, the LT6237C/LT6237I/LT6237H and the LT6238C/LT6238I/LT6238H are guaranteed functional over the temperature range of –40°C to 125°C.

Note 5: The LT6236C/LT6237C/LT6238C are guaranteed to meet specified performance from 0°C to 70°C. The LT6236I/LT6237I/LT6238I are guaranteed to meet specified performance from –40°C to 85°C. The LT6236H/LT6237H/LT6238H are guaranteed to meet specified performance from –40°C to 125°C. The LT6236C/LT6237C/LT6238C are designed, characterized and expected to meet specified performance from –40°C to 85°C, but are not tested or QA sampled at these temperatures.

Note 6: Matching parameters are the difference between the two amplifiers A and D and between B and C of the LT6238 and between the two amplifiers of the LT6237.

Note 7: Minimum supply voltage is guaranteed by power supply rejection ratio test.

Note 8: Output voltage swings are measured between the output and power supply rails.

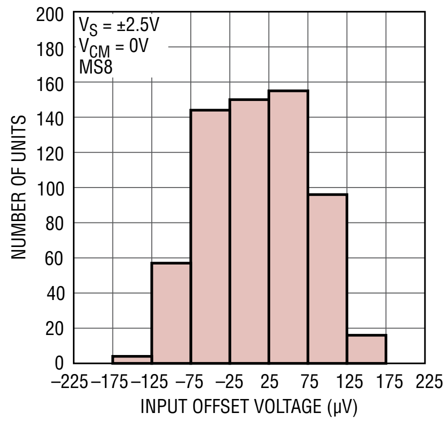
Note 9: Full-power bandwidth is calculated from the slew rate:

$$FPBW = SR/2\pi V_P$$

Note 10: This parameter is not 100% tested.

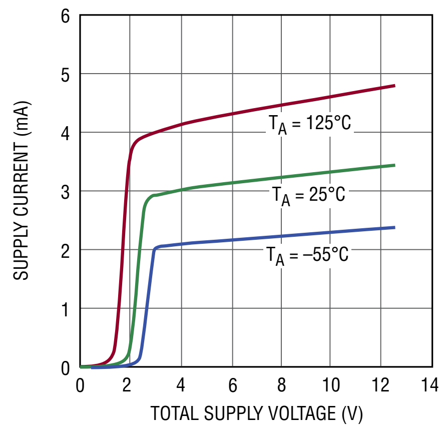
TYPICAL PERFORMANCE CHARACTERISTICS

V_{OS} Distribution



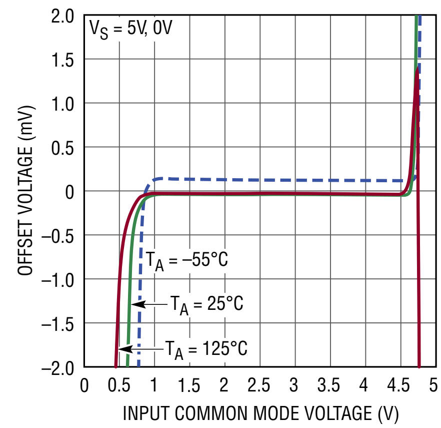
62367 G01

Supply Current vs Supply Voltage (Per Amplifier)



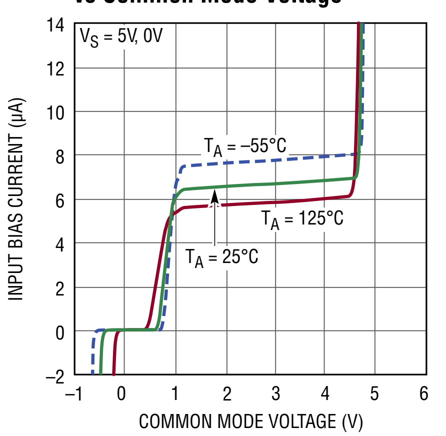
62367 G02

Offset Voltage vs Input Common Mode Voltage



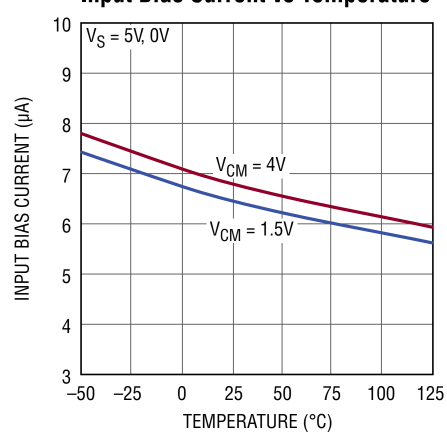
62367 G03

Input Bias Current vs Common Mode Voltage



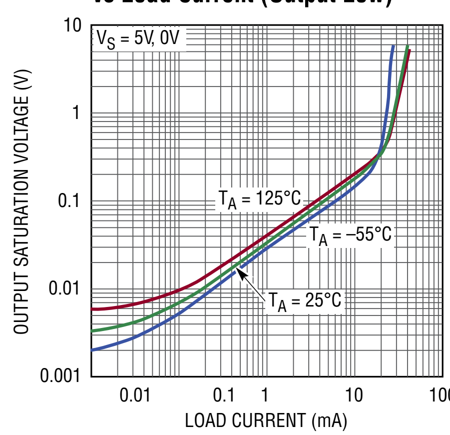
62367 G04

Input Bias Current vs Temperature



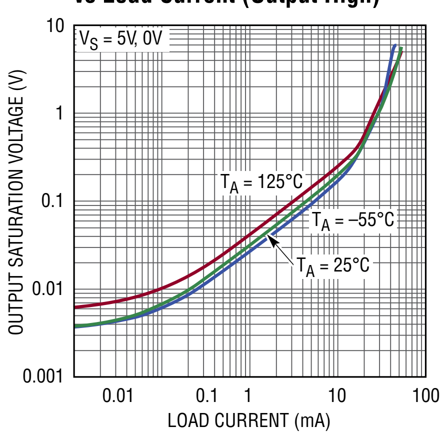
62367 G05

Output Saturation Voltage vs Load Current (Output Low)



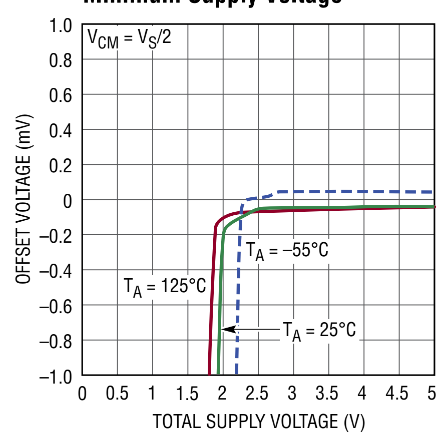
62367 G06

Output Saturation Voltage vs Load Current (Output High)



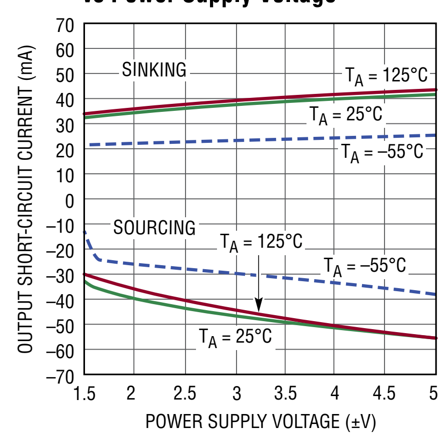
62367 G07

Minimum Supply Voltage



62367 G08

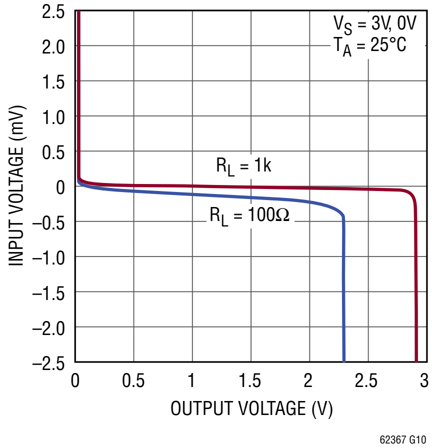
Output Short-Circuit Current vs Power Supply Voltage



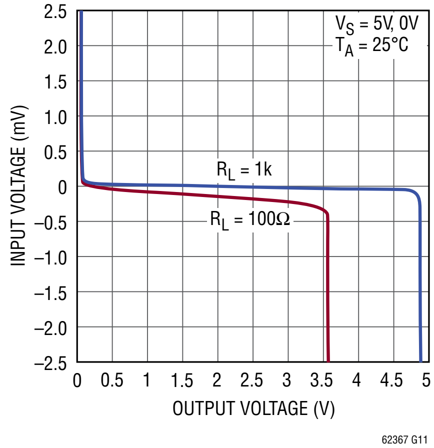
62367 G09

TYPICAL PERFORMANCE CHARACTERISTICS

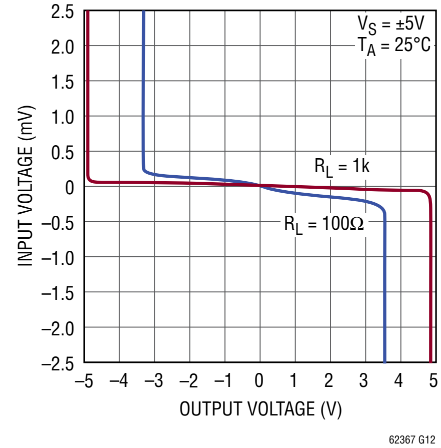
Open-Loop Gain



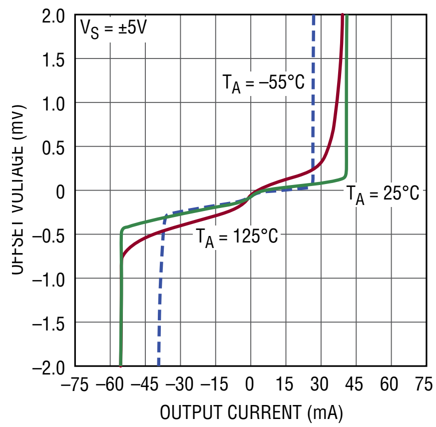
Open-Loop Gain



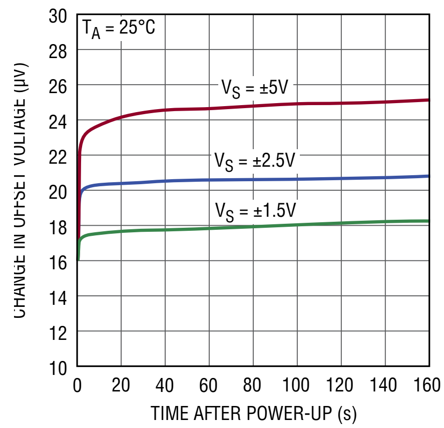
Open-Loop Gain



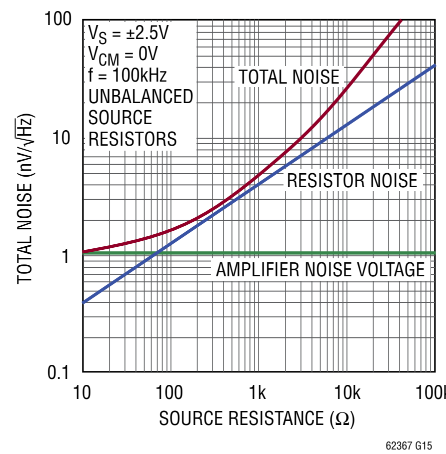
Offset Voltage vs Output Current



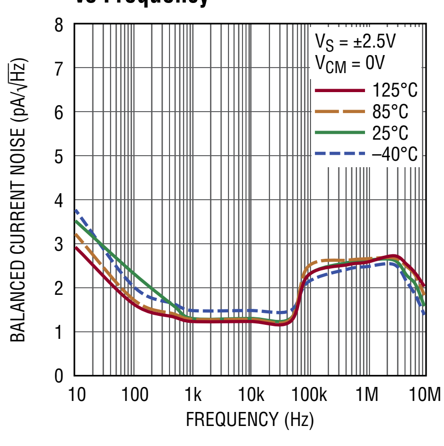
Warm-Up Drift vs Time



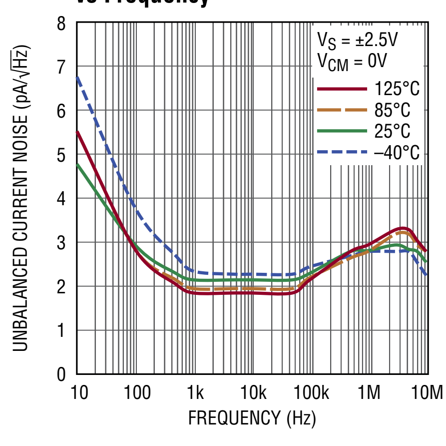
Total Noise vs Total Source Resistance



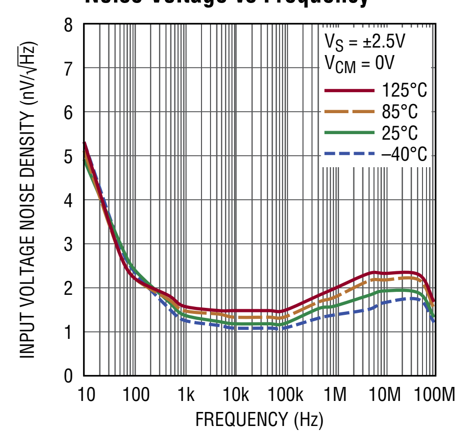
Balanced Current Noise vs Frequency



Unbalanced Current Noise vs Frequency

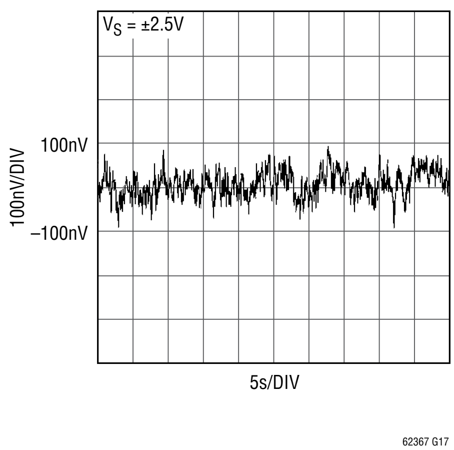


Noise Voltage vs Frequency

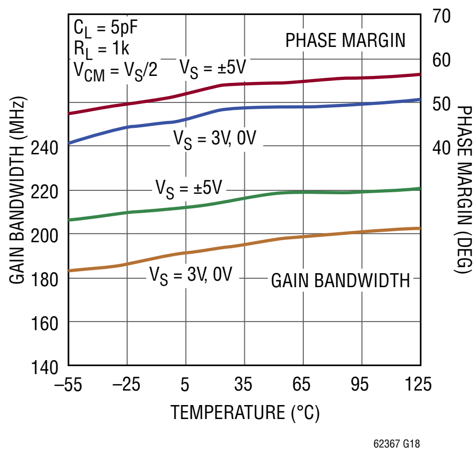


TYPICAL PERFORMANCE CHARACTERISTICS

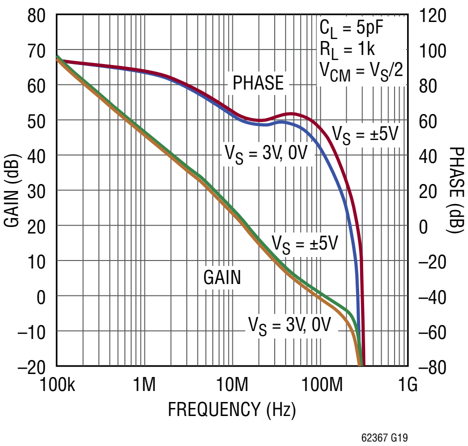
0.1Hz to 10Hz Input Voltage Noise



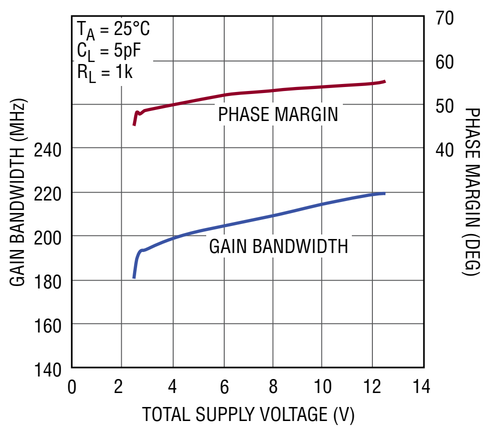
Gain Bandwidth and Phase Margin vs Temperature



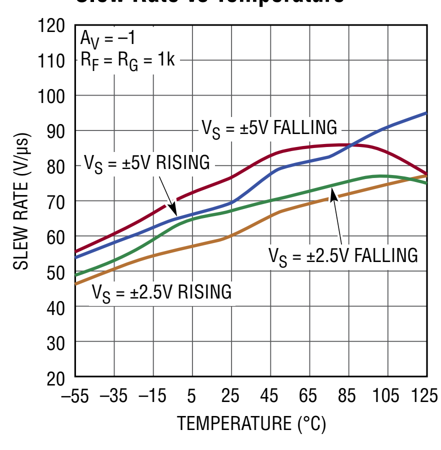
Open-Loop Gain vs Frequency



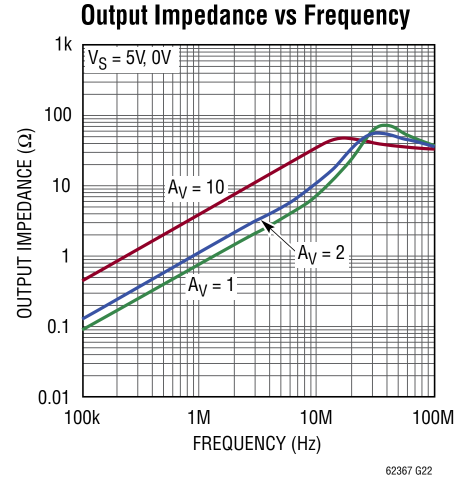
Gain Bandwidth and Phase Margin vs Supply Voltage



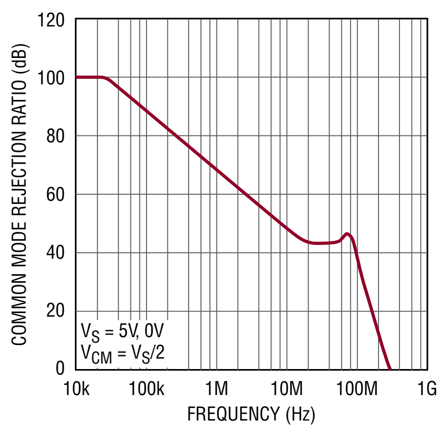
Slew Rate vs Temperature



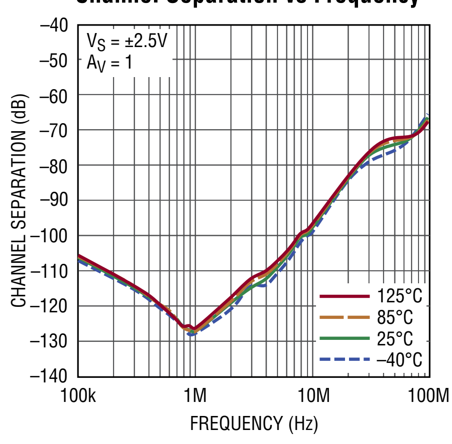
Output Impedance vs Frequency



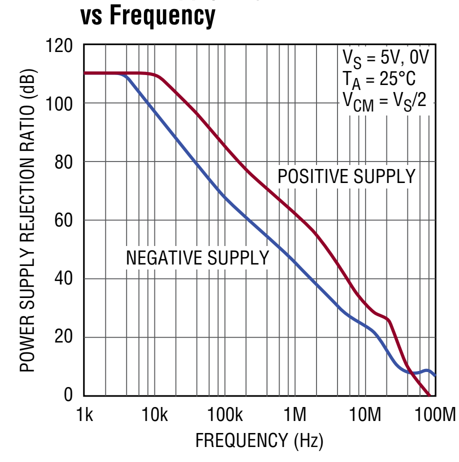
Common Mode Rejection Ratio vs Frequency



Channel Separation vs Frequency

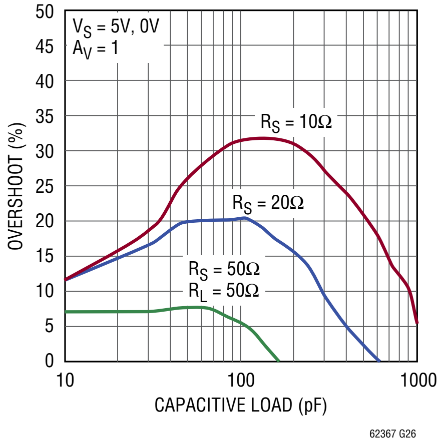


Power Supply Rejection Ratio vs Frequency

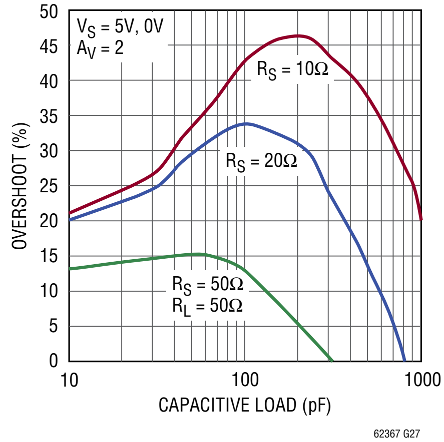


TYPICAL PERFORMANCE CHARACTERISTICS

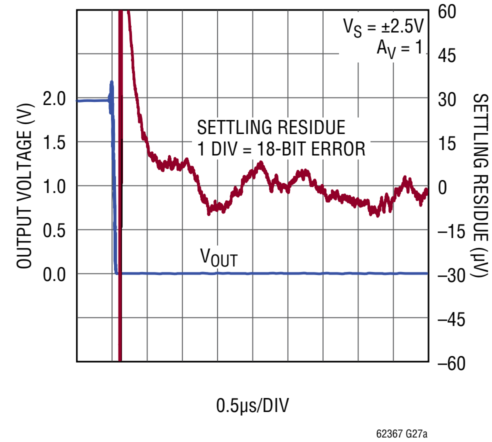
Series Output Resistance and Overshoot vs Capacitive Load



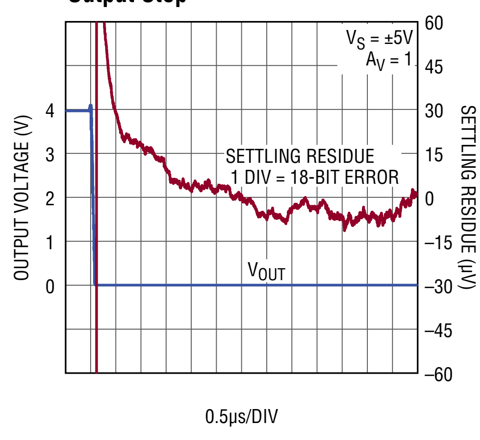
Series Output Resistance and Overshoot vs Capacitive Load



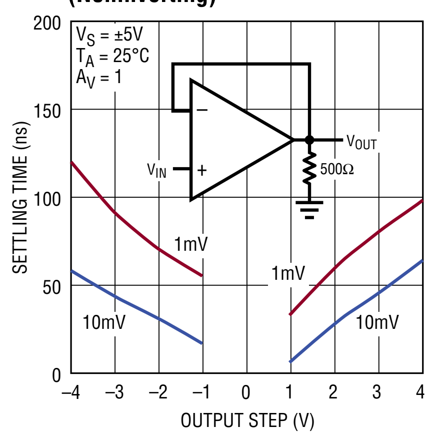
18-Bit Settling Time to $2V_{P-P}$ Output Step



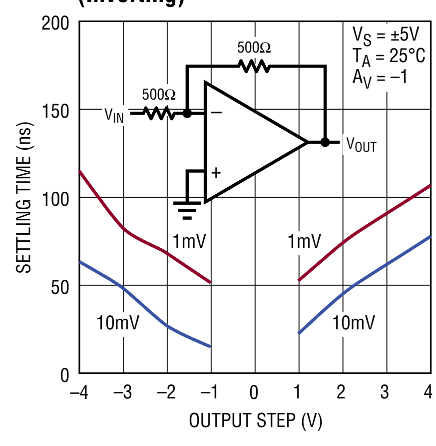
18-Bit Settling Time to $4V_{P-P}$ Output Step



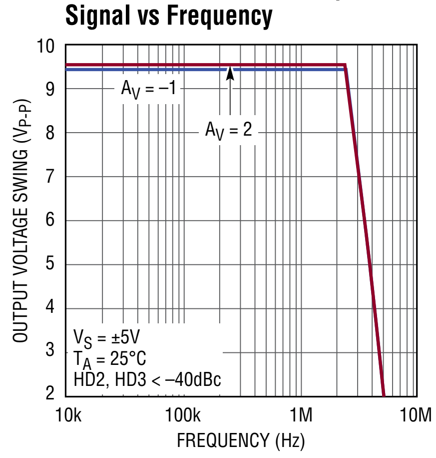
Settling Time vs Output Step (Noninverting)



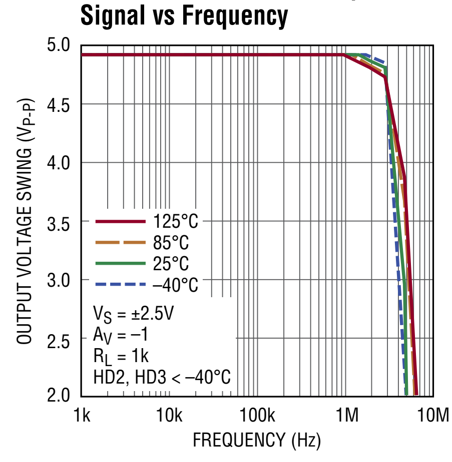
Settling Time vs Output Step (Inverting)



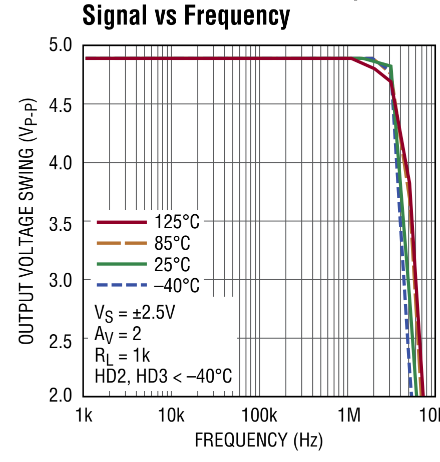
Maximum Undistorted Output Signal vs Frequency



Maximum Undistorted Output Signal vs Frequency

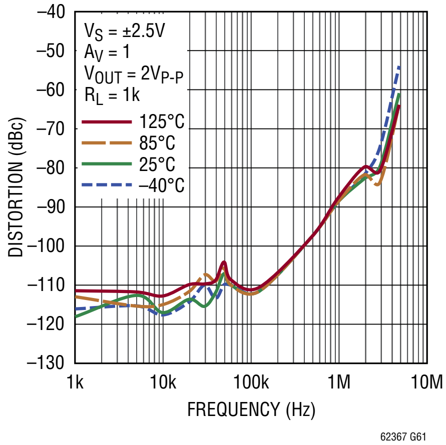


Maximum Undistorted Output Signal vs Frequency

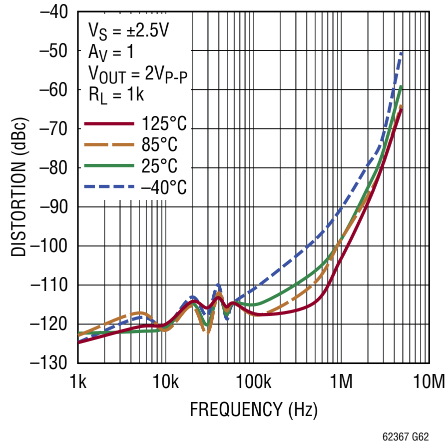


TYPICAL PERFORMANCE CHARACTERISTICS

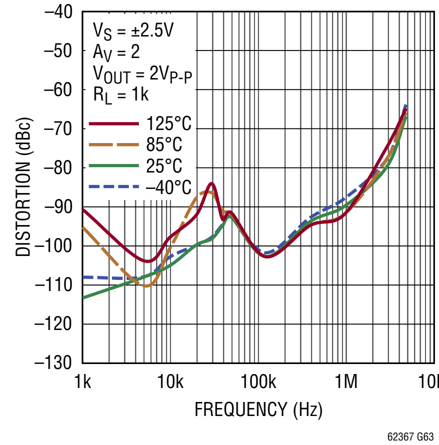
Harmonic Distortion (HD2) vs Frequency



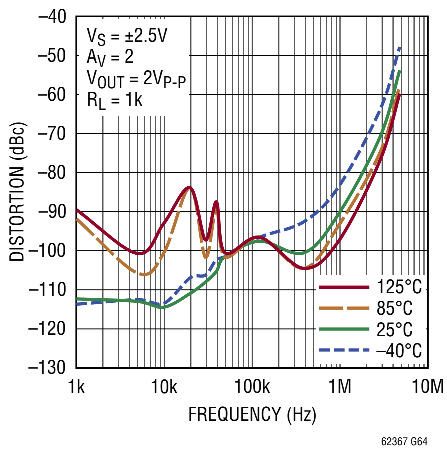
Harmonic Distortion (HD3) vs Frequency



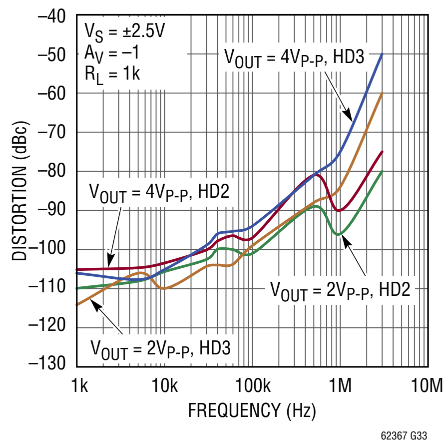
Harmonic Distortion (HD2) vs Frequency



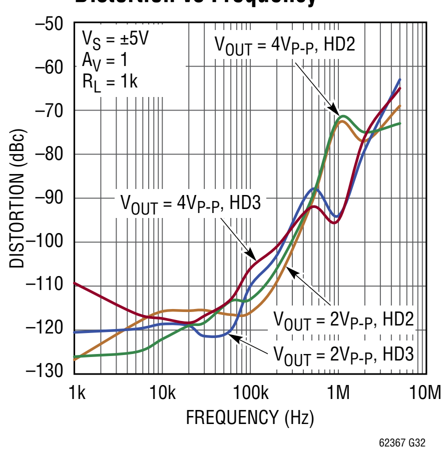
Harmonic Distortion (HD3) vs Frequency



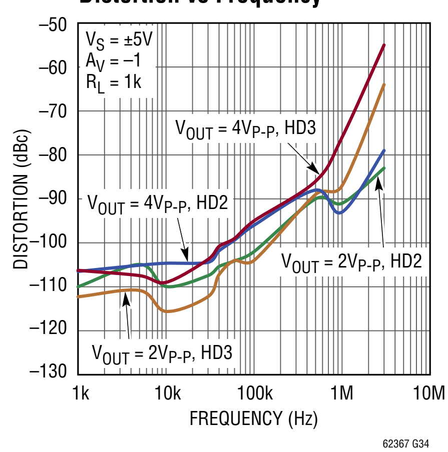
Distortion vs Frequency



Distortion vs Frequency

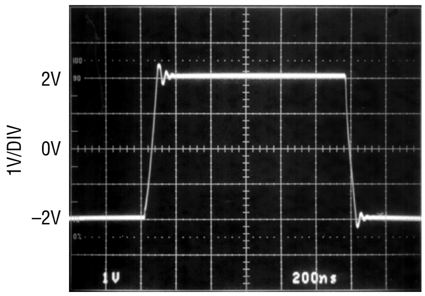


Distortion vs Frequency



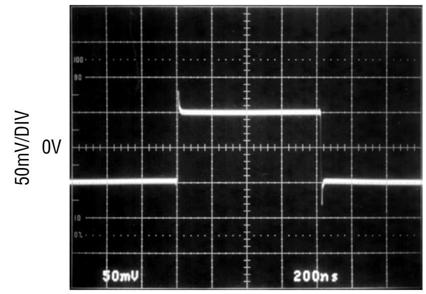
TYPICAL PERFORMANCE CHARACTERISTICS

Large-Signal Response



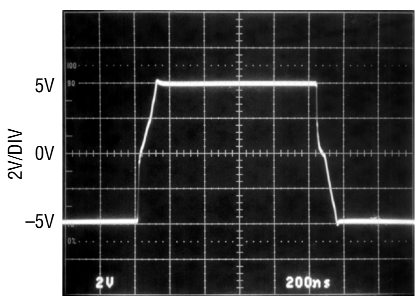
V_S = ±2.5V 200ns/DIV 62367 G35
A_V = –1
R_L = 1k

Small-Signal Response



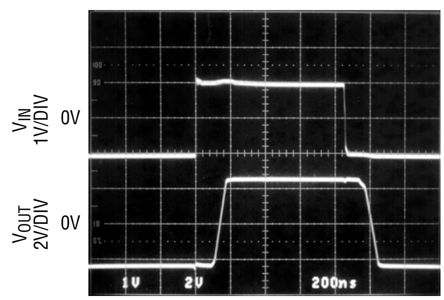
V_S = ±2.5V 200ns/DIV 62367 G36
A_V = 1
R_L = 1k

Large-Signal Response



V_S = ±5V 200ns/DIV 62367 G37
A_V = 1
R_L = 1k

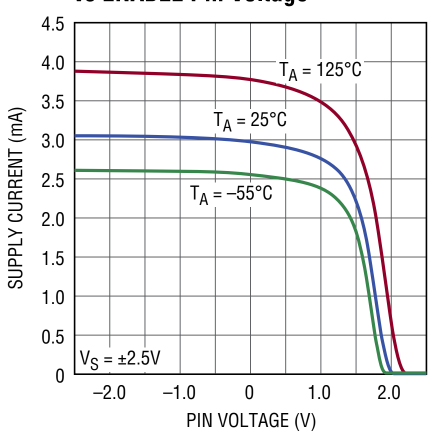
Output Overdrive Recovery



V_S = ±2.5V 200ns/DIV 62367 G38
A_V = 3

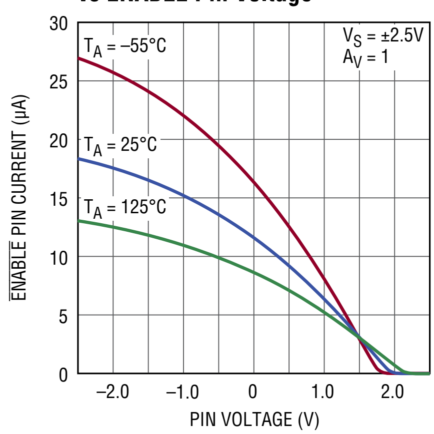
(LT6236) $\overline{\text{ENABLE}}$ Characteristics

Supply Current vs $\overline{\text{ENABLE}}$ Pin Voltage



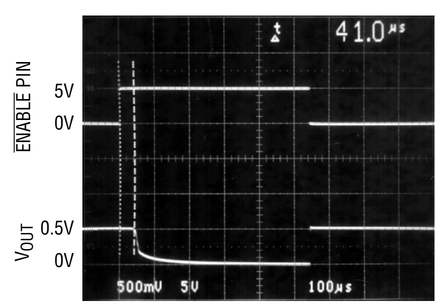
62367 G39

$\overline{\text{ENABLE}}$ Pin Current vs $\overline{\text{ENABLE}}$ Pin Voltage



62367 G40

$\overline{\text{ENABLE}}$ Pin Response Time



V_S = ±2.5V 100µs/DIV 62367 G41
V_{IN} = 0.5V
A_V = 1
R_L = 1k

APPLICATIONS INFORMATION

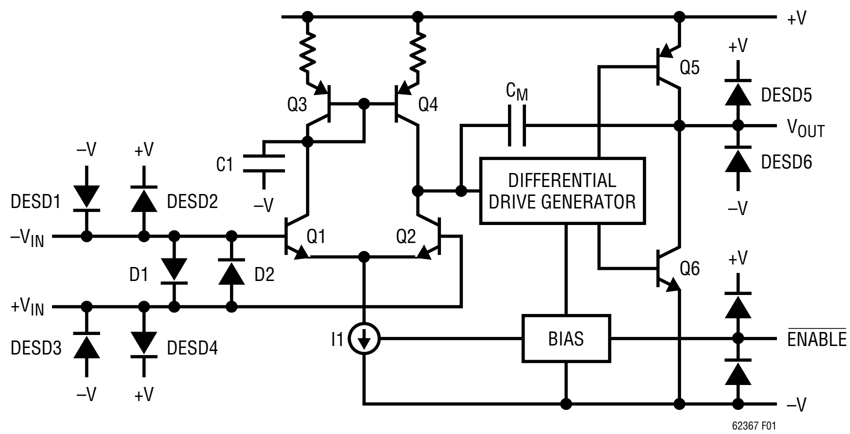


Figure 1. Simplified Schematic

Functional Description

Figure 1 is a simplified schematic of the LT6236/LT6237/LT6238, which has a pair of low noise input transistors Q1 and Q2. A simple current mirror Q3/Q4 converts the differential signal to a single-ended output, and these transistors are degenerated to reduce their contribution to the overall noise. Capacitor C1 reduces the unity cross frequency and improves the frequency stability without degrading the gain bandwidth of the amplifier. Capacitor C_M sets the overall amplifier gain bandwidth. The differential drive generator supplies current to transistors Q5 and Q6 that provide rail-to-rail output swing.

Input Protection

Back-to-back diodes, D1 and D2, limit the differential input voltage to ±0.7V. The inputs of the LT6236/LT6237/LT6238 do not have internal resistors in series with the input transistors. This technique is often used to protect the input devices from over voltage that causes excessive current to flow. The addition of these resistors would significantly degrade the voltage noise of these amplifiers.

For instance, a 100Ω resistor in series with each input would generate $1.8nV/\sqrt{Hz}$ of noise, and the total amplifier noise voltage would rise from $1.1nV/\sqrt{Hz}$ to $2.1nV/\sqrt{Hz}$. Once the input differential voltage exceeds ±0.7V, steady state current conducted through the protection diodes should be limited to ±40mA. This implies 25Ω of protection resistance is necessary per volt of overdrive beyond ±0.7V. These input diodes are rugged enough to handle transient currents due to amplifier slew rate overdrive and clipping without protection resistors. Figure 2 shows the output response to an input overdrive with the amplifier connected as a voltage follower. With the input signal low, current source I1 saturates and the differential drive generator drives Q6 into saturation so the output voltage swings all the way to V^-. The input can swing positive until transistor Q2 saturates into current mirror Q3/Q4. When saturation occurs, the output tries to phase invert, but diode D2 conducts current from the signal source to the output through the feedback connection. The output is clamped a diode drop below the input. In Figure 2, the input signal generator is limiting at about 20mA.

With the amplifier connected in a gain of $A_V \geq 2$, the output can invert with very heavy overdrive. To avoid this inversion, limit the input overdrive to 0.5V beyond the power supply rails.

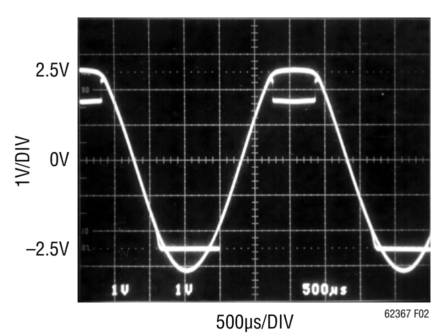


Figure 2. V_S = ±2.5V, A_V = 1 with Large Overdrive

APPLICATIONS INFORMATION

ESD

The LT6236/LT6237/LT6238 have reverse-biased ESD protection diodes on all inputs and outputs as shown in Figure 1. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to 100mA or less, no damage to the device will occur.

Noise

The noise voltage of the LT6236/LT6237/LT6238 is equivalent to that of a 75Ω resistor, and for the lowest possible noise it is desirable to keep the source and feedback resistance at or below this value, i.e. $R_S + R_G||R_{FB} \le 75\Omega$. With $R_S + R_G||R_{FB} = 75\Omega$ the total noise of the amplifier is:

$$e_N = \sqrt{(1.1nV)^2 + (1.1nV)^2} = 1.55nV/\sqrt{Hz}$$

Below this resistance value, the amplifier dominates the noise, but in the region between 75Ω and about 3k, the noise is dominated by the resistor thermal noise. As the total resistance is further increased beyond 3k, the amplifier noise current multiplied by the total resistance eventually dominates the noise.

The product of $e_N \bullet \sqrt{I_{SUPPLY}}$ is an interesting way to gauge low noise amplifiers. Most low noise amplifiers have high I_{SUPPLY}. In applications that require low noise voltage with the lowest possible supply current, this product can be helpful.

The LT6236/LT6237/LT6238 have an $e_N \bullet \sqrt{I_{SUPPLY}}$ of only 1.9 per amplifier, yet it is common to see amplifiers with similar noise specifications to have $e_N \bullet \sqrt{I_{SUPPLY}}$ as high as 13.5. For a complete discussion of amplifier noise, see the LT1028 data sheet.

ENABLE Pin

The LT6236 includes an $\overline{\text{ENABLE}}$ pin that shuts down the amplifier to 10µA maximum supply current. For normal operation, the $\overline{\text{ENABLE}}$ pin must be pulled to at least 2.7V below V^+. The $\overline{\text{ENABLE}}$ pin must be driven high to within 0.35V of V^+ to shut down the amplifier. This can be accomplished with simple gate logic; however care must be taken if the logic and the LT6236 operate from different supplies. If this is the case, open drain logic can be used with a pull-up resistor to ensure that the amplifier remains off. When the $\overline{\text{ENABLE}}$ pin is left floating, the amplifier is inactive. However, care should be taken to control the leakage current through the pin so the amplifier is not inadvertently turned on. See Typical Performance Characteristics.

The output leakage current when disabled is very low; however, current can flow into the input protection diodes, D1 and D2, if the output voltage exceeds the input voltage by a diode drop.

Power Dissipation

The LT6237MS8 combines high speed with large output current in a small package. Due to the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

The power dissipation in the IC is the function of the supply voltage, output voltage and the load resistance. For a given supply voltage, the worst-case power dissipation $P_{D(MAX)}$ occurs at the maximum quiescent supply current and at the output voltage which is half of either supply voltage (or the maximum swing if it is less than half the supply voltage). $P_{D(MAX)}$ is given by:

$$P_{D(MAX)} = (V^+ – V^–)(I_{S(MAX)}) + (V^+/2)^2/R_L$$

Example: An LT6237HMS8 in the 8-Lead MSOP package has a thermal resistance of θ_{JA} = 273°C/W. Operating on ±5V supplies with one amplifier driving a 1k load, the worst-case power dissipation is given by:

$$P_{D(MAX)} = (10V)(11mA) + (2.5V)^2/1000\Omega = 116mW$$

In this example, the maximum ambient temperature that the part is allowed to operate is:

$$T_A = T_J - (P_{D(MAX)} \times 273°C/W)$$

$$T_A = 150°C – (116mW)(273°C/W) = 118.3°C$$

To operate the device at a higher ambient temperature for the same conditions, switch to using two LT6236 in the 6-Lead TSOT-23, or a single LT6237 in the 8-Lead DFN package.

APPLICATIONS INFORMATION

Interfacing to ADCs

When driving an ADC, a single-pole, passive RC filter should be used between the outputs of the LT6236/LT6237/LT6238 and the inputs of the ADC. The sampling process of ADCs creates a charge transient from the switching of the ADC sampling capacitor. This momentarily "shorts" the output of the amplifier as charge is transferred between amplifier and sampling capacitor. The amplifier must recover and settle from this load transient before the acquisition period has ended for a valid representation of the input signal. The RC network between the outputs of the driver and the inputs of the ADC decouples the sampling transient of the ADC. The capacitance serves to provide the bulk of the charge during the sampling process, while the two resistors at the outputs of the LT6236/LT6237/LT6238 are used to dampen and attenuate any charge injected by the ADC. The RC filter provides the benefit of band limiting broadband output noise.

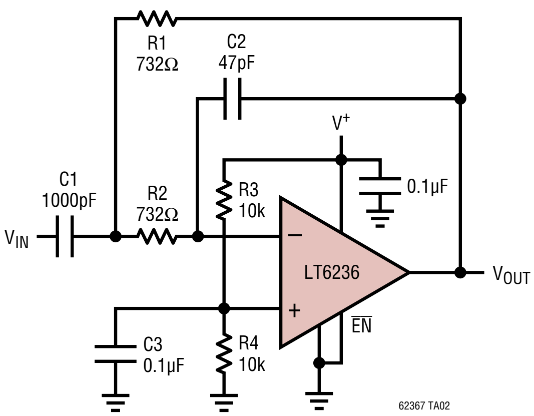
Thanks to the very low wideband noise of the LT6236/LT6237/LT6238, a wideband filter can be used between the amplifier and the ADC without impacting SNR. This is especially important with ADCs or applications that require full settling in between each conversion.

The selection of an appropriate filter depends on the specific ADC, however the following procedure is suggested for choosing filter component values. Begin by selecting an appropriate RC time constant for the input signal. Generally, longer time constants improve SNR at the expense of settling time. Output transient settling to 18-bit accuracy will require over twelve RC time constants. To select the resistor value, the resistors in the decoupling network should be at least 10Ω. Keep in mind that these resistors also serve to decouple the LT6236/LT6237/LT6238 outputs from load capacitance. Too large of a resistor will leave insufficient settling time. Too small of a resistor will not properly dampen the load transient of the sampling process, and prolong the time required for settling. For lowest distortion, choose capacitors with low dielectric absorption such as a C0G multilayer ceramic capacitor. In general, large capacitor values attenuate the fixed nonlinear charge kickback, however very large capacitor values will detrimentally load the driver at the desired input frequency and cause driver distortion. Smaller input swings allow for larger filter capacitor values due to decreased loading demands on the driver. This property may be limited by the particular input amplitude dependence of differential nonlinear kickback for the specific ADC used.

Series resistors should typically be placed at the inputs to the ADC in order to further improve distortion performance. These series resistors function with the ADC sampling capacitor to filter potential ground bounce or other high speed sampling disturbances. Additionally the resistors limit the rise time of residual filter glitches that manage to propagate to the driver outputs. Restricting possible glitch propagation rise time to within the small signal bandwidth of the driver enables less disturbed output settling.

TYPICAL APPLICATIONS

Single Supply, Low Noise, Low Power, Bandpass Filter with Gain = 10



$f_0 = \frac{1}{2\pi RC} = 1MHz$

$C = \sqrt{C1C2}$, R = R1 = R2

$f_0 = \left(\frac{732\Omega}{R}\right)$MHz, MAXIMUM f_0 = 1MHz

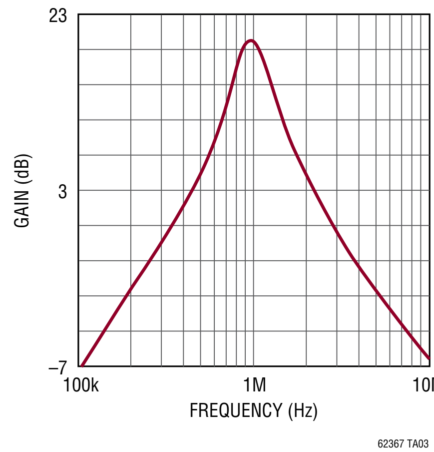
$f_{-3dB} = \frac{f_0}{2.5}$

A_V = 20dB at f_0

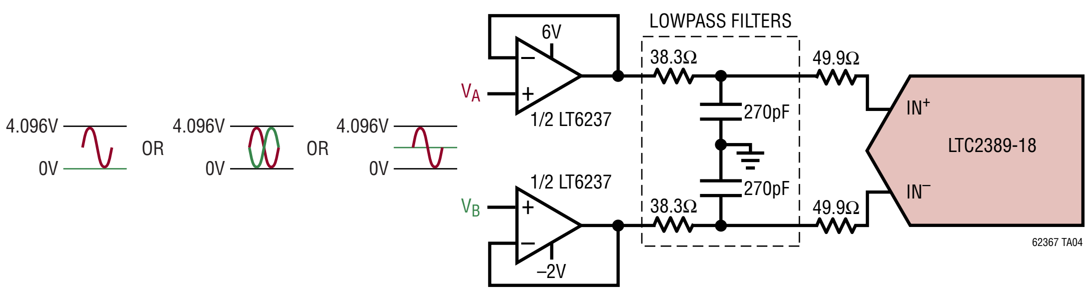
$\overline{EN}$ = 4µV_{RMS} INPUT REFERRED

I_S = 3.7mA FOR V^+ = 5V

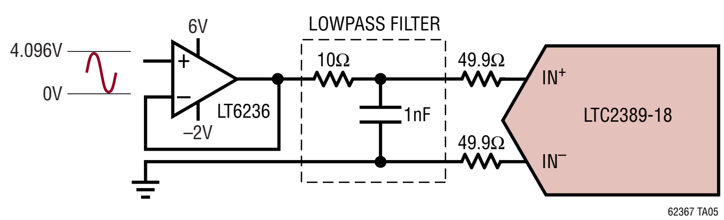
Frequency Response Plot of Bandpass Filter



Driving a Fully Differential ADC



Driving a Single-Ended ADC

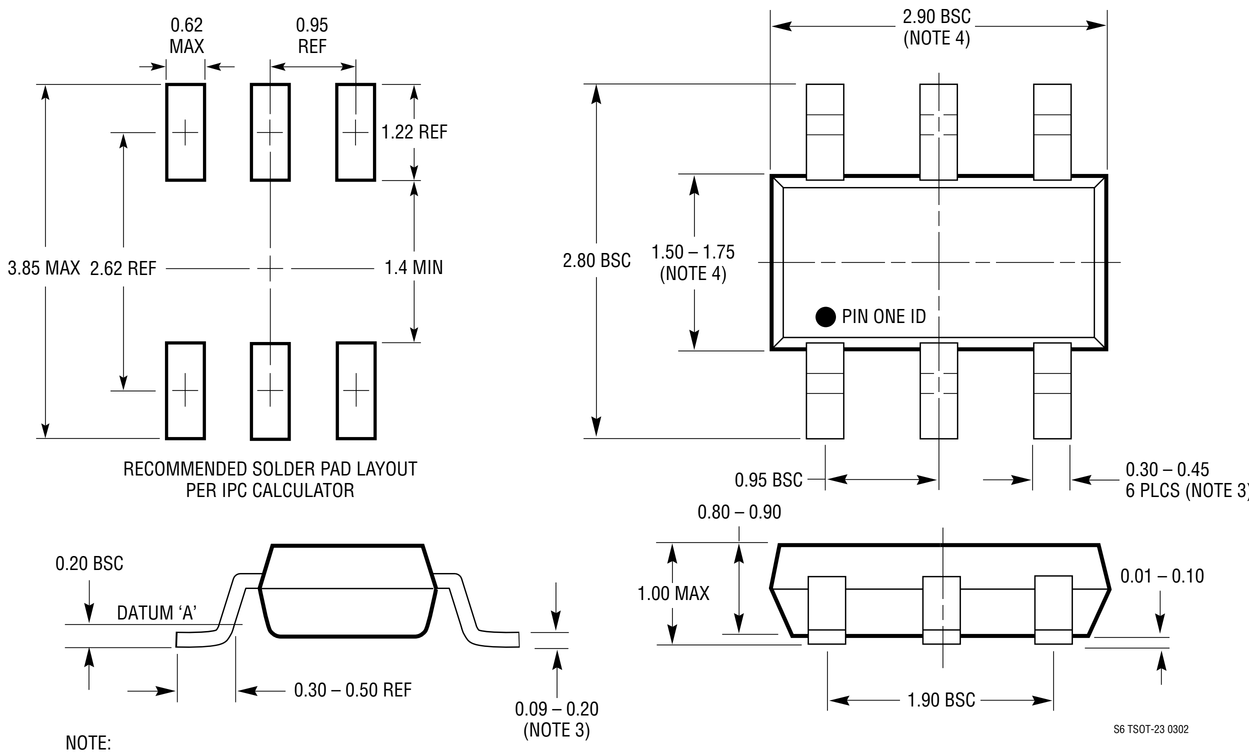


623637fb

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)

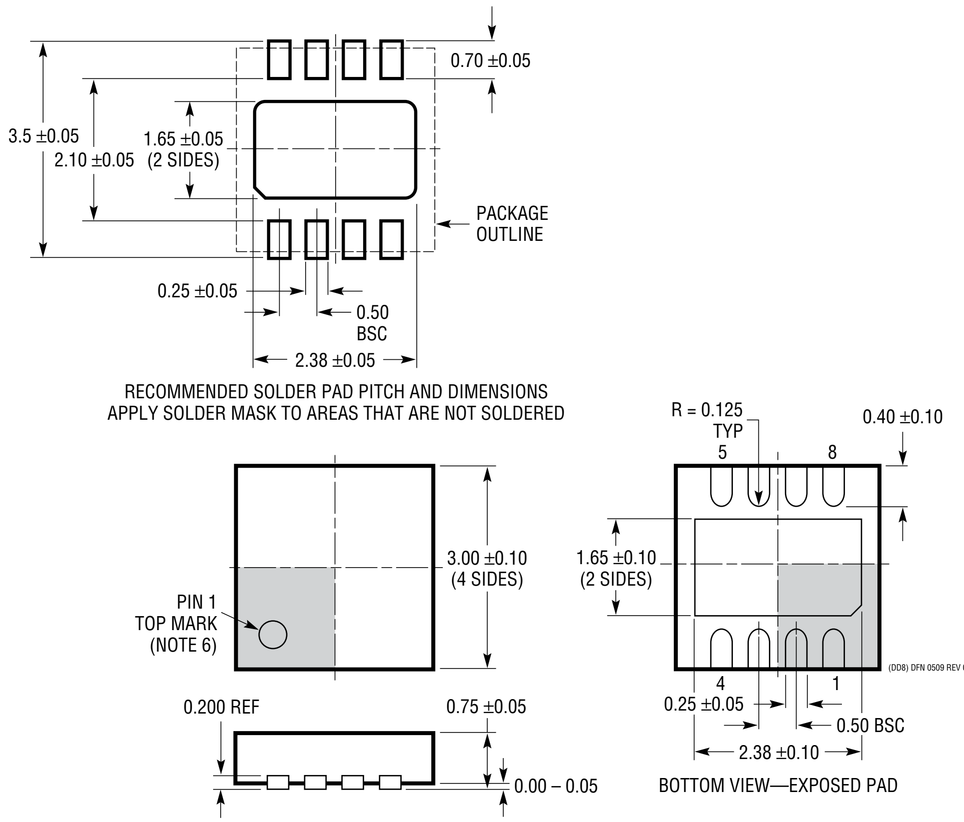


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)

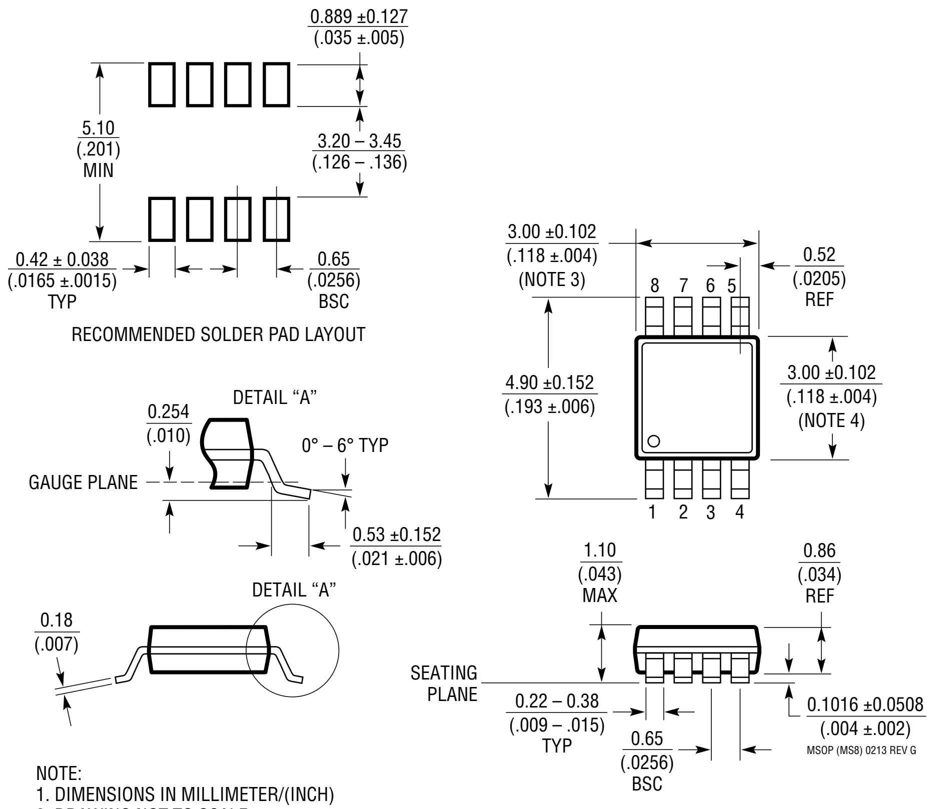


NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)

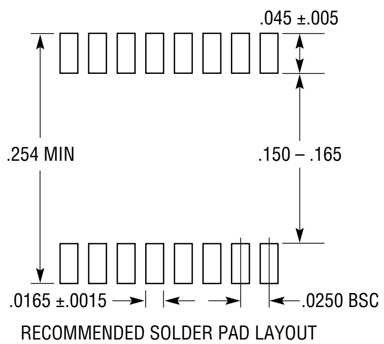


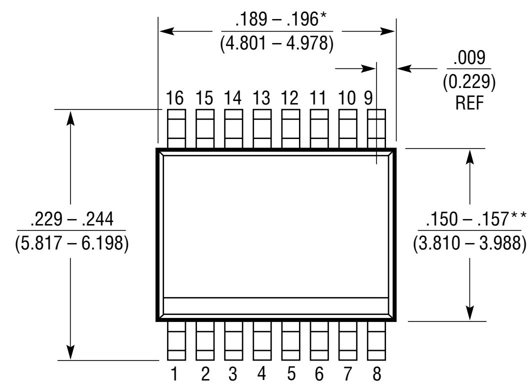
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

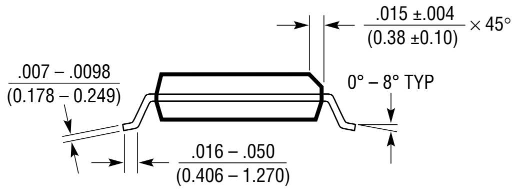
PACKAGE DESCRIPTION

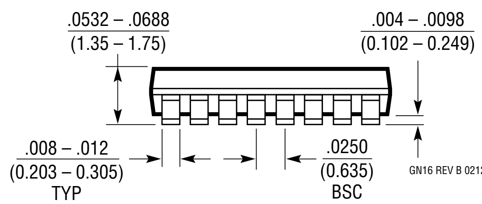
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)









NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

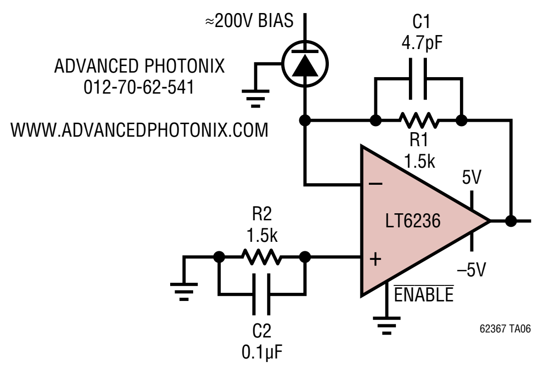
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/13	Added LT6238 quad	All
B	09/14	Corrected I_{SINK} condition for V_{OL} specification. Corrected V_O condition for A_{VOL} specification. Added LT6238 to ESD discussion.	5, 6, 9, 10 9, 10 18

TYPICAL APPLICATION

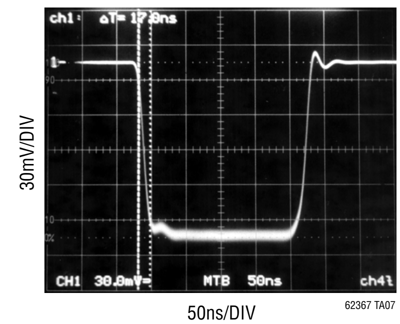
The LT6236 is configured as a transimpedance amplifier with an I-to-V conversion gain of 1.5kΩ set by R1. The LT6236 is ideally suited to this application because of its low input offset voltage and current, and its low noise. This is because the 1.5k resistor has an inherent thermal noise of $5nV/\sqrt{Hz}$ or $3.4pA/\sqrt{Hz}$ at room temperature, while the LT6236 contributes only $1.1nV/\sqrt{Hz}$ and $2.4pA/\sqrt{Hz}$. So, with respect to both voltage and current noises, the LT6236 is actually quieter than the gain resistor. The circuit uses an avalanche photodiode with the cathode biased to approximately 200V. When light is incident on the photodiode, it induces a current I_{PD} which flows into the amplifier circuit. The amplifier output falls negative to maintain balance at its inputs. The transfer function is therefore $V_{OUT} = –I_{PD} • 1.5k$. C1 ensures stability and good settling characteristics. Output offset was measured at 280µV, so low in part because R2 serves to cancel the DC effects of bias current. Output noise was measured at $1.1mV_{P–P}$ on a 100MHz measurement bandwidth, with C2 shunting R2's thermal noise. As shown in the scope photo, the rise time is 17ns, indicating a signal bandwidth of 20MHz.

Low Power Avalanche Photodiode Transimpedance Amplifier
I_S = 3.3mA



OUTPUT OFFSET = 500µV TYPICAL
BANDWIDTH = 20MHz
OUTPUT NOISE = $1.1mV_{P-P}$ (100MHz MEASUREMENT BW)

Photodiode Amplifier Time Domain Response



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
OPERATIONAL AMPLIFIERS		
LT6230/LT6231/LT6232	Single, Dual, Quad Low Noise, Rail-to-Rail Output.	$1.1nV/\sqrt{Hz}$
LT6350	Low Noise, Single-Ended to Differential Converter/ADC Driver	4.8mA, –97dBc Distortion at 100kHz, $4V_{P-P}$ Output
LTC6246/LTC6247/LTC6248	Single/Dual/Quad 180MHz Rail-to-Rail Low Power Op Amps	1mA/Amplifier, $4.2nV/\sqrt{Hz}$
LTC6360	1GHz Very Low Noise Single-Ended SAR ADC Driver with True Zero Output	HD2 = –103dBc and HD3 = –109dBc for $4V_{P-P}$ Output at 40kHz
ADCs		
LTC2389-18	Low Power 18-Bit SAR ADC	2.5Msps
LTC2389-16	Low Power 16-Bit SAR ADC	2.5Msps
LTC2379-18 LTC2378-18 LTC2377-18 LTC2376-18	Low Power 18-Bit SAR ADC	1.6Msps 1Msps 500ksps 250ksps

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