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# 74VHC157

## Quad 2-Input Multiplexer

### Features

- High Speed:  $t_{PD} = 4.1\text{ns}$  (Typ.) at  $V_{CC} = 5\text{V}$
- Low power dissipation:  $I_{CC} = 4\mu\text{A}$  (Max.) at  $T_A = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min.)
- Power down protection is provided on all inputs
- Low noise:  $V_{OLP} = 0.8\text{V}$  (Max.)
- Pin and function compatible with 74HC157

### General Description

The VHC157 is an advanced high speed CMOS Quad 2-Channel Multiplexer fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of four 2-input digital multiplexers with common select and enable inputs. When the  $\overline{\text{ENABLE}}$  input is held "H" level, selection of data is inhibited and all the outputs become "L" level. The SELECT decoding determines whether the  $I_{0x}$  or  $I_{1x}$  inputs get routed to their corresponding outputs.

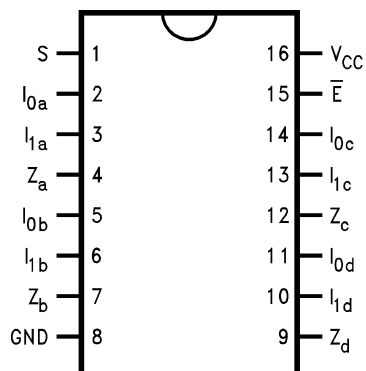
An Input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

### Ordering Information

Order Number	Package Number	Package Description
74VHC157M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC157SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC157MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

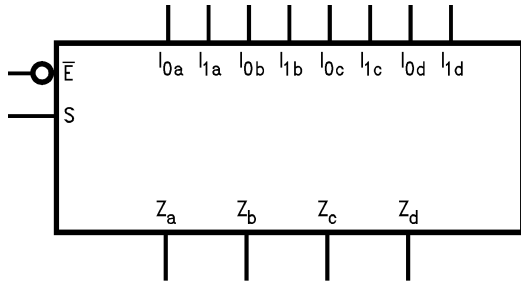
### Connection Diagram



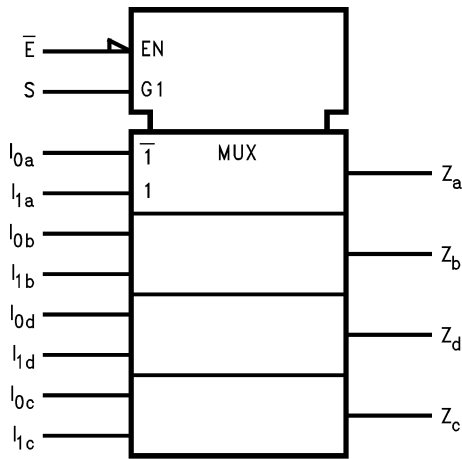
### Pin Description

Pin Names	Description
$I_{0a}-I_{0d}$	Source 0 Data Inputs
$I_{1a}-I_{1d}$	Source 1 Data Inputs
$\overline{\text{E}}$	Enable Input
S	Select Input
$Z_a-Z_d$	Outputs

### Logic Symbols



IEEE/IEC



### Functional Description

The VHC157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ( $\bar{E}$ ) is active-LOW. When  $\bar{E}$  is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The VHC157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$Z_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Z_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

$$Z_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

A common use of the VHC157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The VHC157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

### Truth Table

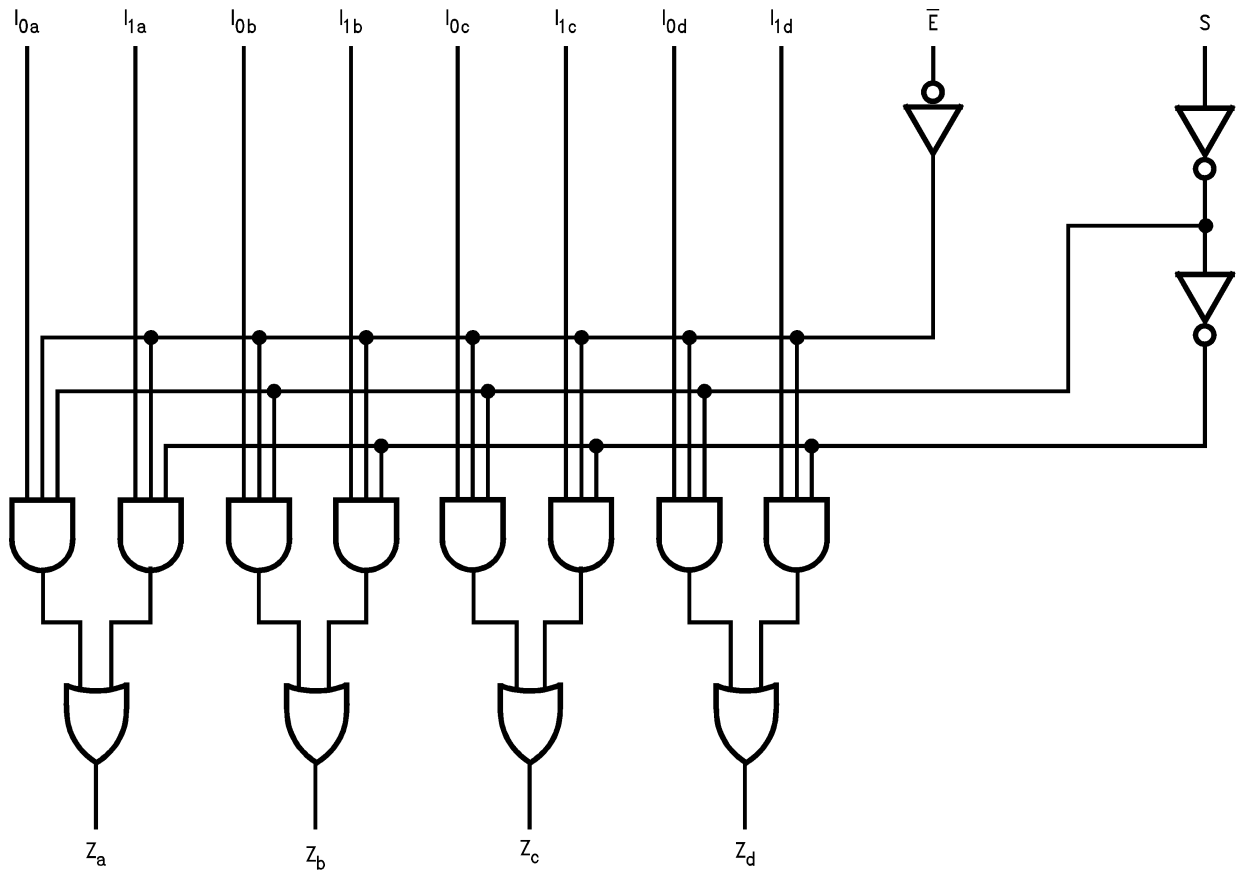
Inputs				Outputs
$\bar{E}$	S	$I_0$	$I_1$	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7.0V
$V_{IN}$	DC Input Voltage	-0.5V to +7.0V
$V_{OUT}$	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
$I_{IK}$	Input Diode Current	-20mA
$I_{OK}$	Output Diode Current	$\pm 20mA$
$I_{OUT}$	DC Output Current	$\pm 25mA$
$I_{CC}$	DC $V_{CC}$ / GND Current	$\pm 50mA$
$T_{STG}$	Storage Temperature	-65°C to +150°C
$T_L$	Lead Temperature (Soldering, 10 seconds)	260°C

## Recommended Operating Conditions<sup>(1)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	2.0V to +5.5V
$V_{IN}$	Input Voltage	0V to +5.5V
$V_{OUT}$	Output Voltage	0V to $V_{CC}$
$T_{OPR}$	Operating Temperature	-40°C to +85°C
$t_r, t_f$	Input Rise and Fall Time, $V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$	0ns/V ~ 100ns/V 0ns/V ~ 20ns/V

### Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		Units			
				Min.	Typ.	Max.	Min.	Max.				
$V_{IH}$	HIGH Level Input Voltage	2.0		1.50			1.50		V			
		3.0–5.5		$0.7 \times V_{CC}$			$0.7 \times V_{CC}$					
$V_{IL}$	LOW Level Input Voltage	2.0				0.50		0.50	V			
		3.0–5.5				$0.3 \times V_{CC}$		$0.3 \times V_{CC}$				
$V_{OH}$	HIGH Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\mu\text{A}$	1.9	2.0		1.9		V		
		3.0			2.9	3.0		2.9				
		4.5			4.4	4.5		4.4				
		3.0				$I_{OH} = -4\text{mA}$	2.58				2.48	
		4.5				$I_{OH} = -8\text{mA}$	3.94				3.80	
$V_{OL}$	LOW Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\mu\text{A}$		0.0	0.1		0.1	V		
		3.0				0.0	0.1		0.1			
		4.5				0.0	0.1		0.1			
		3.0				$I_{OL} = 4\text{mA}$		0.36			0.44	
		4.5				$I_{OL} = 8\text{mA}$		0.36			0.44	
$I_{IN}$	Input Leakage Current	0–5.5	$V_{IN} = 5.5\text{V}$ or GND			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$			
$I_{CC}$	Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND			4.0		40.0	$\mu\text{A}$			

## Noise Characteristics

Symbol	Parameter	$V_{CC}$ (V)	Conditions	$T_A = 25^\circ\text{C}$		Units
				Typ.	Limits	
$V_{OLP}^{(3)}$	Quiet Output Maximum Dynamic $V_{OL}$	5.0	$C_L = 50\text{pF}$	0.3	0.8	V
$V_{OLV}^{(3)}$	Quiet Output Minimum Dynamic $V_{OL}$	5.0	$C_L = 50\text{pF}$	-0.3	-0.8	V
$V_{IHD}^{(3)}$	Minimum HIGH Level Dynamic Input Voltage	5.0	$C_L = 50\text{pF}$		3.5	V
$V_{ILD}^{(3)}$	Maximum LOW Level Dynamic Input Voltage	5.0	$C_L = 50\text{pF}$		1.5	V

**Note:**

2. Parameter guaranteed by design.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, I <sub>n</sub> to Z <sub>n</sub>	3.3 ± 0.3	C <sub>L</sub> = 15pF		6.2	9.7	1.0	11.5	ns
			C <sub>L</sub> = 50pF		8.7	13.2	1.0	15.0	
		5.0 ± 0.5	C <sub>L</sub> = 15pF		4.1	6.4	1.0	7.5	ns
			C <sub>L</sub> = 50pF		5.6	8.4	1.0	9.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, S to Z <sub>n</sub>	3.3 ± 0.3	C <sub>L</sub> = 15pF		8.4	13.2	1.0	15.5	ns
			C <sub>L</sub> = 50pF		10.9	16.7	1.0	19.0	
		5.0 ± 0.5	C <sub>L</sub> = 15pF		5.3	8.1	1.0	9.5	ns
			C <sub>L</sub> = 50pF		6.8	10.1	1.0	11.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, E <sub>n</sub> to Z <sub>n</sub>	3.3 ± 0.3	C <sub>L</sub> = 15pF		8.7	13.6	1.0	16.0	ns
			C <sub>L</sub> = 50pF		11.2	17.1	1.0	19.5	
		5.0 ± 0.5	C <sub>L</sub> = 15pF		5.6	8.6	1.0	10.0	ns
			C <sub>L</sub> = 50pF		7.1	10.6	1.0	12.0	
C <sub>IN</sub>	Input Capacitance		V <sub>CC</sub> = Open		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance		<sup>(3)</sup>		20				pF

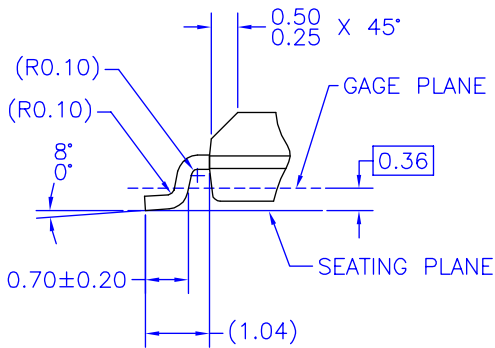
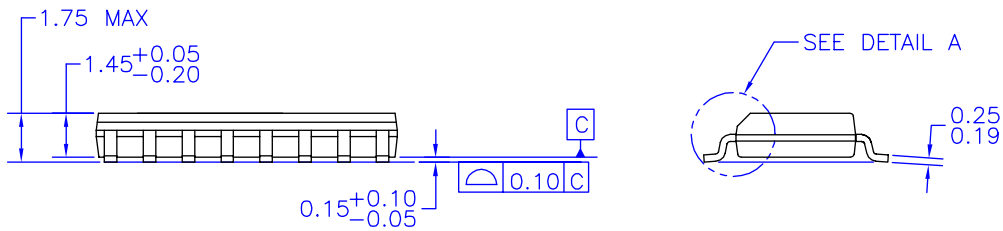
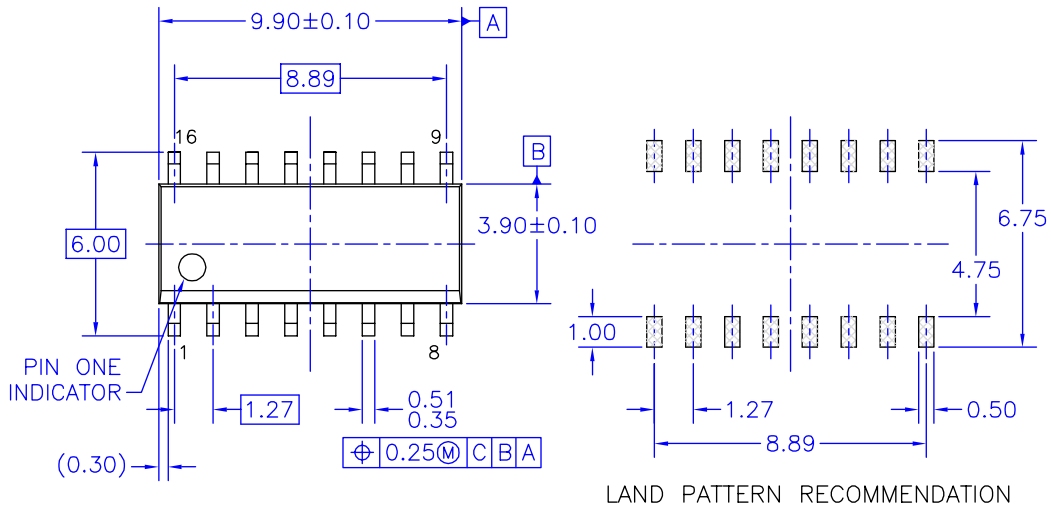
**Note:**

3. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

### Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



DETAIL A  
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AC, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) STANDARD LEAD FINISH:  
200 MICRONS / 5.08 MICRONS MIN.  
LEAD/TIN (SOLDER) ON COPPER.

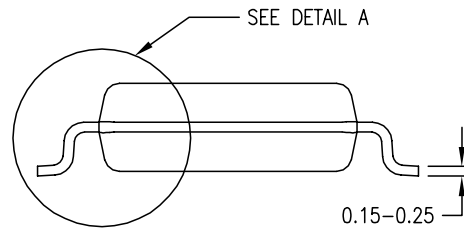
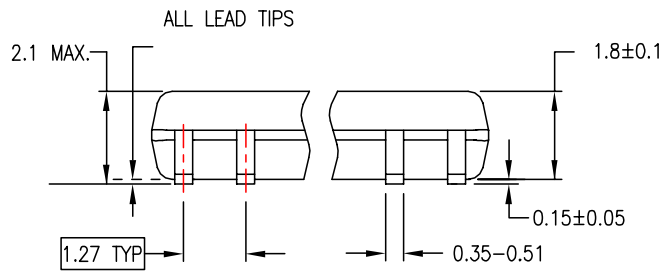
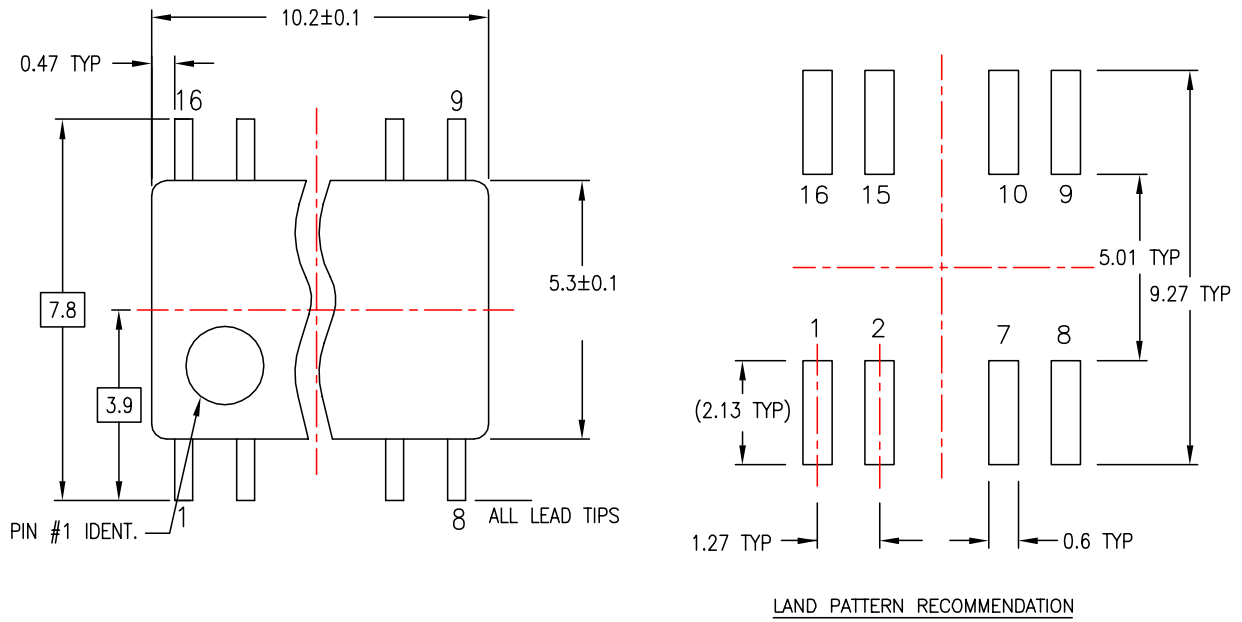
M16AREVK

**Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A**



**Physical Dimensions** (Continued)

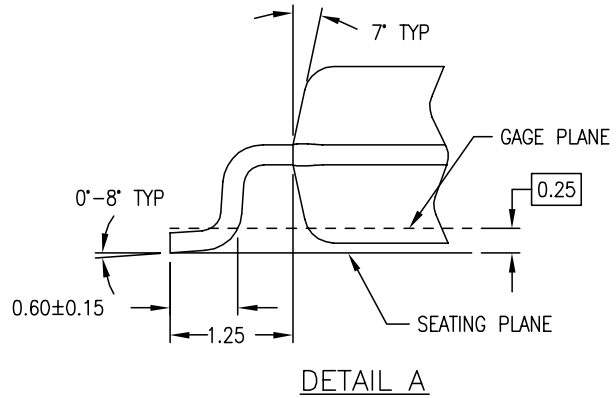
Dimensions are in millimeters unless otherwise noted.



DIMENSIONS ARE IN MILLIMETERS

NOTES:

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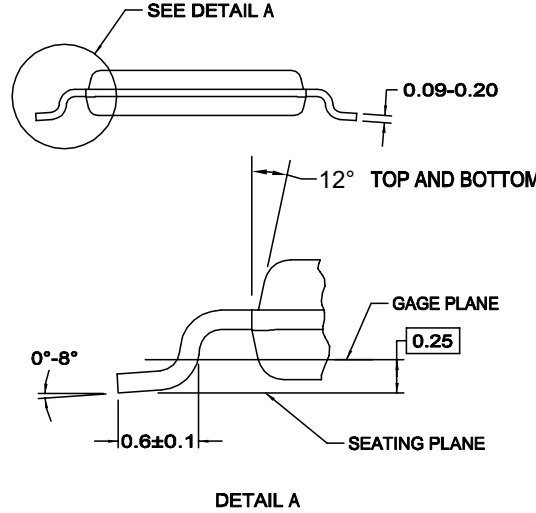
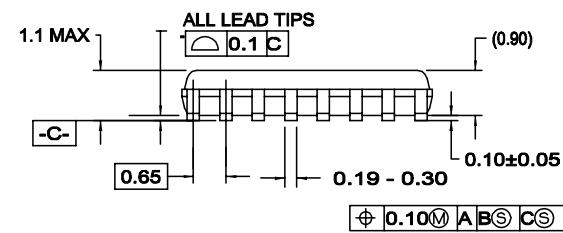
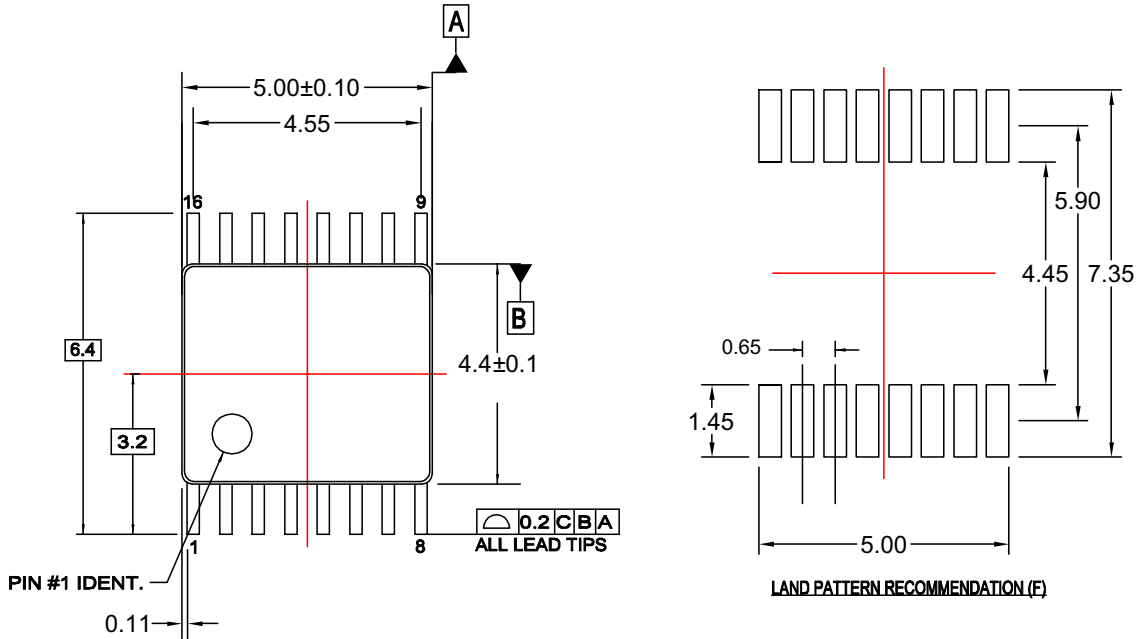


M16DREVC

**Figure 2. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D**

**Physical Dimensions** (Continued)

Dimensions are in millimeters unless otherwise noted.



- NOTES:
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  - B. DIMENSIONS ARE IN MILLIMETERS
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  - D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
  - E. DRAWING FILE NAME: MTC16REV4
  - F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N


MTC16rev4

**Figure 3. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16**



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FAST <sup>®</sup>	PDP-SPM <sup>™</sup>	SuperSOT <sup>™</sup> -6	
FASTr <sup>™</sup>	POP <sup>™</sup>	SuperSOT <sup>™</sup> -8	
FPS <sup>™</sup>	Power220 <sup>®</sup>	SyncFET <sup>™</sup>	
FRFET <sup>®</sup>	Power247 <sup>®</sup>	TCM <sup>™</sup>	
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