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**TEXAS INSTRUMENTS**

**TPS53318, TPS53319**

SLUSAY8E –JUNE 2012–REVISED NOVEMBER 2016

# TPS5331x High-Efficiency, 8-A or 14-A, Synchronous Buck Converter with Eco-mode Control

## 1 Features

- Conversion Input Voltage Range: 1.5 V to 22 V
- VDD Input Voltage Range: 4.5 V to 25 V
- 91% Efficiency from 12 V to 1.5 V at 14 A
- Output Voltage Range: 0.6 V to 5.5 V
- 5-V LDO Output
- Supports Single-Rail Input
- Integrated Power MOSFETs with 8 A (TPS53318) or 14 A (TPS53319) of Continuous Output Current
- Auto-Skip Eco-mode™ for Light-Load Efficiency
- < 110 μA Shut Down Current
- D-CAP™ Mode with Fast Transient Response
- Selectable Switching Frequency from 250 kHz to 1 MHz with External Resistor
- Selectable Auto-Skip or PWM-Only Operation
- Built-in 1% 0.6-V Reference.
- 0.7-ms, 1.4-ms, 2.8-ms and 5.6-ms Selectable Internal Voltage Servo Soft-Start
- Integrated Boost Switch
- Pre-Charged Start-Up Capability
- Adjustable Overcurrent Limit with Thermal Compensation
- Overvoltage, Undervoltage, UVLO and Over-Temperature Protection
- Supports All Ceramic Output Capacitors
- Open-Drain Power Good Indication
- Incorporates NexFET™ Power Block Technology
- 22-Pin QFN (DQP) Package with PowerPAD™

## 2 Applications

- Server/Storage
- Workstations and Desktops
- Telecommunications Infrastructure

## 3 Description

The TPS53318 and TPS53319 devices are D-CAP mode, 8-A or 14-A synchronous switchers with integrated MOSFETs. They are designed for ease of use, low external component count, and space-conscious power systems.

These devices feature accurate 1%, 0.6-V reference, and integrated boost switch. A sample of competitive features include: 1.5-V to 22-V wide conversion input voltage range, very low external component count, D-CAP™ mode control for super fast transient, auto-skip mode operation, internal soft-start control, selectable frequency, and no need for compensation.

The conversion input voltage ranges from 1.5 V to 22 V, the supply voltage range is from 4.5 V to 25 V, and the output voltage range is from 0.6 V to 5.5 V.
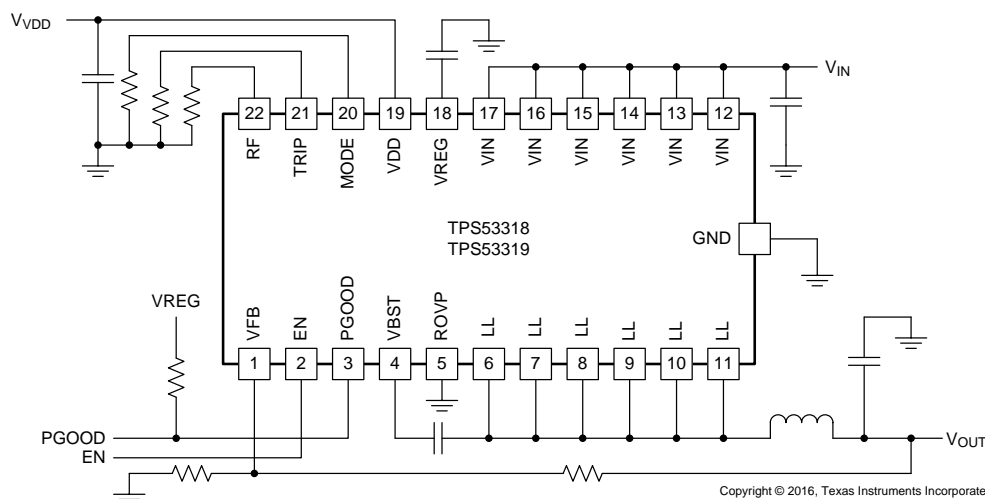
These devices are available in 5 mm x 6 mm, 22-pin QFN package and is specified from –40°C to 85°C.

### Device Information[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS53318 | LSON-CLIP (22) | 6.00 mm x 5.00 mm |
| TPS53319 | | |

(1) For all available packages, see the *Package Option Addendum* section at the end of the datasheet.

**Simplified Application**



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# 4  Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision D (February 2015) to Revision E                                    Page

- Changed Pin 19 From: ground To: $V_{IN}$ 12 V in Figure 34 ...................................................... 21

### Changes from Revision C (December 2014) to Revision D                                    Page

- Added recommendation for ROVP connection when ROVP function is not needed in *Pin Functions* table ........................ 3
- Corrected typographical error. Changed "when the VDD voltage rises above 1 V" to "when the VDD voltage rises above 2 V" in the *5-V LDO and VREG Start-Up* section. .................................................. 14
- Added *ROVP Pin Design Note* in *Redundant Overvoltage Protection (OVP)* section ........................................ 17

### Changes from Revision B (May 2013) to Revision C                                    Page

- Added *Pin Configuration and Functions* section, *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ............................ 1
- Added clarity to *Current Sense, Overcurrent and Short Circuit Protection* section ............................................... 16
- Added Table 2 .................................................................................................. 17

### Changes from Revision A (JUNE 2012) to Revision B                                    Page

- Added clarity to *Overvoltage and Undervoltage Protection* section ............................................... 17
- Updated Figure 50 ............................................................................................ 28

### Changes from Original (JUNE 2012) to Revision A                                    Page

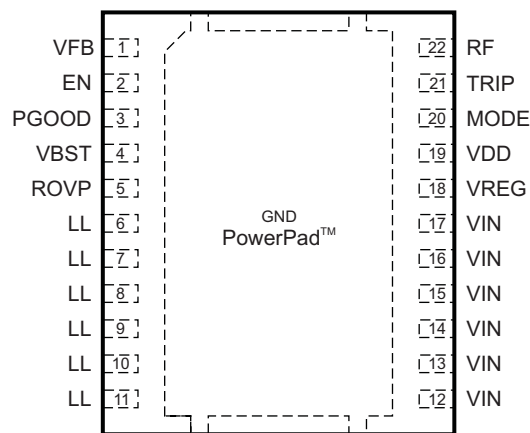- Changed "< 100 μA Shut Down Current" to "< 110 μA Shut Down Current" in Features ...................................................... 1

Product Folder Links: *TPS53318  TPS53319*

# 5  Device Comparison Table

| ORDER NUMBER[1] | OUTPUT CURRENT (A) |
|---|---|
| TPS53318DQP | 8 |
| TPS53319DQP | 14 |

(1)  For detailed ordering information see the *Package Option Addendum* section at the end of this data sheet.

# 6  Pin Configuration and Functions

**DQP (LSON-CLIP) PACKAGE**
**22 PINS**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| VFB | [1] | [22] | RF |
| EN | [2] | [21] | TRIP |
| PGOOD | [3] | [20] | MODE |
| VBST | [4] | [19] | VDD |
| ROVP | [5] | [18] | VREG |
| LL | [6] | [17] | VIN |
| LL | [7] | [16] | VIN |
| LL | [8] | [15] | VIN |
| LL | [9] | [14] | VIN |
| LL | [10] | [13] | VIN |
| LL | [11] | [12] | VIN |

GND
PowerPad™

## Pin Functions

| PIN NAME | PIN NO. | I/O/P[1] | DESCRIPTION |
|---|---|---|---|
| EN | 2 | I | Enable pin. Typical turn-on threshold voltage is 1.3 V. Typical turn-off threshold voltage is 1.0 V. |
| GND | | G | Ground and thermal pad of the device. Use proper number of vias to connect to ground plane. |
| LL | 6 | B | Output of converted power. Connect this pin to the output inductor. |
| | 7 | | |
| | 8 | | |
| | 9 | | |
| | 10 | | |
| | 11 | | |
| MODE | 20 | I | Soft-start and mode selection. Connect a resistor to select soft-start time using Table 3. The soft-start time is detected and stored into internal register during start-up. |
| PGOOD | 3 | O | Open drain power good flag. Provides 1-ms start-up delay after VFB falls in specified limits. When VFB goes out of the specified limits PGOOD goes low after a 2-µs delay |
| ROVP | 5 | I | Redundant overvoltage protection (OVP) input. Use a resistor divider to connect this pin to $V_{OUT}$. Internally pulled down to GND with 1.5-MΩ resistor. If redundant OVP is not needed, connect this pin to GND or make it float. (See *Redundant Overvoltage Protection (OVP)* section) |
| RF | 22 | I | Switching frequency selection. Connect a resistor to GND or VREG to select switching frequency using Table 1. The switching frequency is detected and stored during the startup. |
| TRIP | 21 | I | OCL detection threshold setting pin. $I_{TRIP}$ = 10 µA at room temperature, 3000 ppm/°C current is sourced and set the OCL trip voltage as follows. |
| | | | $V_{OCL} = V_{TRIP}/32$       ($V_{TRIP}$ ≤ 2.4 V, $V_{OCL}$ ≤ 75 mV) |

(1)  I = Input, O = Output, B = Bidirectional, P = Supply, G = Ground

*Submit Documentation Feedback*

## Pin Functions (continued)

| PIN | | I/O/P[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| VBST | 4 | P | Supply input for high-side FET gate driver (boost terminal). Connect capacitor from this pin to LL node. Internally connected to VREG via bootstrap MOSFET switch. |
| VDD | 19 | P | Controller power supply input. VDD input voltage range is from 4.5 V to 25 V. |
| VFB | 1 | I | Output feedback input. Connect this pin to $V_{OUT}$ through a resistor divider. |
| VIN | 12 | P | Conversion power input. The conversion input voltage range is from 1.5 V to 22 V. |
| | 13 | | |
| | 14 | | |
| | 15 | | |
| | 16 | | |
| | 17 | | |
| VREG | 18 | P | 5-V low drop out (LDO) output. Supplies the internal analog circuitry and driver circuitry. |
| Thermal Pad | | G | Ground and thermal pad of the device. Use proper number of vias to connect to ground plane. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings[1]

| | | | VALUE | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| Input voltage range | VIN (main supply) | | −0.3 | 30 | V |
| | VDD | | −0.3 | 28 | |
| | VBST | | −0.3 | 32 | |
| | VBST (with respect to LL) | | −0.3 | 7 | |
| | EN, MODE, TRIP, RF, ROVP, VFB | | −0.3 | 7 | |
| Output voltage range | LL | DC | −2 | 30 | V |
| | | Pulse < 20ns, E = 5 μJ | −7 | 32 | |
| | PGOOD, VREG | | −0.3 | 7 | |
| | GND | | −0.3 | 0.3 | |
| Source/Sink current | VBST | | 50 | | mA |
| Operating free-air temperature, $T_A$ | | | −40 | 85 | °C |
| Junction temperature range, $T_J$ | | | −40 | 150 | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | | | 300 | |
| Storage temperature, $T_{stg}$ | | | −55 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

Product Folder Links: *TPS53318  TPS53319*

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage range | VIN (main supply) | 1.5 | 22 | V |
|  | VDD | 4.5 | 25 |  |
|  | VBST | 4.5 | 28 |  |
|  | VBST (with respect to LL) | 4.5 | 6.5 |  |
|  | EN, MODE, TRIP, RF, ROVP, VFB | −0.1 | 6.5 |  |
| Output voltage range | LL | −1 | 27 | V |
|  | PGOOD, VREG | −0.1 | 6.5 |  |
| Junction temperature range, $T_J$ |  | −40 | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC[1] | | TPS53318 TPS53319 | UNIT |
|---|---|---|---|
| | | DQP | |
| | | 22 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 27.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 17.1 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 5.9 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.8 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 5.8 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.2 | |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Electrical Characteristics

Over recommended free-air temperature range, $V_{VDD}$ = 12 V (unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $V_{VIN}$ | VIN pin power conversion input voltage | | 1.5 | | 22 | V |
| $V_{VDD}$ | Supply input voltage | | 4.5 | | 25.0 | V |
| $I_{VIN(leak)}$ | VIN pin leakage current | $V_{EN}$ = 0 V | | | 1 | µA |
| $I_{VDD}$ | VDD supply current | $T_A$ = 25°C, No load, $V_{EN}$ = 5 V, $V_{VFB}$ = 0.630 V | | 420 | 590 | µA |
| $I_{VDDSDN}$ | VDD shutdown current | $T_A$ = 25°C, No load, $V_{EN}$ = 0 V | | | 110 | µA |
| **INTERNAL REFERENCE VOLTAGE** | | | | | | |
| $V_{VFB}$ | VFB regulation voltage | CCM condition[1] | | 0.600 | | V |
| $V_{VFB}$ | VFB regulation voltage | $T_A$ = 25°C | 0.597 | 0.600 | 0.603 | V |
| | | 0°C ≤ $T_A$ ≤ 85°C | 0.5952 | 0.600 | 0.6048 | |
| | | −40°C ≤ $T_A$ ≤ 85°C | 0.594 | 0.600 | 0.606 | |
| $I_{VFB}$ | VFB input current | $V_{VFB}$ = 0.630 V, $T_A$ = 25°C | | 0.01 | 0.20 | µA |
| **LDO OUTPUT** | | | | | | |
| $V_{VREG}$ | LDO output voltage | 0 mA ≤ $I_{VREG}$ ≤ 30 mA | 4.77 | 5.00 | 5.36 | V |
| $I_{VREG}$ | LDO output current[1] | Maximum current allowed from LDO | | | 30 | mA |
| $V_{DO}$ | Low drop out voltage | $V_{VDD}$ = 4.5 V, $I_{VREG}$ = 30 mA | | | 250 | mV |
| **BOOT STRAP SWITCH** | | | | | | |
| $V_{FBST}$ | Forward voltage | $V_{VREG-VBST}$, $I_F$ = 10 mA, $T_A$ = 25°C | | 0.1 | 0.2 | V |
| $I_{VBSTLK}$ | VBST leakage current | $V_{VBST}$ = 23 V, $V_{SW}$ = 17 V, $T_A$ = 25°C | | 0.01 | 1.50 | µA |

(1) Ensured by design. Not production tested.

## Electrical Characteristics (continued)

Over recommended free-air temperature range, $V_{VDD}$ = 12 V (unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DUTY AND FREQUENCY CONTROL** | | | | | | |
| $t_{OFF(min)}$ | Minimum off-time | $T_A$ = 25°C | 150 | 260 | 400 | ns |
| $t_{ON(min)}$ | Minimum on-time | $V_{IN}$ = 17 V, $V_{OUT}$ = 0.6 V, $f_{SW}$ = 1 MHz, $T_A$ = 25 °C [1] | | 35 | | ns |
| **SOFT-START TIMING** | | | | | | |
| $t_{SS}$ | Internal soft-start time from $V_{OUT}$ = 0 V to 95% of $V_{OUT}$ | $R_{MODE}$ = 39 kΩ | | 0.7 | | ms |
| | | $R_{MODE}$ = 100 kΩ | | 1.4 | | |
| | | $R_{MODE}$ = 200 kΩ | | 2.8 | | |
| | | $R_{MODE}$ = 470 kΩ | | 5.6 | | |
| **OUTPUT VOLTAGE DISCHARGE** | | | | | | |
| $I_{DSCHG}$ | Output voltage discharge current | $V_{EN}$ = 0 V, $V_{SW}$ = 0.5 V | 5.0 | 6.6 | 9.0 | mA |
| **POWERGOOD** | | | | | | |
| $V_{THPG}$ | PG threshold | PG in from lower | 92.5% | 95.0% | 98.5% | |
| | | PG in from higher | 107.5% | 110.0% | 112.5% | |
| | | PG hysteresis | 2.5% | 5.0% | 7.5% | |
| $R_{PG}$ | PG transistor on-resistance | | 15 | 30 | 60 | Ω |
| $t_{PGDEL}$ | PG delay | Delay for PG in | 0.8 | 1 | 1.2 | ms |
| **LOGIC THRESHOLD AND SETTING CONDITIONS** | | | | | | |
| $V_{EN}$ | EN Voltage | Enable | 1.0 | 1.3 | 1.6 | V |
| | | Disable | 0.8 | 1.0 | 1.2 | |
| $I_{EN}$ | EN Input current | $V_{EN}$ = 5 V | | | 1.0 | µA |
| $f_{SW}$ | Switching frequency | $R_{RF}$ = 0 Ω to GND, $T_A$ = 25°C [2] | 200 | 250 | 300 | kHz |
| | | $R_{RF}$ = 187 kΩ to GND, $T_A$ = 25°C [2] | 250 | 300 | 350 | |
| | | $R_{RF}$ = 619 kΩ, to GND, $T_A$ = 25°C [2] | 350 | 400 | 450 | |
| | | $R_{RF}$ = Open, $T_A$ = 25°C [2] | 450 | 500 | 550 | |
| | | $R_{RF}$ = 866 kΩ to VREG, $T_A$ = 25°C [2] | 540 | 600 | 660 | |
| | | $R_{RF}$ = 309 kΩ to VREG, $T_A$ = 25°C [2] | 670 | 750 | 820 | |
| | | $R_{RF}$ = 124 kΩ to VREG, $T_A$ = 25°C [2] | 770 | 850 | 930 | |
| | | $R_{RF}$ = 0 Ω to VREG, $T_A$ = 25°C [2] | 880 | 970 | 1070 | |
| **PROTECTION: CURRENT SENSE** | | | | | | |
| $I_{TRIP}$ | TRIP source current | $V_{TRIP}$ = 1 V, $T_A$ = 25°C | | 10 | | µA |
| $TC_{ITRIP}$ | TRIP current temperature coefficient | On the basis of 25°C [2] | | 3000 | | ppm/°C |
| $V_{TRIP}$ | Current limit threshold setting range | TPS53318 | $V_{TRIP-GND}$ | 0.4 | | 1.5 | V |
| | | TPS53319 | | | 2.4 | |
| $V_{OCL}$ | Current limit threshold | $V_{TRIP}$ = 1.2 V | 37.5 | | | mV |
| | | $V_{TRIP}$ = 0.4 | | 12.5 | | |
| $V_{OCLN}$ | Negative current limit threshold | $V_{TRIP}$ = 1.2 V | | −37.5 | | mV |
| | | $V_{TRIP}$ = 0.4 V | | −12.5 | | |
| $I_{OCP}$ | Valley current limit threshold | $R_{TRIP}$ = 66.5 kΩ, 0°C ≤ $T_A$ ≤ 125°C | 4.6 | 5.4 | 6.3 | A |
| | | $R_{TRIP}$ = 66.5 kΩ, −40°C ≤ $T_A$ ≤ 125°C | 4.4 | 5.4 | 6.3 | |
| $V_{AZCADJ}$ | Auto zero cross adjustable range | Positive | 3 | 15 | | mV |
| | | Negative | | −15 | −3 | |

(2) Not production tested. Test condition is $V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, $I_{OUT}$ = 5 A using application circuit shown in Figure 45.

Product Folder Links: *TPS53318  TPS53319*

## Electrical Characteristics (continued)

Over recommended free-air temperature range, $V_{VDD}$ = 12 V (unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **PROTECTION: UVP and OVP** | | | | | | |
| $V_{OVP}$ | OVP trip threshold | OVP detect | 115% | 120% | 125% | |
| $t_{OVPDEL}$ | OVP propagation delay | VFB delay with 50-mV overdrive | | 1 | | µs |
| $V_{UVP}$ | Output UVP trip threshold | UVP detect | 65% | 70% | 75% | |
| $t_{UVPDEL}$ | Output UVP propagation delay | | 0.8 | 1.0 | 1.2 | ms |
| $t_{UVPEN}$ | Output UVP enable delay | From enable to UVP workable | 1.5 | 2.3 | 3.0 | ms |
| **UVLO** | | | | | | |
| $V_{UVVREG}$ | VREG UVLO threshold | Wake up | 4.00 | 4.20 | 4.33 | V |
| | | Hysteresis | | 0.25 | | |
| **PROTECTION: UVP and OVP** | | | | | | |
| $V_{OVP}$ | OVP trip threshold | OVP detect | 115% | 120% | 125% | |
| $t_{OVPDEL}$ | OVP propagation delay | VFB delay with 50-mV overdrive | | 1 | | µs |
| $V_{UVP}$ | Output UVP trip threshold | UVP detect | 65% | 70% | 75% | |
| $t_{UVPDEL}$ | Output UVP proprogation delay | | 0.8 | 1.0 | 1.2 | ms |
| $t_{UVPEN}$ | Output UVP enable delay | From enable to UVP workable | 1.5 | 2.3 | 3.0 | ms |
| **UVLO** | | | | | | |
| $V_{UVVREG}$ | VREG UVLO threshold | Wake up | 4.00 | 4.20 | 4.33 | V |
| | | Hysteresis | | 0.25 | | |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SDN}$ | Thermal shutdown threshold | Shutdown temperature[2] | | 145 | | °C |
| | | Hysteresis[2] | | 10 | | |

## 7.6 Typical Characteristics
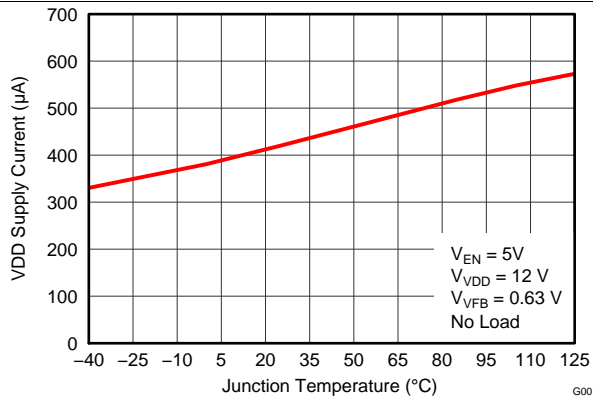


**Figure 1. VDD Supply Current vs. Junction Temperature**

$V_{EN}$ = 5V
$V_{VDD}$ = 12 V
$V_{VFB}$ = 0.63 V
No Load
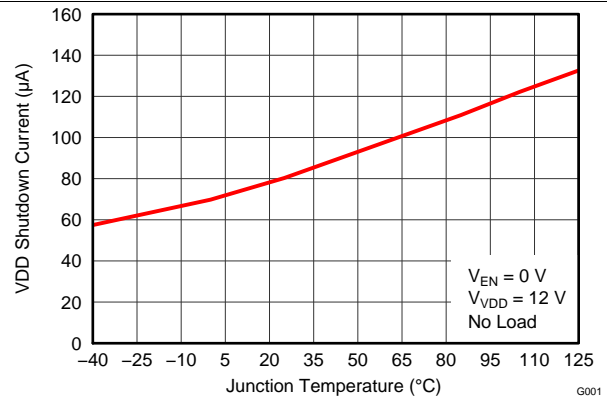


**Figure 2. VDD Shutdown Current vs. Junction Temperature**

$V_{EN}$ = 0 V
$V_{VDD}$ = 12 V
No Load
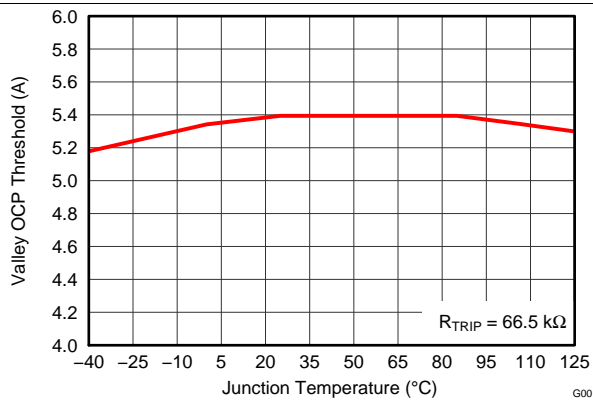


**Figure 3. Valley OCP Threshold vs Temperature**

$R_{TRIP}$ = 66.5 kΩ
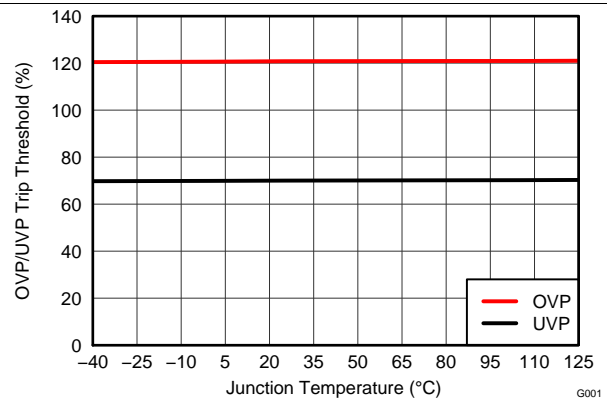


**Figure 4. OVP/UVP Trip Threshold vs. Junction Temperature**

OVP
UVP
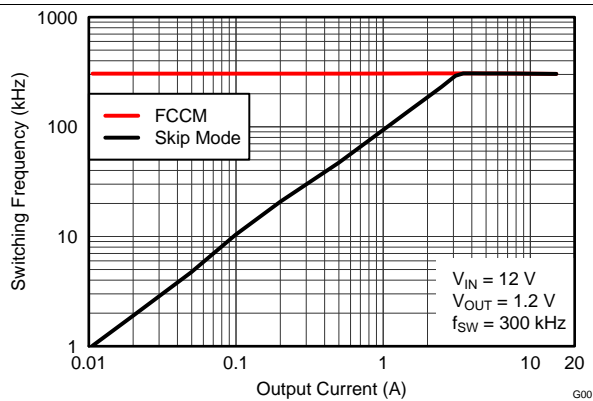


**Figure 5. Switching Frequency vs. Output Current**

FCCM
Skip Mode

$V_{IN}$ = 12 V
$V_{OUT}$ = 1.2 V
$f_{SW}$ = 300 kHz
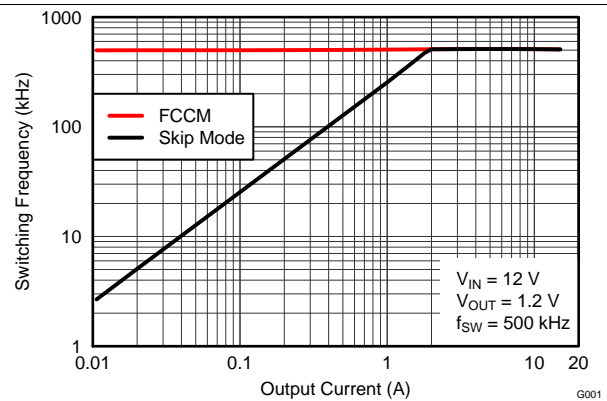


**Figure 6. Switching Frequency vs. Output Current**

FCCM
Skip Mode

$V_{IN}$ = 12 V
$V_{OUT}$ = 1.2 V
$f_{SW}$ = 500 kHz

Product Folder Links: *TPS53318  TPS53319*

## Typical Characteristics (continued)



**Figure 7. Switching Frequency vs. Output Current**
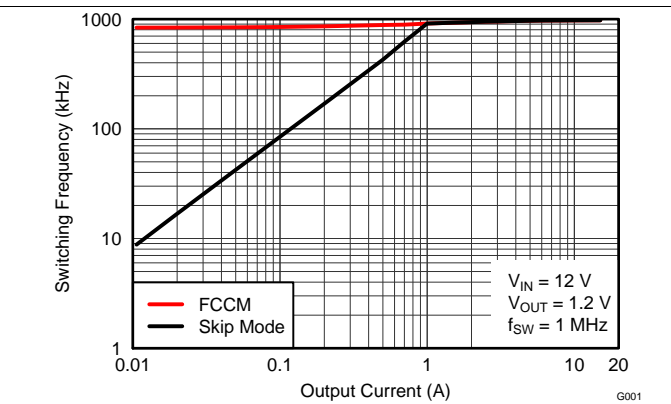


**Figure 8. Switching Frequency vs. Output Current**
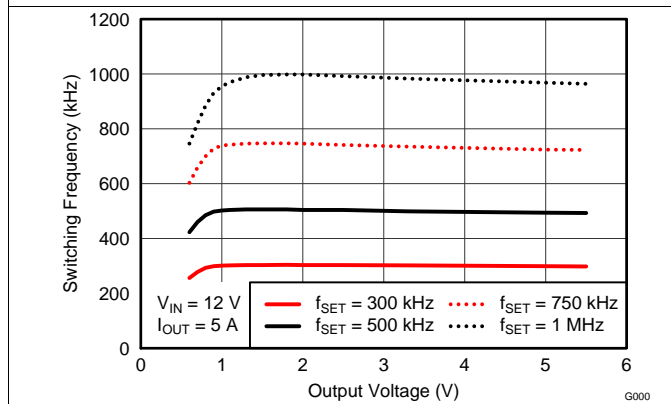


**Figure 9. Switching Frequency vs. Output Voltage**
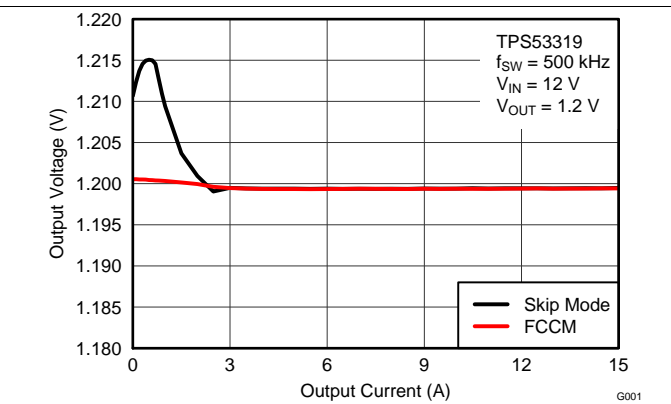


**Figure 10. Output Voltage vs. Output Current**
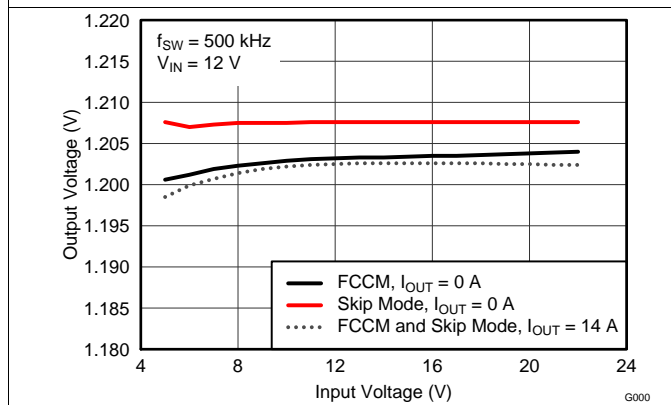


**Figure 11. Output Voltage vs. Input Voltage**
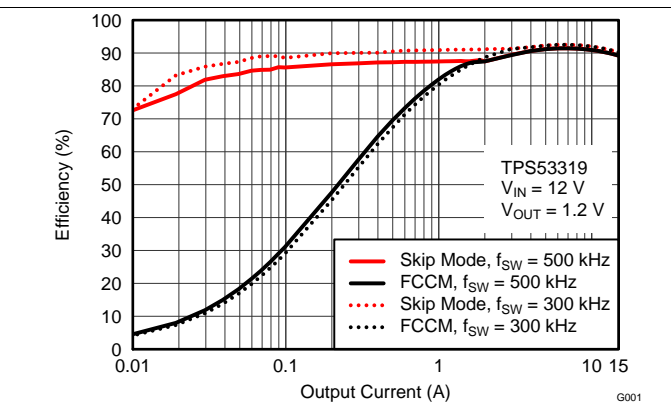


**Figure 12. Efficiency vs Output Current**

## Typical Characteristics (continued)
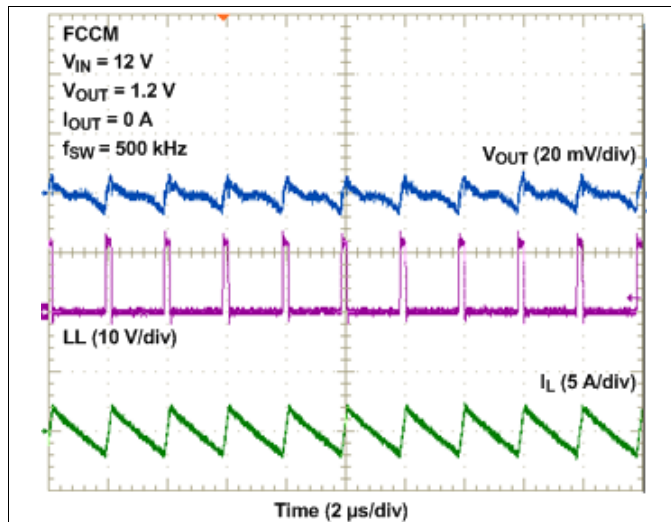


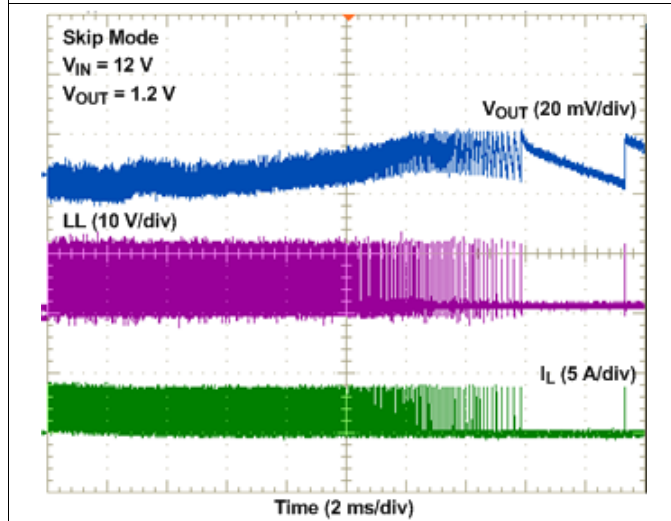**Figure 13. 1.2-V Output FCCM Mode Steady-State Operation**
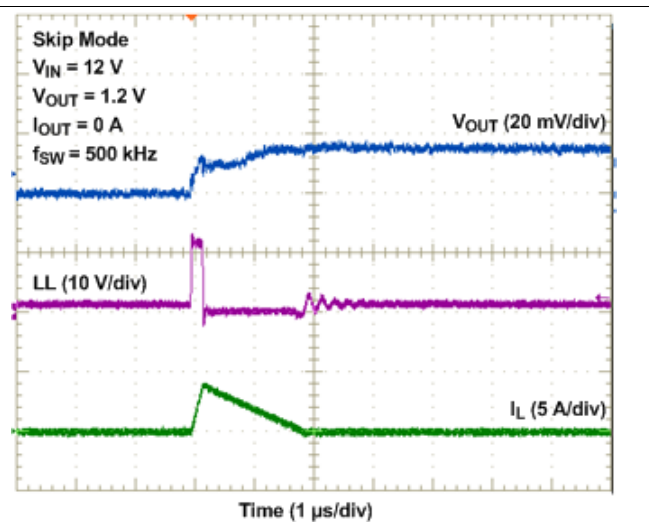


**Figure 14. 1.2-V Output Skip Mode Steady-State Operation**



**Figure 15. CCM to DCM Transition**
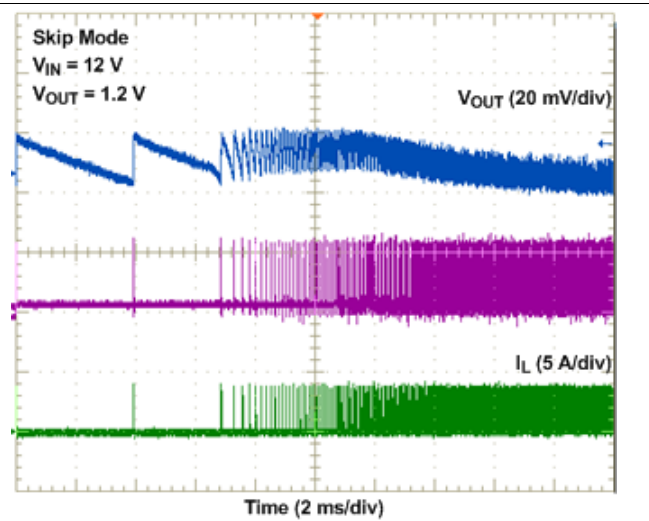


**Figure 16. DCM to CCM Transition**
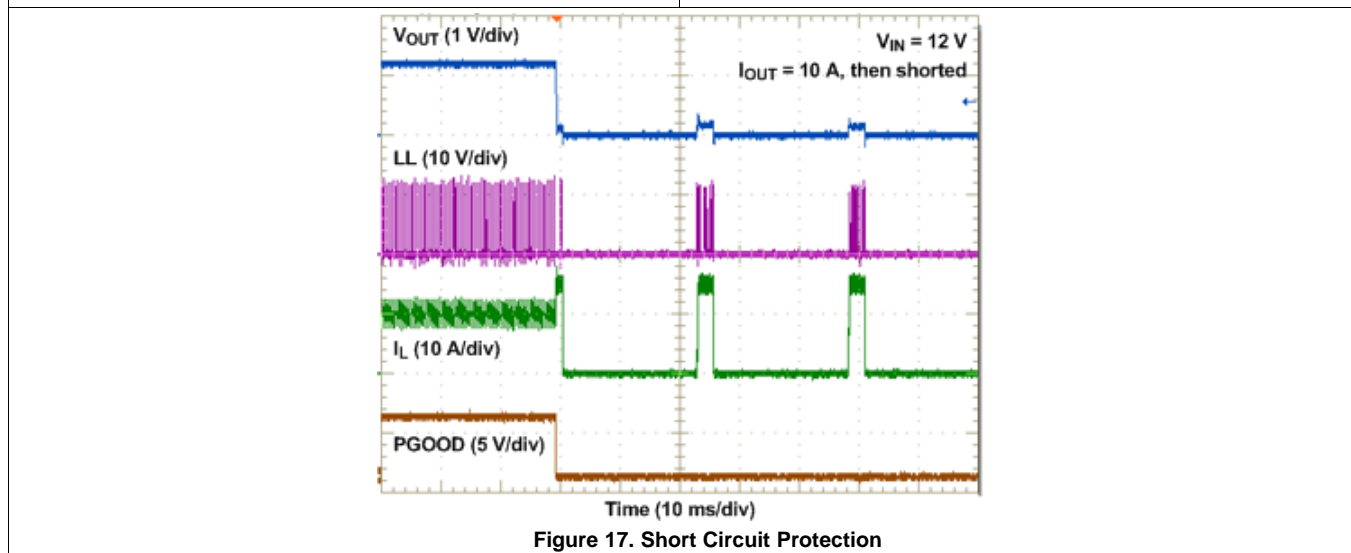


**Figure 17. Short Circuit Protection**

Product Folder Links: *TPS53318  TPS53319*

## 7.7 TPS53319 Typical Characteristics
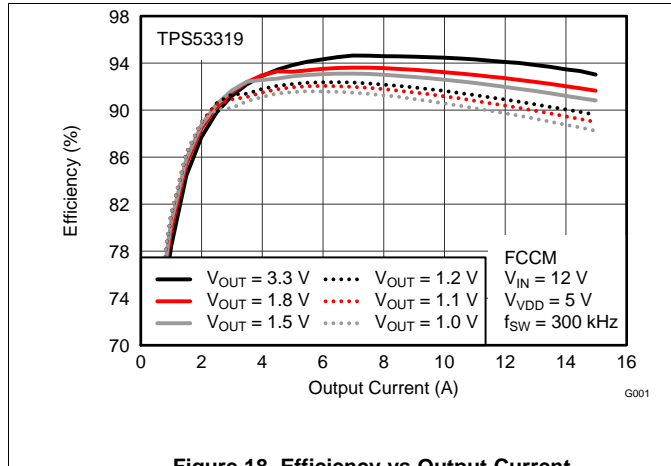


**Figure 18. Efficiency vs Output Current**
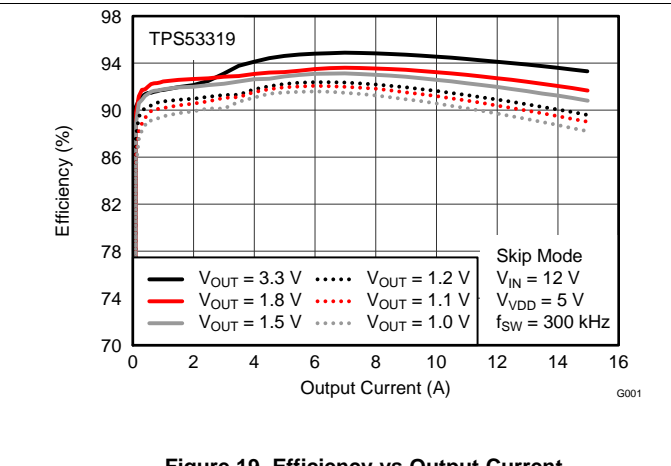


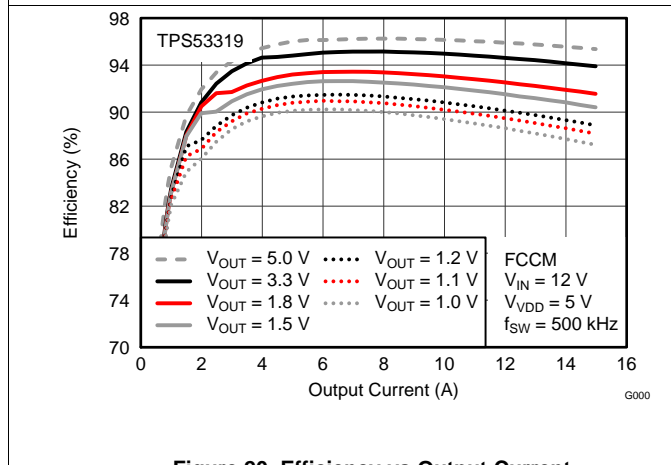**Figure 19. Efficiency vs Output Current**



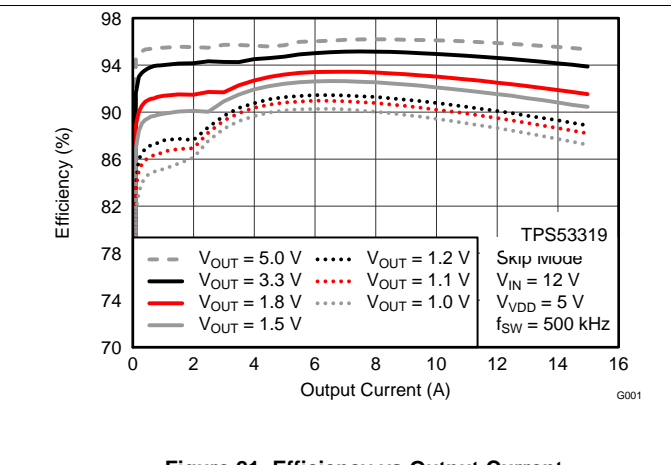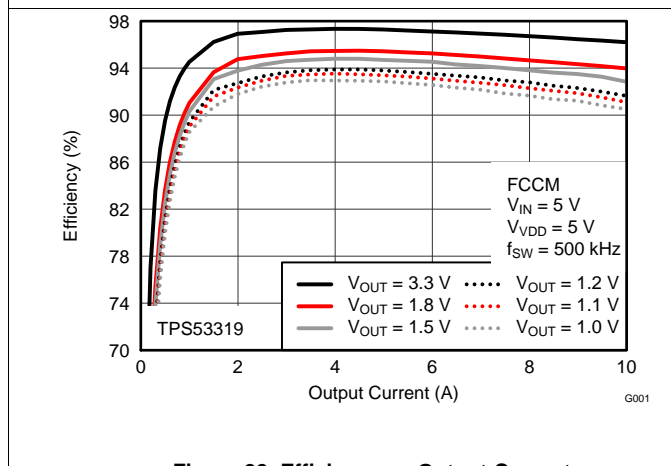**Figure 20. Efficiency vs Output Current**



**Figure 21. Efficiency vs Output Current**



**Figure 22. Efficiency vs Output Current**
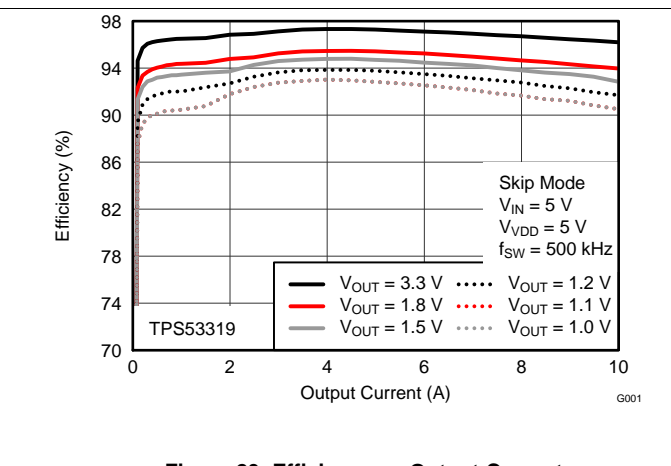


**Figure 23. Efficiency vs Output Current**

Product Folder Links: *TPS53318  TPS53319*

## 7.8 TPS53318 Typical Characteristics



**Figure 24. Efficiency vs Output Current**



**Figure 25. Efficiency vs Output Current**



**Figure 26. Efficiency vs Output Current**



**Figure 27. Efficiency vs Output Current**



**Figure 28. Efficiency vs Output Current**
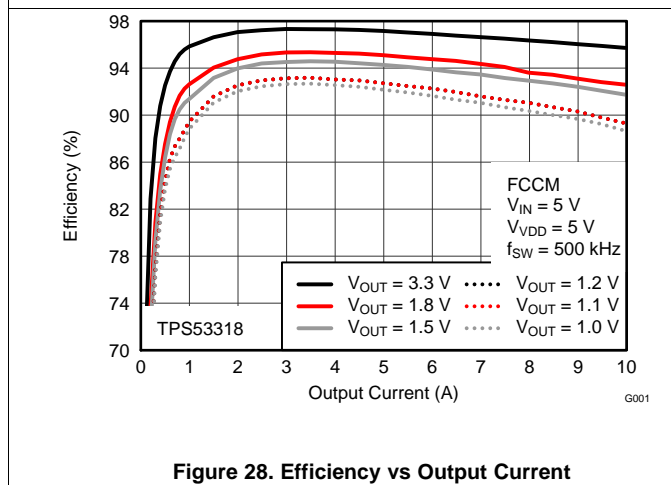


**Figure 29. Efficiency vs Output Current**

Product Folder Links: *TPS53318  TPS53319*
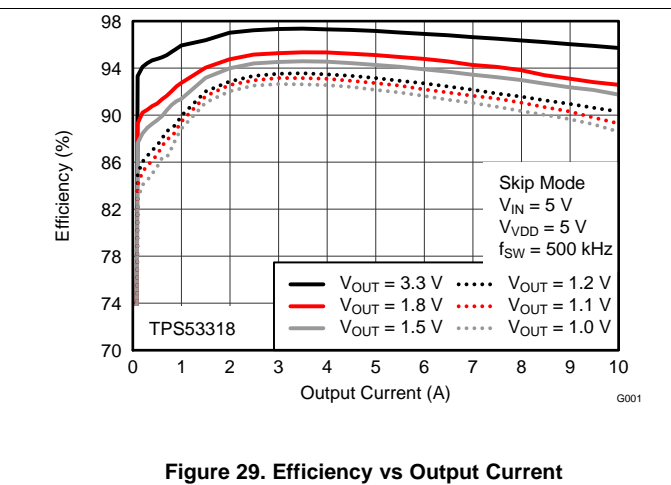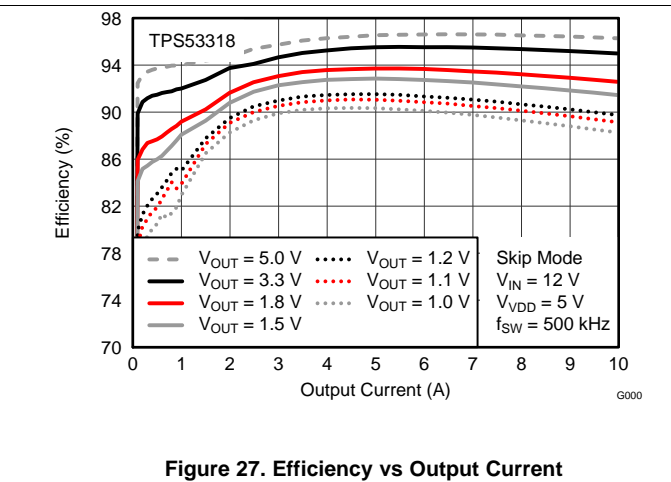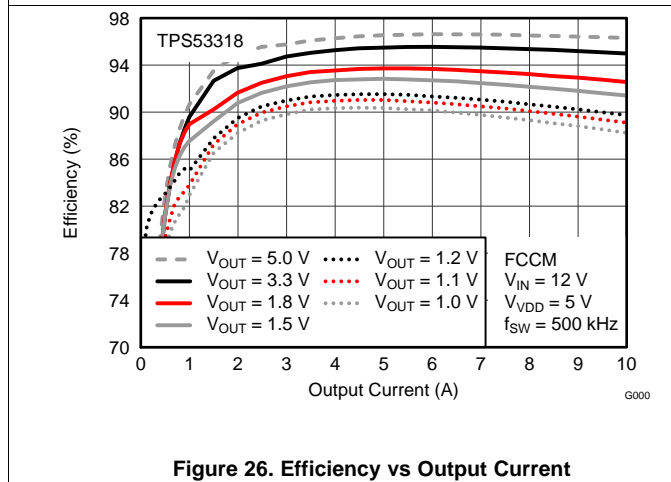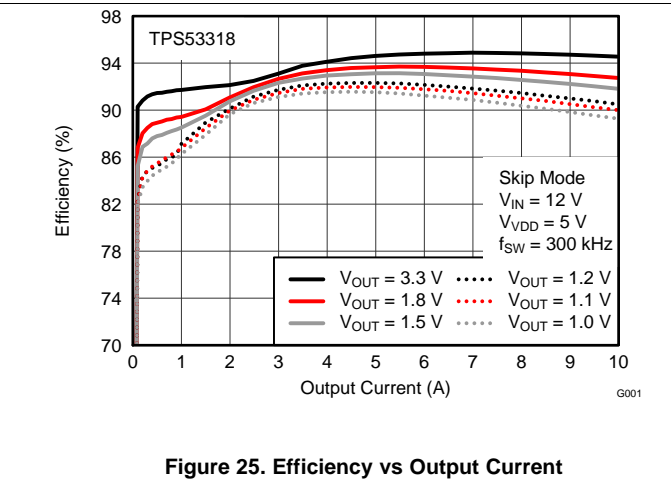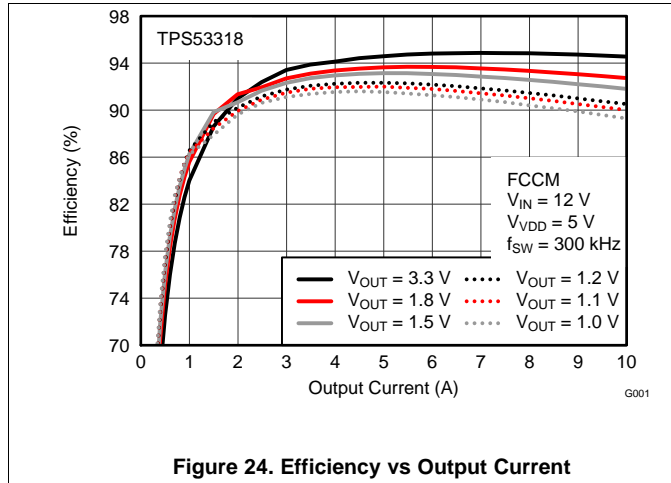
# 8 Detailed Description

## 8.1 Overview

The TPS53318 and TPS53319 devices are high-efficiency, single channel, synchronous buck converters suitable for low output voltage point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP™ mode control combined with an adaptive on-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC-DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 1.5 V to 22 V and the VDD bias voltage is from 4.5 V to 25 V. The D-CAP™ mode uses the equivalent series resistance (ESR) of the output capacitor(s) to sense the device current. One advantage of this control scheme is that it does not require an external phase compensation network. This allows a simple design with a low external component count. Eight preset switching frequency values can be chosen using a resistor connected from the RF pin to ground or VREG. Adaptive on-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

These devices have a MODE pin to select between auto-skip mode and forced continuous conduction mode (FCCM) for light load conditions. The MODE pin also sets the selectable soft-start time ranging from 0.7 ms to 5.6 ms as shown in Table 3.

## 8.2 Functional Block Diagram
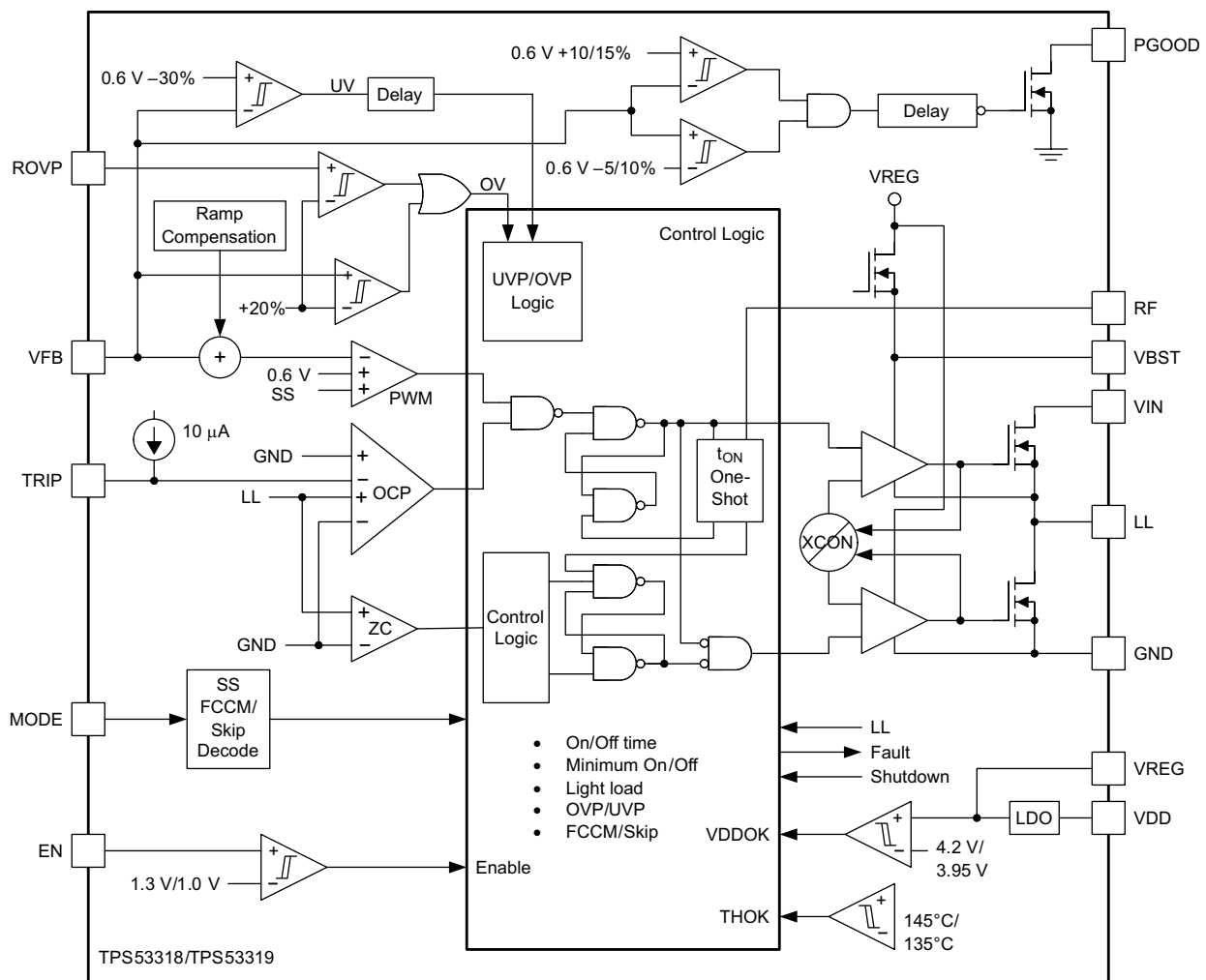


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(1) The thresholds shown in the *Functional Block Diagram* are typical values. Refer to the *Electrical Characteristics* table for threshold tolerance specifications.

Product Folder Links: *TPS53318  TPS53319*

## 8.3 Feature Description

### 8.3.1 5-V LDO and VREG Start-Up

Both the TPS53318 and TPS53319 devices provide an internal 5-V LDO function using input from VDD and output to VREG. When the VDD voltage rises above 2 V, the internal LDO is enabled and outputs voltage to the VREG pin. The VREG voltage provides the bias voltage for the internal analog circuitry and also provides the supply voltage for the gate drives.
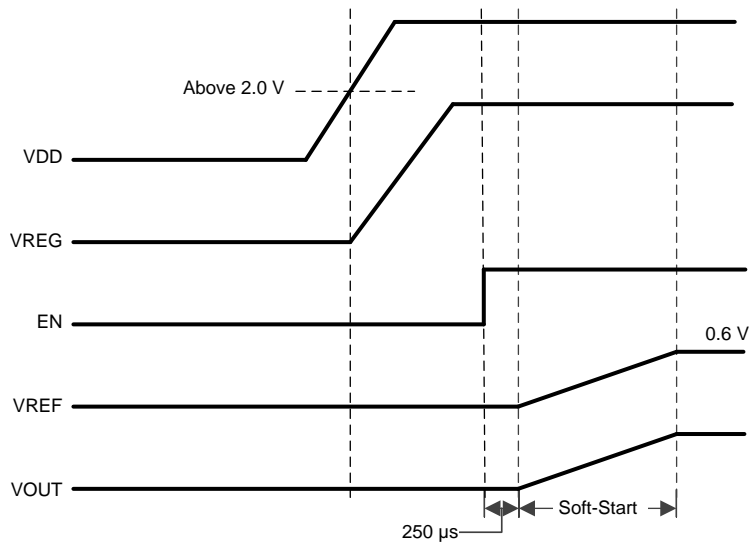


**Figure 30. Power-Up Sequence Voltage Waveforms**

**NOTE**
The 5-V LDO is not controlled by the EN pin. The LDO starts-up any time VDD rises to approximately 2 V. (see Figure 30).

### 8.3.2 Adaptive On-Time D-CAP™ Control and Frequency Selection

Neither the TPS53318 nor the TPS53319 device has a dedicated oscillator to determine switching frequency. However, the device operates with pseudo-constant frequency by feed-forwarding the input and output voltages into the on-time one-shot timer. The adaptive on-time control adjusts the on-time to be inversely proportional to the input voltage and proportional to the output voltage as shown in Equation 1.

$$t_{ON} \propto \frac{V_{OUT}}{V_{IN}}$$

(1)

This makes the switching frequency fairly constant in steady state conditions over a wide input voltage range. The switching frequency is selectable from eight preset values by a resistor connected between the RF pin and GND or between the RF pin and the VREG pin as shown in Table 1. Maintaining open resistance sets the switching frequency to 500 kHz.

**Table 1. Resistor and Switching Frequency**

| RESISTOR (R$_{RF}$) CONNECTIONS | | SWITCHING FREQUENCY (f$_{SW}$) (kHz) |
|---|---|---|
| VALUE (kΩ) | CONNECT TO | |
| 0 | GND | 250 |
| 187 | GND | 300 |
| 619 | GND | 400 |
| OPEN | n/a | 500 |
| 866 | VREG | 600 |
| 309 | VREG | 750 |
| 124 | VREG | 850 |
| 0 | VREG | 970 |

The off-time is modulated by a PWM comparator. The VFB node voltage (the mid-point of resistor divider) is compared to the internal 0.6-V reference voltage added with a ramp signal. When both signals match, the PWM comparator asserts a set signal to terminate the off time (turn off the low-side MOSFET and turn on high-side MOSFET). The set signal is valid if the inductor current level is below the OCP threshold, otherwise the off time is extended until the current level falls below the threshold.

The waveforms shown in Figure 31 show on-time control without ramp compensation. The waveforms shown in Figure 32 show on-time control without ramp compensation.
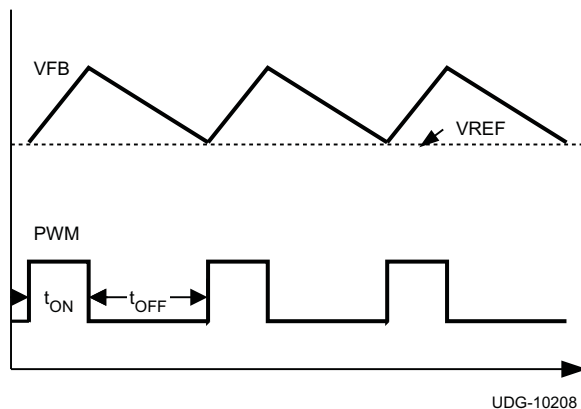


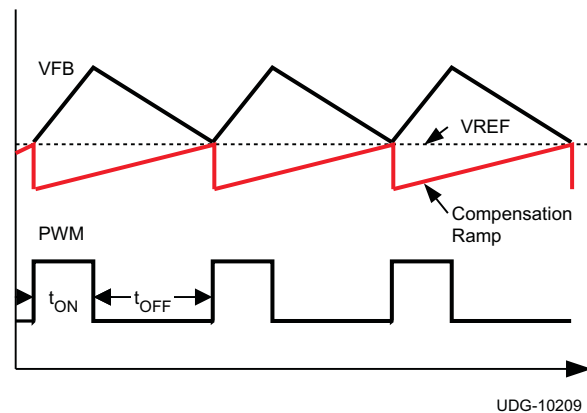**Figure 31. On-Time Control Without Ramp Compensation**



**Figure 32. On-Time Control With Ramp Compensation**

### 8.3.3 Ramp Signal

The TPS53318 and TPS53319 devices add a ramp signal to the 0.6-V reference in order to improve jitter performance. As described in the previous section, the feedback voltage is compared with the reference information to keep the output voltage in regulation. By adding a small ramp signal to the reference, the signal-to-noise ratio at the onset of a new switching cycle is improved. Therefore the operation becomes less jittery and more stable. The ramp signal is controlled to start with –7 mV at the beginning of an on-cycle and becomes 0 mV at the end of an off-cycle in steady state.

During skip mode operation, under discontinuous conduction mode (DCM), the switching frequency is lower than the nominal frequency and the off-time is longer than the off-time in CCM. Because of the longer off-time, the ramp signal extends after crossing 0 mV. However, it is clamped at 3 mV to minimize the DC offset.

### 8.3.4 Adaptive Zero Crossing

The TPS53318 and TPS53319 devices have an adaptive zero crossing circuit which performs optimization of the zero inductor current detection at skip mode operation. This function pursues ideal low-side MOSFET turning off timing and compensates inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. It prevents SW-node swing-up caused by too late detection and minimizes diode conduction period caused by too early detection. As a result, better light load efficiency is delivered.

### 8.3.5 Output Discharge Control

When the EN pin becomes low, the TPS53318 and TPS53319 devices discharge the output capacitor using the internal MOSFET connected between the SW pin and the PGND pin while the high-side and low-side MOSFETs are maintained in the OFF state. The typical discharge resistance is 75 Ω. The soft discharge occurs only as EN becomes low. The discharge circuit is powered by VDD. While VDD remains high, the discharge circuit remains active.

### 8.3.6 Power-Good

The TPS53318 and TPS53319 devices have power-good output that indicates high when switcher output is within the target. The power-good function is activated after soft-start has finished. If the output voltage becomes within +10% and –5% of the target value, internal comparators detect power-good state and the power-good signal becomes high after a 1-ms internal delay. If the output voltage goes outside of +15% or –10% of the target value, the power-good signal becomes low after two microsecond (2-$\mu$s) internal delay. The power-good output is an open drain output and must be pulled up externally.

The power-good MOSFET is powered through the VDD pin. $V_{VDD}$ must be >1 V in order to have a valid power-good logic. It is recommended to pull PGOOD up to VREG (or a voltage divided from VREG).

### 8.3.7 Current Sense, Overcurrent and Short Circuit Protection

The TPS53318 and TPS53319 device offer cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the OFF state and the controller maintains the OFF state during the period in that the inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost effective solution, TPS53319 device supports temperature compensated MOSFET $R_{DS(on)}$ sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor, $R_{TRIP}$. The TRIP terminal sources current ($I_{TRIP}$) which is 10 $\mu$A typically at room temperature, and the trip level is set to the OCL trip voltage $V_{TRIP}$ as shown in Equation 2.

$$V_{TRIP}\,(mV) = R_{TRIP}\,(k\Omega) \times I_{TRIP}\,(\mu A)$$

(2)

The inductor current is monitored by the LL pin. The GND pin is used as the positive current sensing node and the LL pin is used as the negative current sense node. The trip current, $I_{TRIP}$ has a 3000ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. For each device, $I_{TRIP}$ is also adjusted based on the device-specific on-resistance measurement in production tests to eliminate the any OCP variation from device to device. Duty-cycle should not be over 45% in order to provide the most accurate OCP.

As the comparison is made during the OFF state, $V_{TRIP}$ sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, $I_{OCP}$, can be calculated as shown in Equation 3.

$$I_{OCP} = \frac{V_{TRIP}}{\left(32 \times R_{DS(on)}\right)} + \frac{I_{IND(ripple)}}{2} = \frac{R_{TRIP}}{12.3 \times 10^3} + \frac{1}{2 \times L \times f_{SW}} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}}$$

where

- $R_{TRIP}$ is in k$\Omega$ (3)

In an overcurrent or short-circuit condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to decrease. Eventually, it crosses the undervoltage protection threshold and shuts down. After a hiccup delay (16 ms plus 0.7 ms soft-start period), the controller restarts. If the overcurrent condition remains, the procedure is repeated and the device enters hiccup mode.

$$t_{HIC(wait)} = \left(2^n + 257\right) \times 4\,\mu s$$

where

- n = 8, 9, 10, or 11 depending on soft-start time selection (4)

$$t_{HIC(dly)} = 7 \times \left(2^n + 257\right) \times 4\,\mu s$$

(5)

**Table 2. Hiccup Timing**

| SELECTED SOFT-START TIME ($t_{SS}$)(ms) | HICCUP WAIT TIME ($t_{HIC(wait)}$)(ms) | HICCUP DELAY TIME ($t_{HIC(delay)}$)(ms) |
|---|---|---|
| 0.7 | 2.052 | 14.364 |
| 1.4 | 3.076 | 21.532 |
| 2.8 | 5.124 | 35.868 |
| 5.6 | 9.220 | 64.540 |

For the TPS53318 device, the OCP threshold is internally clamped to 10.5 A. The recommended $R_{TRIP}$ value for the TPS53318 device is less than 150 kΩ.

### 8.3.8 Overvoltage and Undervoltage Protection

The TPS53318 and TPS53319 devices monitor the resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, the device latches OFF both high-side and low-side MOSFETs drivers. The controller restarts after a hiccup delay (refer to Table 2). This function is enabled 1.5-ms after the soft-start is completed.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and latches ON the low-side MOSFET driver. The output voltage decreases. Before the latch-off action for both the high-side and low-side drivers, the output voltage must be pulled down below the UVP threshold voltage for a period of 1 ms. After the 1 ms period, the drivers are latched off.

### 8.3.9 Redundant Overvoltage Protection (OVP)

The TPS53318 and TPS53319 devices have a redundant input for OVP protection. The ROVP pin senses the voltage divided from output voltage and sends it to the OVP comparator. If this voltage is higher than 120% of the target voltage, the overvoltage protection engages and the low-side FET is turned on. When the output voltage is lower than the UVP threshold then the device latches off.

This redundant OVP function typically protects against a situation where the feedback loop is open or where a VFB pin short to GND exists. The ROVP pin has an internal 1.5-MΩ pull-down resistor.

**ROVP PIN DESIGN NOTE**
For an application that does not require a redundant OVP feature, the highly preferred design ties the ROVP pin to GND. If the application cannot allow an ROVP pin connection to GND, ensure that the design minimizes any potential noise injection to the ROVP pin at all cost.

### 8.3.10 UVLO Protection

The TPS53318 and TPS53319 devices use VREG undervoltage lockout protection (UVLO). When the VREG voltage is lower than 3.95 V, the device shuts off. When the VREG voltage is higher than 4.2 V, the device restarts. This is a non-latch protection.

### 8.3.11 Thermal Shutdown

The TPS53318 and TPS53319 devices monitor the internal die temperature. If the temperature exceeds the threshold value (typically 145°C), the device shuts down. When the temperature falls about 10°C below the threshold value, the device will turn back on. This is a non-latch protection.

### 8.3.12 Small Signal Model

From small-signal loop analysis, a buck converter using D-CAP™ mode can be simplified as shown in Figure 33.
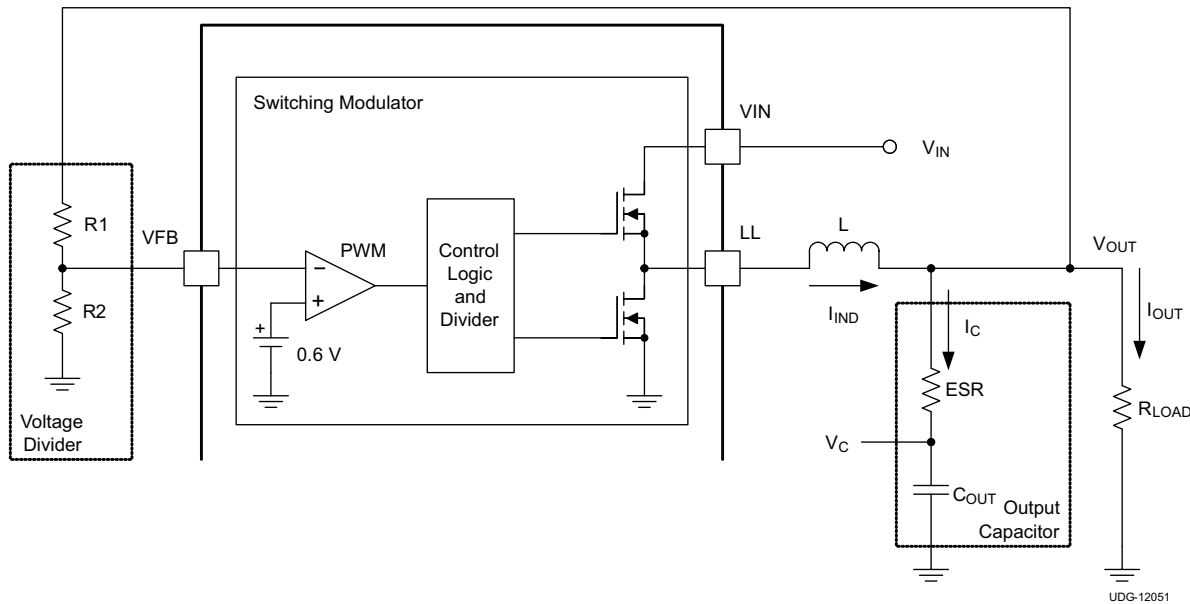


**Figure 33. Simplified Modulator Model**

The output voltage is compared with the internal reference voltage (ramp signal is ignored here for simplicity). The PWM comparator determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator can be assumed high enough to keep the voltage at the beginning of each on cycle substantially constant.

$$H(s) = \frac{1}{s \times ESR \times C_{OUT}}$$

(6)

For loop stability, the 0-dB frequency, $f_0$, defined below need to be lower than 1/4 of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{4}$$

(7)

According to the equation above, the loop stability of D-CAP™ mode modulator is mainly determined by the capacitor's chemistry. For example, specialty polymer capacitors (SP-CAP) have an output capacitance in the order of several 100 µF and ESR in range of 10 mΩ. These makes $f_0$ on the order of 100 kHz or less, creating a stable loop. However, ceramic capacitors have an $f_0$ at more than 700 kHz, and need special care when used with this modulator. An application circuit for ceramic capacitor is described in the *External Component Selection Using All Ceramic Output Capacitors* section.

### 8.3.13 External Component Selection Using All Ceramic Output Capacitors

When a ceramic output capacitor is used, the stability criteria in Equation 7 cannot be satisfied. The ripple injection approach as shown in Figure 34 is implemented to increase the ripple on the VFB pin and make the system stable. In addition to the selections made using steps 1 through step 6 in the *Detailed Design Procedure* section, the ripple injection components must be selected. The C2 value can be fixed at 1 nF. The value of C1 can be selected between 10 nF to 200 nF.

$$\frac{L \times C_{OUT}}{R7 \times C1} > N \times \frac{t_{ON}}{2}$$

where

- N is the coefficient to account for L and $C_{OUT}$ variation

(8)

N is also used to provide enough margin for stability. It is recommended N = 2 for $V_{OUT}$ ≤ 1.8 V and N = 4 for $V_{OUT}$ ≥ 3.3 V or when L ≤ 250 nH. The higher $V_{OUT}$ needs a higher N value because the effective output capacitance is reduced significantly with higher DC bias. For example, a 6.3-V, 22-µF ceramic capacitor may have only 8 µF of effective capacitance when biased at 5 V.

Because the VFB pin voltage is regulated at the valley, the increased ripple on the VFB pin causes the increase of the VFB DC value. The AC ripple coupled to the VFB pin has two components, one coupled from SW node and the other coupled from the VOUT pin and they can be calculated using Equation 9 and Equation 10 when neglecting the output voltage ripple caused by equivalent series inductance (ESL).

$$V_{INJ\_SW} = \frac{V_{IN} - V_{OUT}}{R7 \times C1} \times \frac{D}{f_{SW}}$$

(9)

$$V_{INJ\_OUT} = ESR \times I_{IND(ripple)} + \frac{I_{IND(ripple)}}{8 \times C_{OUT} \times f_{SW}}$$

(10)

It is recommended that $V_{INJ\_SW}$ to be less than 50 mV. If the calculated $V_{INJ\_SW}$ is higher than 50 mV, then other parameters need to be adjusted to reduce it. For example, $C_{OUT}$ can be increased to satisfy Equation 8 with a higher R7 value, thereby reducing $V_{INJ\_SW}$.

The DC voltage at the VFB pin can be calculated by Equation 11:

$$V_{VFB} = 0.6 + \frac{V_{INJ\_SW} + V_{INJ\_OUT}}{2}$$

(11)

And the resistor divider value can be determined by Equation 12:

$$R1 = \frac{V_{OUT} - V_{VFB}}{V_{VFB}} \times R2$$

(12)

## 8.4 Device Functional Modes

### 8.4.1 Enable, Soft Start, and Mode Selection

When the EN pin voltage rises above the enable threshold voltage (typically 1.3 V), the controller enters its start-up sequence. The internal LDO regulator starts immediately and regulates to 5 V at the VREG pin. The controller calibrates the switching frequency setting resistance attached to the RF pin during the first 250 µs. It then stores the switching frequency code in the internal registers. During this period, the MODE pin also senses the resistance attached to this pin and determines the soft-start time. Switching is inhibited during this phase. In the second phase, an internal DAC starts ramping up the reference voltage from 0 V to 0.6 V. Depending on the MODE pin setting, the ramping up time varies from 0.7 ms to 5.6 ms. Smooth and constant ramp-up of the output voltage is maintained during start-up regardless of load current.

---

**NOTE**
Enable voltage should not higher then VREG for 0.8 V.

---

**Table 3. Soft-Start and MODE Settings**

| MODE SELECTION | ACTION | SOFT-START TIME ($t_{SS}$) (ms) | $R_{MODE}$ (kΩ) |
|---|---|---|---|
| Auto Skip | Pull down to GND | 0.7 | 39 |
| | | 1.4 | 100 |
| | | 2.8 | 200 |
| | | 5.6 | 475 |
| Forced CCM[1] | Connect to PGOOD | 0.7 | 39 |
| | | 1.4 | 100 |
| | | 2.8 | 200 |
| | | 5.6 | 475 |

(1)    Device enters FCCM after the PGOOD pin goes high when MODE is connected to PGOOD through the resistor $R_{MODE}$.

After the soft-start period begins, the MODE pin becomes the input of an internal comparator which determines auto skip or FCCM mode operation. If MODE voltage is higher than 1.3 V, the converter enters into FCCM mode. Otherwise it operates in auto skip mode at light-load condition. Typically, when FCCM mode is selected, the MODE pin connects to the PGOOD pin via the $R_{MODE}$ resistor, so that before PGOOD goes high, the converter remains in auto skip mode.

### 8.4.2 Auto-Skip Eco-mode™ Light Load Operation

While $R_{MODE}$ pulls the MODE pin low , the controller automatically reduces the switching frequency at light-load conditions to maintain high efficiency. More specifically, as the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The synchronous MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode (DCM). The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light-load operation $I_{OUT(LL)}$ (i.e., the threshold between continuous and discontinuous conduction mode) can be calculated as shown in Equation 13.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

where

- $f_{SW}$ is the PWM switching frequency  (13)

Switching frequency versus output current in the light-load condition is a function of L, $V_{IN}$ and $V_{OUT}$, but it decreases almost proportionally to the output current from the $I_{OUT(LL)}$ given in Equation 13. For example, it is 60 kHz at $I_{OUT(LL)}$/5 if the frequency setting is 300 kHz.

### 8.4.3 Forced Continuous Conduction Mode

When the MODE pin is tied to PGOOD through a resistor, the controller keeps continuous conduction mode (CCM) in light load condition. In this mode, switching frequency is kept almost constant over the entire load range which is suitable for applications need tight control of the switching frequency at a cost of lower efficiency.

# 9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The TPS53318 and TPS53319 devices are high-efficiency, single channel, synchronous buck converters suitable for low output voltage point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP™ mode control combined with an adaptive on-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC-DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 1.5 V to 22 V and the VDD bias voltage is from 4.5 V to 25 V. The D-CAP™ mode uses the equivalent series resistance (ESR) of the output capacitor(s) to sense the device current. One advantage of this control scheme is that it does not require an external phase compensation network allowing for a simple design with a low external component count. Eight preset switching frequency values can be chosen using a resistor connected from the RF pin to ground or VREG. Adaptive on-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

## 9.2 Typical Applications

### 9.2.1 Application Using Bulk Output Capacitors, Redundant Overvoltage Protection Function (OVP) Disabled
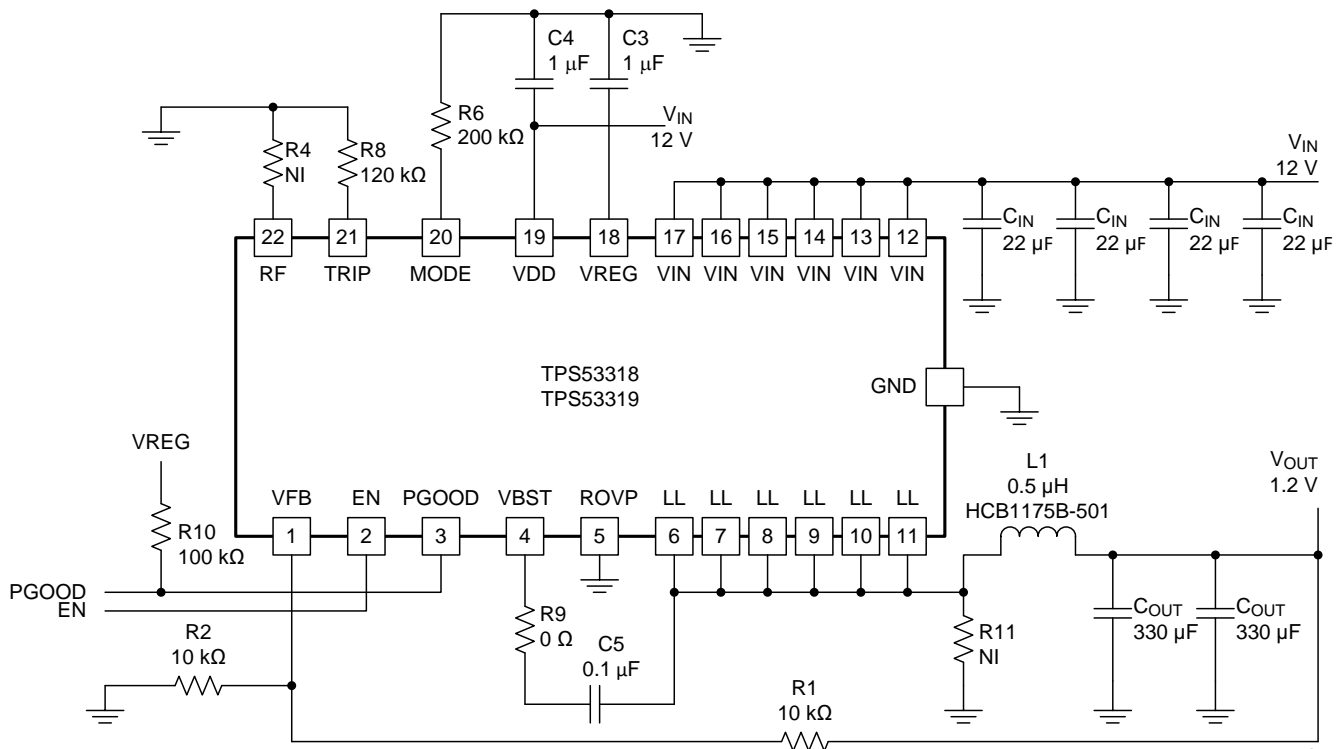


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**Figure 34. Typical Application Circuit, Overvoltage Protection Disabled**

## Typical Applications (continued)

### 9.2.1.1 Design Requirements

This design uses the parameters listed in Table 4.

**Table 4. Design Specifications**

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| $V_{IN}$ | Voltage range | | 5 | 12 | 18 | V |
| $I_{MAX}$ | Maximum input current | $V_{IN}$ = 5 V, $I_{OUT}$ = 8 A | | 2.5 | | A |
| | No load input current | $V_{IN}$ = 12 V, $I_{OUT}$ = 0 A with auto-skip mode | | 1 | | mA |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| $V_{OUT}$ | Output voltage | | | 1.2 | | V |
| | Output voltage regulation | Line regulation, 5 V ≤ $V_{IN}$ ≤ 14 V with FCCM | | 0.2% | | |
| | | Load regulation, $V_{IN}$ = 12 V, 0 A ≤ $I_{OUT}$ ≤ 8 A with FCCM | | 0.5% | | |
| $V_{RIPPLE}$ | Output voltage ripple | $V_{IN}$ = 12 V, $I_{OUT}$ = 8 A with FCCM | | 10 | | $mV_{PP}$ |
| $I_{LOAD}$ | Output load current | | 0 | | 8 | A |
| $I_{OVER}$ | Output overcurrent | | | 11 | | |
| $t_{SS}$ | Soft-start time | | | 1 | | ms |
| **SYSTEMS CHARACTERISTICS** | | | | | | |
| $f_{SW}$ | Switching frequency | | | 500 | 1000 | kHz |
| η | Peak efficiency | $V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, $I_{OUT}$ = 4 A | | 91% | | |
| | Full load efficiency | $V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, $I_{OUT}$ = 8 A | | 91.5% | | |
| $T_A$ | Operating temperature | | | 25 | | °C |

### 9.2.1.2 Detailed Design Procedure

The external components selection is a simple process when using organic semiconductors or special polymer output capacitors.

#### 9.2.1.2.1 Step One: Select Operation Mode and Soft-Start Time

Select operation mode and soft-start time using Table 3.

#### 9.2.1.2.2 Step Two: Select Switching Frequency

Select the switching frequency from 250 kHz to 1 MHz using Table 1.

#### 9.2.1.2.3 Step Three: Choose the Inductor

The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current. Larger ripple current increases output ripple voltage and improves signal-to-noise ratio and helps ensure stable operation, but increases inductor core loss. Using 1/3 ripple current to maximum output current ratio, the inductance can be determined by Equation 14.

$$L = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \tag{14}$$

The inductor requires a low DCR to achieve good efficiency. It also requires enough room above peak inductor current before saturation. The peak inductor current can be estimated in Equation 15.

$$I_{IND(peak)} = \frac{V_{TRIP}}{32 \times R_{DS(on)}} + \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \tag{15}$$

#### 9.2.1.2.4 Step Four: Choose the Output Capacitor(s)

When organic semiconductor capacitor(s) or specialty polymer capacitor(s) are used, for loop stability, capacitance and ESR should satisfy Equation 7. For jitter performance, Equation 16 is a good starting point to determine ESR.

$$ESR = \frac{V_{OUT} \times 10\,mV \times (1-D)}{0.6\,V \times I_{IND(ripple)}} = \frac{10\,mV \times L \times f_{SW}}{0.6\,V} = \frac{L \times f_{SW}}{60}(\Omega)$$

where

- D is the duty factor.
- The required output ripple slope is approximately 10 mV per $t_{SW}$ (switching period) in terms of VFB terminal voltage.                                                                                                  (16)

#### 9.2.1.2.5 Step Five: Determine the Value of R1 and R2

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in Figure 33. R1 is connected between VFB pin and the output, and R2 is connected between the VFB pin and GND. Recommended R2 value is from 10 kΩ to 20 kΩ. Determine R1 using Equation 17.

$$R1 = \frac{V_{OUT} - \dfrac{I_{IND(ripple)} \times ESR}{2} - 0.6}{0.6} \times R2$$

                                                                                                                   (17)

#### 9.2.1.2.6 Step Six: Choose the Overcurrent Setting Resistor

The overcurrent setting resistor, $R_{TRIP}$, can be determined by Equation 18.

$$R_{TRIP} = \left( I_{OCP} - \left( \frac{1}{2 \times L \times f_{SW}} \right) \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \right) \times 12.3$$

where

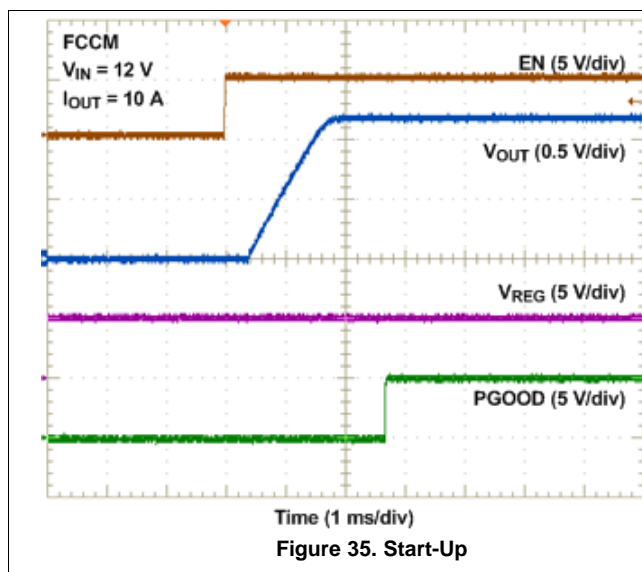- $R_{TRIP}$ is in kΩ                                                                                                  (18)
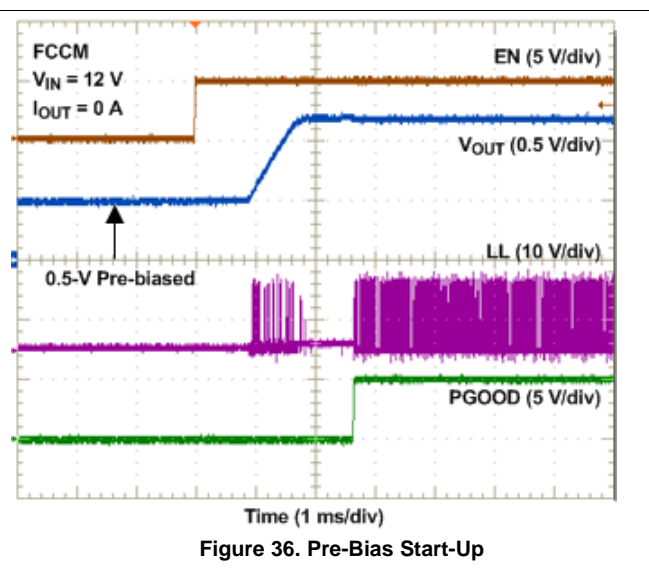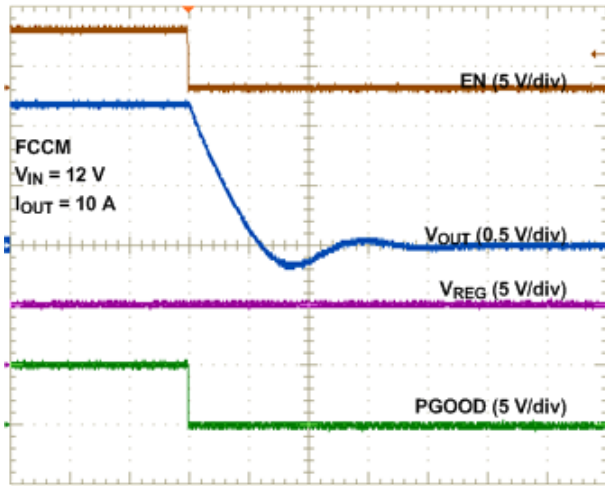
### 9.2.1.3 Application Curves



**Figure 35. Start-Up**



**Figure 36. Pre-Bias Start-Up**

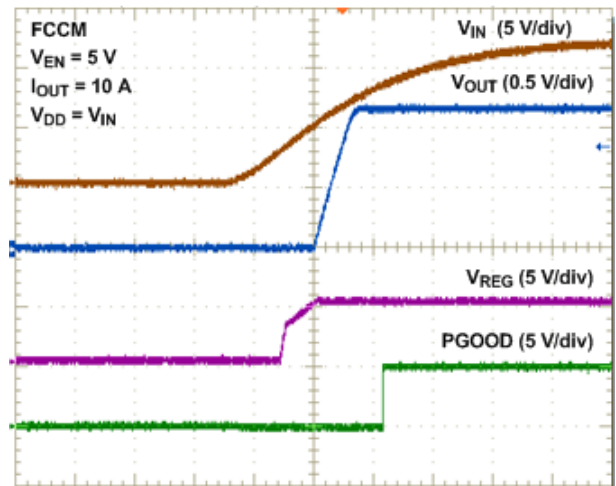**Figure 37. Shutdown**



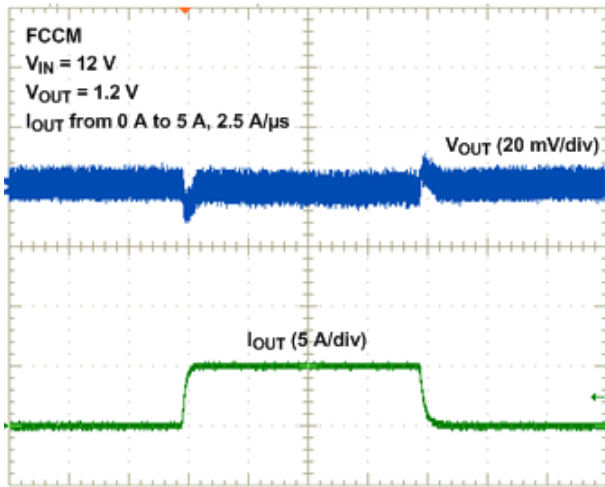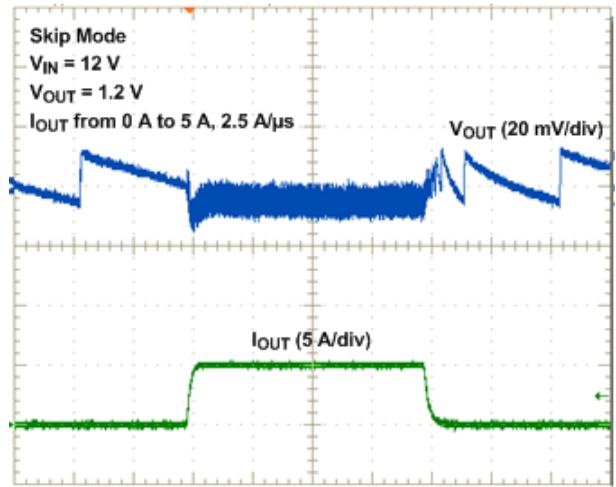**Figure 38. UVLO Start-Up**



**Figure 39. FCCM Load Transient**


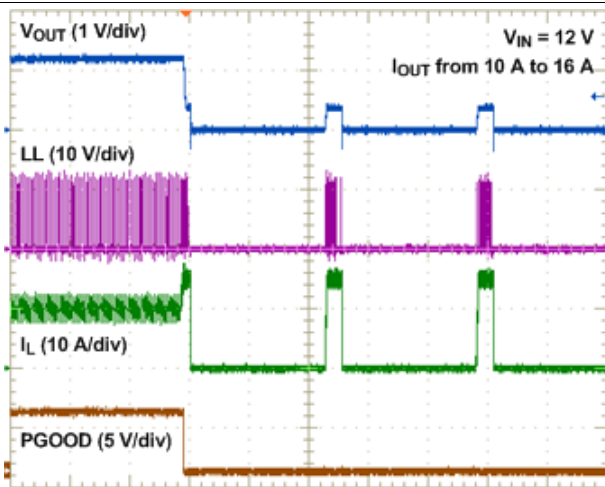
**Figure 40. Skip Mode Load Transeint**



**Figure 41. Overcurrent Protection**



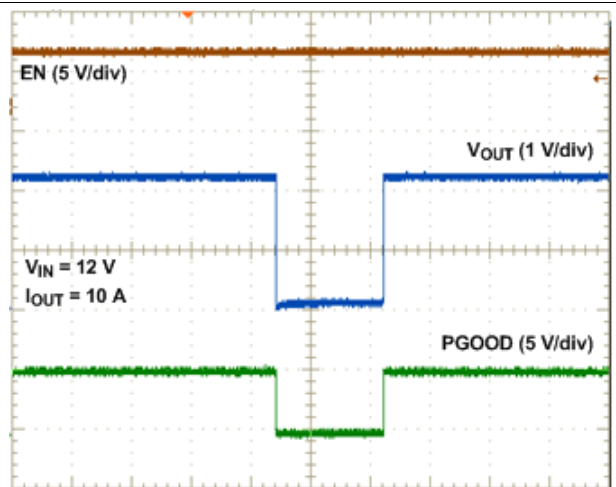**Figure 42. Over-Temperature Protection**
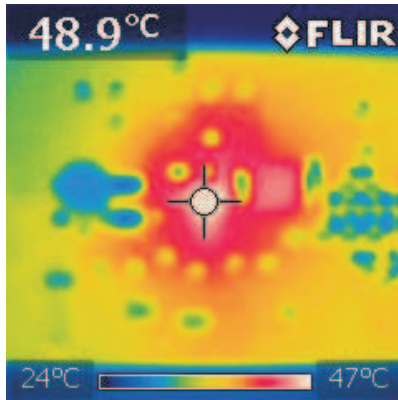
TPS53319 EVM     $V_{IN}$ = 12 V     $V_{OUT}$ = 1.2 V
$I_{OUT}$ = 14 A     $f_{SW}$ = 500 kHz     $T_A$ = 25°C
     No airflow

**Figure 43.  Thermal Signature**
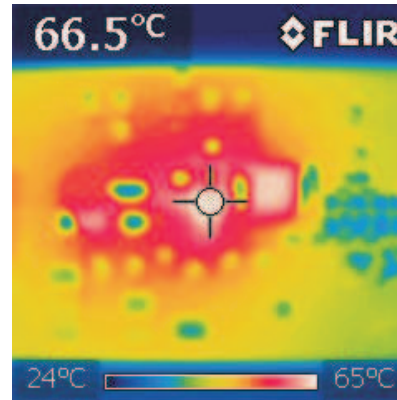


TPS53319 EVM     $V_{IN}$ = 12 V     $V_{OUT}$ = 5 V
$I_{OUT}$ = 14 A     $f_{SW}$ = 500 kHz     $T_A$ = 25°C
     No airflow

**Figure 44. Thermal Signature**

     *Submit Documentation Feedback*     25

### 9.2.2 Application Using Ceramic Output Capacitors, Redundant Overvoltage Protection Function (OVP) Enabled
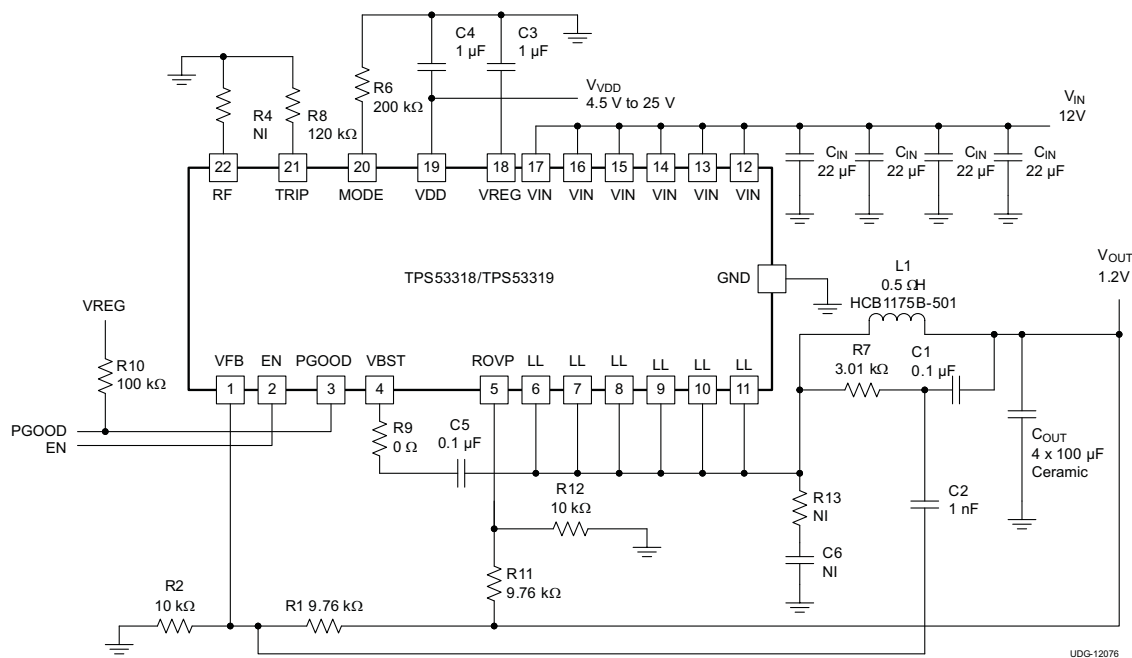


**Figure 45. Typical Application Circuit, Redundent OVP Enabled**

#### 9.2.2.1 Design Requirements

This design uses the parameters listed in Table 4.

#### 9.2.2.2 Detailed Design Procedure

The detailed design procedure for this design example is similar to the procedure for the previous design example. The differences are discussed in the following two sections.

##### 9.2.2.2.1 External Component Selection Using All Ceramic Output Capacitors

Refer to *External Component Selection Using All Ceramic Output Capacitors* for guidelines for this design with all ceramic output capacitors.

##### 9.2.2.2.2 Redundant Overvoltage Protection

The redundant overvoltage level is programmed according to the output voltage setting, it is controlled by resistors R11 and R12 as shown in Figure 45. Connect resistor R11 between the ROVP pin and the output, and connect resistor R12 between the ROVP pin and GND. This design recommends that the value of resistor R11 match the value of resistor R1 (or slightly higher), and that the value of resistor R2 match the value of resistor R12.

### 9.2.2.3 Application Curves



**Figure 46. Start-Up**



**Figure 47. Pre-Bias Start-Up**



**Figure 48. Shutdown**



**Figure 49. UVLO Start-Up**
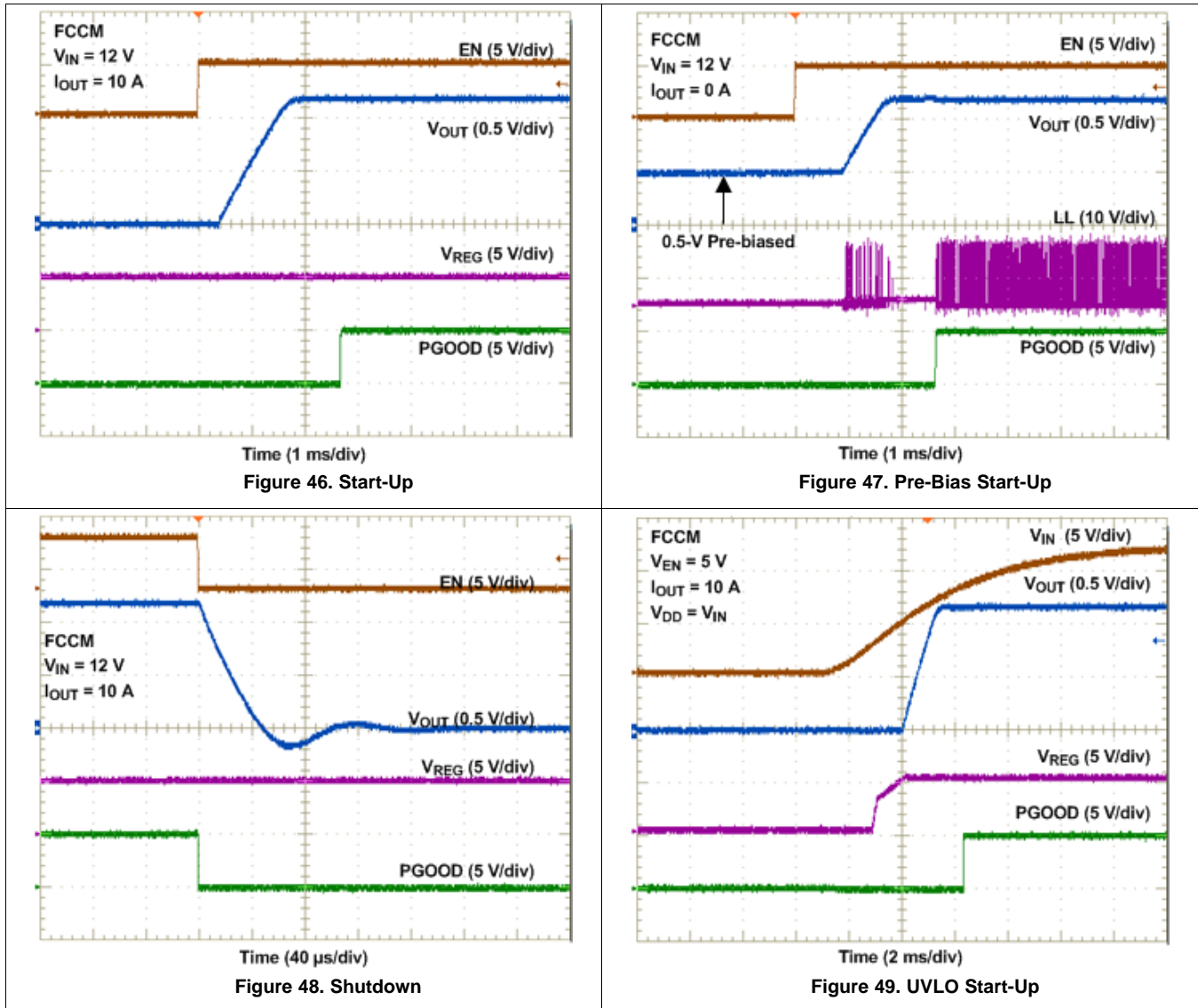
## 10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 1.5 V and 22 V (4.5 V to 25 V biased). This input supply must be well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in the *Layout* section.

## 11 Layout

### 11.1 Layout Guidelines

- The power components (including input/output capacitors, inductor and TPS53318 device or TPS53319 device) should be placed on one side of the PCB (solder side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE and RF should be placed away from high-voltage switching nodes such as LL, VBST to avoid coupling. Use internal layer(s) as ground

## Layout Guidelines (continued)

plane(s) and shield feedback trace from power traces and components.

- Place the VIN decoupling capacitors as close to the VIN and PGND pins as possible to minimize the input AC current loop.
- Because the TPS53319 device controls output voltage referring to voltage across VOUT capacitor, the top-side resistor of the voltage divider should be connected to the positive node of the VOUT capacitor. The GND of the bottom side resistor should be connected to the GND pad of the device. The trace from these resistors to the VFB pin should be short and thin.
- Place the frequency setting resistor ($R_F$), OCP setting resistor ($R_{TRIP}$) and mode setting resistor ($R_{MODE}$) as close to the device as possible. Use the common GND via to connect them to GND plane if applicable.
- Place the VDD and VREG decoupling capacitors as close to the device as possible. Ensure to provide GND vias for each decoupling capacitor and make the loop as small as possible.
- For better noise filtering on VDD, a dedicated and localized decoupling support is strongly recommended.
- The PCB trace defined as switch node, which connects the LL pins and high-voltage side of the inductor, should be as short and wide as possible.
- Connect the ripple injection $V_{OUT}$ signal ($V_{OUT}$ side of the C1 capacitor in Figure 45) from the terminal of ceramic output capacitor. The AC coupling capacitor (C2 in Figure 45) should be placed near the device, and R7 and C1 can be placed near the power stage.
- Use separated vias or trace to connect LL node to snubber, boot strap capacitor and ripple injection resistor. Do not combine these connections.
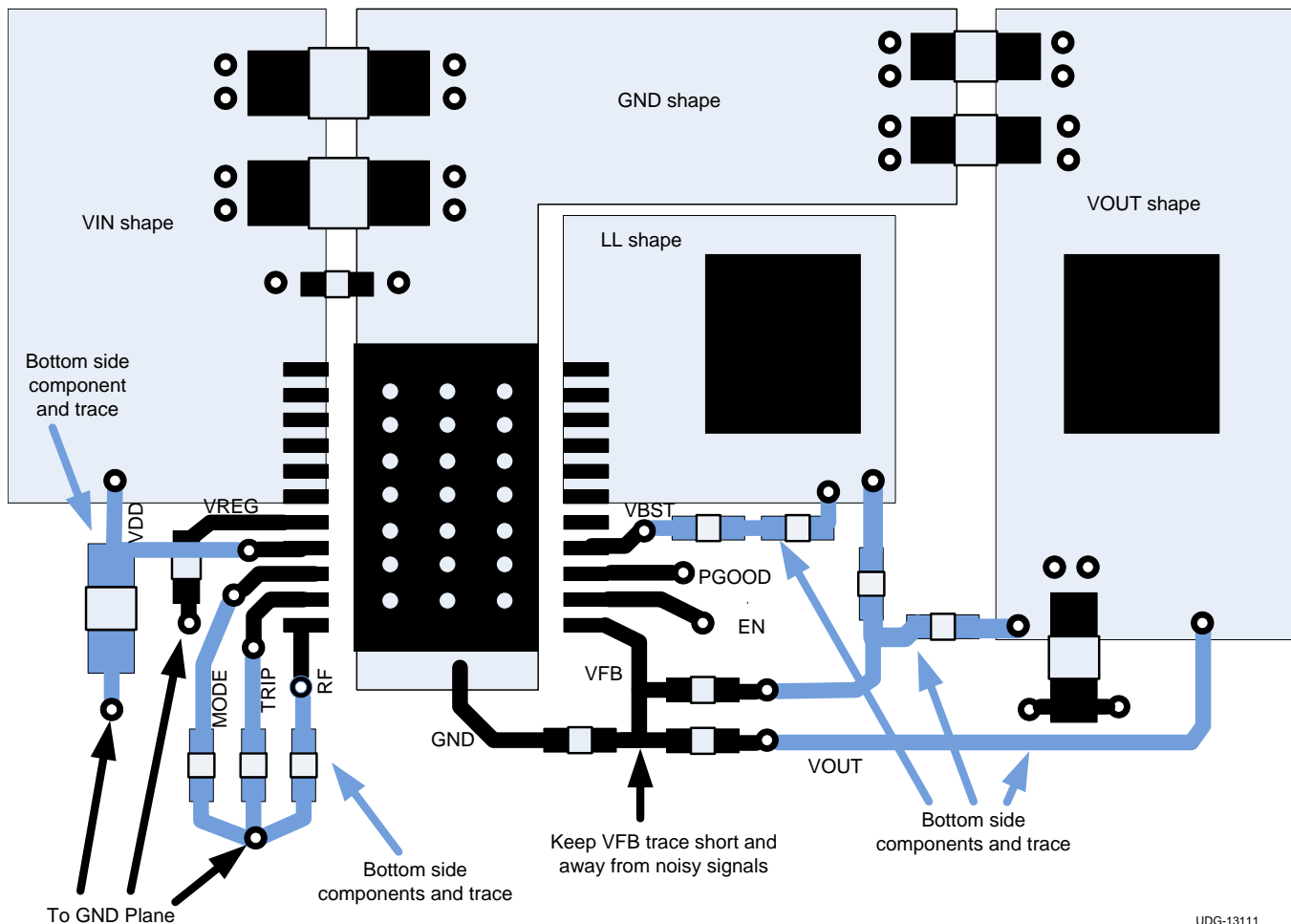
## 11.2  Layout Example



**Figure 50.  Layout Recommendation**

Product Folder Links: *TPS53318  TPS53319*

# 12 Device and Documentation Support

## 12.1 Device Support

### 12.1.1 Development Support

Reference Design: 7-V to 12-V Input, 1.2-V Output, 8-A Step-Down Converter for Powering Rails in Altera Arria V FPGA, PMP8824

Evaluation Module: Synchronous Switcher with Integrated MOSFETs, TPS53319EVM-136

TPS53318 TINA-TI Transient Spice Model, SLUM381

## 12.2 Related Links

Table 5 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 5. Related Links**

| DEVICES | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TPS53318 | Click here | Click here | Click here | Click here | Click here |
| TPS53319 | Click here | Click here | Click here | Click here | Click here |

## 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.5 Trademarks

Eco-mode, D-CAP, NexFET, PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.6 Electrostatic Discharge Caution

![ESD warning symbol] These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.7 Glossary

SLYZ022 — *TI Glossary*.

   This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS53318DQPR | ACTIVE | LSON-CLIP | DQP | 22 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | 53318DQP | Samples |
| TPS53318DQPT | ACTIVE | LSON-CLIP | DQP | 22 | 250 | Green (RoHS & no Sb/Br) | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | 53318DQP | Samples |
| TPS53319DQPR | ACTIVE | LSON-CLIP | DQP | 22 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | 53319DQP | Samples |
| TPS53319DQPT | ACTIVE | LSON-CLIP | DQP | 22 | 250 | Green (RoHS & no Sb/Br) | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | 53319DQP | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
|----|-------------------------------------------------------|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

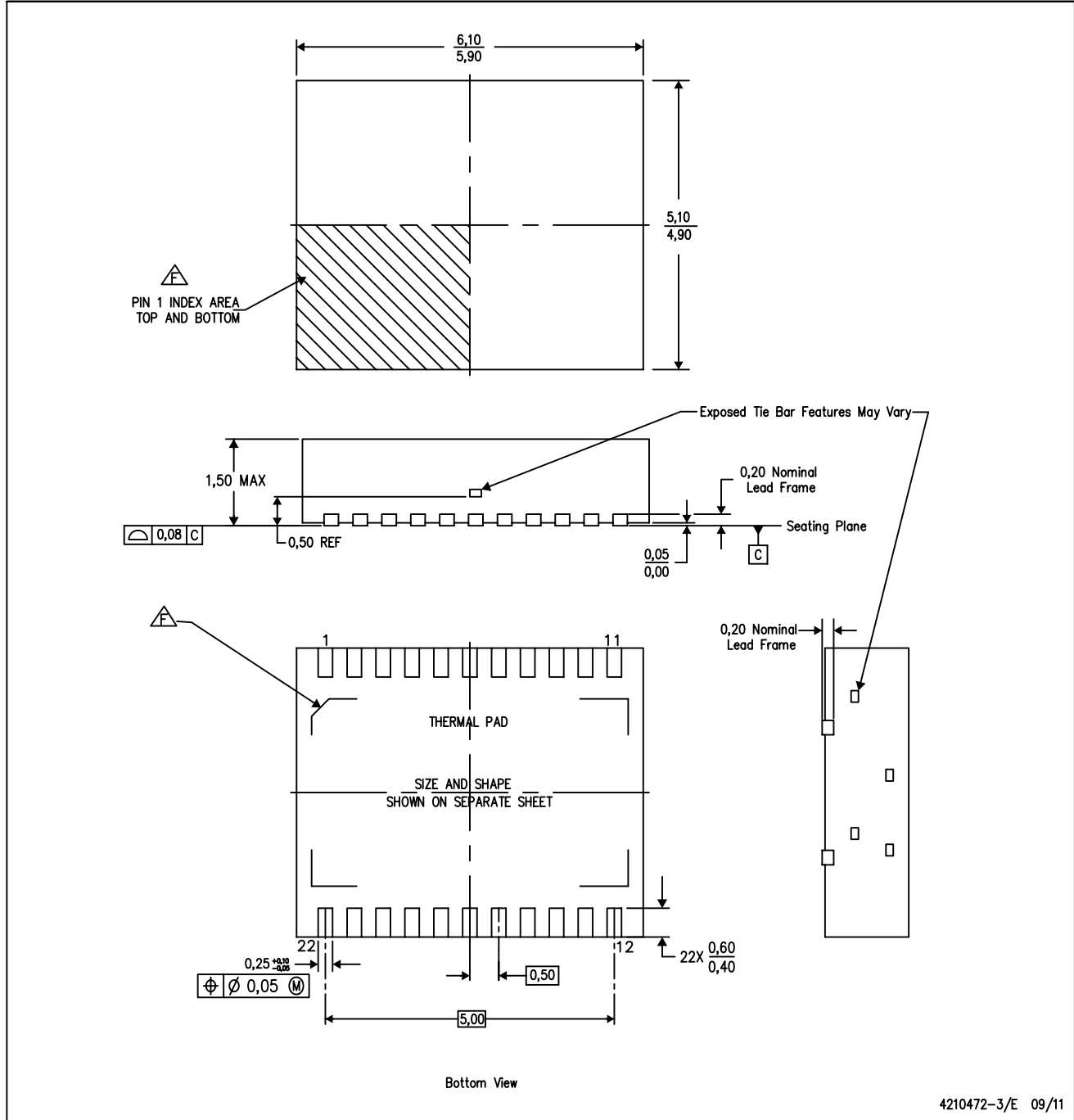| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|------|-------------------|-------------------|---------|---------|---------|---------|--------|---------------|
| TPS53318DQPR | LSON-CLIP | DQP | 22 | 2500 | 330.0 | 12.4 | 5.3 | 6.3 | 1.8 | 8.0 | 12.0 | Q1 |
| TPS53318DQPT | LSON-CLIP | DQP | 22 | 250 | 180.0 | 12.4 | 5.3 | 6.3 | 1.8 | 8.0 | 12.0 | Q1 |
| TPS53319DQPR | LSON-CLIP | DQP | 22 | 2500 | 330.0 | 12.4 | 5.3 | 6.3 | 1.8 | 8.0 | 12.0 | Q1 |
| TPS53319DQPT | LSON-CLIP | DQP | 22 | 250 | 180.0 | 12.4 | 5.3 | 6.3 | 1.8 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX  DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS53318DQPR | LSON-CLIP | DQP | 22 | 2500 | 367.0 | 367.0 | 35.0 |
| TPS53318DQPT | LSON-CLIP | DQP | 22 | 250 | 210.0 | 185.0 | 35.0 |
| TPS53319DQPR | LSON-CLIP | DQP | 22 | 2500 | 367.0 | 367.0 | 35.0 |
| TPS53319DQPT | LSON-CLIP | DQP | 22 | 250 | 210.0 | 185.0 | 35.0 |

DQP (R−PSON−N22)                    PLASTIC SMALL OUTLINE NO−LEAD

6,10
5,90

5,10
4,90

⟨F⟩
PIN 1 INDEX AREA
TOP AND BOTTOM

Exposed Tie Bar Features May Vary

1,50 MAX

0,20 Nominal
Lead Frame

Seating Plane

□ 0,08 C

0,50 REF

0,05
0,00

C

⟨F⟩

0,20 Nominal
Lead Frame

1          11

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

22          12

0,25 +0,10 −0,05

⊕ Ø 0,05 Ⓜ

0,50

5,00

22X 0,60
0,40

Bottom View

4210472−3/E  09/11

NOTES:   A.  All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.  This drawing is subject to change without notice.
         C.  Small Outline No−Lead (SON) package configuration.
         D.  The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.  See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
    ⟨F⟩  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
         The Pin 1 identifiers are either a molded, marked, or metal feature.

DQP (R—PSON—N22)                    PLASTIC SMALL OUTLINE NO—LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
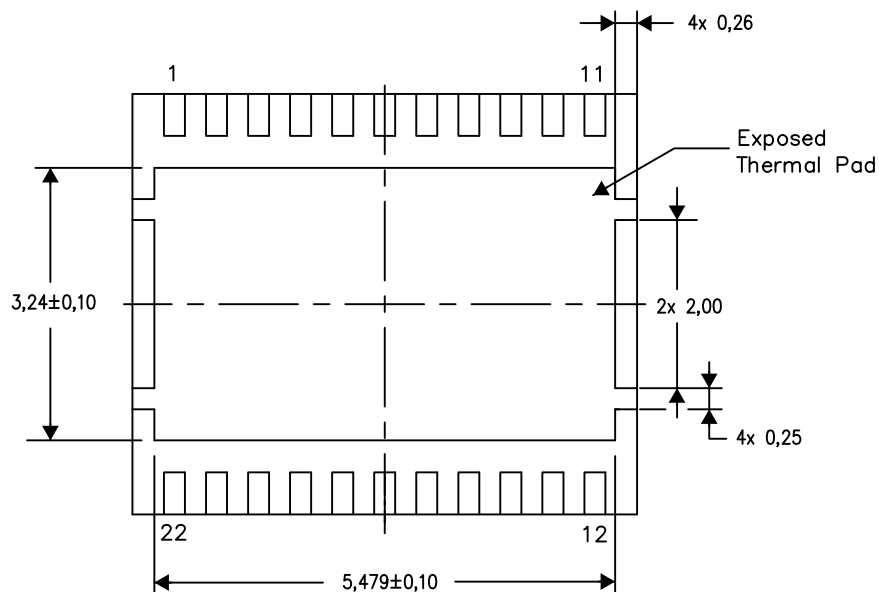


Bottom View

Exposed Thermal Pad Dimensions

4211024–3/H  08/15

NOTE:   All linear dimensions are in millimeters

DQP (R−PSON−N22)                    PLASTIC SMALL OUTLINE NO−LEAD
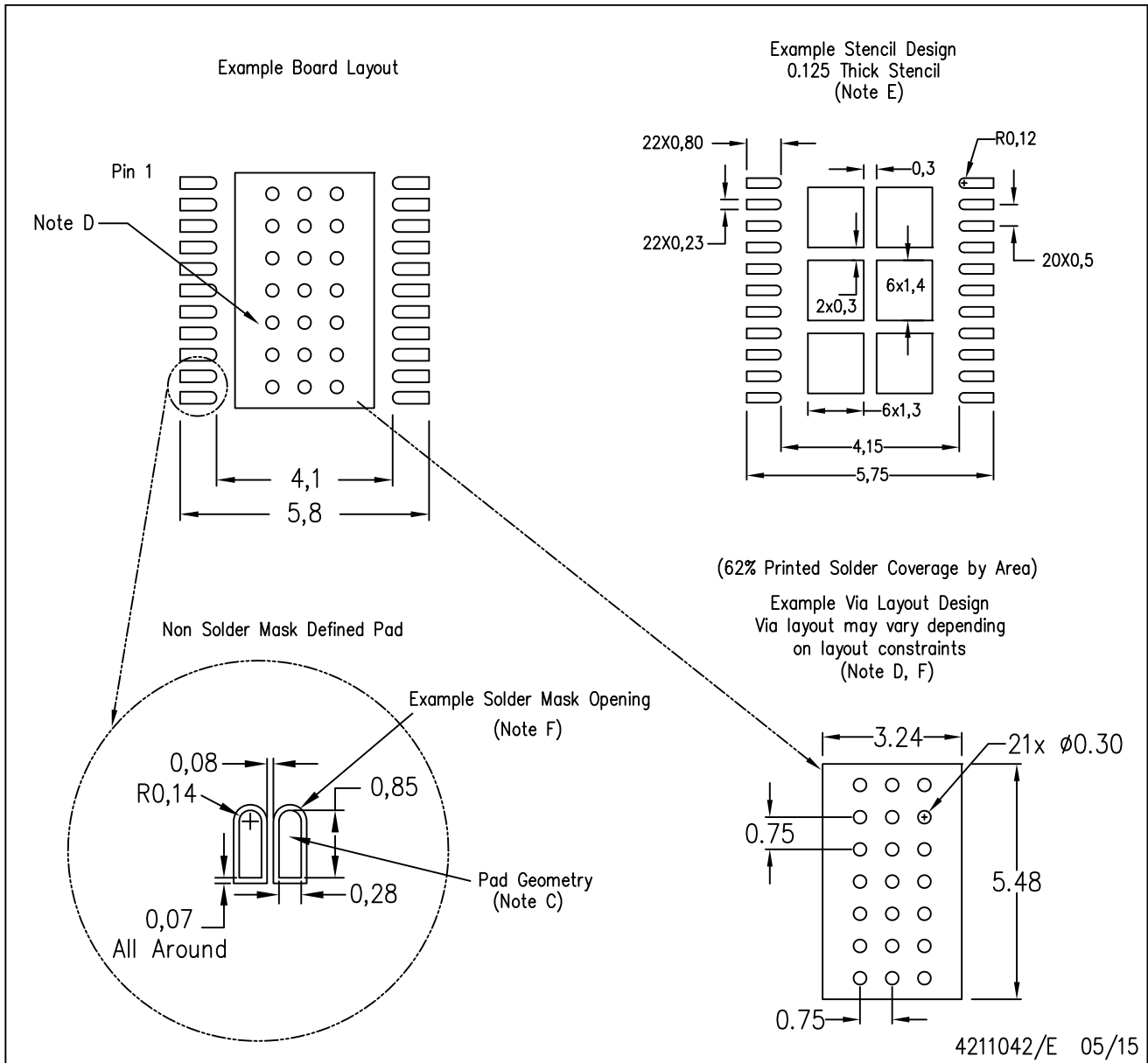
Example Board Layout

Example Stencil Design
0.125 Thick Stencil
(Note E)

Pin 1

Note D

22X0,80

22X0,23

R0,12

0,3

20X0,5

6x1,4

2x0,3

6x1,3

4,1

4,15

5,8

5,75

(62% Printed Solder Coverage by Area)

Example Via Layout Design
Via layout may vary depending
on layout constraints
(Note D, F)

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note F)

3.24

21x ∅0.30

0,08

R0,14

0,85

0.75

5.48

0,28

Pad Geometry
(Note C)

0,07

0.75

All Around

4211042/E  05/15

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate designs.
         D.   This package is designed to be soldered to a thermal pad on the board.  Refer to Application Note,
              QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout.
              These documents are available at www.ti.com <http://www.ti.com>.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations.  Refer to IPC 7525 for stencil design
              considerations.
         F.   Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
              recommendations for vias placed in the thermal pad.

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