

# NTD70N03R

## Power MOSFET

72 A, 25 V, N-Channel DPAK

### Features

- Planar HD3e Process for Fast Switching Performance
- Low  $R_{DS(on)}$  to Minimize Conduction Loss
- Low  $C_{ISS}$  to Minimize Driver Loss
- Low Gate Charge
- Pb-Free Packages are Available

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	25	$V_{dc}$
Gate-to-Source Voltage - Continuous	$V_{GS}$	$\pm 20$	$V_{dc}$
Thermal Resistance - Junction-to-Case	$R_{\theta JC}$	2.4	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	62.5	W
Drain Current			
- Continuous @ $T_C = 25^\circ\text{C}$ , Chip	$I_D$	72.0	A
- Continuous @ $T_C = 25^\circ\text{C}$ , Limited by Package	$I_D$	62.8	A
- Continuous @ $T_A = 25^\circ\text{C}$ , Limited by Wires	$I_D$	32	A
- Single Pulse ( $t_p = 10 \mu\text{s}$ )	$I_{DM}$	140	A
Thermal Resistance - Junction-to-Ambient (Note 1)	$R_{\theta JA}$	80	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.87	W
Drain Current - Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	12.0	A
Thermal Resistance - Junction-to-Ambient (Note 2)	$R_{\theta JA}$	110	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.36	W
Drain Current - Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	10.0	A
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy - Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 30 V_{dc}$ , $V_{GS} = 10 V_{dc}$ , $I_L = 12 A_{pk}$ , $L = 1 \text{ mH}$ , $R_G = 25 \Omega$ )	$E_{AS}$	71.7	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 s	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

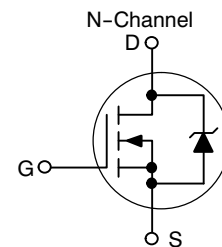
1. When surface mounted to an FR4 board using 0.5 sq. in. pad size.
2. When surface mounted to an FR4 board using minimum recommended pad size.



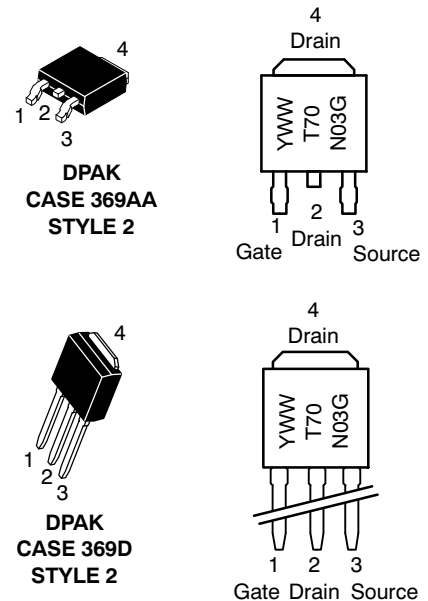
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$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
25 V	5.6 m $\Omega$	72 A



### MARKING DIAGRAMS



70N03 = Device Code  
 Y = Year  
 WW = Work Week  
 G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTD70N03R

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C Unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 V <sub>dc</sub> , I <sub>D</sub> = 250 μA <sub>dc</sub> ) Temperature Coefficient (Positive)	V <sub>(br)DSS</sub>	25 -	28 20.5	- -	V <sub>dc</sub> mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> ) (V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	- -	- -	1.5 10	μA <sub>dc</sub>
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 V <sub>dc</sub> , V <sub>DS</sub> = 0 V <sub>dc</sub> )	I <sub>GSS</sub>	-	-	±100	nA <sub>dc</sub>

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA <sub>dc</sub> ) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 -	1.5 4.0	2.0 -	V <sub>dc</sub> mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V <sub>GS</sub> = 4.5 V <sub>dc</sub> , I <sub>D</sub> = 20 A <sub>dc</sub> ) (V <sub>GS</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 20 A <sub>dc</sub> )	R <sub>DS(on)</sub>	- -	8.1 5.6	13 8.0	mΩ
Forward Transconductance (Note 3) (V <sub>DS</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 15 A <sub>dc</sub> )	g <sub>FS</sub>	-	27	-	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V, f = 1 MHz)	C <sub>ISS</sub>	-	1333	-	pF
Output Capacitance		C <sub>OSS</sub>	-	600	-	
Transfer Capacitance		C <sub>RSS</sub>	-	218	-	

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V <sub>GS</sub> = 10 V <sub>dc</sub> , V <sub>DD</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 36 A <sub>dc</sub> , R <sub>G</sub> = 3 Ω)	t <sub>d(on)</sub>	-	6.9	-	ns
Rise Time		t <sub>r</sub>	-	1.3	-	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	18.4	-	
Fall Time		t <sub>f</sub>	-	5.5	-	
Gate Charge	(V <sub>GS</sub> = 5 V <sub>dc</sub> , I <sub>D</sub> = 36 A <sub>dc</sub> , V <sub>DS</sub> = 10 V <sub>dc</sub> ) (Note 3)	Q <sub>T</sub>	-	13.2	-	nC
		Q <sub>GS</sub>	-	3.3	-	
		Q <sub>DS</sub>	-	6.5	-	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = 20 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> ) (Note 3) (I <sub>S</sub> = 20 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , T <sub>J</sub> = 125°C)	V <sub>SD</sub>	- -	0.86 0.73	1.2 -	V <sub>dc</sub>
Reverse Recovery Time	(I <sub>S</sub> = 36 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , dI <sub>S</sub> /dt = 100 A/μs) (Note 3)	t <sub>rr</sub>	-	27.9	-	ns
		t <sub>a</sub>	-	14.8	-	
		t <sub>b</sub>	-	13.1	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	-	19	-	nC

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

4. Switching characteristics are independent of operating junction temperatures.

# NTD70N03R

## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

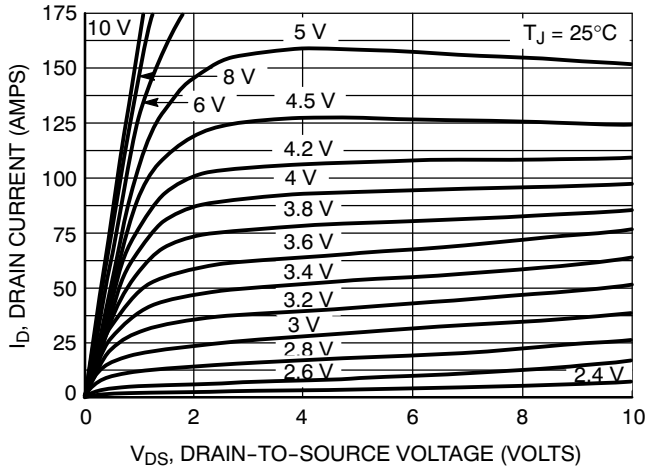


Figure 1. On-Region Characteristics

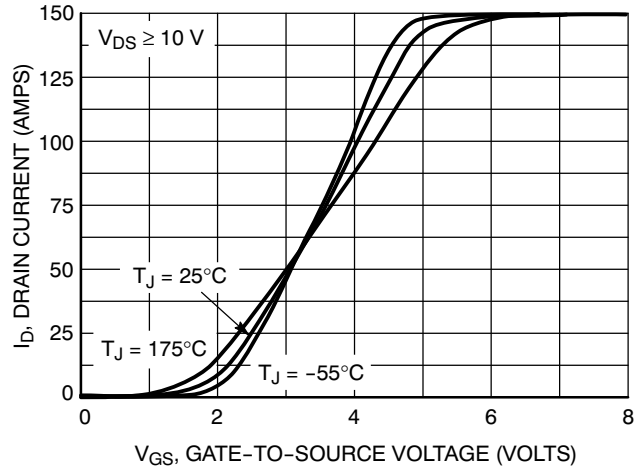


Figure 2. Transfer Characteristics

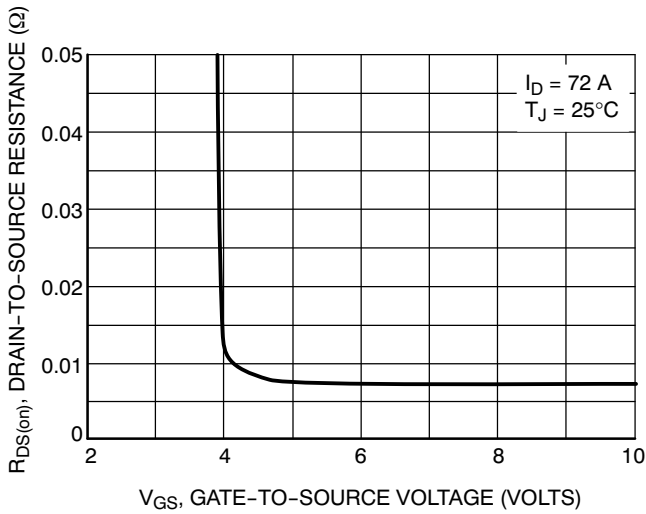


Figure 3. On-Resistance versus Gate-to-Source Voltage

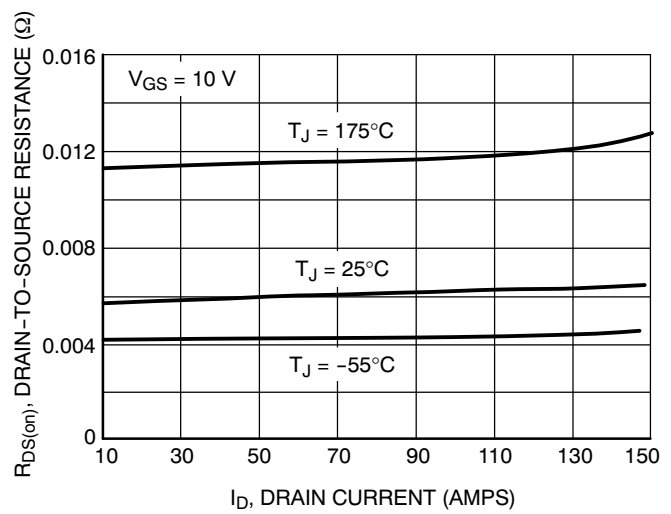


Figure 4. On-Resistance versus Drain Current and Gate Voltage

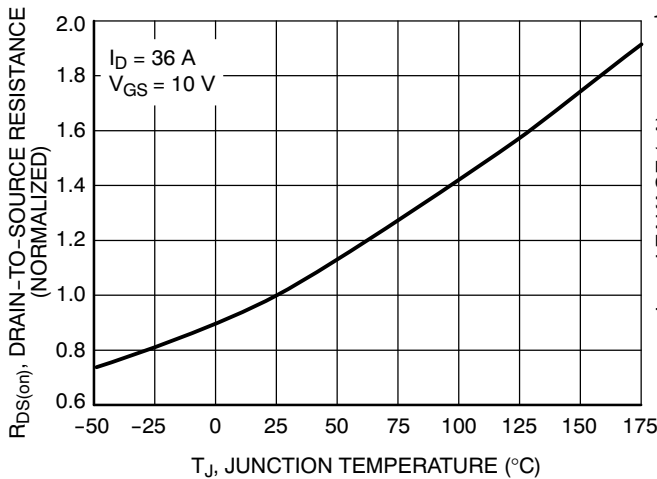


Figure 5. On-Resistance Variation with Temperature

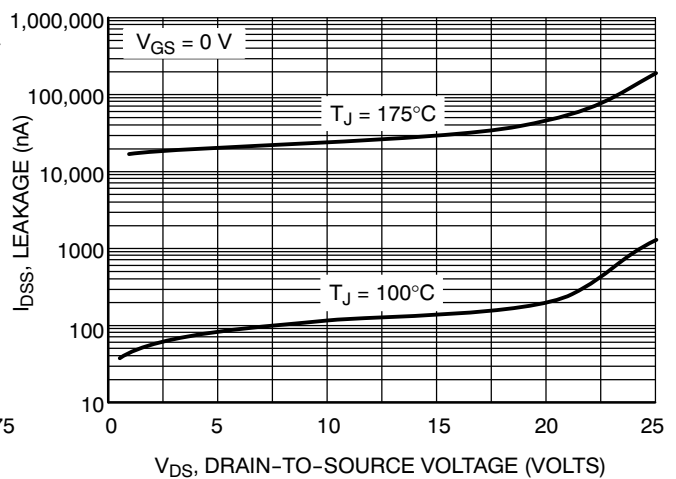


Figure 6. Drain-to-Source Leakage Current versus Voltage

# NTD70N03R

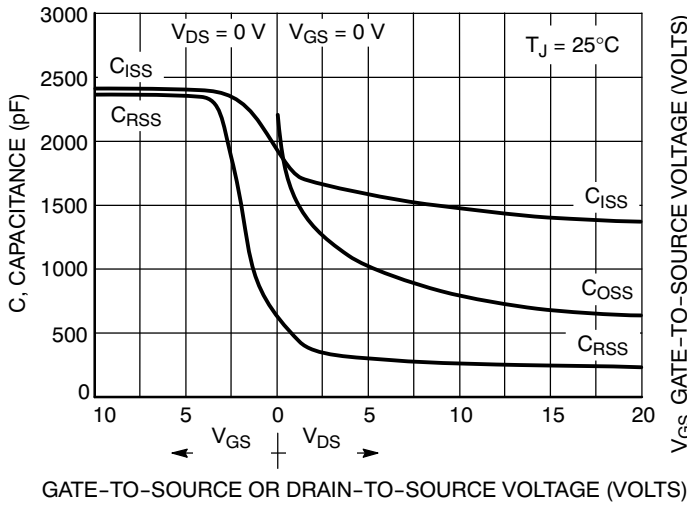


Figure 7. Capacitance Variation

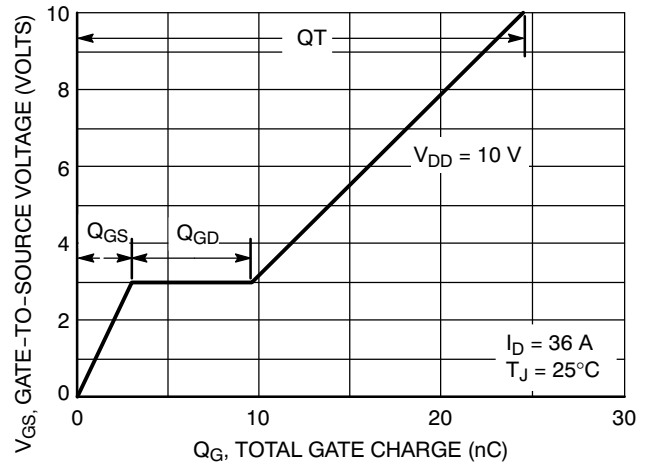


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

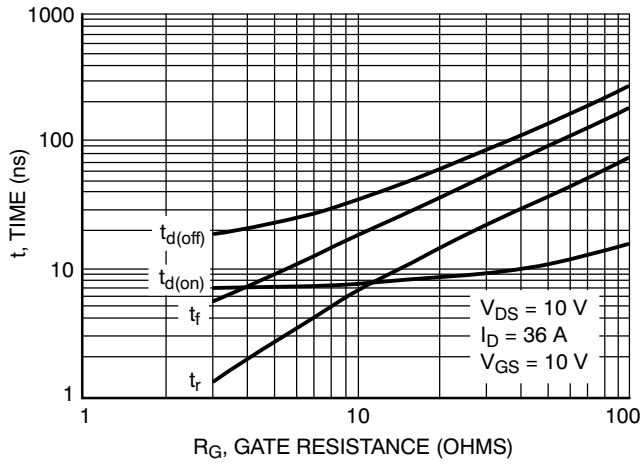


Figure 9. Resistive Switching Time Variation versus Gate Resistance

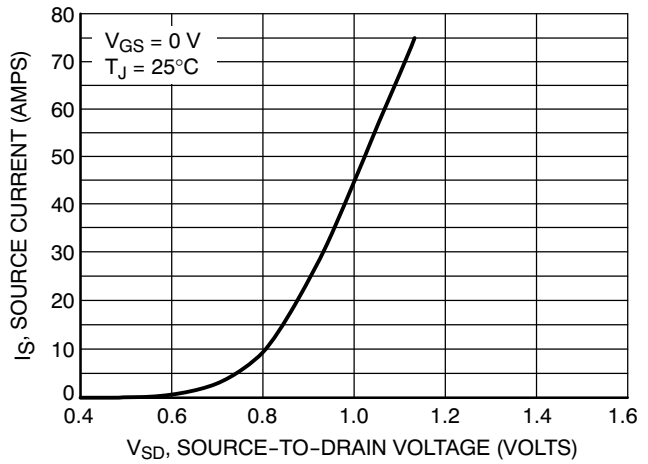


Figure 10. Diode Forward Voltage versus Current

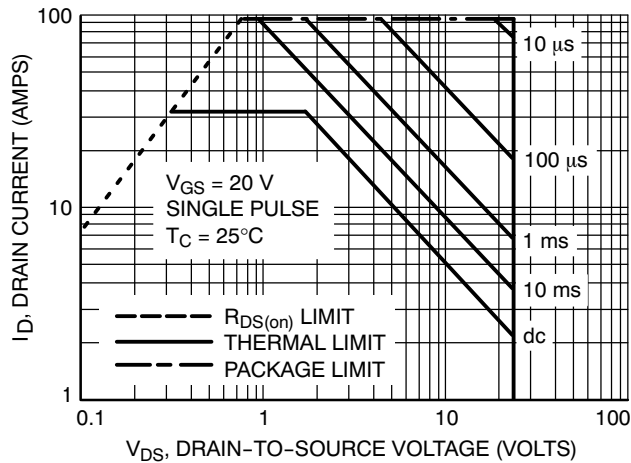


Figure 11. Maximum Rated Forward Biased Safe Operating Area

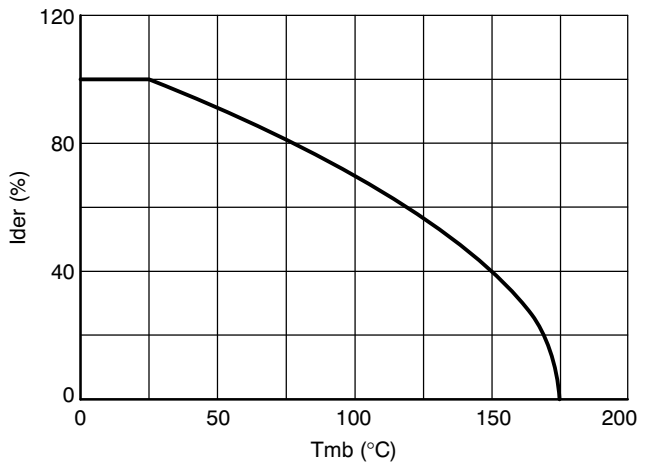


Figure 12. Normalized Continuous Drain Current as a function of Mounting Base Temperature

# NTD70N03R

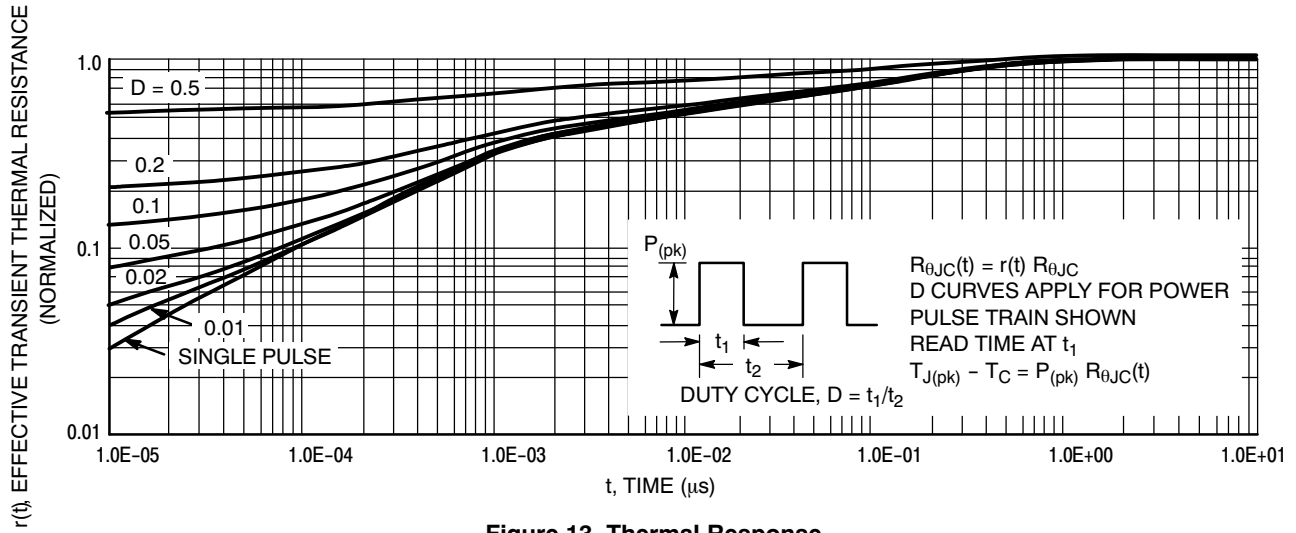


Figure 13. Thermal Response

## ORDERING INFORMATION

Order Number	Package	Shipping <sup>†</sup>
NTD70N03R	DPAK-3	75 Units / Rail
NTD70N03RG	DPAK-3 (Pb-Free)	75 Units / Rail
NTD70N03RT4	DPAK-3	2500 / Tape & Reel
NTD70N03RT4G	DPAK-3 (Pb-Free)	2500 / Tape & Reel
NTD70N03R-1	DPAK-3 Straight Lead	75 Units / Rail
NTD70N03R-1G	DPAK-3 Straight Lead (Pb-Free)	75 Units / Rail

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



### IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010



SCALE 1:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- |  |   |  |  |
|--|---|--|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p> | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>      | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p> |
| <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>         | <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>        | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> |  |

### MARKING DIAGRAMS



- xxxxxxxx = Device Code  
A = Assembly Location  
IL = Wafer Lot  
Y = Year  
WW = Work Week

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<b>DESCRIPTION:</b>	<b>IPAK (DPAK INSERTION MOUNT)</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS



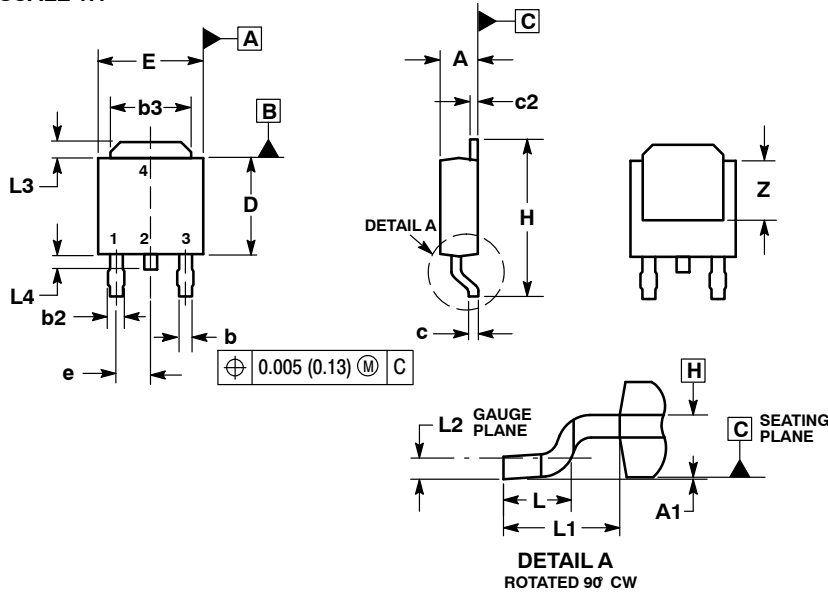
SCALE 1:1

### DPAK (SINGLE GAUGE)

#### CASE 369AA-01

#### ISSUE B

DATE 03 JUN 2010



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

- |  |   |  |  |
|--|---|--|--|
| <p>STYLE 1:</p> <p>PIN 1. BASE</p> <p>2. COLLECTOR</p> <p>3. EMITTER</p> <p>4. COLLECTOR</p> | <p>STYLE 2:</p> <p>PIN 1. GATE</p> <p>2. DRAIN</p> <p>3. SOURCE</p> <p>4. DRAIN</p> | <p>STYLE 3:</p> <p>PIN 1. ANODE</p> <p>2. CATHODE</p> <p>3. ANODE</p> <p>4. CATHODE</p>  | <p>STYLE 4:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. GATE</p> <p>4. ANODE</p> |
| <p>STYLE 5:</p> <p>PIN 1. GATE</p> <p>2. ANODE</p> <p>3. CATHODE</p> <p>4. ANODE</p>         | <p>STYLE 6:</p> <p>PIN 1. MT1</p> <p>2. MT2</p> <p>3. GATE</p> <p>4. MT2</p>        | <p>STYLE 7:</p> <p>PIN 1. GATE</p> <p>2. ANODE</p> <p>3. EMITTER</p> <p>4. COLLECTOR</p> |  |

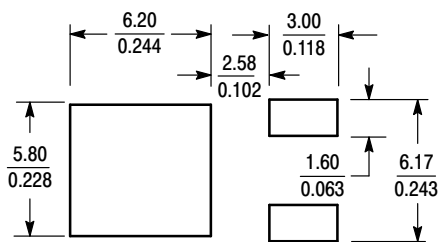
### GENERIC MARKING DIAGRAM\*



- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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