

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

- **Low Supply-Voltage Range: 1.8 V to 3.6 V**
- **Ultralow Power Consumption**
 - Active Mode: 330 μ A at 1 MHz, 2.2 V
 - Standby Mode: 1.1 μ A
 - Off Mode (RAM Retention): 0.2 μ A
- **Five Power-Saving Modes**
- **Wake-Up From Standby Mode in Less Than 6 μ s**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **Three-Channel Internal DMA**
- **12-Bit Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan Feature**
- **Dual 12-Bit Digital-to-Analog (D/A) Converters With Synchronization**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **16-Bit Timer_B With Three or Seven Capture/Compare-With-Shadow Registers**
- **On-Chip Comparator**
- **Serial Communication Interface (USART0), Functions as Asynchronous UART or Synchronous SPI or I²C™ Interface**
- **Serial Communication Interface (USART1), Functions as Asynchronous UART or Synchronous SPI Interface**
- **Supply Voltage Supervisor/Monitor With Programmable Level Detection**
- **Brownout Detector**
- **Bootstrap Loader**
- **Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse**
- **Family Members Include**
 - MSP430F155
16KB+256B Flash Memory
512B RAM
 - MSP430F156
24KB+256B Flash Memory
1KB RAM
 - MSP430F157
32KB+256B Flash Memory,
1KB RAM
 - MSP430F167
32KB+256B Flash Memory,
1KB RAM
 - MSP430F168
48KB+256B Flash Memory,
2KB RAM
 - MSP430F169
60KB+256B Flash Memory,
2KB RAM
 - MSP430F1610
32KB+256B Flash Memory
5KB RAM
 - MSP430F1611
48KB+256B Flash Memory
10KB RAM
 - MSP430F1612
55KB+256B Flash Memory
5KB RAM
- **Available in 64-Pin QFP Package (PM) and 64-Pin QFN Package (RTD)**
- **For Complete Module Descriptions, See the *MSP430x1xx Family User's Guide*, Literature Number SLAU049**

I²C is a registered trademark of Philips Incorporated.

description

The Texas Instruments MSP430 family of ultralow power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 μ s.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2011, Texas Instruments Incorporated

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

description (continued)

The MSP430F15x/16x/161x series are microcontroller configurations with two built-in 16-bit timers, a fast 12-bit A/D converter, dual 12-bit D/A converter, one or two universal serial synchronous/asynchronous communication interfaces (USART), I²C, DMA, and 48 I/O pins. In addition, the MSP430F161x series offers extended RAM addressing for memory-intensive applications and large C-stack requirements.

Typical applications include sensor systems, industrial control applications, hand-held meters, etc.

| AVAILABLE OPTIONS | | |
|-------------------|-------------------------|--------------------------|
| T _A | PACKAGED DEVICES | |
| | PLASTIC 64-PIN QFP (PM) | PLASTIC 64-PIN QFN (RTD) |
| -40°C to 85°C | MSP430F155IPM | MSP430F155IRTD |
| | MSP430F156IPM | MSP430F156IRTD |
| | MSP430F157IPM | MSP430F157IRTD |
| | MSP430F167IPM | MSP430F167IRTD |
| | MSP430F168IPM | MSP430F168IRTD |
| | MSP430F169IPM | MSP430F169IRTD |
| | MSP430F1610IPM | MSP430F1610IRTD |
| | MSP430F1611IPM | MSP430F1611IRTD |
| | MSP430F1612IPM | MSP430F1612IRTD |

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DEVELOPMENT TOOL SUPPORT

All MSP430 microcontrollers include an Embedded Emulation Module (EEM) allowing advanced debugging and programming through easy to use development tools. Recommended hardware options include the following:

- Debugging and Programming Interface
 - MSP-FET430UIF (USB)
 - MSP-FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
 - MSP-FET430U64 (PM package)
- Standalone Target Board
 - MSP-TS430PM64 (PM package)
- Production Programmer
 - MSP-GANG430



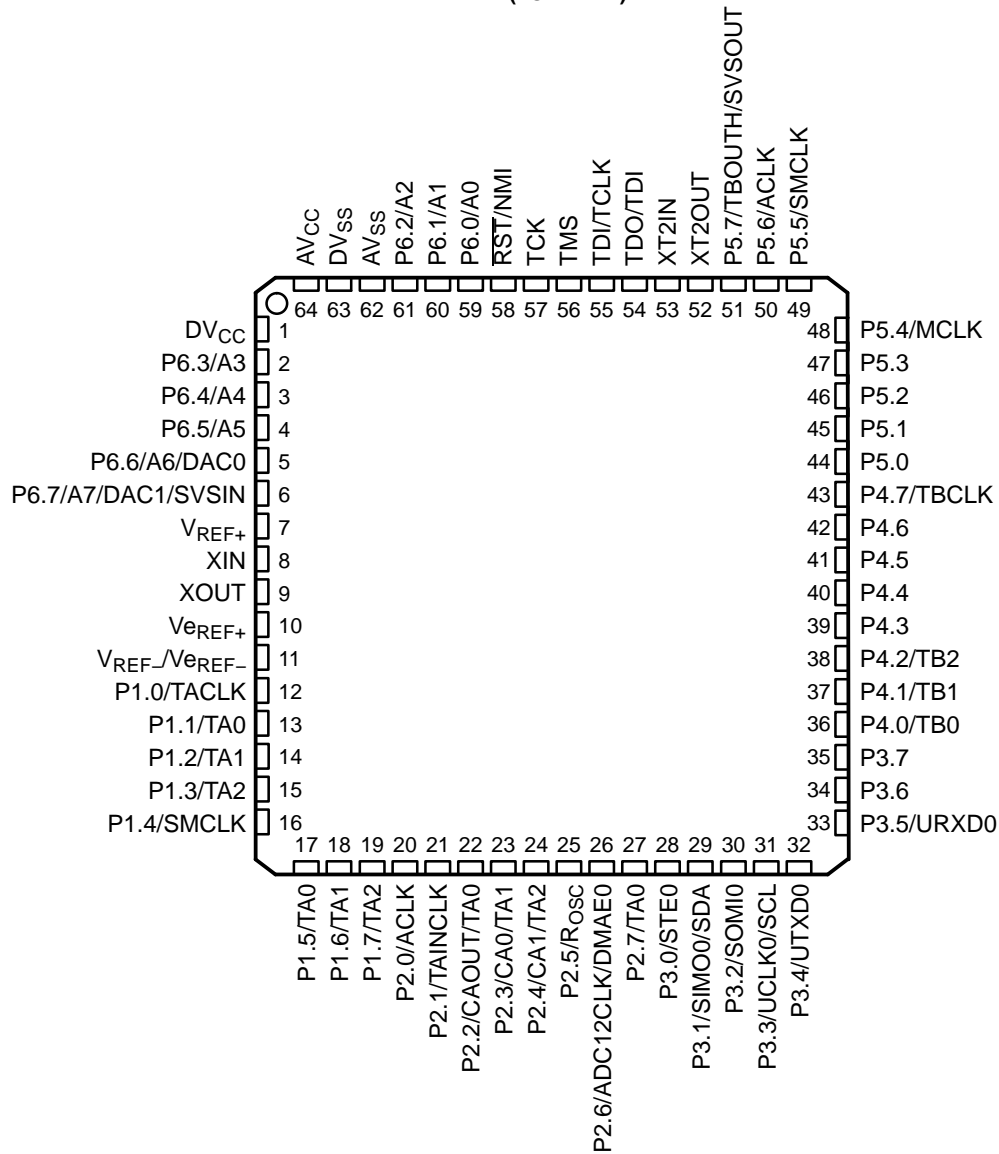
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

pin designation, MSP430F155, MSP430F156, and MSP430F157

PM, RTD PACKAGE
(TOP VIEW)

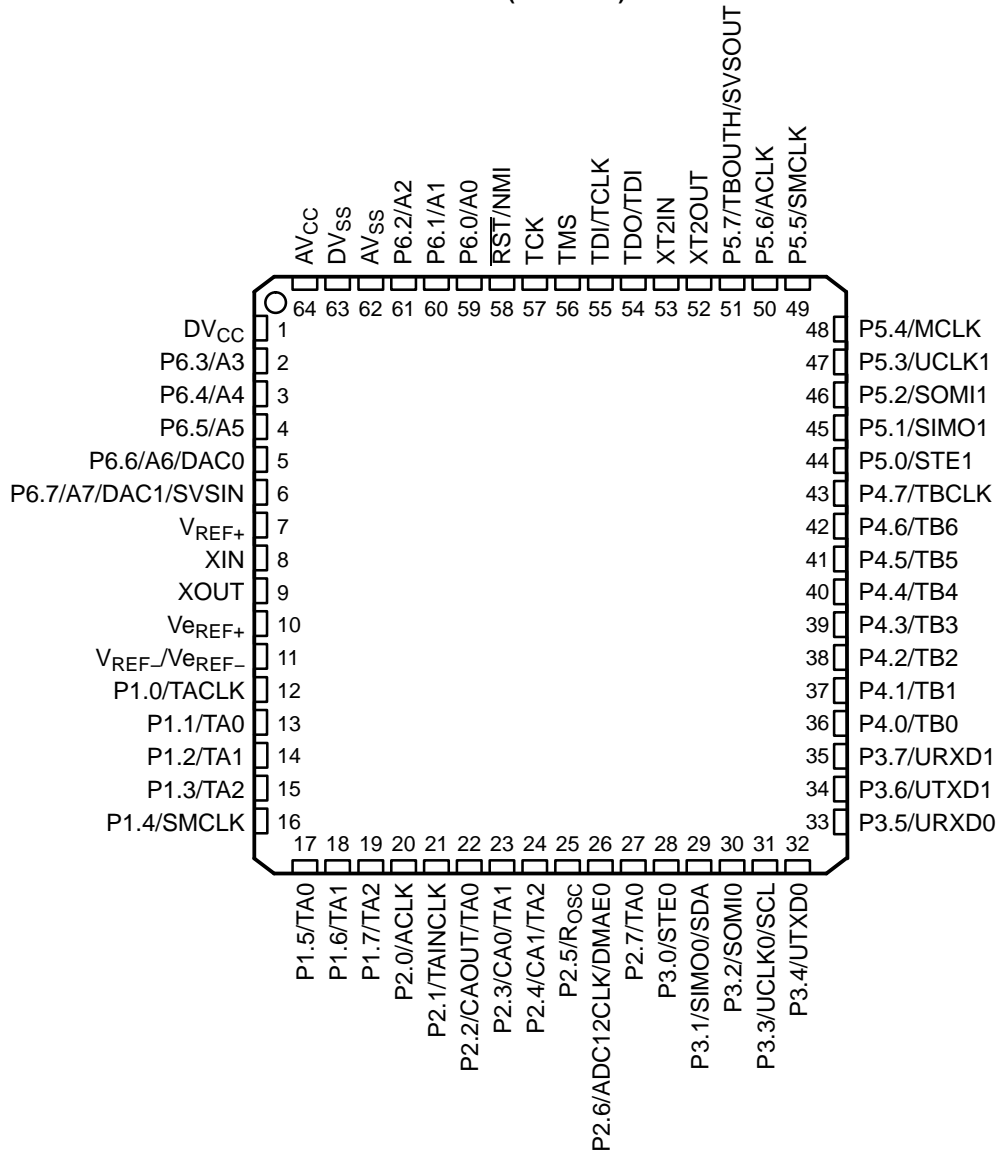


MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

pin designation, MSP430F167, MSP430F168, MSP430F169

PM, RTD PACKAGE
(TOP VIEW)

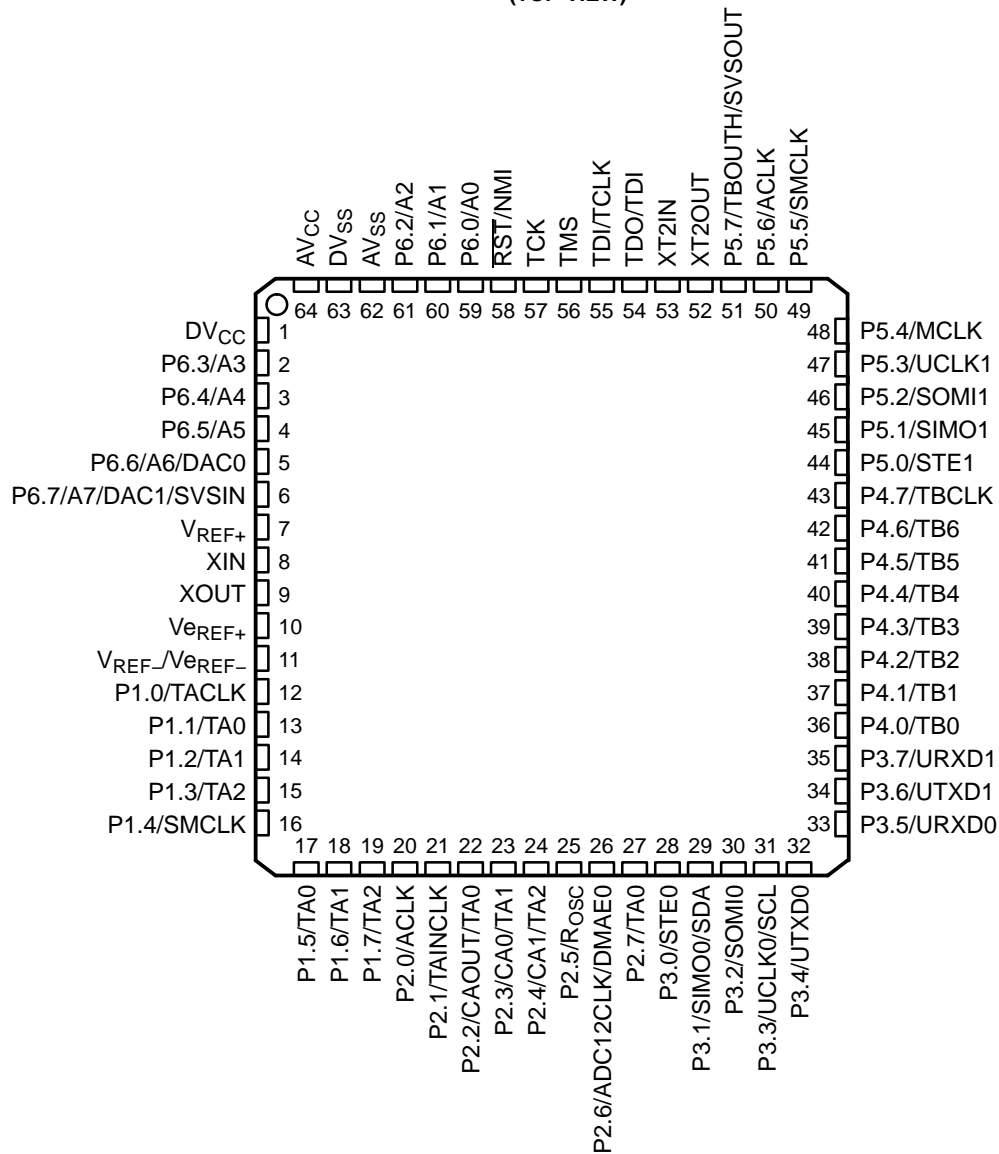


MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

pin designation, MSP430F1610, MSP430F1611, MSP430F1612

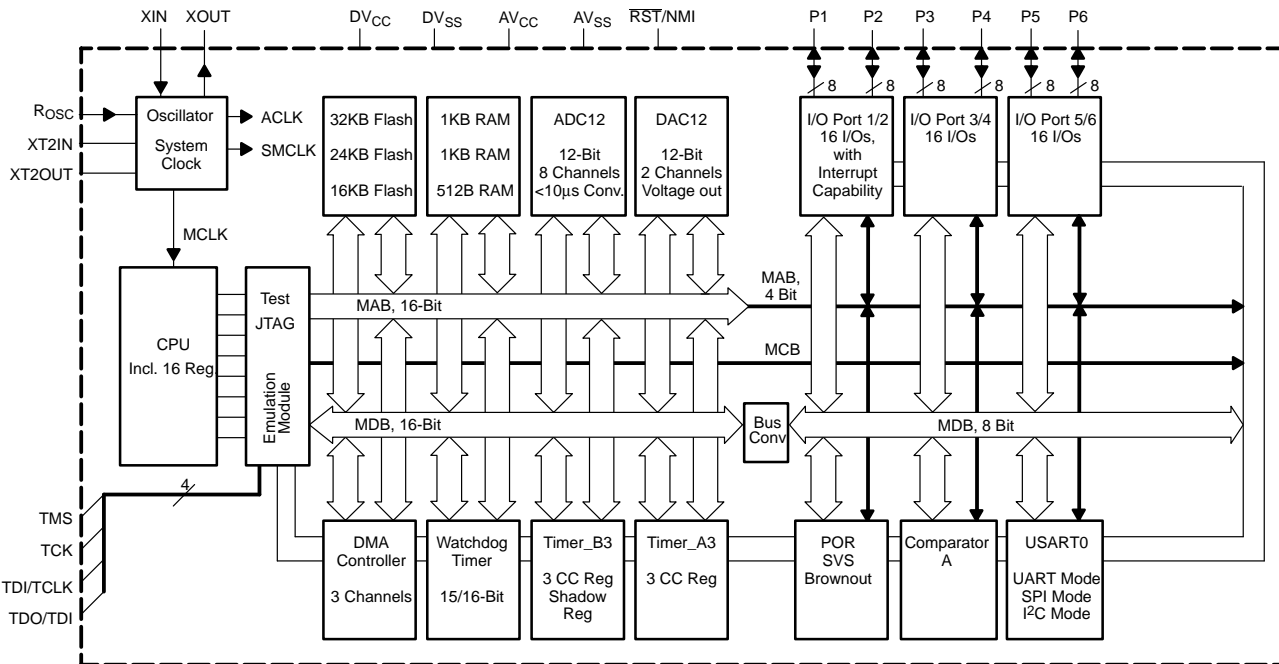
PM, RTD PACKAGE
(TOP VIEW)



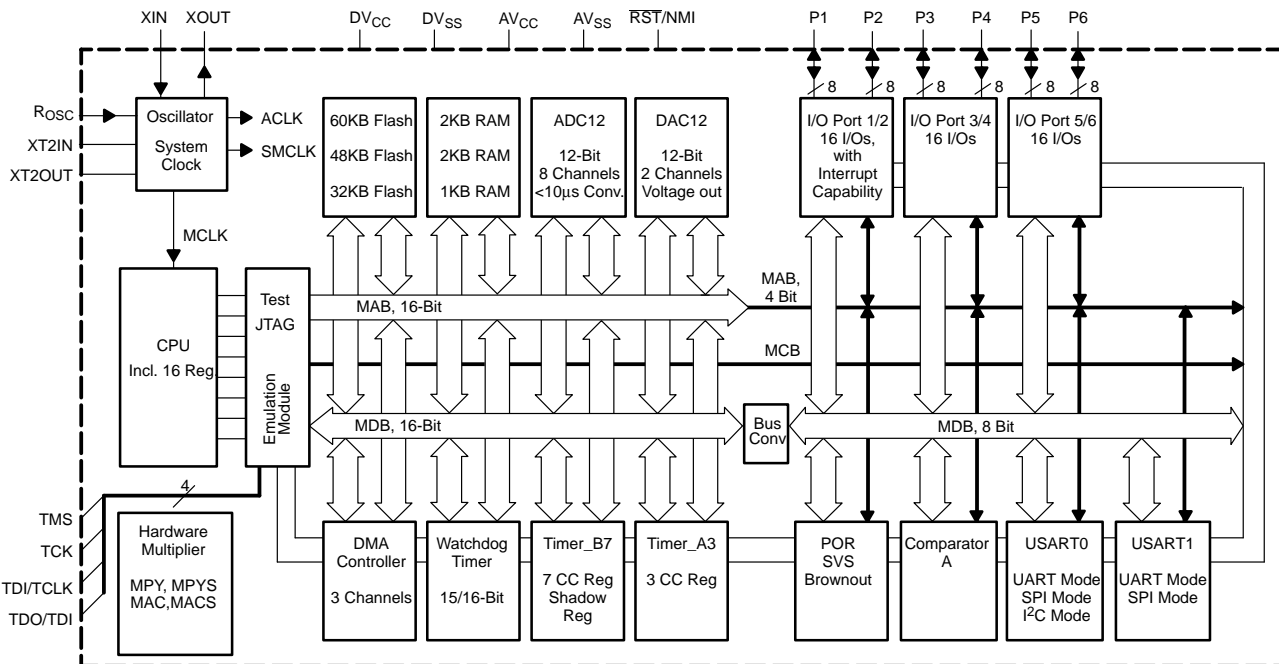
MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

functional block diagram, MSP430F15x



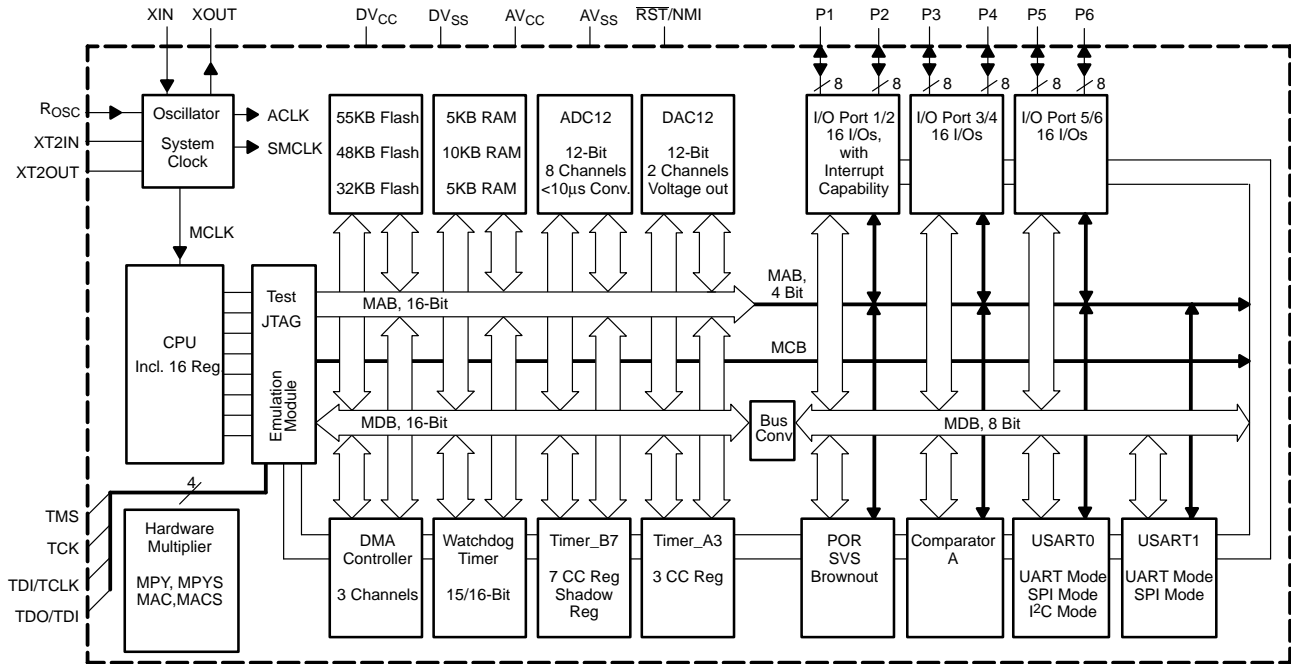
functional block diagram, MSP430F16x



MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

functional block diagram, MSP430F161x



MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|-------------------------|-----|-----|---|
| AV _{CC} | 64 | | Analog supply voltage, positive terminal. Supplies only the analog portion of ADC12 and DAC12. |
| AV _{SS} | 62 | | Analog supply voltage, negative terminal. Supplies only the analog portion of ADC12 and DAC12. |
| DV _{CC} | 1 | | Digital supply voltage, positive terminal. Supplies all digital parts. |
| DV _{SS} | 63 | | Digital supply voltage, negative terminal. Supplies all digital parts. |
| P1.0/TACLK | 12 | I/O | General-purpose digital I/O pin/Timer_A, clock signal TACLK input |
| P1.1/TA0 | 13 | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit |
| P1.2/TA1 | 14 | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output |
| P1.3/TA2 | 15 | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output |
| P1.4/SMCLK | 16 | I/O | General-purpose digital I/O pin/SMCLK signal output |
| P1.5/TA0 | 17 | I/O | General-purpose digital I/O pin/Timer_A, compare: Out0 output |
| P1.6/TA1 | 18 | I/O | General-purpose digital I/O pin/Timer_A, compare: Out1 output |
| P1.7/TA2 | 19 | I/O | General-purpose digital I/O pin/Timer_A, compare: Out2 output |
| P2.0/ACLK | 20 | I/O | General-purpose digital I/O pin/ACLK output |
| P2.1/TAINCLK | 21 | I/O | General-purpose digital I/O pin/Timer_A, clock signal at INCLK |
| P2.2/CAOUT/TA0 | 22 | I/O | General-purpose digital I/O pin/Timer_A, capture: CCI0B input/Comparator_A output/BSL receive |
| P2.3/CA0/TA1 | 23 | I/O | General-purpose digital I/O pin/Timer_A, compare: Out1 output/Comparator_A input |
| P2.4/CA1/TA2 | 24 | I/O | General-purpose digital I/O pin/Timer_A, compare: Out2 output/Comparator_A input |
| P2.5/Rosc | 25 | I/O | General-purpose digital I/O pin/input for external resistor defining the DCO nominal frequency |
| P2.6/ADC12CLK/ DMAE0 | 26 | I/O | General-purpose digital I/O pin/conversion clock – 12-bit ADC/DMA channel 0 external trigger |
| P2.7/TA0 | 27 | I/O | General-purpose digital I/O pin/Timer_A, compare: Out0 output |
| P3.0/STE0 | 28 | I/O | General-purpose digital I/O pin/slave transmit enable – USART0/SPI mode |
| P3.1/SIM00/SDA | 29 | I/O | General-purpose digital I/O pin/slave in/master out of USART0/SPI mode, I ² C data – USART0/I ² C mode |
| P3.2/SOMI0 | 30 | I/O | General-purpose digital I/O pin/slave out/master in of USART0/SPI mode |
| P3.3/UCLK0/SCL | 31 | I/O | General-purpose digital I/O pin/external clock input – USART0/UART or SPI mode, clock output – USART0/SPI mode, I ² C clock – USART0/I ² C mode |
| P3.4/UTXD0 | 32 | I/O | General-purpose digital I/O pin/transmit data out – USART0/UART mode |
| P3.5/URXD0 | 33 | I/O | General-purpose digital I/O pin/receive data in – USART0/UART mode |
| P3.6/UTXD1† | 34 | I/O | General-purpose digital I/O pin/transmit data out – USART1/UART mode |
| P3.7/URXD1† | 35 | I/O | General-purpose digital I/O pin/receive data in – USART1/UART mode |
| P4.0/TB0 | 36 | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI0A/B input, compare: Out0 output |
| P4.1/TB1 | 37 | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI1A/B input, compare: Out1 output |
| P4.2/TB2 | 38 | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI2A/B input, compare: Out2 output |
| P4.3/TB3† | 39 | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI3A/B input, compare: Out3 output |
| P4.4/TB4† | 40 | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI4A/B input, compare: Out4 output |
| P4.5/TB5† | 41 | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI5A/B input, compare: Out5 output |
| P4.6/TB6† | 42 | I/O | General-purpose digital I/O pin/Timer_B, capture: CCI6A input, compare: Out6 output |
| P4.7/TBCLK | 43 | I/O | General-purpose digital I/O pin/Timer_B, clock signal TBCLK input |
| P5.0/STE1† | 44 | I/O | General-purpose digital I/O pin/slave transmit enable – USART1/SPI mode |
| P5.1/SIM01† | 45 | I/O | General-purpose digital I/O pin/slave in/master out of USART1/SPI mode |
| P5.2/SOMI1† | 46 | I/O | General-purpose digital I/O pin/slave out/master in of USART1/SPI mode |
| P5.3/UCLK1† | 47 | I/O | General-purpose digital I/O pin/external clock input – USART1/UART or SPI mode, clock output – USART1/SPI mode |

† 16x, 161x devices only



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

Terminal Functions (Continued)

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|--------------------------------------|-----|-----|--|
| P5.4/MCLK | 48 | I/O | General-purpose digital I/O pin/main system clock MCLK output |
| P5.5/SMCLK | 49 | I/O | General-purpose digital I/O pin/submain system clock SMCLK output |
| P5.6/ACLK | 50 | I/O | General-purpose digital I/O pin/auxiliary clock ACLK output |
| P5.7/TBOOUTH/ SVSOUT | 51 | I/O | General-purpose digital I/O pin/switch all PWM digital output ports to high impedance – Timer_B TB0 to TB6/SVS comparator output |
| P6.0/A0 | 59 | I/O | General-purpose digital I/O pin/analog input a0 – 12-bit ADC |
| P6.1/A1 | 60 | I/O | General-purpose digital I/O pin/analog input a1 – 12-bit ADC |
| P6.2/A2 | 61 | I/O | General-purpose digital I/O pin/analog input a2 – 12-bit ADC |
| P6.3/A3 | 2 | I/O | General-purpose digital I/O pin/analog input a3 – 12-bit ADC |
| P6.4/A4 | 3 | I/O | General-purpose digital I/O pin/analog input a4 – 12-bit ADC |
| P6.5/A5 | 4 | I/O | General-purpose digital I/O pin/analog input a5 – 12-bit ADC |
| P6.6/A6/DAC0 | 5 | I/O | General-purpose digital I/O pin/analog input a6 – 12-bit ADC/DAC12.0 output |
| P6.7/A7/DAC1/ SVSIN | 6 | I/O | General-purpose digital I/O pin/analog input a7 – 12-bit ADC/DAC12.1 output/SVS input |
| RST/NMI | 58 | I | Reset input, nonmaskable interrupt input port, or bootstrap loader start (in Flash devices). |
| TCK | 57 | I | Test clock. TCK is the clock input port for device programming test and bootstrap loader start |
| TDI/TCLK | 55 | I | Test data input or test clock input. The device protection fuse is connected to TDI/TCLK. |
| TDO/TDI | 54 | I/O | Test data output port. TDO/TDI data output or programming data input terminal |
| TMS | 56 | I | Test mode select. TMS is used as an input port for device programming and test. |
| V _{REF+} | 10 | I | Input for an external reference voltage |
| V _{REF+} | 7 | O | Output of positive terminal of the reference voltage in the ADC12 |
| V _{REF-} /V _{REF-} | 11 | I | Negative terminal for the reference voltage for both sources, the internal reference voltage, or an external applied reference voltage |
| XIN | 8 | I | Input port for crystal oscillator XT1. Standard or watch crystals can be connected. |
| XOUT | 9 | O | Output terminal of crystal oscillator XT1 |
| XT2IN | 53 | I | Input port for crystal oscillator XT2. Only standard crystals can be connected. |
| XT2OUT | 52 | O | Output terminal of crystal oscillator XT2 |
| QFN Pad | NA | NA | QFN package pad connection to DV _{SS} recommended (RTD package only) |

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; Table 2 shows the address modes.

| | |
|--------------------------|-----------|
| Program Counter | PC/R0 |
| Stack Pointer | SP/R1 |
| Status Register | SR/CG1/R2 |
| Constant Generator | CG2/R3 |
| General-Purpose Register | R4 |
| General-Purpose Register | R5 |
| General-Purpose Register | R6 |
| General-Purpose Register | R7 |
| General-Purpose Register | R8 |
| General-Purpose Register | R9 |
| General-Purpose Register | R10 |
| General-Purpose Register | R11 |
| General-Purpose Register | R12 |
| General-Purpose Register | R13 |
| General-Purpose Register | R14 |
| General-Purpose Register | R15 |

Table 1. Instruction Word Formats

| | | |
|-----------------------------------|-----------------|-------------------------|
| Dual operands, source-destination | e.g., ADD R4,R5 | R4 + R5 ----> R5 |
| Single operands, destination only | e.g., CALL R8 | PC --->(TOS), R8---> PC |
| Relative jump, un/conditional | e.g., JNE | Jump-on-equal bit = 0 |

Table 2. Address Mode Descriptions

| ADDRESS MODE | S | D | SYNTAX | EXAMPLE | OPERATION |
|------------------------|---|---|-----------------|------------------|------------------------------------|
| Register | ● | ● | MOV Rs,Rd | MOV R10,R11 | R10 --> R11 |
| Indexed | ● | ● | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5)---> M(6+R6) |
| Symbolic (PC relative) | ● | ● | MOV EDE,TONI | | M(EDE) ---> M(TONI) |
| Absolute | ● | ● | MOV &MEM,&TCDAT | | M(MEM) ---> M(TCDAT) |
| Indirect | ● | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) ---> M(Tab+R6) |
| Indirect autoincrement | ● | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) ---> R11 R10 + 2---> R10 |
| Immediate | ● | | MOV #X,TONI | MOV #45,TONI | #45 ---> M(TONI) |

NOTE: S = source D = destination



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - ACLK and SMCLK remain active. MCLK is disabled
 - DCO's dc generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc generator remains enabled
 - ACLK remains active
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc generator is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc generator is disabled
 - Crystal oscillator is stopped

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|--|---|--------------|-------------|
| Power-up External Reset Watchdog Flash memory | WDTIFG KEYV (see Note 1) | Reset | 0FFFEh | 15, highest |
| NMI Oscillator Fault Flash memory access violation | NMIIFG (see Notes 1 and 3) OFIFG (see Notes 1 and 3) ACCVIFG (see Notes 1 and 3) | (Non)maskable (Non)maskable (Non)maskable | 0FFFCh | 14 |
| Timer_B7 (see Note 5) | TBCCR0 CCIFG (see Note 2) | Maskable | 0FFFAh | 13 |
| Timer_B7 (see Note 5) | TBCCR1 to TBCCR6 CCIFGs, TBIFG (see Notes 1 and 2) | Maskable | 0FFF8h | 12 |
| Comparator_A | CAIFG | Maskable | 0FFF6h | 11 |
| Watchdog timer | WDTIFG | Maskable | 0FFF4h | 10 |
| USART0 receive | URXIFG0 | Maskable | 0FFF2h | 9 |
| USART0 transmit I ² C transmit/receive/others | UTXIFG0 I2CIFG (see Note 4) | Maskable | 0FFF0h | 8 |
| ADC12 | ADC12IFG (see Notes 1 and 2) | Maskable | 0FFEEh | 7 |
| Timer_A3 | TACCR0 CCIFG (see Note 2) | Maskable | 0FFECCh | 6 |
| Timer_A3 | TACCR1 and TACCR2 CCIFGs, TAIFG (see Notes 1 and 2) | Maskable | 0FFEAh | 5 |
| I/O port P1 (eight flags) | P1IFG.0 to P1IFG.7 (see Notes 1 and 2) | Maskable | 0FFE8h | 4 |
| USART1 receive | URXIFG1 | Maskable | 0FFE6h | 3 |
| USART1 transmit | UTXIFG1 | Maskable | 0FFE4h | 2 |
| I/O port P2 (eight flags) | P2IFG.0 to P2IFG.7 (see Notes 1 and 2) | Maskable | 0FFE2h | 1 |
| DAC12 DMA | DAC12_0IFG, DAC12_1IFG DMA0IFG, DMA1IFG, DMA2IFG (see Notes 1 and 2) | Maskable | 0FFE0h | 0, lowest |

- NOTES:
- Multiple source flags
 - Interrupt flags are located in the module.
 - (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
 - I²C interrupt flags located in the module
 - Timer_B7 in MSP430F16x/161x family has 7 CCRs; Timer_B3 in MSP430F15x family has 3 CCRs; in Timer_B3 there are only interrupt flags TBCCR0, 1 and 2 CCIFGs and the interrupt-enable bits TBCCR0, 1 and 2 CCIEs.



special function registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|-------|---|---|------|-------|
| 0h | UTXIE0 | URXIE0 | ACCVIE | NMIIE | | | OFIE | WDTIE |
| | rw-0 | rw-0 | rw-0 | rw-0 | | | rw-0 | rw-0 |

WDTIE: Watchdog timer interrupt enable. Inactive if watchdog mode is selected.
Active if watchdog timer is configured as general-purpose timer.

OFIE: Oscillator fault interrupt enable

NMIIE: Nonmaskable interrupt enable

ACCVIE: Flash memory access violation interrupt enable

URXIE0: USART0: UART and SPI receive-interrupt enable

UTXIE0: USART0: UART and SPI transmit-interrupt enable

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|--------|--------|---|---|---|---|
| 01h | | | UTXIE1 | URXIE1 | | | | |
| | | | rw-0 | rw-0 | | | | |

URXIE1†: USART1: UART and SPI receive interrupt enable

UTXIE1†: USART1: UART and SPI transmit interrupt enable

† URXIE1 and UTXIE1 are not present in MSP430F15x devices.

interrupt flag register 1 and 2

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---|--------|---|---|-------|--------|
| 02h | UTXIFG0 | URXIFG0 | | NMIIFG | | | OFIFG | WDTIFG |
| | rw-1 | rw-0 | | rw-0 | | | rw-1 | rw-(0) |

WDTIFG: Set on watchdog-timer overflow (in watchdog mode) or security key violation
Reset on V_{CC} power-on, or a reset condition at the RST/NMI pin in reset mode

OFIFG: Flag set on oscillator fault

NMIIFG: Set via RST/NMI pin

URXIFG0: USART0: UART and SPI receive flag

UTXIFG0: USART0: UART and SPI transmit flag

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---------|---------|---|---|---|---|
| 03h | | | UTXIFG1 | URXIFG1 | | | | |
| | | | rw-1 | rw-0 | | | | |

URXIFG1‡: USART1: UART and SPI receive flag

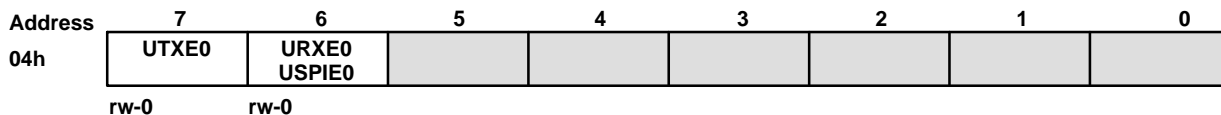
UTXIFG1‡: USART1: UART and SPI transmit flag

‡ URXIFG1 and UTXIFG1 are not present in MSP430F15x devices.

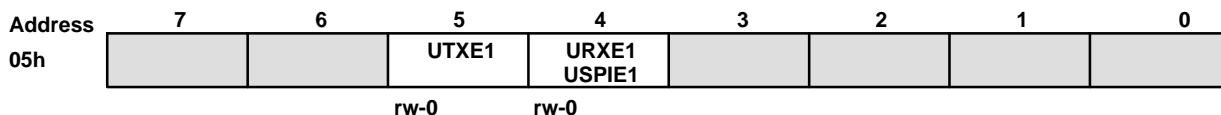
MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

module enable registers 1 and 2



- URXE0: USART0: UART mode receive enable
- UTXE0: USART0: UART mode transmit enable
- USPIE0: USART0: SPI mode transmit and receive enable



- URXE1†: USART1: UART mode receive enable
- UTXE1†: USART1: UART mode transmit enable
- USPIE1†: USART1: SPI mode transmit and receive enable

† URXE1, UTXE1, and USPIE1 are not present in MSP430F15x devices.

Legend: rw: Bit Can Be Read and Written
 rw-0: Bit Can Be Read and Written. It Is Reset by PUC.
 SFR Bit Not Present in Device



MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

memory organization, MSP430F15x

| | | MSP430F155 | MSP430F156 | MSP430F157 |
|---|---------------|-----------------------------|-----------------------------|-----------------------------|
| Memory Main: interrupt vector Main: code memory | Size Flash | 16KB 0FFFFh – 0FFE0h | 24KB 0FFFFh – 0FFE0h | 32KB 0FFFFh – 0FFE0h |
| | Flash | 0FFFFh – 0C000h | 0FFFFh – 0A000h | 0FFFFh – 08000h |
| Information memory | Size Flash | 256 Byte 010FFh – 01000h | 256 Byte 010FFh – 01000h | 256 Byte 010FFh – 01000h |
| Boot memory | Size ROM | 1KB 0FFFh – 0C00h | 1KB 0FFFh – 0C00h | 1KB 0FFFh – 0C00h |
| RAM | Size | 512B 03FFh – 0200h | 1KB 05FFh – 0200h | 1KB 05FFh – 0200h |
| Peripherals | 16-bit | 01FFh – 0100h | 01FFh – 0100h | 01FFh – 0100h |
| | 8-bit | 0FFh – 010h | 0FFh – 010h | 0FFh – 010h |
| | 8-bit SFR | 0Fh – 00h | 0Fh – 00h | 0Fh – 00h |

memory organization, MSP430F16x

| | | MSP430F167 | MSP430F168 | MSP430F169 |
|---|---------------|-----------------------------|-----------------------------|-----------------------------|
| Memory Main: interrupt vector Main: code memory | Size Flash | 32KB 0FFFFh – 0FFE0h | 48KB 0FFFFh – 0FFE0h | 60KB 0FFFFh – 0FFE0h |
| | Flash | 0FFFFh – 08000h | 0FFFFh – 04000h | 0FFFFh – 01100h |
| Information memory | Size Flash | 256 Byte 010FFh – 01000h | 256 Byte 010FFh – 01000h | 256 Byte 010FFh – 01000h |
| Boot memory | Size ROM | 1KB 0FFFh – 0C00h | 1KB 0FFFh – 0C00h | 1KB 0FFFh – 0C00h |
| RAM | Size | 1KB 05FFh – 0200h | 2KB 09FFh – 0200h | 2KB 09FFh – 0200h |
| Peripherals | 16-bit | 01FFh – 0100h | 01FFh – 0100h | 01FFh – 0100h |
| | 8-bit | 0FFh – 010h | 0FFh – 010h | 0FFh – 010h |
| | 8-bit SFR | 0Fh – 00h | 0Fh – 00h | 0Fh – 00h |

memory organization, MSP430F161x

| | | MSP430F1610 | MSP430F1611 | MSP430F1612 |
|---|---------------|-----------------------------|-----------------------------|-----------------------------|
| Memory Main: interrupt vector Main: code memory | Size Flash | 32KB 0FFFFh – 0FFE0h | 48KB 0FFFFh – 0FFE0h | 55KB 0FFFFh – 0FFE0h |
| | Flash | 0FFFFh – 08000h | 0FFFFh – 04000h | 0FFFFh – 02500h |
| RAM (Total) | Size | 5KB 024FFh – 01100h | 10KB 038FFh – 01100h | 5KB 024FFh – 01100h |
| Extended | Size | 3KB 024FFh – 01900h | 8KB 038FFh – 01900h | 3KB 024FFh – 01900h |
| Mirrored | Size | 2KB 018FFh – 01100h | 2KB 018FFh – 01100h | 2KB 018FFh – 01100h |
| Information memory | Size Flash | 256 Byte 010FFh – 01000h | 256 Byte 010FFh – 01000h | 256 Byte 010FFh – 01000h |
| Boot memory | Size ROM | 1KB 0FFFh – 0C00h | 1KB 0FFFh – 0C00h | 1KB 0FFFh – 0C00h |
| RAM (mirrored at 018FFh - 01100h) | Size | 2KB 09FFh – 0200h | 2KB 09FFh – 0200h | 2KB 09FFh – 0200h |
| Peripherals | 16-bit | 01FFh – 0100h | 01FFh – 0100h | 01FFh – 0100h |
| | 8-bit | 0FFh – 010h | 0FFh – 010h | 0FFh – 010h |
| | 8-bit SFR | 0Fh – 00h | 0Fh – 00h | 0Fh – 00h |



MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

| BSL FUNCTION | PM, RTD PACKAGE PINS |
|---------------|----------------------|
| Data Transmit | 13 - P1.1 |
| Data Receive | 22 - P2.2 |

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0 to n. Segments A and B are also called *information memory*.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.

| MSP430F15x and MSP430F16x | | | | | MSP430F161x | | | |
|---------------------------|--------|--------|--------|--------|-------------|--------|--------|----------------------|
| 16KB | 24KB | 32KB | 48KB | 60KB | 32KB | 48KB | 55KB | |
| 0FFFFh | 0FFFFh | 0FFFFh | 0FFFFh | 0FFFFh | 0FFFFh | 0FFFFh | 0FFFFh | Main Memory |
| 0FE00h | 0FE00h | 0FE00h | 0FE00h | 0FE00h | 0FE00h | 0FE00h | 0FE00h | |
| 0FDFFh | 0FDFFh | 0FDFFh | 0FDFFh | 0FDFFh | 0FDFFh | 0FDFFh | 0FDFFh | |
| 0FC00h | 0FC00h | 0FC00h | 0FC00h | 0FC00h | 0FC00h | 0FC00h | 0FC00h | |
| 0FBFFh | 0FBFFh | 0FBFFh | 0FBFFh | 0FBFFh | 0FBFFh | 0FBFFh | 0FBFFh | |
| 0FA00h | 0FA00h | 0FA00h | 0FA00h | 0FA00h | 0FA00h | 0FA00h | 0FA00h | |
| 0F9FFh | 0F9FFh | 0F9FFh | 0F9FFh | 0F9FFh | 0F9FFh | 0F9FFh | 0F9FFh | |
| 0C400h | 0A400h | 08400h | 04400h | 01400h | 08400h | 04400h | 02800h | |
| 0C3FFh | 0A3FFh | 083FFh | 043FFh | 013FFh | 083FFh | 043FFh | 027FFh | |
| 0C200h | 0A200h | 08200h | 04200h | 01200h | 08200h | 04200h | 02600h | |
| 0C1FFh | 0A1FFh | 081FFh | 041FFh | 011FFh | 081FFh | 041FFh | 025FFh | |
| 0C000h | 0A000h | 08000h | 04000h | 01100h | 08000h | 04000h | 02500h | RAM (*F161x only) |
| | | | | | 024FFh | 038FFh | 024FFh | |
| 010FFh | 010FFh | 010FFh | 010FFh | 010FFh | 01100h | 01100h | 01100h | Info Memory |
| | | | | | 010FFh | 010FFh | 010FFh | |
| 01080h | 01080h | 01080h | 01080h | 01080h | 01080h | 01080h | 01080h | |
| 0107Fh | 0107Fh | 0107Fh | 0107Fh | 0107Fh | 0107Fh | 0107Fh | 0107Fh | |
| 01000h | 01000h | 01000h | 01000h | 01000h | 01000h | 01000h | 01000h | |

† MSP430F169 and MSP430F1612 flash segment n = 256 bytes.

peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, see the *MSP430x1xx Family User's Guide*, literature number SLAU049.

DMA controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12 conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode without having to awaken to move data to or from a peripheral.

oscillator and system clock

The clock system in the MSP430F15x and MSP430F16x(x) family of devices is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low-power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 μ s. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

brownout, supply voltage supervisor (SVS)

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must insure the default DCO settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

digital I/O

There are six 8-bit I/O ports implemented—ports P1 through P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

hardware multiplier (MSP430F16x/161x only)

The multiplication operation is supported by a dedicated peripheral module. The module performs 16×16 , 16×8 , 8×16 , and 8×8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

USART0

The MSP430F15x and the MSP430F16x(x) have one hardware universal synchronous/asynchronous receive transmit (USART0) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin), asynchronous UART and I2C communication protocols using double-buffered transmit and receive channels.

The I²C support is compliant with the Philips I²C specification version 2.1 and supports standard mode (up to 100 kbps) and fast mode (up to 400 kbps). In addition, 7-bit and 10-bit device addressing modes are supported, as well as master and slave modes. The USART0 also supports 16-bit-wide I²C data transfers and has two dedicated DMA channels to maximize bus throughput. Extensive interrupt capability is also given in the I²C mode.

USART1 (MSP430F16x/161x only)

The MSP430F16x(x) devices have a second hardware universal synchronous/asynchronous receive transmit (USART1) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels. With the exception of I2C support, operation of USART1 is identical to USART0.

Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| TIMER_A3 SIGNAL CONNECTIONS | | | | | |
|-----------------------------|---------------------|-------------------|--------------|----------------------|-------------------|
| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
| 12 - P1.0 | TACLK | TACLK | Timer | NA | |
| | ACLK | ACLK | | | |
| | SMCLK | SMCLK | | | |
| 21 - P2.1 | TAINCLK | INCLK | | | |
| 13 - P1.1 | TA0 | CCI0A | CCR0 | TA0 | 13 - P1.1 |
| 22 - P2.2 | TA0 | CCI0B | | | 17 - P1.5 |
| | DV _{SS} | GND | | | 27 - P2.7 |
| | DV _{CC} | V _{CC} | | | |
| 14 - P1.2 | TA1 | CCI1A | CCR1 | TA1 | 14 - P1.2 |
| | CAOUT (internal) | CCI1B | | | 18 - P1.6 |
| | DV _{SS} | GND | | | 23 - P2.3 |
| | DV _{CC} | V _{CC} | | | ADC12 (internal) |
| 15 - P1.3 | TA2 | CCI2A | CCR2 | TA2 | 15 - P1.3 |
| | ACLK (internal) | CCI2B | | | 19 - P1.7 |
| | DV _{SS} | GND | | | 24 - P2.4 |
| | DV _{CC} | V _{CC} | | | |

Timer_B3 (MSP430F15x only)

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.



Timer_B7 (MSP430F16x/161x only)

Timer_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer_B7 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| TIMER_B3/B7 SIGNAL CONNECTIONS† | | | | | |
|---------------------------------|---------------------|-------------------|--------------|----------------------|-------------------|
| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
| 43 - P4.7 | TBCLK | TBCLK | Timer | NA | |
| | ACLK | ACLK | | | |
| | SMCLK | SMCLK | | | |
| 43 - P4.7 | TBCLK | INCLK | | | |
| 36 - P4.0 | TB0 | CCI0A | CCR0 | TB0 | 36 - P4.0 |
| 36 - P4.0 | TB0 | CCI0B | | | ADC12 (internal) |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |
| 37 - P4.1 | TB1 | CCI1A | CCR1 | TB1 | 37 - P4.1 |
| 37 - P4.1 | TB1 | CCI1B | | | ADC12 (internal) |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |
| 38 - P4.2 | TB2 | CCI2A | CCR2 | TB2 | 38 - P4.2 |
| 38 - P4.2 | TB2 | CCI2B | | | |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |
| 39 - P4.3 | TB3 | CCI3A | CCR3 | TB3 | 39 - P4.3 |
| 39 - P4.3 | TB3 | CCI3B | | | |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |
| 40 - P4.4 | TB4 | CCI4A | CCR4 | TB4 | 40 - P4.4 |
| 40 - P4.4 | TB4 | CCI4B | | | |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |
| 41 - P4.5 | TB5 | CCI5A | CCR5 | TB5 | 41 - P4.5 |
| 41 - P4.5 | TB5 | CCI5B | | | |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |
| 42 - P4.6 | TB6 | CCI6A | CCR6 | TB6 | 42 - P4.6 |
| | ACLK (internal) | CCI6B | | | |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |

† Timer_B3 implements three capture/compare blocks (CCR0, CCR1 and CCR2 only).

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

Comparator_A

The primary function of the comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

ADC12

The ADC12 module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

DAC12

The DAC12 module is a 12-bit, R-ladder, voltage output DAC. The DAC12 may be used in 8- or 12-bit mode, and may be used in conjunction with the DMA controller. When multiple DAC12 modules are present, they may be grouped together for synchronous operation.



peripheral file map

| PERIPHERAL FILE MAP | | | |
|----------------------------|-----------------------------------|------------|-------|
| DMA | DMA channel 2 transfer size | DMA2SZ | 01F6h |
| | DMA channel 2 destination address | DMA2DA | 01F4h |
| | DMA channel 2 source address | DMA2SA | 01F2h |
| | DMA channel 2 control | DMA2CTL | 01F0h |
| | DMA channel 1 transfer size | DMA1SZ | 01EEh |
| | DMA channel 1 destination address | DMA1DA | 01ECh |
| | DMA channel 1 source address | DMA1SA | 01EAh |
| | DMA channel 1 control | DMA1CTL | 01E8h |
| | DMA channel 0 transfer size | DMA0SZ | 01E6h |
| | DMA channel 0 destination address | DMA0DA | 01E4h |
| | DMA channel 0 source address | DMA0SA | 01E2h |
| | DMA channel 0 control | DMA0CTL | 01E0h |
| | DMA module control 1 | DMACTL1 | 0124h |
| | DMA module control 0 | DMACTL0 | 0122h |
| DAC12 | DAC12_1 data | DAC12_1DAT | 01CAh |
| | DAC12_1 control | DAC12_1CTL | 01C2h |
| | DAC12_0 data | DAC12_0DAT | 01C8h |
| | DAC12_0 control | DAC12_0CTL | 01C0h |
| ADC12 | Interrupt-vector-word register | ADC12IV | 01A8h |
| | Interrupt-enable register | ADC12IE | 01A6h |
| | Interrupt-flag register | ADC12IFG | 01A4h |
| | Control register 1 | ADC12CTL1 | 01A2h |
| | Control register 0 | ADC12CTL0 | 01A0h |
| | Conversion memory 15 | ADC12MEM15 | 015Eh |
| | Conversion memory 14 | ADC12MEM14 | 015Ch |
| | Conversion memory 13 | ADC12MEM13 | 015Ah |
| | Conversion memory 12 | ADC12MEM12 | 0158h |
| | Conversion memory 11 | ADC12MEM11 | 0156h |
| | Conversion memory 10 | ADC12MEM10 | 0154h |
| | Conversion memory 9 | ADC12MEM9 | 0152h |
| | Conversion memory 8 | ADC12MEM8 | 0150h |
| | Conversion memory 7 | ADC12MEM7 | 014Eh |
| | Conversion memory 6 | ADC12MEM6 | 014Ch |
| | Conversion memory 5 | ADC12MEM5 | 014Ah |
| | Conversion memory 4 | ADC12MEM4 | 0148h |
| | Conversion memory 3 | ADC12MEM3 | 0146h |
| | Conversion memory 2 | ADC12MEM2 | 0144h |
| | Conversion memory 1 | ADC12MEM1 | 0142h |
| Conversion memory 0 | ADC12MEM0 | 0140h | |

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

peripheral file map (continued)

| PERIPHERAL FILE MAP (CONTINUED) | | | |
|--|-------------------------------|-------------|-------|
| ADC12 (continued) | ADC memory-control register15 | ADC12MCTL15 | 08Fh |
| | ADC memory-control register14 | ADC12MCTL14 | 08Eh |
| | ADC memory-control register13 | ADC12MCTL13 | 08Dh |
| | ADC memory-control register12 | ADC12MCTL12 | 08Ch |
| | ADC memory-control register11 | ADC12MCTL11 | 08Bh |
| | ADC memory-control register10 | ADC12MCTL10 | 08Ah |
| | ADC memory-control register9 | ADC12MCTL9 | 089h |
| | ADC memory-control register8 | ADC12MCTL8 | 088h |
| | ADC memory-control register7 | ADC12MCTL7 | 087h |
| | ADC memory-control register6 | ADC12MCTL6 | 086h |
| | ADC memory-control register5 | ADC12MCTL5 | 085h |
| | ADC memory-control register4 | ADC12MCTL4 | 084h |
| | ADC memory-control register3 | ADC12MCTL3 | 083h |
| | ADC memory-control register2 | ADC12MCTL2 | 082h |
| | ADC memory-control register1 | ADC12MCTL1 | 081h |
| | ADC memory-control register0 | ADC12MCTL0 | 080h |
| Timer_B7/ Timer_B3 (see Note 1) | Capture/compare register 6 | TBCCR6 | 019Eh |
| | Capture/compare register 5 | TBCCR5 | 019Ch |
| | Capture/compare register 4 | TBCCR4 | 019Ah |
| | Capture/compare register 3 | TBCCR3 | 0198h |
| | Capture/compare register 2 | TBCCR2 | 0196h |
| | Capture/compare register 1 | TBCCR1 | 0194h |
| | Capture/compare register 0 | TBCCR0 | 0192h |
| | Timer_B register | TBR | 0190h |
| | Capture/compare control 6 | TBCCTL6 | 018Eh |
| | Capture/compare control 5 | TBCCTL5 | 018Ch |
| | Capture/compare control 4 | TBCCTL4 | 018Ah |
| | Capture/compare control 3 | TBCCTL3 | 0188h |
| | Capture/compare control 2 | TBCCTL2 | 0186h |
| | Capture/compare control 1 | TBCCTL1 | 0184h |
| | Capture/compare control 0 | TBCCTL0 | 0182h |
| | Timer_B control | TBCTL | 0180h |
| Timer_B interrupt vector | TBIV | 011Eh | |
| Timer_A3 | Reserved | | 017Eh |
| | Reserved | | 017Ch |
| | Reserved | | 017Ah |
| | Reserved | | 0178h |
| | Capture/compare register 2 | TACCR2 | 0176h |
| | Capture/compare register 1 | TACCR1 | 0174h |
| | Capture/compare register 0 | TACCR0 | 0172h |
| | Timer_A register | TAR | 0170h |
| | Reserved | | 016Eh |
| | Reserved | | 016Ch |
| | Reserved | | 016Ah |
| Reserved | | 0168h | |

NOTE 1: Timer_B7 in MSP430F16x/161x family has seven CCRs, Timer_B3 in MSP430F15x family has three CCRs.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

peripheral file map (continued)

| PERIPHERAL FILE MAP (CONTINUED) | | | |
|--|--------------------------------------|---------|-------|
| Timer_A3 (continued) | Capture/compare control 2 | TACCTL2 | 0166h |
| | Capture/compare control 1 | TACCTL1 | 0164h |
| | Capture/compare control 0 | TACCTL0 | 0162h |
| | Timer_A control | TACTL | 0160h |
| | Timer_A interrupt vector | TAIV | 012Eh |
| Hardware Multiplier (MSP430F16x and MSP430F161x only) | Sum extend | SUMEXT | 013Eh |
| | Result high word | RESHI | 013Ch |
| | Result low word | RESLO | 013Ah |
| | Second operand | OP2 | 0138h |
| | Multiply signed +accumulate/operand1 | MACS | 0136h |
| | Multiply+accumulate/operand1 | MAC | 0134h |
| | Multiply signed/operand1 | MPYS | 0132h |
| | Multiply unsigned/operand1 | MPY | 0130h |
| Flash | Flash control 3 | FCTL3 | 012Ch |
| | Flash control 2 | FCTL2 | 012Ah |
| | Flash control 1 | FCTL1 | 0128h |
| Watchdog | Watchdog Timer control | WDTCTL | 0120h |
| USART1 (MSP430F16x and MSP430F161x only) | Transmit buffer | U1TXBUF | 07Fh |
| | Receive buffer | U1RXBUF | 07Eh |
| | Baud rate | U1BR1 | 07Dh |
| | Baud rate | U1BR0 | 07Ch |
| | Modulation control | U1MCTL | 07Bh |
| | Receive control | U1RCTL | 07Ah |
| | Transmit control | U1TCTL | 079h |
| | USART control | U1CTL | 078h |
| USART0 (UART or SPI mode) | Transmit buffer | U0TXBUF | 077h |
| | Receive buffer | U0RXBUF | 076h |
| | Baud rate | U0BR1 | 075h |
| | Baud rate | U0BR0 | 074h |
| | Modulation control | U0MCTL | 073h |
| | Receive control | U0RCTL | 072h |
| | Transmit control | U0TCTL | 071h |
| | USART control | U0CTL | 070h |
| USART0 (I²C mode) | I2C interrupt vector | I2CIV | 011Ch |
| | I2C slave address | I2CSA | 011Ah |
| | I2C own address | I2COA | 0118h |
| | I2C data | I2CDR | 076h |
| | I2C SCLL | I2CSCLL | 075h |
| | I2C SCLH | I2CSCLH | 074h |
| | I2C PSC | I2CPSC | 073h |
| | I2C data control | I2CDCTL | 072h |
| | I2C transfer control | I2CTCTL | 071h |
| | USART control | U0CTL | 070h |
| | I2C data count | I2CNDAT | 052h |
| | I2C interrupt flag | I2CIFG | 051h |
| | I2C interrupt enable | I2CIE | 050h |

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

peripheral file map (continued)

| PERIPHERAL FILE MAP (CONTINUED) | | | |
|---------------------------------|---|---------------------|-------|
| Comparator_A | Comparator_A port disable | CAPD | 05Bh |
| | Comparator_A control2 | CACTL2 | 05Ah |
| | Comparator_A control1 | CACTL1 | 059h |
| Basic Clock | Basic clock system control2 | BCSCTL2 | 058h |
| | Basic clock system control1 | BCSCTL1 | 057h |
| | DCO clock frequency control | DCOCTL | 056h |
| BrownOUT, SVS | SVS control register (reset by brownout signal) | SVSCTL | 055h |
| Port P6 | Port P6 selection | P6SEL | 037h |
| | Port P6 direction | P6DIR | 036h |
| | Port P6 output | P6OUT | 035h |
| | Port P6 input | P6IN | 034h |
| Port P5 | Port P5 selection | P5SEL | 033h |
| | Port P5 direction | P5DIR | 032h |
| | Port P5 output | P5OUT | 031h |
| | Port P5 input | P5IN | 030h |
| Port P4 | Port P4 selection | P4SEL | 01Fh |
| | Port P4 direction | P4DIR | 01Eh |
| | Port P4 output | P4OUT | 01Dh |
| | Port P4 input | P4IN | 01Ch |
| Port P3 | Port P3 selection | P3SEL | 01Bh |
| | Port P3 direction | P3DIR | 01Ah |
| | Port P3 output | P3OUT | 019h |
| | Port P3 input | P3IN | 018h |
| Port P2 | Port P2 selection | P2SEL | 02Eh |
| | Port P2 interrupt enable | P2IE | 02Dh |
| | Port P2 interrupt-edge select | P2IES | 02Ch |
| | Port P2 interrupt flag | P2IFG | 02Bh |
| | Port P2 direction | P2DIR | 02Ah |
| | Port P2 output | P2OUT | 029h |
| | Port P2 input | P2IN | 028h |
| | Port P1 | Port P1 selection | P1SEL |
| Port P1 interrupt enable | | P1IE | 025h |
| Port P1 interrupt-edge select | | P1IES | 024h |
| Port P1 interrupt flag | | P1IFG | 023h |
| Port P1 direction | | P1DIR | 022h |
| Port P1 output | | P1OUT | 021h |
| Port P1 input | | P1IN | 020h |
| Special Functions | | SFR module enable 2 | ME2 |
| | SFR module enable 1 | ME1 | 004h |
| | SFR interrupt flag2 | IFG2 | 003h |
| | SFR interrupt flag1 | IFG1 | 002h |
| | SFR interrupt enable2 | IE2 | 001h |
| | SFR interrupt enable1 | IE1 | 000h |



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

| | |
|--|----------------------------|
| Voltage applied at V_{CC} to V_{SS} | -0.3 V to 4.1 V |
| Voltage applied to any pin (see Note) | -0.3 V to $V_{CC} + 0.3$ V |
| Diode current at any device terminal | ± 2 mA |
| Storage temperature, T_{stg} : Unprogrammed device | -55°C to 150°C |
| Programmed device | -55°C to 85°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS} . The JTAG fuse-blow voltage, V_{FB} , is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|--|------|--------|------|------|
| Supply voltage during program execution, V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$) | MSP430F15x/16x/161x | 1.8 | | 3.6 | V |
| Supply voltage during flash memory programming, V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$) | MSP430F15x/16x/161x | 2.7 | | 3.6 | V |
| Supply voltage during program execution, SVS enabled (see Note 1), V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$) | MSP430F15x/16x/161x | 2 | | 3.6 | V |
| Supply voltage, V_{SS} ($AV_{SS} = DV_{SS} = V_{SS}$) | | 0 | | 0 | V |
| Operating free-air temperature range, T_A | MSP430F15x/16x/161x | -40 | | 85 | °C |
| LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Notes 2 and 3) | LF selected, XTS=0 Watch crystal | | 32.768 | | kHz |
| | XT1 selected, XTS=1 Ceramic resonator | 450 | | 8000 | |
| | XT1 selected, XTS=1 Crystal | 1000 | | 8000 | |
| XT2 crystal frequency, $f_{(XT2)}$ | Ceramic resonator | | 450 | 8000 | kHz |
| | Crystal | | 1000 | 8000 | |
| Processor frequency (signal MCLK), $f_{(System)}$ | $V_{CC} = 1.8$ V | | DC | 4.15 | MHz |
| | $V_{CC} = 3.6$ V | | DC | 8 | |

- NOTES: 1. The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing the supply voltage. POR is going inactive when the V_{CC} is raised above the minimum supply voltage plus the hysteresis of the SVS circuitry.
2. In LF mode, the LFXT1 oscillator requires a watch crystal. A 5.1-M Ω resistor from XOUT to V_{SS} is recommended when $V_{CC} < 2.5$ V. In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or crystal up to 4.15 MHz at $V_{CC} \geq 2.2$ V. In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or crystal up to 8 MHz at $V_{CC} \geq 2.8$ V.
3. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

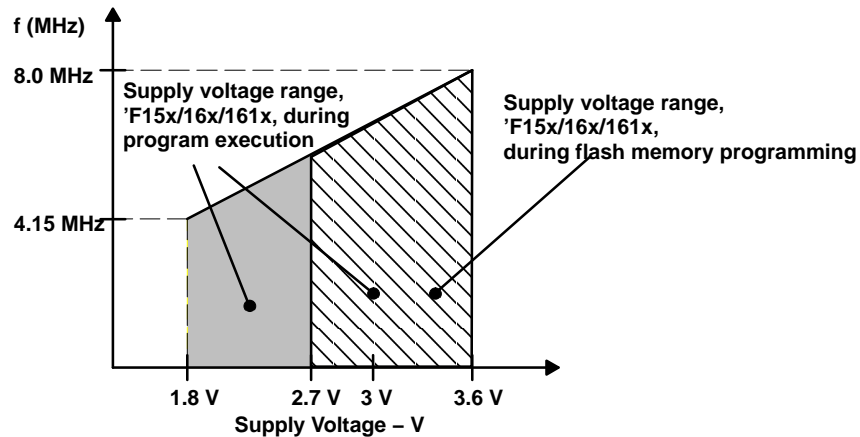


Figure 1. Frequency vs Supply Voltage, MSP430F15x/16x/161x

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

MSP430F15x/16x supply current into $AV_{CC} + DV_{CC}$ excluding external current ($AV_{CC} = DV_{CC} = V_{CC}$)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|--------------|---|---|------------|-----|-----|---------------|------|
| $I_{(AM)}$ | Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)} = 1$ MHz, $f_{(ACLK)} = 32,768$ Hz XTS=0, SELM=(0,1) | $T_A = -40^{\circ}\text{C}$ to 85°C | 2.2 V | 330 | 400 | μA | |
| | | | 3 V | 500 | 600 | | |
| | Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)} = 4,096$ Hz, $f_{(ACLK)} = 4,096$ Hz XTS=0, SELM=3 | $T_A = -40^{\circ}\text{C}$ to 85°C | 2.2 V | 2.5 | 7 | μA | |
| | | | 3 V | 9 | 20 | | |
| $I_{(LPM0)}$ | Low-power mode, (LPM0) $f_{(MCLK)} = 0$ MHz, $f_{(SMCLK)} = 1$ MHz, $f_{(ACLK)} = 32,768$ Hz XTS=0, SELM=(0,1) (see Note 1) | $T_A = -40^{\circ}\text{C}$ to 85°C | 2.2 V | 50 | 60 | μA | |
| | | | 3 V | 75 | 90 | | |
| $I_{(LPM2)}$ | Low-power mode, (LPM2), $f_{(MCLK)} = f_{(SMCLK)} = 0$ MHz, $f_{(ACLK)} = 32,768$ Hz, SCG0 = 0 | $T_A = -40^{\circ}\text{C}$ to 85°C | 2.2 V | 11 | 14 | μA | |
| | | | 3 V | 17 | 22 | | |
| $I_{(LPM3)}$ | Low-power mode, (LPM3) $f_{(MCLK)} = f_{(SMCLK)} = 0$ MHz, $f_{(ACLK)} = 32,768$ Hz, SCG0 = 1 (see Note 2) | $T_A = -40^{\circ}\text{C}$ | 2.2 V | 1.1 | 1.6 | μA | |
| | | $T_A = 25^{\circ}\text{C}$ | | 1.1 | 1.6 | | |
| | | $T_A = 85^{\circ}\text{C}$ | | 2.2 | 3.0 | | |
| | | $T_A = -40^{\circ}\text{C}$ | 3 V | 2.2 | 2.8 | | |
| | | $T_A = 25^{\circ}\text{C}$ | | 2.0 | 2.6 | | |
| | | $T_A = 85^{\circ}\text{C}$ | | 3.0 | 4.3 | | |
| $I_{(LPM4)}$ | Low-power mode, (LPM4) $f_{(MCLK)} = 0$ MHz, $f_{(SMCLK)} = 0$ MHz, $f_{(ACLK)} = 0$ Hz, SCG0 = 1 | $T_A = -40^{\circ}\text{C}$ | 2.2V / 3 V | 0.1 | 0.5 | μA | |
| | | $T_A = 25^{\circ}\text{C}$ | | 0.2 | 0.5 | | |
| | | $T_A = 85^{\circ}\text{C}$ | | 1.3 | 2.5 | | |

NOTES: 1. Timer_B is clocked by $f_{(DCOCLK)} = 1$ MHz. All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
2. WDT is clocked by $f_{(ACLK)} = 32,768$ Hz. All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current. The current consumption in LPM2 and LPM3 are measured with ACLK selected.

Current consumption of active mode versus system frequency

$$I_{(AM)} = I_{(AM)} [1 \text{ MHz}] \times f(\text{System}) [\text{MHz}]$$

Current consumption of active mode versus supply voltage

$$I_{(AM)} = I_{(AM)} [3 \text{ V}] + 210 \mu\text{A/V} \times (V_{CC} - 3 \text{ V})$$



electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

MSP430F161x supply current into $AV_{CC} + DV_{CC}$ excluding external current ($AV_{CC} = DV_{CC} = V_{CC}$)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT | |
|--------------|---|---|------------|----------------------------|-----|-----|---------------|-----|
| $I_{(AM)}$ | Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)} = 1$ MHz, $f_{(ACLK)} = 32,768$ Hz XTS=0, SELM=(0,1) | $T_A = -40^{\circ}\text{C}$ to 85°C | 2.2 V | | 330 | 400 | μA | |
| | | | 3 V | | 500 | 600 | | |
| | Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)} = 4,096$ Hz, $f_{(ACLK)} = 4,096$ Hz XTS=0, SELM=3 | $T_A = -40^{\circ}\text{C}$ to 85°C | 2.2 V | | 2.5 | 7 | μA | |
| | | | 3 V | | 9 | 20 | | |
| $I_{(LPM0)}$ | Low-power mode, (LPM0) $f_{(MCLK)} = 0$ MHz, $f_{(SMCLK)} = 1$ MHz, $f_{(ACLK)} = 32,768$ Hz XTS=0, SELM=(0,1) (see Note 1) | $T_A = -40^{\circ}\text{C}$ to 85°C | 2.2 V | | 50 | 60 | μA | |
| | | | 3 V | | 75 | 95 | | |
| $I_{(LPM2)}$ | Low-power mode, (LPM2), $f_{(MCLK)} = f_{(SMCLK)} = 0$ MHz, $f_{(ACLK)} = 32,768$ Hz, SCG0 = 0 | $T_A = -40^{\circ}\text{C}$ to 85°C | 2.2 V | | 11 | 14 | μA | |
| | | | 3 V | | 17 | 22 | | |
| $I_{(LPM3)}$ | Low-power mode, (LPM3) $f_{(MCLK)} = f_{(SMCLK)} = 0$ MHz, $f_{(ACLK)} = 32,768$ Hz, SCG0 = 1 (see Note 2) | $T_A = -40^{\circ}\text{C}$ | 2.2 V | | 1.3 | 1.6 | μA | |
| | | | | $T_A = 25^{\circ}\text{C}$ | | 1.3 | | 1.6 |
| | | | | $T_A = 85^{\circ}\text{C}$ | | 3.0 | | 6.0 |
| | | $T_A = -40^{\circ}\text{C}$ | 3 V | | 2.6 | 3.0 | | |
| | | | | $T_A = 25^{\circ}\text{C}$ | | 2.6 | | 3.0 |
| | | | | $T_A = 85^{\circ}\text{C}$ | | 4.4 | | 8.0 |
| $I_{(LPM4)}$ | Low-power mode, (LPM4) $f_{(MCLK)} = 0$ MHz, $f_{(SMCLK)} = 0$ MHz, $f_{(ACLK)} = 0$ Hz, SCG0 = 1 | $T_A = -40^{\circ}\text{C}$ | 2.2V / 3 V | | 0.2 | 0.5 | μA | |
| | | | | $T_A = 25^{\circ}\text{C}$ | | 0.2 | | 0.5 |
| | | | | $T_A = 85^{\circ}\text{C}$ | | 2.0 | | 5.0 |

- NOTES: 1. Timer_B is clocked by $f_{(DCOCLK)} = 1$ MHz. All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
2. WDT is clocked by $f_{(ACLK)} = 32,768$ Hz. All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current. The current consumption in LPM2 and LPM3 are measured with ACLK selected.

Current consumption of active mode versus system frequency

$$I_{(AM)} = I_{(AM)} [1 \text{ MHz}] \times f_{(\text{System})} [\text{MHz}]$$

Current consumption of active mode versus supply voltage

$$I_{(AM)} = I_{(AM)} [3 \text{ V}] + 210 \mu\text{A/V} \times (V_{CC} - 3 \text{ V})$$

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs – ports P1, P2, P3, P4, P5, P6, \overline{RST}/NMI , JTAG (TCK, TMS, TDI/TCLK, TDO/TDI)

| PARAMETER | | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------|---|-----------------|-----|-----|------|------|
| V _{IT+} | Positive-going input threshold voltage | 2.2 V | 1.1 | | 1.5 | V |
| | | 3 V | 1.5 | | 1.98 | |
| V _{IT-} | Negative-going input threshold voltage | 2.2 V | 0.4 | | 0.9 | V |
| | | 3 V | 0.9 | | 1.3 | |
| V _{hys} | Input voltage hysteresis (V _{IT+} – V _{IT-}) | 2.2 V | 0.3 | | 1.1 | V |
| | | 3 V | 0.5 | | 1 | |

inputs Px.x, TA_x, TB_x

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------|--|--|-----------------|-----|-----|-----|------|
| t _(int) | External interrupt timing | Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag (see Note 1) | 2.2 V | 62 | | | ns |
| | | | 3 V | 50 | | | |
| t _(cap) | Timer_A, Timer_B capture timing | TA0, TA1, TA2 TB0, TB1, TB2, TB3, TB4, TB5, TB6 (see Note 2) | 2.2 V | 62 | | | ns |
| | | | 3 V | 50 | | | |
| f _(TAext) | Timer_A, Timer_B clock frequency externally applied to pin | TACLK, TBCLK, INCLK: t _(H) = t _(L) | 2.2 V | | | 8 | MHz |
| f _(TBext) | | | 3 V | | | 10 | |
| f _(TAint) | Timer_A, Timer_B clock frequency | SMCLK or ACLK signal selected | 2.2 V | | | 8 | MHz |
| f _(TBint) | | | 3 V | | | 10 | |

- NOTES: 1. The external signal sets the interrupt flag every time the minimum t_(int) parameters are met. It may be set even with trigger signals shorter than t_(int).
2. Seven capture/compare registers in 'F16x/161x and three capture/compare registers in 'F15x.

leakage current – ports P1, P2, P3, P4, P5, P6 (see Note 1)

| PARAMETER | | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|-----------------|---------|----------------------------------|-----------------|-----|-----|-----|------|
| I _{lkg(Px.y)} | Leakage current | Port Px | V _(Px.y) (see Note 2) | 2.2 V/3 V | | | ±50 | nA |

- NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.



MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – ports P1, P2, P3, P4, P5, P6

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|-----------------|---------------------------|---|-----------------------|--|-----------------------|-----|-----|------|
| V _{OH} | High-level output voltage | I _{OH(max)} = -1.5 mA, V _{CC} = 2.2 V, See Note 1 | V _{CC} -0.25 | | V _{CC} | | V | |
| | | I _{OH(max)} = -6 mA, V _{CC} = 2.2 V, See Note 2 | V _{CC} -0.6 | | V _{CC} | | | |
| | | I _{OH(max)} = -1.5 mA, V _{CC} = 3 V, See Note 1 | V _{CC} -0.25 | | V _{CC} | | | |
| | | I _{OH(max)} = -6 mA, V _{CC} = 3 V, See Note 2 | V _{CC} -0.6 | | V _{CC} | | | |
| V _{OL} | Low-level output voltage | I _{OL(max)} = 1.5 mA, V _{CC} = 2.2 V, See Note 1 | V _{SS} | | V _{SS} +0.25 | | V | |
| | | I _{OL(max)} = 6 mA, V _{CC} = 2.2 V, See Note 2 | V _{SS} | | V _{SS} +0.6 | | | |
| | | I _{OL(max)} = 1.5 mA, V _{CC} = 3 V, See Note 1 | V _{SS} | | V _{SS} +0.25 | | | |
| | | I _{OL(max)} = 6 mA, V _{CC} = 3 V, See Note 2 | V _{SS} | | V _{SS} +0.6 | | | |

- NOTES: 1. The maximum total current, I_{OH(max)} and I_{OL(max)}, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
 2. The maximum total current, I_{OH(max)} and I_{OL(max)}, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

output frequency

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--|--|---|---|---------------|-----|---------------------|------|
| f _(Px.y) | (1 ≤ x ≤ 6, 0 ≤ y ≤ 7) | C _L = 20 pF, I _L = ±1.5 mA | V _{CC} = 2.2 V / 3 V | DC | | f _{System} | MHz |
| f _(ACLK) f _(MCLK) f _(SMCLK) | P2.0/ACLK, P5.6/ACLK P5.4/MCLK, P1.4/SMCLK, P5.5/SMCLK | C _L = 20 pF | V _{CC} = 2.2 V / 3 V | | | f _{System} | MHz |
| t _(Xdc) | Duty cycle of output frequency | P1.0/TACLK C _L = 20 pF V _{CC} = 2.2 V / 3 V | f _(ACLK) = f _(LFXT1) = f _(XT1) | 40% | | 60% | |
| | | | f _(ACLK) = f _(LFXT1) = f _(LF) | 30% | | 70% | |
| | | | f _(ACLK) = f _(LFXT1) | | 50% | | |
| | | P1.1/TA0/MCLK, C _L = 20 pF, V _{CC} = 2.2 V / 3 V | f _(MCLK) = f _(XT1) | 40% | | 60% | |
| | | | f _(MCLK) = f _(DCOCLK) | 50%– 15 ns | 50% | 50%+ 15 ns | |
| | | P1.4/TBCLK/SMCLK, C _L = 20 pF, V _{CC} = 2.2 V / 3 V | f _(SMCLK) = f _(XT2) | 40% | | 60% | |
| f _(SMCLK) = f _(DCOCLK) | 50%– 15 ns | 50% | 50%+ 15 ns | | | | |

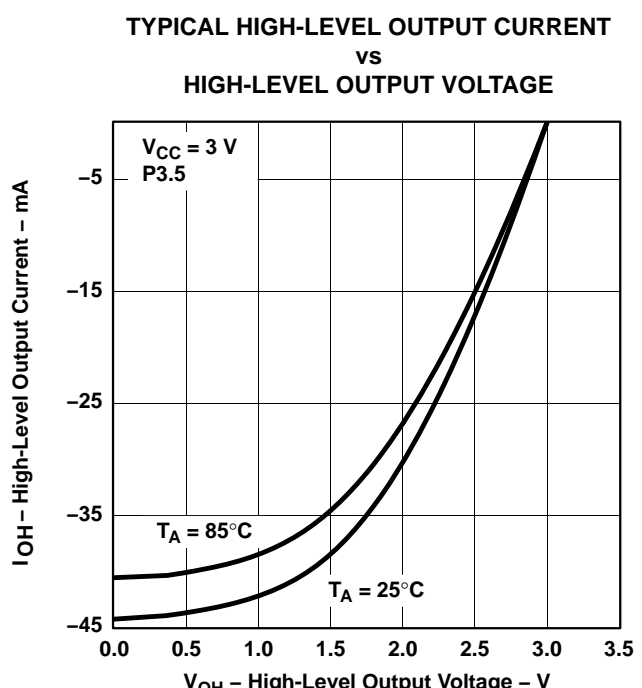
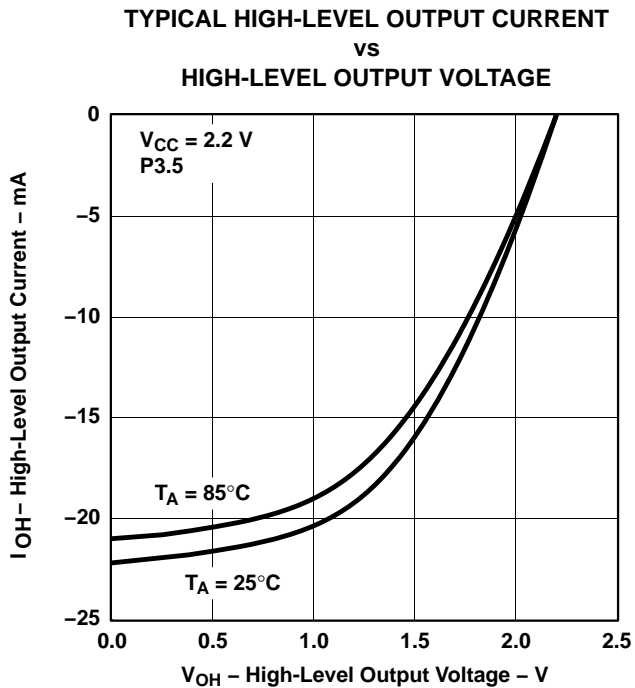
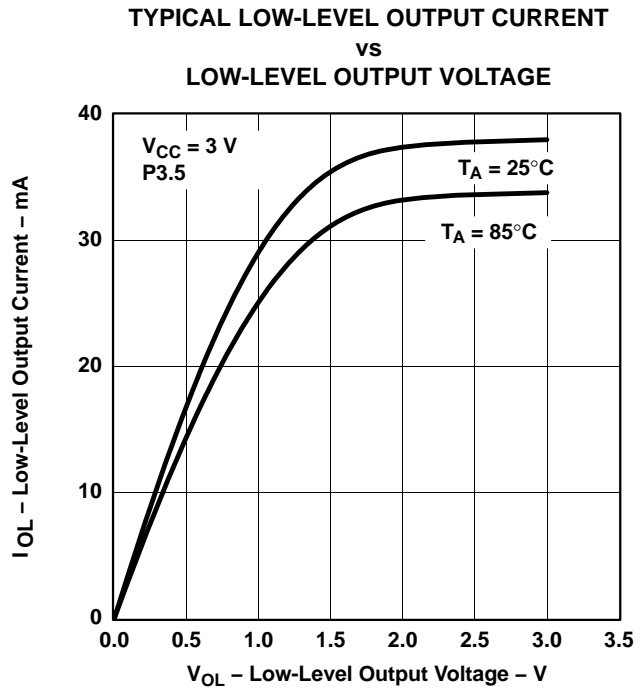
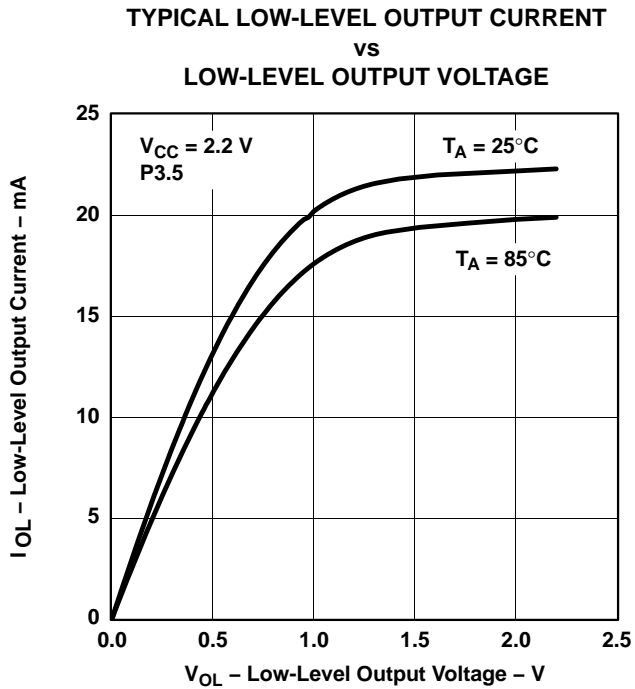


MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – ports P1, P2, P3, P4, P5, P6 (continued)



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

wake-up LPM3

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|---|-----|-----|-----|---------------|
| $t_{(LPM3)}$ Delay time | $V_{CC} = 2.2\text{ V}/3\text{ V}$, $f_{DCO} \geq f_{DCO43}$ | | | 6 | μs |

RAM

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|-----------------|-----|-----|-----|------|
| V_{RAMh} See Note 1 | CPU HALTED | 1.6 | | | V |

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

Comparator_A (see Note 1)

| PARAMETER | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|--|--|-----------|------|------|------------|---------------|
| $I_{(DD)}$ | CAON=1, CARSEL=0, CAREF=0 | 2.2 V | 25 | 40 | | μA |
| | | 3 V | 45 | 60 | | |
| $I_{(Refladder/Refdiode)}$ | CAON=1, CARSEL=0, CAREF=1/2/3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2 | 2.2 V | 30 | 50 | | μA |
| | | 3 V | 45 | 71 | | |
| $V_{(IC)}$ Common-mode input voltage | CAON =1 | 2.2 V/3 V | 0 | | $V_{CC}-1$ | V |
| $V_{(Ref025)}$ $\frac{\text{Voltage @ } 0.25 V_{CC} \text{ node}}{V_{CC}}$ | PCA0=1, CARSEL=1, CAREF=1, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2 | 2.2 V/3 V | 0.23 | 0.24 | 0.25 | |
| $V_{(Ref050)}$ $\frac{\text{Voltage @ } 0.5 V_{CC} \text{ node}}{V_{CC}}$ | PCA0=1, CARSEL=1, CAREF=2, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2 | 2.2 V/3 V | 0.47 | 0.48 | 0.5 | |
| $V_{(RefVT)}$ (see Figure 6 and Figure 7) | PCA0=1, CARSEL=1, CAREF=3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2 $T_A = 85^\circ\text{C}$ | 2.2 V | 390 | 480 | 540 | mV |
| | | 3 V | 400 | 490 | 550 | |
| $V_{(offset)}$ Offset voltage | See Note 2 | 2.2 V/3 V | -30 | | 30 | mV |
| V_{hys} Input hysteresis | CAON=1 | 2.2 V/3 V | 0 | 0.7 | 1.4 | mV |
| $t_{(response LH)}$ | $T_A = 25^\circ\text{C}$, Overdrive 10 mV, Without filter: CAF=0 | 2.2 V | 130 | 210 | 300 | ns |
| | | 3 V | 80 | 150 | 240 | |
| | $T_A = 25^\circ\text{C}$, Overdrive 10 mV, With filter: CAF=1 | 2.2 V | 1.4 | 1.9 | 3.4 | μs |
| | | 3 V | 0.9 | 1.5 | 2.6 | |
| $t_{(response HL)}$ | $T_A = 25^\circ\text{C}$, Overdrive 10 mV, Without filter: CAF=0 | 2.2 V | 130 | 210 | 300 | ns |
| | | 3 V | 80 | 150 | 240 | |
| | $T_A = 25^\circ\text{C}$, Overdrive 10 mV, With filter: CAF=1 | 2.2 V | 1.4 | 1.9 | 3.4 | μs |
| | | 3 V | 0.9 | 1.5 | 2.6 | |

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{(kg(Px.x))}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

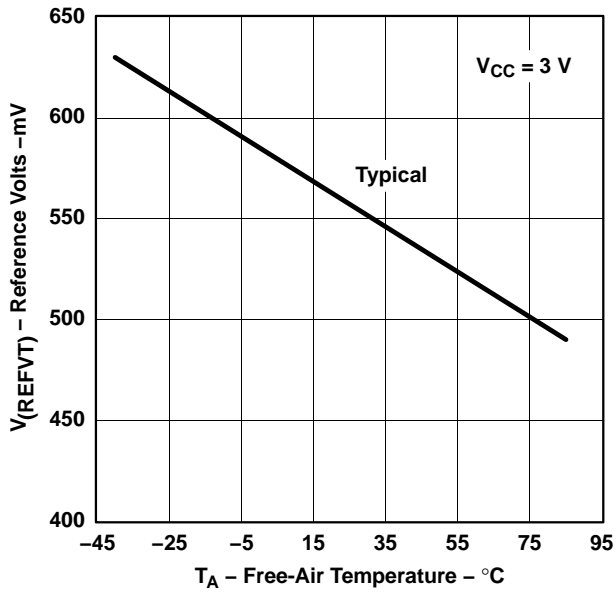


Figure 6. V_(REFVT) vs Temperature, V_{CC} = 3 V

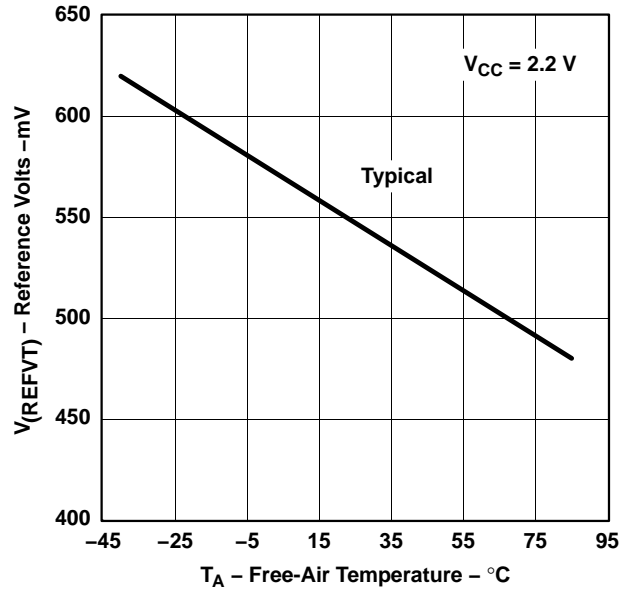


Figure 7. V_(REFVT) vs Temperature, V_{CC} = 2.2 V

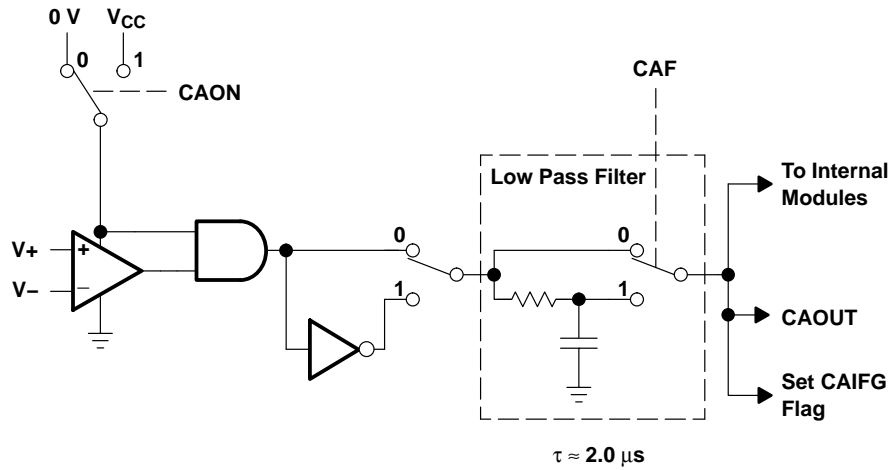


Figure 8. Block Diagram of Comparator_A Module

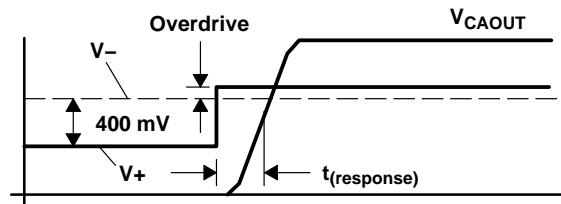


Figure 9. Overdrive Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

POR/brownout reset (BOR) (see Notes 1 and 2)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|---|-----|---------------------------|------|---------------|
| $t_{d(BOR)}$ | | | | 2000 | μs |
| $V_{CC(Start)}$ | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 10) | | $0.7 \times V_{(B_IT-)}$ | | V |
| $V_{(B_IT-)}$ | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 10 through Figure 12) | | | 1.71 | V |
| $V_{hys(B_IT-)}$ | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 10) | 70 | 130 | 180 | mV |
| $t_{(reset)}$ | Pulse length needed at RST/NMI pin to accepted reset internally, $V_{CC} = 2.2 \text{ V}/3 \text{ V}$ | 2 | | | μs |

- NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B_IT-)} + V_{hys(B_IT-)}$ is $\leq 1.8 \text{ V}$.
2. During power up, the CPU begins code execution following a period of $t_{BOR(delay)}$ after $V_{CC} = V_{(B_IT-)} + V_{hys(B_IT-)}$. The default DCO settings must not be changed until $V_{CC} \geq V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x1xx Family User's Guide* (SLAU049) for more information on the brownout/SVS circuit.

typical characteristics

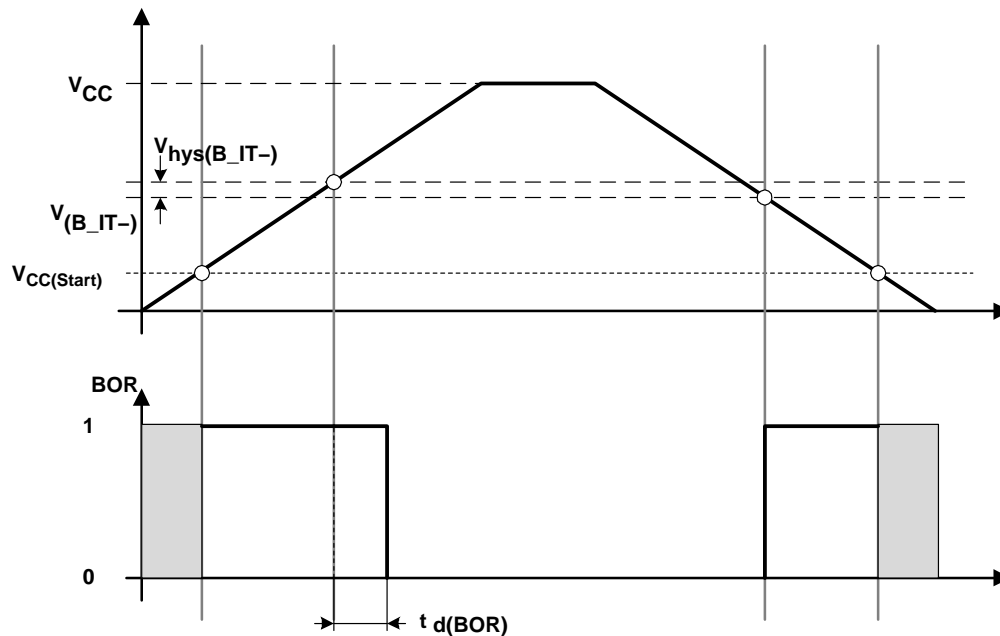


Figure 10. POR/Brownout Reset (BOR) vs Supply Voltage

typical characteristics (continued)

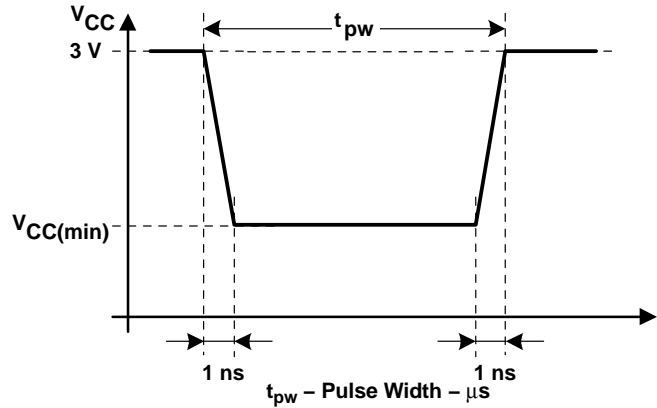
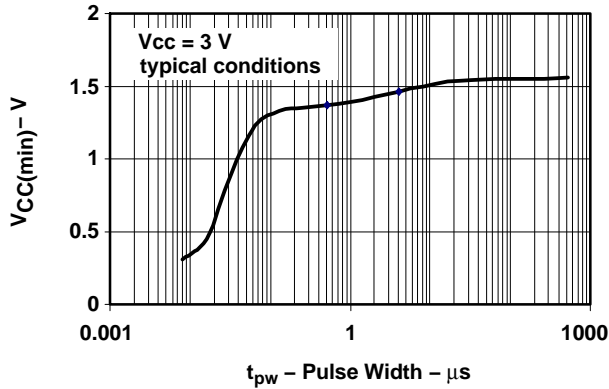


Figure 11. V_{CC(min)} Level With a Square Voltage Drop to Generate a POR/Brownout Signal

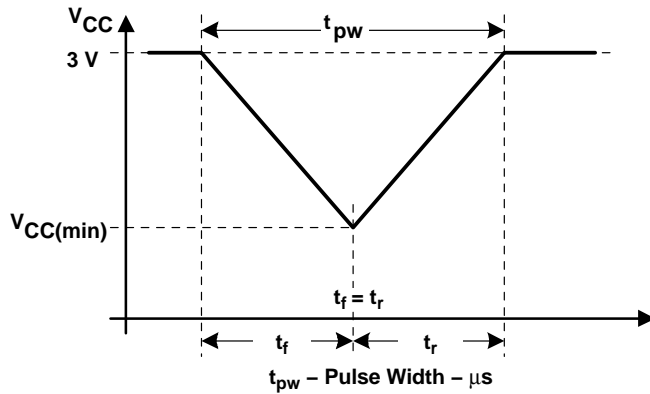
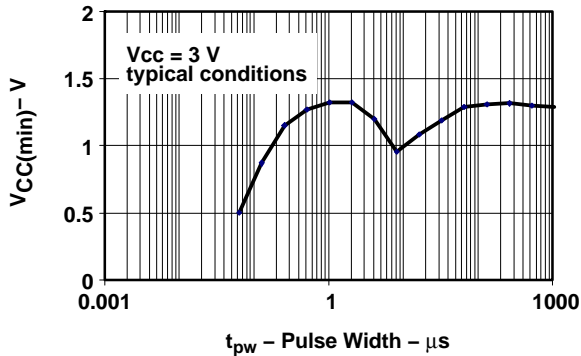


Figure 12. V_{CC(min)} Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

SVS (supply voltage supervisor/monitor)

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT | |
|-------------------------------|---|---------------|-------------------------------|-------------------|-------------------------------|----|
| $t_{(SVSR)}$ | $dV_{CC}/dt > 30 \text{ V/ms}$ (see Figure 13) | 5 | | 150 | μs | |
| | $dV_{CC}/dt \leq 30 \text{ V/ms}$ | | | 2000 | | |
| $t_{d(SVSON)}$ | SVSON, switch from VLD = 0 to VLD \neq 0, $V_{CC} = 3 \text{ V}$ | | 150 | 300 | μs | |
| t_{settle} | VLD \neq 0 [†] | | | 12 | μs | |
| $V_{(SVSstart)}$ | VLD \neq 0, $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 13) | | 1.55 | 1.7 | V | |
| $V_{\text{hys}(SVS_IT-)}$ | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 13) | VLD = 1 | 70 | 120 | 155 | mV |
| | | VLD = 2 to 14 | $V_{(SVS_IT-)} \times 0.004$ | | $V_{(SVS_IT-)} \times 0.008$ | |
| | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 13), External voltage applied on A7 | VLD = 15 | 4.4 | | 10.4 | mV |
| $V_{(SVS_IT-)}$ | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 13 and Figure 14) | VLD = 1 | 1.8 | 1.9 | 2.05 | V |
| | | VLD = 2 | 1.94 | 2.1 | 2.25 | |
| | | VLD = 3 | 2.05 | 2.2 | 2.37 | |
| | | VLD = 4 | 2.14 | 2.3 | 2.48 | |
| | | VLD = 5 | 2.24 | 2.4 | 2.6 | |
| | | VLD = 6 | 2.33 | 2.5 | 2.71 | |
| | | VLD = 7 | 2.46 | 2.65 | 2.86 | |
| | | VLD = 8 | 2.58 | 2.8 | 3 | |
| | | VLD = 9 | 2.69 | 2.9 | 3.13 | |
| | | VLD = 10 | 2.83 | 3.05 | 3.29 | |
| | | VLD = 11 | 2.94 | 3.2 | 3.42 | |
| | | VLD = 12 | 3.11 | 3.35 | 3.61 [†] | |
| | | VLD = 13 | 3.24 | 3.5 | 3.76 [†] | |
| | VLD = 14 | 3.43 | 3.7 [†] | 3.99 [†] | | |
| | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 13 and Figure 14), External voltage applied on A7 | VLD = 15 | 1.1 | 1.2 | 1.3 | |
| $I_{CC(SVS)}$ (see Note 1) | VLD \neq 0, $V_{CC} = 2.2 \text{ V}/3 \text{ V}$ | | 10 | 15 | μA | |

[†] The recommended operating voltage range is limited to 3.6 V.

[‡] t_{settle} is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD \neq 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be $> 50 \text{ mV}$.

NOTE 1: The current consumption of the SVS module is not included in the I_{CC} current consumption data.

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

typical characteristics

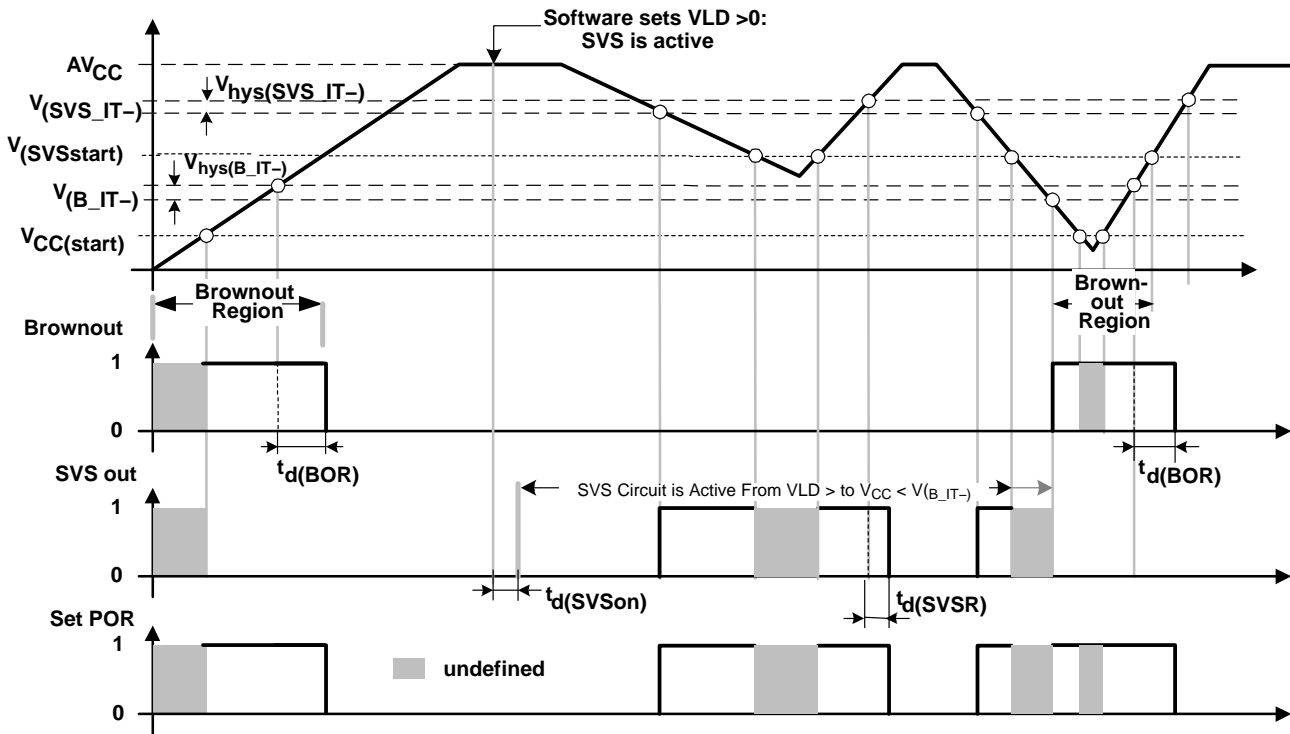


Figure 13. SVS Reset (SVSR) vs Supply Voltage

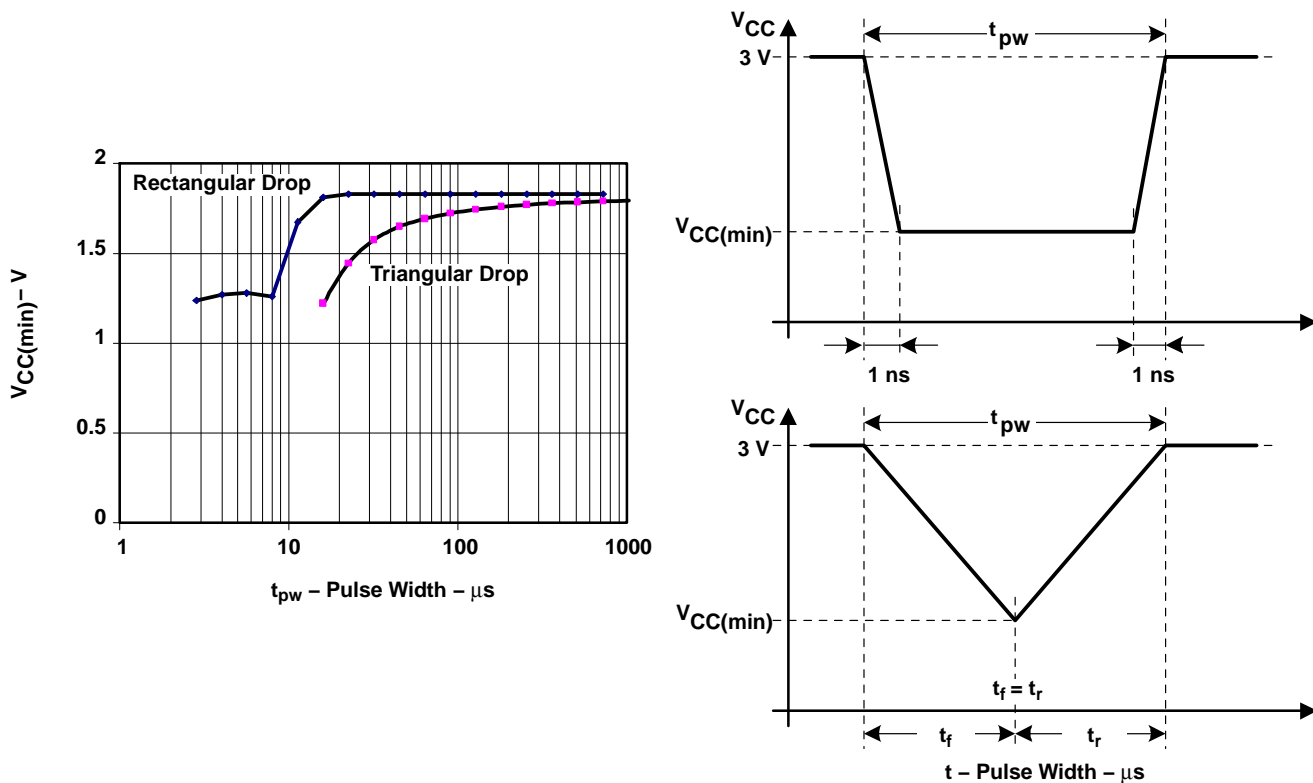


Figure 14. $V_{CC(min)}$: Square Voltage Drop and Triangle Voltage Drop to Generate an SVS Signal ($VLD = 1$)

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

DCO (see Note 1)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------|---|-----------------|--------------------------|--------------------------|--------------------------|------|
| f _(DCO03) | R _{sel} = 0, DCO = 3, MOD = 0, DCOR = 0, T _A = 25°C | 2.2 V | 0.08 | 0.12 | 0.15 | MHz |
| | | 3 V | 0.08 | 0.13 | 0.16 | |
| f _(DCO13) | R _{sel} = 1, DCO = 3, MOD = 0, DCOR = 0, T _A = 25°C | 2.2 V | 0.14 | 0.19 | 0.23 | MHz |
| | | 3 V | 0.14 | 0.18 | 0.22 | |
| f _(DCO23) | R _{sel} = 2, DCO = 3, MOD = 0, DCOR = 0, T _A = 25°C | 2.2 V | 0.22 | 0.30 | 0.36 | MHz |
| | | 3 V | 0.22 | 0.28 | 0.34 | |
| f _(DCO33) | R _{sel} = 3, DCO = 3, MOD = 0, DCOR = 0, T _A = 25°C | 2.2 V | 0.37 | 0.49 | 0.59 | MHz |
| | | 3 V | 0.37 | 0.47 | 0.56 | |
| f _(DCO43) | R _{sel} = 4, DCO = 3, MOD = 0, DCOR = 0, T _A = 25°C | 2.2 V | 0.61 | 0.77 | 0.93 | MHz |
| | | 3 V | 0.61 | 0.75 | 0.90 | |
| f _(DCO53) | R _{sel} = 5, DCO = 3, MOD = 0, DCOR = 0, T _A = 25°C | 2.2 V | 1 | 1.2 | 1.5 | MHz |
| | | 3 V | 1 | 1.3 | 1.5 | |
| f _(DCO63) | R _{sel} = 6, DCO = 3, MOD = 0, DCOR = 0, T _A = 25°C | 2.2 V | 1.6 | 1.9 | 2.2 | MHz |
| | | 3 V | 1.69 | 2.0 | 2.29 | |
| f _(DCO73) | R _{sel} = 7, DCO = 3, MOD = 0, DCOR = 0, T _A = 25°C | 2.2 V | 2.4 | 2.9 | 3.4 | MHz |
| | | 3 V | 2.7 | 3.2 | 3.65 | |
| f _(DCO47) | R _{sel} = 4, DCO = 7, MOD = 0, DCOR = 0, T _A = 25°C | 2.2 V/3 V | f _{DCO40} × 1.7 | f _{DCO40} × 2.1 | f _{DCO40} × 2.5 | MHz |
| f _(DCO77) | R _{sel} = 7, DCO = 7, MOD = 0, DCOR = 0, T _A = 25°C | 2.2 V | 4 | 4.5 | 4.9 | MHz |
| | | 3 V | 4.4 | 4.9 | 5.4 | |
| S _{Rsel} | S _R = f _{Rsel+1} / f _{Rsel} | 2.2 V/3 V | 1.35 | 1.65 | 2 | |
| S _{DCO} | S _{DCO} = f _(DCO+1) / f _(DCO) | 2.2 V/3 V | 1.07 | 1.12 | 1.16 | |
| D _t | Temperature drift, R _{sel} = 4, DCO = 3, MOD = 0 (see Note 2) | 2.2 V | -0.31 | -0.36 | -0.40 | %°C |
| | | 3 V | -0.33 | -0.38 | -0.43 | |
| D _V | Drift with V _{CC} variation, R _{sel} = 4, DCO = 3, MOD = 0 (see Note 2) | 2.2 V/3 V | 0 | 5 | 10 | %/V |

- NOTES: 1. The DCO frequency may not exceed the maximum system frequency defined by parameter processor frequency, f_(System).
2. This parameter is not production tested.

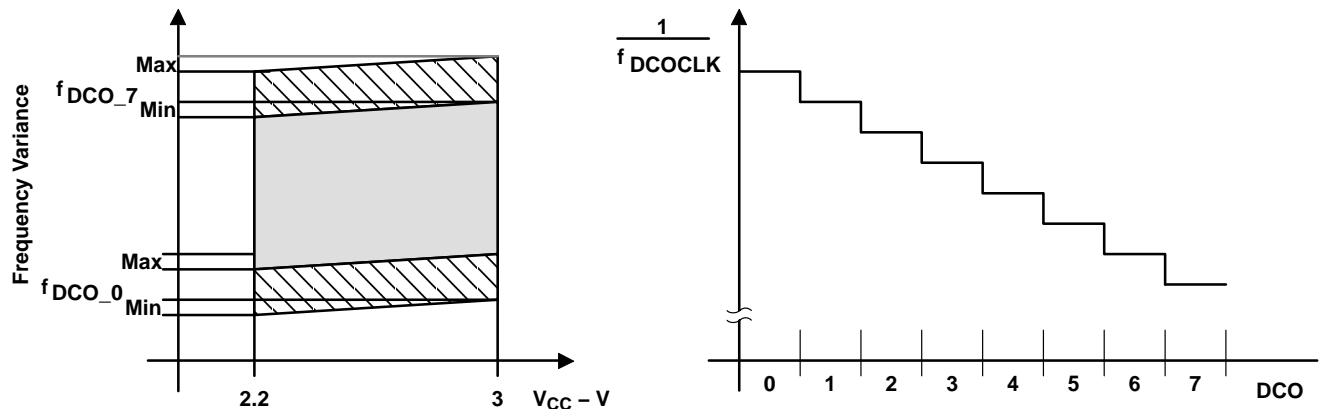


Figure 15. DCO Characteristics

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- Individual devices have a minimum and maximum operation frequency. The specified parameters for $f_{(DCOx0)}$ to $f_{(DCOx7)}$ are valid for all devices.
- All ranges selected by Rsel(n) overlap with Rsel(n+1): Rsel0 overlaps Rsel1, ... Rsel6 overlaps Rsel7.
- DCO control bits DCO0, DCO1, and DCO2 have a step size as defined by parameter S_{DCO}.
- Modulation control bits MOD0 to MOD4 select how often $f_{(DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{(DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{(DCO)} \times f_{(DCO+1)}}{MOD \times f_{(DCO)} + (32 - MOD) \times f_{(DCO+1)}}$$

DCO when using R_{OSC} (see Note 1)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|---|-----------------|-----|----------|-----|------|
| f _{DCO} , DCO output frequency | R _{sel} = 4, DCO = 3, MOD = 0, DCOR = 1, T _A = 25°C | 2.2 V | | 1.8±15% | | MHz |
| | | 3 V | | 1.95±15% | | MHz |
| D _t , Temperature drift | R _{sel} = 4, DCO = 3, MOD = 0, DCOR = 1 | 2.2 V/3 V | | ±0.1 | | %/°C |
| D _v , Drift with V _{CC} variation | R _{sel} = 4, DCO = 3, MOD = 0, DCOR = 1 | 2.2 V/3 V | | 10 | | %/V |

NOTES: 1. R_{OSC} = 100kΩ. Metal film resistor, type 0257. 0.6 watt with 1% tolerance and T_K = ±50ppm/°C.

crystal oscillator, LFXT1 oscillator (see Note 1)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | |
|---|---|---------------------------------|-----------------|-----------------------|------|-------------------|-----------------|
| C _{XIN} Integrated input capacitance | XTS=0; LF oscillator selected, V _{CC} = 2.2 V/3 V | | 12 | | pF | | |
| | XTS=1; XT1 oscillator selected, V _{CC} = 2.2 V/3 V | | 2 | | | | |
| C _{XOUT} Integrated output capacitance | XTS=0; LF oscillator selected, V _{CC} = 2.2 V/3 V | | 12 | | pF | | |
| | XTS=1; XT1 oscillator selected, V _{CC} = 2.2 V/3 V | | 2 | | | | |
| V _{IL} | V _{CC} = 2.2 V/3 V (see Note 2) | XTS = 0 or 1 XT1 or LF modes | V _{SS} | 0.2 × V _{CC} | V | | |
| V _{IH} | | | | | | XTS = 0, LF mode | V _{CC} |
| | | | | | | XTS = 1, XT1 mode | V _{CC} |

- NOTES: 1. The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
2. Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

crystal oscillator, XT2 oscillator (see Note 1)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|-----------------|-----------------------|-----------------|------|
| C _{XIN} Integrated input capacitance | V _{CC} = 2.2 V/3 V | | 2 | | pF |
| C _{XOUT} Integrated output capacitance | V _{CC} = 2.2 V/3 V | | 2 | | pF |
| V _{IL} | V _{CC} = 2.2 V/3 V (see Note 2) | V _{SS} | 0.2 × V _{CC} | V _{CC} | V |
| V _{IH} | | | | | |

- NOTES: 1. The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
2. Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

USART0, USART1 (see Note 1)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-------------------------|-----|-----|-----|------|
| t _(τ) USART0/USART1: deglitch time | V _{CC} = 2.2 V | 200 | 430 | 800 | ns |
| | V _{CC} = 3 V | 150 | 280 | 500 | |

NOTE 1: The signal applied to the USART0/USART1 receive signal/terminal (URXD0/1) should meet the timing requirements of t_(τ) to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of t_(τ). The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0/1 line.



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, power supply and input range conditions (see Note 1)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------|--|--|-------|-------|------|------------|----------|
| V_{AVCC} | Analog supply voltage | V_{AVCC} and DV_{CC} are connected together V_{AVSS} and DV_{SS} are connected together $V_{(AVSS)} = V_{(DVSS)} = 0\text{ V}$ | | 2.2 | | 3.6 | V |
| $V_{(P6.x/Ax)}$ | Analog input voltage range (see Note 2) | All P6.0/A0 to P6.7/A7 terminals. Analog inputs selected in ADC12MCTLx register and P6Sel.x=1 $0 \leq x \leq 7$; $V_{(AVSS)} \leq V_{P6.x/Ax} \leq V_{(AVCC)}$ | | 0 | | V_{AVCC} | V |
| I_{ADC12} | Operating supply current into V_{AVCC} terminal (see Note 3) | $f_{ADC12CLK} = 5.0\text{ MHz}$ ADC12ON = 1, REFON = 0 SHT0=0, SHT1=0, ADC12DIV=0 | 2.2 V | | 0.65 | 1.3 | mA |
| | | | 3 V | | 0.8 | 1.6 | |
| I_{REF+} | Operating supply current into V_{AVCC} terminal (see Note 4) | $f_{ADC12CLK} = 5.0\text{ MHz}$ ADC12ON = 0, REFON = 1, REF2_5V = 1 | 3 V | | 0.5 | 0.8 | mA |
| | | | 2.2 V | | 0.5 | 0.8 | |
| | | $f_{ADC12CLK} = 5.0\text{ MHz}$ ADC12ON = 0, REFON = 1, REF2_5V = 0 | 2.2 V | | 0.5 | 0.8 | mA |
| | | | 3 V | | 0.5 | 0.8 | |
| C_i^\dagger | Input capacitance | Only one terminal can be selected at one time, P6.x/Ax | | 2.2 V | | 40 | pF |
| R_I^\dagger | Input MUX ON resistance | $0V \leq V_{Ax} \leq V_{AVCC}$ | | 3 V | | 2000 | Ω |

† Not production tested, limits verified by design

- NOTES: 1. The leakage current is defined in the leakage current table with P6.x/Ax parameter.
2. The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
3. The internal reference supply current is not included in current consumption parameter I_{ADC12} .
4. The internal reference current is supplied via terminal V_{AVCC} . Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

12-bit ADC, external reference (see Note 1)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------------------------|---|---|-----------|-----|-----|------------|---------------|
| V_{eREF+} | Positive external reference voltage input | $V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 2) | | 1.4 | | V_{AVCC} | V |
| V_{REF-}/V_{eREF-} | Negative external reference voltage input | $V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 3) | | 0 | | 1.2 | V |
| $(V_{eREF+} - V_{REF-}/V_{eREF-})$ | Differential external reference voltage input | $V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 4) | | 1.4 | | V_{AVCC} | V |
| I_{VeREF+} | Static input current | $0V \leq V_{eREF+} \leq V_{AVCC}$ | 2.2 V/3 V | | | ± 1 | μA |
| I_{VREF-}/V_{eREF-} | Static input current | $0V \leq V_{eREF-} \leq V_{AVCC}$ | 2.2 V/3 V | | | ± 1 | μA |

- NOTES: 1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_i , is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
3. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
4. The accuracy limits minimum differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, built-in reference

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | |
|--------------------------|--|---|----------------------|------|-----|-----------|-----------------|
| V_{REF+} | Positive built-in reference voltage output | REF2_5V = 1 for 2.5 V $I_{VREF+max} \leq I_{VREF+} \leq I_{VREF+min}$ | $V_{CC} = 3 V$ | 2.4 | 2.5 | 2.6 | V |
| | | REF2_5V = 0 for 1.5 V $I_{VREF+max} \leq I_{VREF+} \leq I_{VREF+min}$ | $V_{CC} = 2.2 V/3 V$ | 1.44 | 1.5 | 1.56 | |
| $AV_{CC(min)}$ | AV _{CC} minimum voltage, Positive built-in reference active | REF2_5V = 0, $I_{VREF+max} \leq I_{VREF+} \leq I_{VREF+min}$ | | 2.2 | | | V |
| | | REF2_5V = 1, $-0.5mA \leq I_{VREF+} \leq I_{VREF+min}$ | | 2.8 | | | |
| | | REF2_5V = 1, $-1mA \leq I_{VREF+} \leq I_{VREF+min}$ | | 2.9 | | | |
| I_{VREF+} | Load current out of V_{REF+} terminal | | $V_{CC} = 2.2 V$ | 0.01 | | -0.5 | mA |
| | | | $V_{CC} = 3 V$ | 0.01 | | -1 | |
| $I_{L(VREF+)}^\dagger$ | Load-current regulation V_{REF+} terminal | $I_{VREF+} = 500 \mu A \pm 100 \mu A$ Analog input voltage $\sim 0.75 V$, REF2_5V = 0 | $V_{CC} = 2.2 V$ | | | ± 2 | LSB |
| | | | $V_{CC} = 3 V$ | | | | |
| $I_{L(VREF+)}^\ddagger$ | Load-current regulation V_{REF+} terminal | $I_{VREF+} = 500 \mu A \pm 100 \mu A$ Analog input voltage $\sim 1.25 V$, REF2_5V = 1 | $V_{CC} = 3 V$ | | | ± 2 | LSB |
| | | | | | | | |
| $I_{DL(VREF+)}^\ddagger$ | Load current regulation V_{REF+} terminal | $I_{VREF+} = 100 \mu A \rightarrow 900 \mu A$, $C_{VREF+} = 5 \mu F$, ax $\sim 0.5 \times V_{REF+}$, Error of conversion result ≤ 1 LSB | $V_{CC} = 3 V$ | | | 20 | ns |
| C_{VREF+} | Capacitance at pin V_{REF+} (see Note 1) | REFON = 1, $0 mA \leq I_{VREF+} \leq I_{VREF+max}$ | $V_{CC} = 2.2 V/3 V$ | 5 | 10 | | μF |
| T_{REF+}^\dagger | Temperature coefficient of built-in reference | I_{VREF+} is a constant in the range of $0 mA \leq I_{VREF+} \leq 1 mA$ | $V_{CC} = 2.2 V/3 V$ | | | ± 100 | ppm/ $^\circ C$ |
| t_{REFON}^\dagger | Settle time of internal reference voltage (see Figure 16 and Note 2) | $I_{VREF+} = 0.5 mA$, $C_{VREF+} = 10 \mu F$, $V_{REF+} = 1.5 V$, $V_{AVCC} = 2.2 V$ | | | | 17 | ms |

† Not production tested, limits characterized

‡ Not production tested, limits verified by design

NOTES: 1. The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins V_{REF+} and AV_{SS} and V_{REF-}/V_{eREF-} and AV_{SS} : 10 μF tantalum and 100 nF ceramic.

2. The condition is that the error in a conversion started after t_{REFON} is less than ± 0.5 LSB. The settling time depends on the external capacitive load.

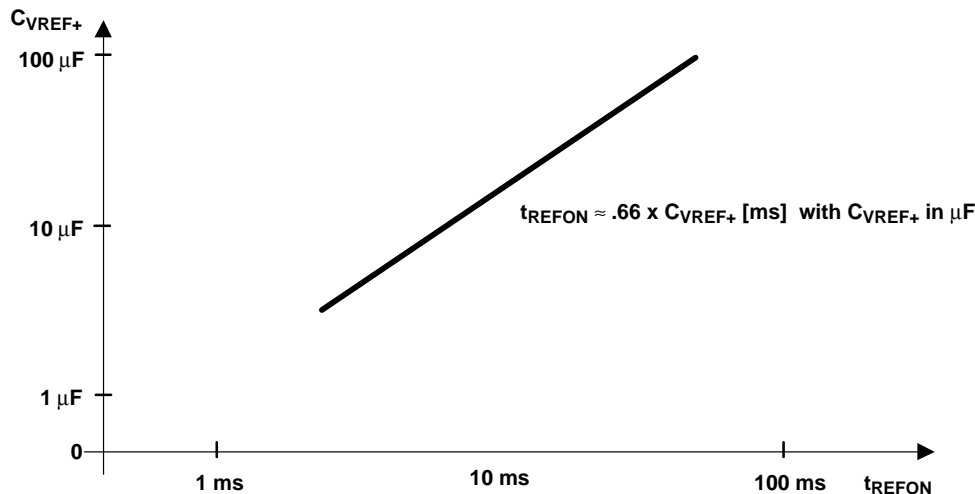


Figure 16. Typical Settling Time of Internal Reference t_{REFON} vs External Capacitor on V_{REF+}



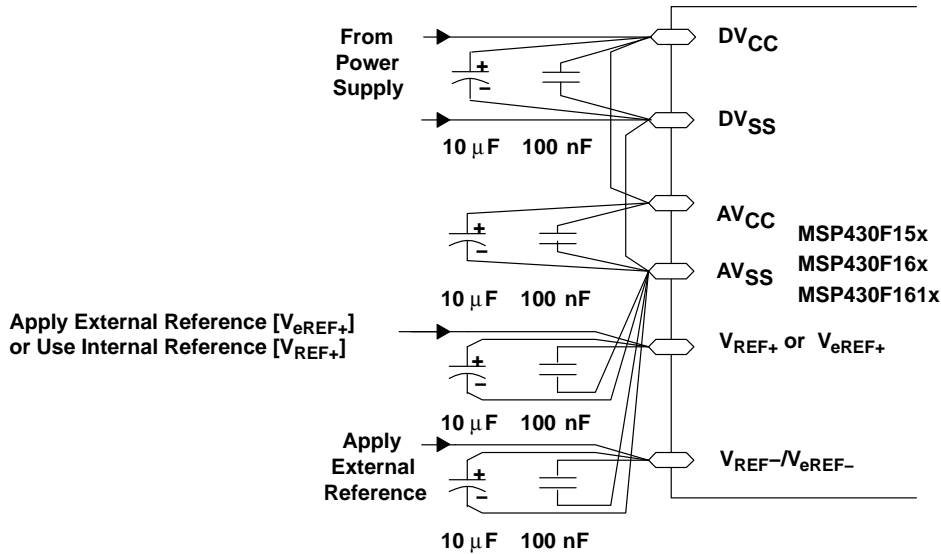


Figure 17. Supply Voltage and Reference Voltage Design V_{REF-}/V_{REF+} External Supply

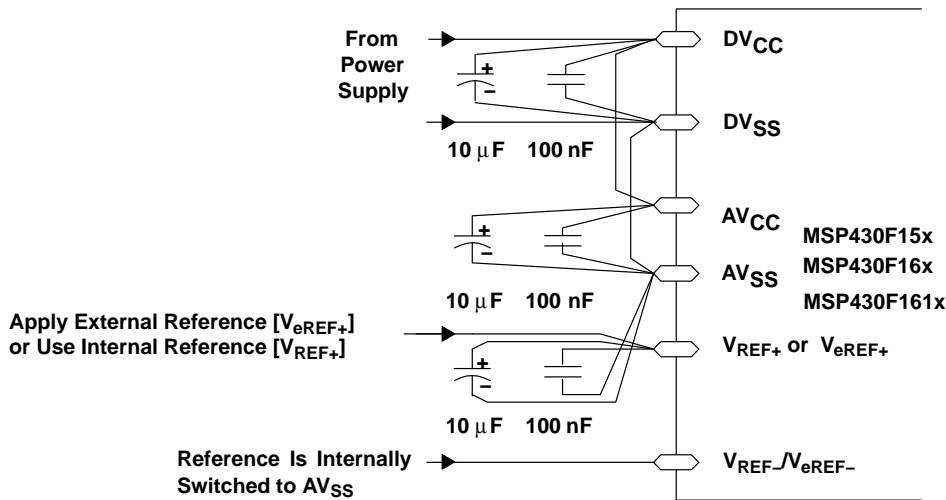


Figure 18. Supply Voltage and Reference Voltage Design $V_{REF-}/V_{REF+} = AV_{SS}$, Internally Connected

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, timing parameters

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | |
|-----------------------------------|---|--|------------|---|------|-----|-----|
| f _{ADC12CLK} | For specified performance of ADC12 linearity parameters | 2.2V/3 V | 0.45 | 5 | 6.3 | MHz | |
| f _{ADC12OSC} | Internal ADC12 oscillator | ADC12DIV=0, f _{ADC12CLK} =f _{ADC12OSC} | 2.2 V/ 3 V | 3.7 | 5 | 6.3 | MHz |
| t _{CONVERT} | Conversion time | C _{VREF+} ≥ 5 μF, Internal oscillator, f _{ADC12OSC} = 3.7 MHz to 6.3 MHz | 2.2 V/ 3 V | 2.06 | 3.51 | μs | |
| | | External f _{ADC12CLK} from ACLK, MCLK or SMCLK: ADC12SSEL ≠ 0 | | 13×ADC12DIV× 1/f _{ADC12CLK} | | μs | |
| t _{ADC12ON} [†] | Turn on settling time of the ADC | (see Note 1) | | | 100 | ns | |
| t _{Sample} [‡] | Sampling time | R _S = 400 Ω, R _I = 1000 Ω, C _I = 30 pF | 3 V | 1220 | | ns | |
| | | τ = [R _S + R _I] × C _I (see Note 2) | 2.2 V | 1400 | | | |

[†] Not production tested, limits characterized

[‡] Not production tested, limits verified by design

NOTES: 1. The condition is that the error in a conversion started after t_{ADC12ON} is less than ±0.5 LSB. The reference and input signal are already settled.

2. Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:

$$t_{\text{Sample}} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800 \text{ ns where } n = \text{ADC resolution} = 12, R_S = \text{external source resistance.}$$

12-bit ADC, linearity parameters

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|----------------|---|-----------|-----|------|------|-----|
| E _I | 1.4 V ≤ (V _{eREF+} - V _{REF-/V_{eREF-}}) _{min} ≤ 1.6 V | 2.2 V/3 V | | ±2 | LSB | |
| | 1.6 V < (V _{eREF+} - V _{REF-/V_{eREF-}}) _{min} ≤ [V _{AVCC}] | | | ±1.7 | | |
| E _D | (V _{eREF+} - V _{REF-/V_{eREF-}}) _{min} ≤ (V _{eREF+} - V _{REF-/V_{eREF-}}), C _{VREF+} = 10 μF (tantalum) and 100 nF (ceramic) | 2.2 V/3 V | | ±1 | LSB | |
| E _O | (V _{eREF+} - V _{REF-/V_{eREF-}}) _{min} ≤ (V _{eREF+} - V _{REF-/V_{eREF-}}), Internal impedance of source R _S < 100 Ω, C _{VREF+} = 10 μF (tantalum) and 100 nF (ceramic) | 2.2 V/3 V | | ±2 | ±4 | LSB |
| E _G | (V _{eREF+} - V _{REF-/V_{eREF-}}) _{min} ≤ (V _{eREF+} - V _{REF-/V_{eREF-}}), C _{VREF+} = 10 μF (tantalum) and 100 nF (ceramic) | 2.2 V/3 V | | ±1.1 | ±2 | LSB |
| E _T | (V _{eREF+} - V _{REF-/V_{eREF-}}) _{min} ≤ (V _{eREF+} - V _{REF-/V_{eREF-}}), C _{VREF+} = 10 μF (tantalum) and 100 nF (ceramic) | 2.2 V/3 V | | ±2 | ±5 | LSB |



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, temperature sensor and built-in V_{MID}

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|---|-------|------|----------|-------|
| I _{SENSOR} | Operating supply current into AV _{CC} terminal (see Note 1) | REFON = 0, INCH = 0Ah, ADC12ON=NA, T _A = 25°C | 2.2 V | 40 | 120 | μA |
| | | | 3 V | 60 | 160 | |
| V _{SENSOR} [†] | (see Note 2) | ADC12ON = 1, INCH = 0Ah, T _A = 0°C | 2.2 V | 986 | | mV |
| | | | 3 V | 986 | | |
| TC _{SENSOR} [†] | | ADC12ON = 1, INCH = 0Ah | 2.2 V | 3.55 | 3.55±3% | mV/°C |
| | | | 3 V | 3.55 | 3.55±3% | |
| t _{SENSOR(sample)} [†] | Sample time required if channel 10 is selected (see Note 3) | ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB | 2.2 V | 30 | | μs |
| | | | 3 V | 30 | | |
| I _{V_{MID}} | Current into divider at channel 11 (see Note 4) | ADC12ON = 1, INCH = 0Bh, | 2.2 V | | NA | μA |
| | | | 3 V | | NA | |
| V _{MID} | AV _{CC} divider at channel 11 | ADC12ON = 1, INCH = 0Bh, V _{MID} is ~0.5 x V _{AVCC} | 2.2 V | 1.1 | 1.1±0.04 | V |
| | | | 3 V | 1.5 | 1.5±0.04 | |
| t _{V_{MID}(sample)} | Sample time required if channel 11 is selected (see Note 5) | ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB | 2.2 V | 1400 | | ns |
| | | | 3 V | 1220 | | |

[†] Not production tested, limits characterized

- NOTES:
1. The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON=1), or (ADC12ON=1 AND INCH=0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
 2. The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended in order to minimize the offset error of the built-in temperature sensor.
 3. The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time t_{SENSOR(on)}.
 4. No additional current is needed. The V_{MID} is used during sampling.
 5. The on-time t_{V_{MID}(on)} is included in the sampling time t_{V_{MID}(sample)}; no additional on time is needed.

12-bit DAC, supply specifications

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------|--|--|-----------------|------|-----|------|------|
| AV _{CC} | Analog supply voltage | AV _{CC} = DV _{CC} , AV _{SS} = DV _{SS} = 0 V | | 2.20 | | 3.60 | V |
| I _{DD} | Supply Current: Single DAC Channel (see Notes 1 and 2) | DAC12AMPx=2, DAC12IR=0, DAC12_xDAT=0800h | 2.2V/3V | | 50 | 110 | μA |
| | | DAC12AMPx=2, DAC12IR=1, DAC12_xDAT=0800h, V _{eREF+} =V _{REF+} = AV _{CC} | 2.2V/3V | | 50 | 110 | |
| | | DAC12AMPx=5, DAC12IR=1, DAC12_xDAT=0800h, V _{eREF+} =V _{REF+} = AV _{CC} | 2.2V/3V | | 200 | 440 | |
| | | DAC12AMPx=7, DAC12IR=1, DAC12_xDAT=0800h, V _{eREF+} =V _{REF+} = AV _{CC} | 2.2V/3V | | 700 | 1500 | |
| PSRR | Power supply rejection ratio (see Notes 3 and 4) | DAC12_xDAT = 800h, V _{REF} = 1.5 V ΔAV _{CC} = 100mV | 2.2V | | | | dB |
| | | DAC12_xDAT = 800h, V _{REF} = 1.5 V or 2.5 V ΔAV _{CC} = 100mV | 3V | | 70 | | |

- NOTES:
1. No load at the output pin, DAC12_0 or DAC12_1, assuming that the control bits for the shared pins are set properly.
 2. Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
 3. PSRR = 20*log{ΔAV_{CC}/ΔV_{DAC12_xOUT}}.
 4. V_{REF} is applied externally. The internal reference is not used.

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (see Figure 19)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------|---|--|-----------------|-----|------|-------|------------------|
| Resolution | | (12-bit Monotonic) | | 12 | | | bits |
| INL | Integral nonlinearity (see Note 1) | V _{ref} = 1.5 V DAC12AMPx = 7, DAC12IR = 1 | 2.2V | | ±2.0 | ±8.0 | LSB |
| | | V _{ref} = 2.5 V DAC12AMPx = 7, DAC12IR = 1 | 3V | | | | |
| DNL | Differential nonlinearity (see Note 1) | V _{ref} = 1.5 V DAC12AMPx = 7, DAC12IR = 1 | 2.2V | | ±0.4 | ±1.0 | LSB |
| | | V _{ref} = 2.5 V DAC12AMPx = 7, DAC12IR = 1 | 3V | | | | |
| E _O | Offset voltage w/o calibration (see Notes 1, 2) | V _{ref} = 1.5 V DAC12AMPx = 7, DAC12IR = 1 | 2.2V | | | ±21 | mV |
| | | V _{ref} = 2.5 V DAC12AMPx = 7, DAC12IR = 1 | 3V | | | | |
| | Offset voltage with calibration (see Notes 1, 2) | V _{ref} = 1.5 V DAC12AMPx = 7, DAC12IR = 1 | 2.2V | | | ±2.5 | |
| | | V _{ref} = 2.5 V DAC12AMPx = 7, DAC12IR = 1 | 3V | | | | |
| d _{E(O)/dT} | Offset error temperature coefficient (see Note 1) | | 2.2V/3V | | 30 | | µV/C |
| E _G | Gain error (see Note 1) | V _{REF} = 1.5 V | 2.2V | | | ±3.50 | % FSR |
| | | V _{REF} = 2.5 V | 3V | | | | |
| d _{E(G)/dT} | Gain temperature coefficient (see Note 1) | | 2.2V/3V | | 10 | | ppm of FSR/°C |
| t _{Offset_Cal} | Time for offset calibration (see Note 3) | DAC12AMPx=2 | 2.2V/3V | | | 100 | ms |
| | | DAC12AMPx=3,5 | 2.2V/3V | | | 32 | |
| | | DAC12AMPx=4,6,7 | 2.2V/3V | | | 6 | |

- NOTES: 1. Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients "a" and "b" of the first order equation: $y = a + b \cdot x$. $V_{DAC12_xOUT} = E_O + (1 + E_G) \cdot (V_{eREF+}/4095) \cdot DAC12_xDAT$, DAC12IR = 1.
2. The offset calibration works on the output operational amplifier. Offset Calibration is triggered setting bit DAC12CALON
3. The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. It is recommended that the DAC12 module be configured prior to initiating calibration. Port activity during calibration may effect accuracy and is not recommended.

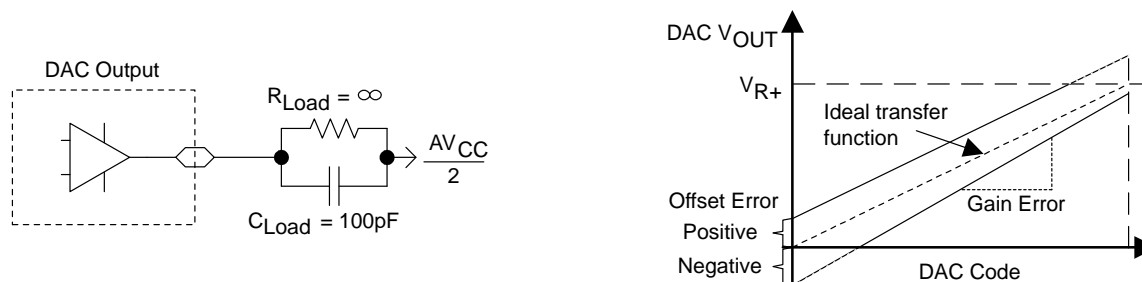
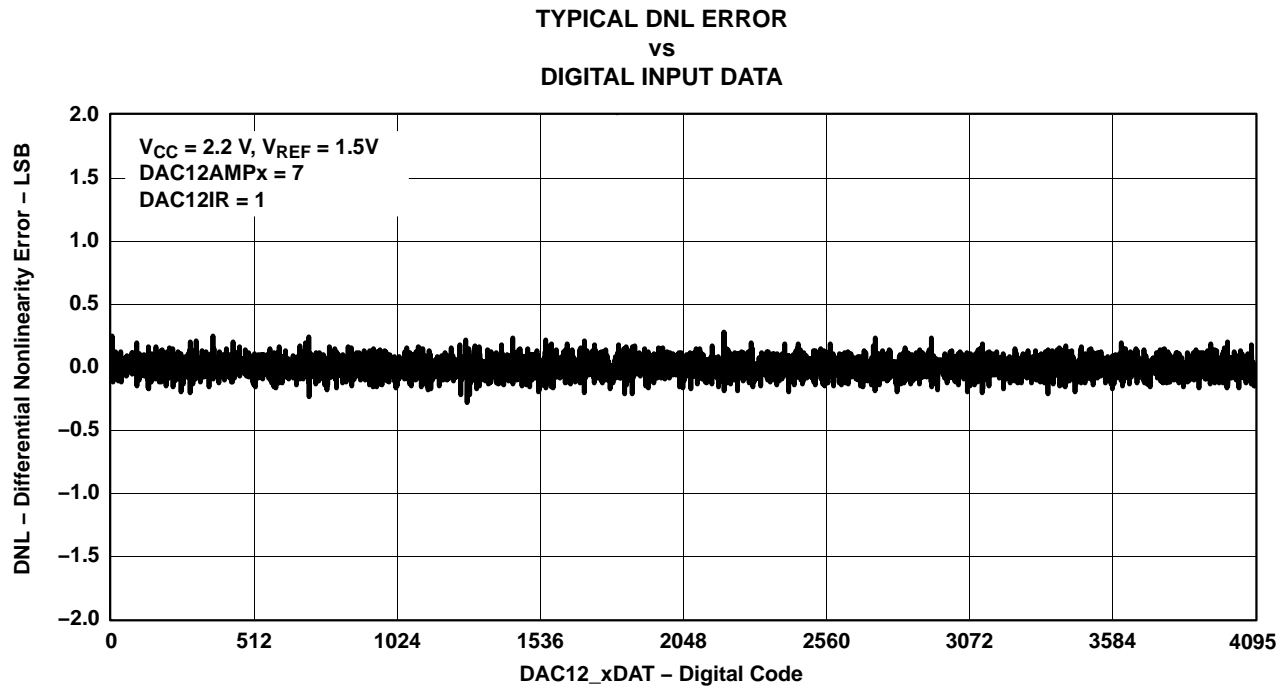
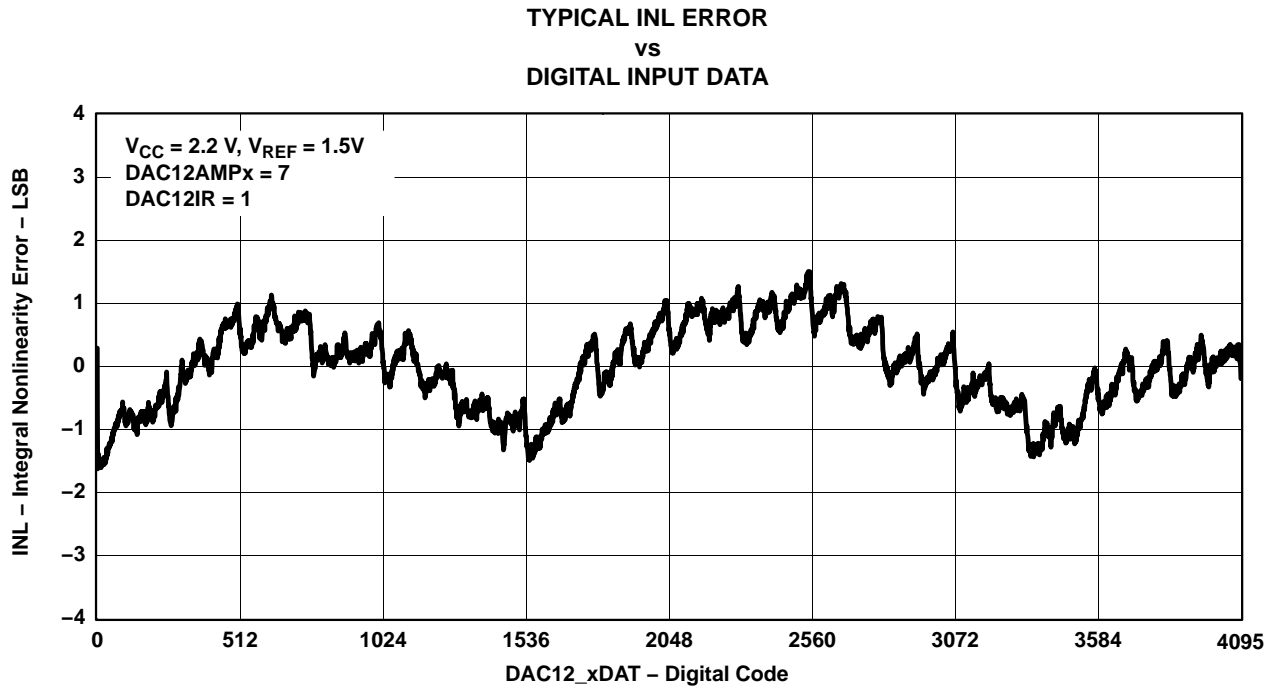


Figure 19. Linearity Test Load Conditions and Gain/Offset Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (continued)



MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, output specifications

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|---|-----------------|------------------------|-----|------------------|------|
| V _O Output voltage range (see Note 1, Figure 22) | No Load, V _{REF+} = AV _{CC} , DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7 | 2.2V/3V | 0 | | 0.005 | V |
| | No Load, V _{REF+} = AV _{CC} , DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7 | 2.2V/3V | AV _{CC} -0.05 | | AV _{CC} | V |
| | R _{Load} = 3 kΩ, V _{REF+} = AV _{CC} , DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7 | 2.2V/3V | 0 | | 0.1 | V |
| | R _{Load} = 3 kΩ, V _{REF+} = AV _{CC} , DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7 | 2.2V/3V | AV _{CC} -0.13 | | AV _{CC} | V |
| C _{L(DAC12)} | Max DAC12 load capacitance | 2.2V/3V | | | 100 | pF |
| I _{L(DAC12)} | Max DAC12 load current | 2.2V | -0.5 | | +0.5 | mA |
| | | 3V | -1.0 | | +1.0 | mA |
| R _{O/P(DAC12)} | R _{Load} = 3 kΩ V _{O/P(DAC12)} = 0 V DAC12AMPx = 7 DAC12_xDAT = 0h | 2.2V/3V | | 150 | 250 | Ω |
| | R _{Load} = 3 kΩ V _{O/P(DAC12)} = AV _{CC} DAC12AMPx = 7 DAC12_xDAT = 0FFFh | 2.2V/3V | | 150 | 250 | |
| | R _{Load} = 3 kΩ 0.3 V < V _{O/P(DAC12)} ≤ AV _{CC} - 0.3 V DAC12AMPx = 7 | 2.2V/3V | | 1 | 4 | |

NOTES: 1. Data is valid after the offset calibration of the output amplifier.

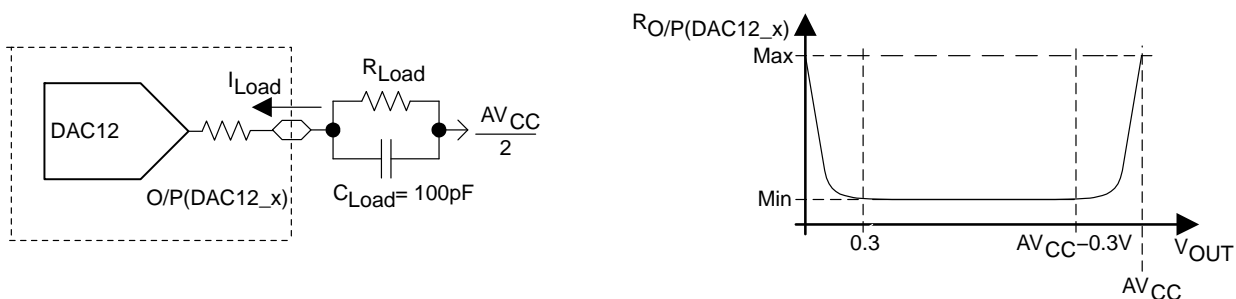


Figure 22. DAC12_x Output Resistance Tests

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

12-bit DAC, reference input specifications

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|--|-------------------------------|---|---------|---------------------|-----------------------|------|----|
| V _{REF+} | Reference input voltage range | DAC12IR=0 (see Notes 1 and 2) | | AV _{CC} /3 | AV _{CC} +0.2 | V | |
| | | DAC12IR=1 (see Notes 3 and 4) | 2.2V/3V | AV _{CC} | AV _{CC} +0.2 | | |
| R _{i(VREF+)} , R _{i(VREF-)} | Reference input resistance | DAC12_0 IR = DAC12_1 IR = 0 | 2.2V/3V | 20 | | MΩ | |
| | | DAC12_0 IR = 1, DAC12_1 IR = 0 | 2.2V/3V | 40 | 48 | 56 | kΩ |
| | | DAC12_0 IR = 0, DAC12_1 IR = 1 | 2.2V/3V | | | | |
| | | DAC12_0 IR = DAC12_1 IR = 1, DAC12_0 SREFx = DAC12_1 SREFx (see Note 5) | 2.2V/3V | 20 | 24 | 28 | kΩ |

- NOTES: 1. For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).
 2. The maximum voltage applied at reference input voltage terminal V_{REF+} = [AV_{CC} - V_{E(O)}] / [3*(1 + E_G)].
 3. For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV_{CC}).
 4. The maximum voltage applied at reference input voltage terminal V_{REF+} = [AV_{CC} - V_{E(O)}] / (1 + E_G).
 5. When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel reducing the reference input resistance.

12-bit DAC, dynamic specifications; V_{ref} = V_{CC}, DAC12IR = 1 (see Figure 23 and Figure 24)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------------|---|---------------------------|---------|------|------|------|
| t _{ON} | DAC12_xDAT = 800h, Error _{V(O)} < ±0.5 LSB (see Note 1, Figure 23) | DAC12AMPx = 0 → {2, 3, 4} | 2.2V/3V | 60 | 120 | μs |
| | | DAC12AMPx = 0 → {5, 6} | 2.2V/3V | 15 | 30 | |
| | | DAC12AMPx = 0 → 7 | 2.2V/3V | 6 | 12 | |
| t _{S(FS)} | DAC12_xDAT = 80h → F7Fh → 80h | DAC12AMPx = 2 | 2.2V/3V | 100 | 200 | μs |
| | | DAC12AMPx = 3,5 | 2.2V/3V | 40 | 80 | |
| | | DAC12AMPx = 4,6,7 | 2.2V/3V | 15 | 30 | |
| t _{S(C-C)} | DAC12_xDAT = 3F8h → 408h → 3F8h BF8h → C08h → BF8h | DAC12AMPx = 2 | 2.2V/3V | 5 | | μs |
| | | DAC12AMPx = 3,5 | 2.2V/3V | 2 | | |
| | | DAC12AMPx = 4,6,7 | 2.2V/3V | 1 | | |
| SR | DAC12_xDAT = 80h → F7Fh → 80h | DAC12AMPx = 2 | 2.2V/3V | 0.05 | 0.12 | V/μs |
| | | DAC12AMPx = 3,5 | 2.2V/3V | 0.35 | 0.7 | |
| | | DAC12AMPx = 4,6,7 | 2.2V/3V | 1.5 | 2.7 | |
| Glitch energy: full-scale | DAC12_xDAT = 80h → F7Fh → 80h | DAC12AMPx = 2 | 2.2V/3V | 10 | | nV-s |
| | | DAC12AMPx = 3,5 | 2.2V/3V | 10 | | |
| | | DAC12AMPx = 4,6,7 | 2.2V/3V | 10 | | |

- NOTES: 1. R_{Load} and C_{Load} connected to AV_{SS} (not AV_{CC}/2) in Figure 23.
 2. Slew rate applies to output voltage steps ≥ 200mV.

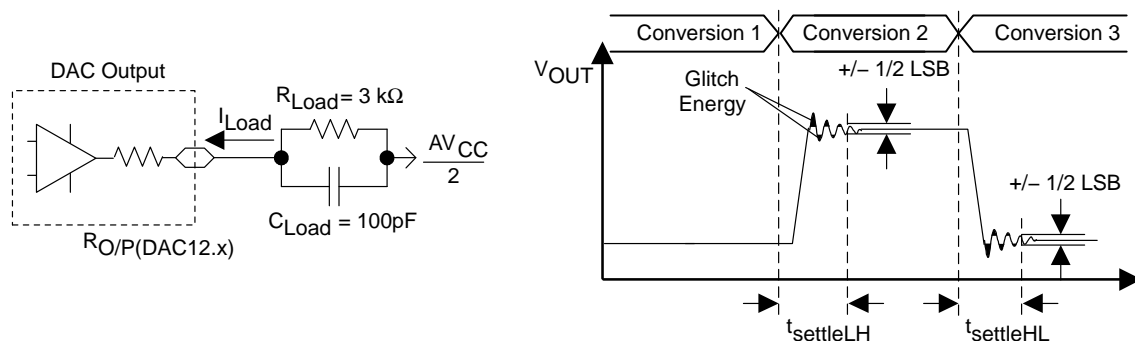


Figure 23. Settling Time and Glitch Energy Testing

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

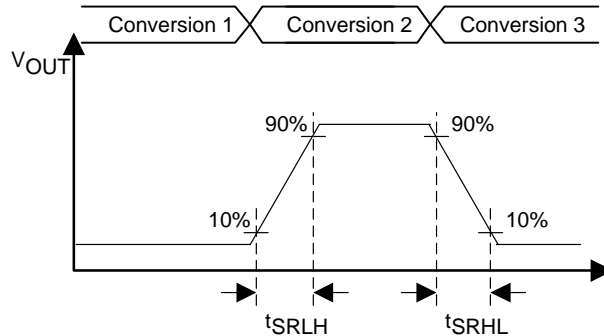


Figure 24. Slew Rate Testing

12-bit DAC, dynamic specifications continued ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|---|-----------------|-----|-----|-----|------|
| BW _{-3dB} 3-dB bandwidth, V _{DC} =1.5V, V _{AC} =0.1V _{PP} (see Figure 25) | DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h | 2.2V/3V | 40 | | | kHz |
| | DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h | 2.2V/3V | 180 | | | |
| | DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h | 2.2V/3V | 550 | | | |
| Channel to channel crosstalk (see Note 1 and Figure 26) | DAC12_0DAT = 800h, No Load, DAC12_1DAT = 80h<->F7Fh, R _{Load} = 3kΩ f _{DAC12_1OUT} = 10kHz @ 50/50 duty cycle | 2.2V/3V | | -80 | | dB |
| | DAC12_0DAT = 80h<->F7Fh, R _{Load} = 3kΩ, DAC12_1DAT = 800h, No Load f _{DAC12_0OUT} = 10kHz @ 50/50 duty cycle | 2.2V/3V | | -80 | | |

NOTES: 1. R_{LOAD} = 3 kΩ, C_{LOAD} = 100 pF

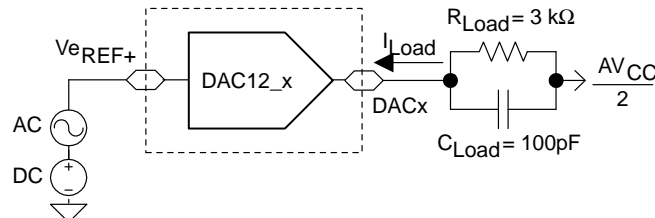


Figure 25. Test Conditions for 3-dB Bandwidth Specification

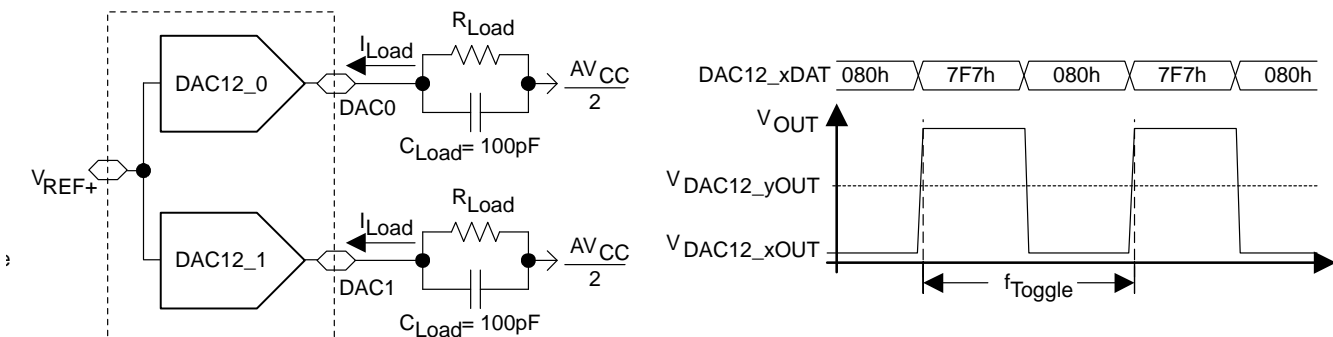


Figure 26. Crosstalk Test Conditions

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

flash memory

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------------|---|-----------------------|-----------------|-----------------|-----------------|-----|------------------|
| V _{CC(PGM/ERASE)} | Program and erase supply voltage | | | 2.7 | | 3.6 | V |
| f _{FTG} | Flash timing generator frequency | | | 257 | | 476 | kHz |
| I _{PGM} | Supply current from DV _{CC} during program | | 2.7 V/ 3.6 V | | 3 | 5 | mA |
| I _{ERASE} | Supply current from DV _{CC} during erase | | 2.7 V/ 3.6 V | | 3 | 7 | mA |
| t _{CPT} | Cumulative program time | see Note 1 | 2.7 V/ 3.6 V | | | 4 | ms |
| t _{CMErase} | Cumulative mass erase time | see Note 2 | 2.7 V/ 3.6 V | 200 | | | ms |
| | Program/Erase endurance | | | 10 ⁴ | 10 ⁵ | | cycles |
| t _{Retention} | Data retention duration | T _J = 25°C | | 100 | | | years |
| t _{Word} | Word or byte program time | see Note 3 | | | 35 | | t _{FTG} |
| t _{Block, 0} | Block program time for 1 st byte or word | | | | 30 | | |
| t _{Block, 1-63} | Block program time for each additional byte or word | | | | 21 | | |
| t _{Block, End} | Block program end-sequence wait time | | | | 6 | | |
| t _{Mass Erase} | Mass erase time | | | | 5297 | | |
| t _{Seq Erase} | Segment erase time | | | | 4819 | | |

- NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
 2. The mass erase duration generated by the flash timing generator is at least 11.1ms (= 5297x1/f_{FTG,max} = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
 3. These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1/f_{FTG}).

JTAG interface

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | NOM | MAX | UNIT |
|-----------------------|---|-----------------|-----------------|-----|-----|-----|------|
| f _{TCK} | TCK input frequency | see Note 1 | 2.2 V | 0 | | 5 | MHz |
| | | | 3 V | 0 | | 10 | MHz |
| R _{Internal} | Internal pull-up resistance on TMS, TCK, TDI/TCLK | see Note 2 | 2.2 V/ 3 V | 25 | 60 | 90 | kΩ |

- NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
 2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

JTAG fuse (see Note 1)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | NOM | MAX | UNIT |
|---------------------|---|-----------------------|-----------------|-----|-----|-----|------|
| V _{CC(FB)} | Supply voltage during fuse-blow condition | T _A = 25°C | | 2.5 | | | V |
| V _{FB} | Voltage level on TDI/TCLK for fuse-blow: F versions | | | 6 | | 7 | V |
| I _{FB} | Supply current into TDI/TCLK during fuse blow | | | | | 100 | mA |
| t _{FB} | Time to blow fuse | | | | | 1 | ms |

- NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

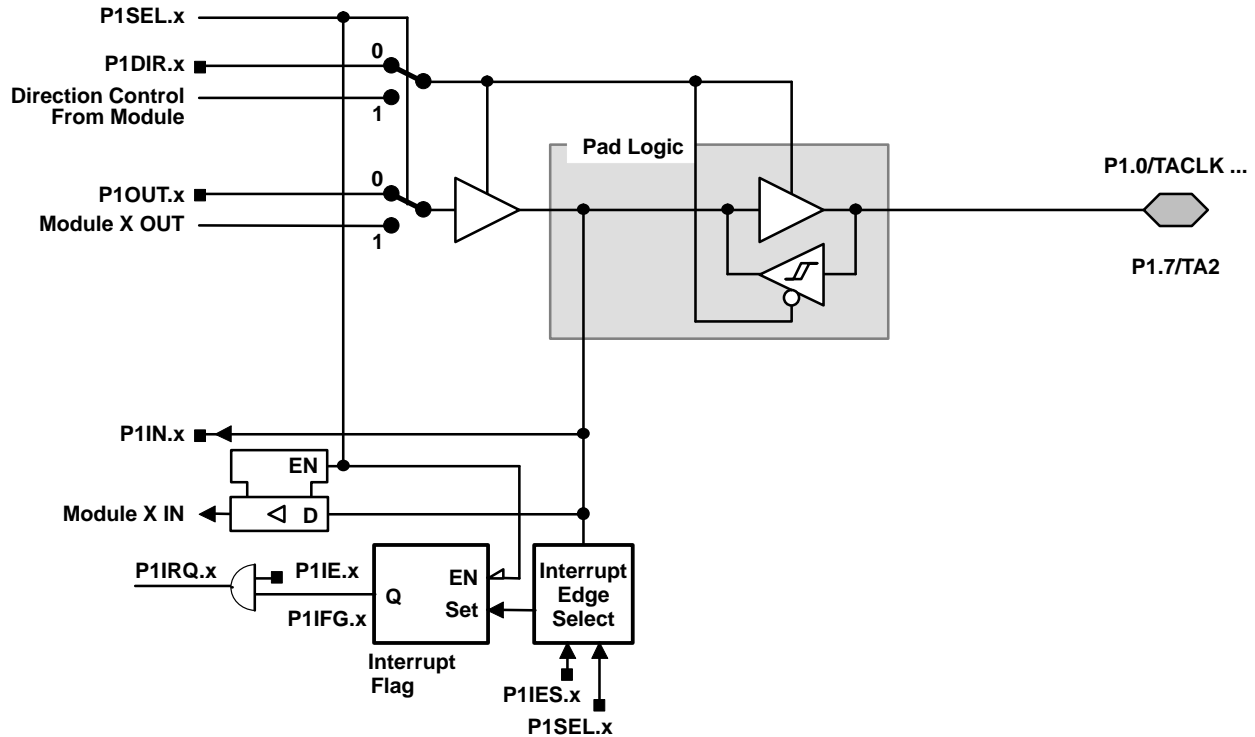
MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

APPLICATION INFORMATION

input/output schematics

port P1, P1.0 to P1.7, input/output with Schmitt trigger



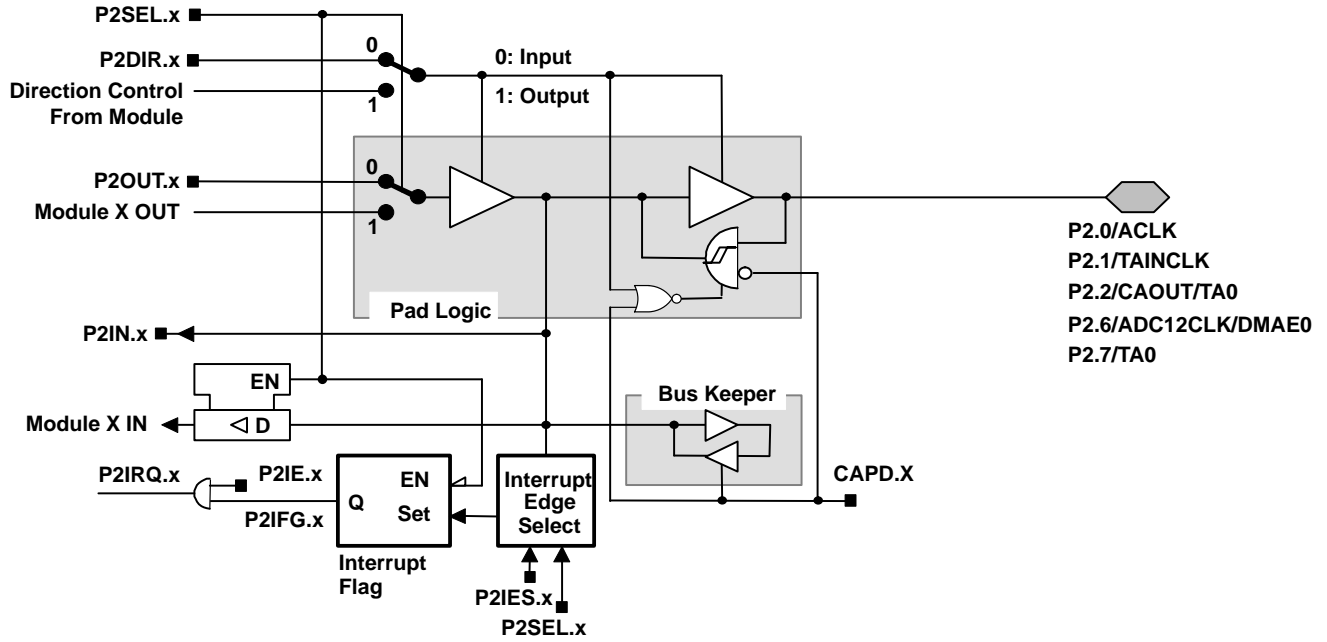
| PnSel.x | PnDIR.x | Dir. CONTROL FROM MODULE | PnOUT.x | MODULE X OUT | PnIN.x | MODULE X IN | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|--------------------------|---------|--------------------------|--------|--------------------|--------|---------|---------|
| P1Sel.0 | P1DIR.0 | P1DIR.0 | P1OUT.0 | DV _{SS} | P1IN.0 | TACLK [†] | P1IE.0 | P1IFG.0 | P1IES.0 |
| P1Sel.1 | P1DIR.1 | P1DIR.1 | P1OUT.1 | Out0 signal [†] | P1IN.1 | CCI0A [†] | P1IE.1 | P1IFG.1 | P1IES.1 |
| P1Sel.2 | P1DIR.2 | P1DIR.2 | P1OUT.2 | Out1 signal [†] | P1IN.2 | CCI1A [†] | P1IE.2 | P1IFG.2 | P1IES.2 |
| P1Sel.3 | P1DIR.3 | P1DIR.3 | P1OUT.3 | Out2 signal [†] | P1IN.3 | CCI2A [†] | P1IE.3 | P1IFG.3 | P1IES.3 |
| P1Sel.4 | P1DIR.4 | P1DIR.4 | P1OUT.4 | SMCLK | P1IN.4 | unused | P1IE.4 | P1IFG.4 | P1IES.4 |
| P1Sel.5 | P1DIR.5 | P1DIR.5 | P1OUT.5 | Out0 signal [†] | P1IN.5 | unused | P1IE.5 | P1IFG.5 | P1IES.5 |
| P1Sel.6 | P1DIR.6 | P1DIR.6 | P1OUT.6 | Out1 signal [†] | P1IN.6 | unused | P1IE.6 | P1IFG.6 | P1IES.6 |
| P1Sel.7 | P1DIR.7 | P1DIR.7 | P1OUT.7 | Out2 signal [†] | P1IN.7 | unused | P1IE.7 | P1IFG.7 | P1IES.7 |

[†] Signal from or to Timer_A

APPLICATION INFORMATION

input/output schematics (continued)

port P2, P2.0 to P2.2, P2.6, and P2.7 input/output with Schmitt trigger



x: Bit Identifier 0 to 2, 6, and 7 for Port P2

| PnSel.x | PnDIR.x | Dir. CONTROL FROM MODULE | PnOUT.x | MODULE X OUT | PnIN.x | MODULE X IN | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|--------------------------|---------|--------------------------|--------|--------------------|--------|---------|---------|
| P2Sel.0 | P2DIR.0 | P2DIR.0 | P2OUT.0 | ACLK | P2IN.0 | unused | P2IE.0 | P2IFG.0 | P2IES.0 |
| P2Sel.1 | P2DIR.1 | P2DIR.1 | P2OUT.1 | DV _{SS} | P2IN.1 | INCLK [‡] | P2IE.1 | P2IFG.1 | P2IES.1 |
| P2Sel.2 | P2DIR.2 | P2DIR.2 | P2OUT.2 | CAOUT [†] | P2IN.2 | CCI0B [‡] | P2IE.2 | P2IFG.2 | P2IES.2 |
| P2Sel.6 | P2DIR.6 | P2DIR.6 | P2OUT.6 | ADC12CLK [¶] | P2IN.6 | DMAE0 [#] | P2IE.6 | P2IFG.6 | P2IES.6 |
| P2Sel.7 | P2DIR.7 | P2DIR.7 | P2OUT.7 | Out0 signal [§] | P2IN.7 | unused | P2IE.7 | P2IFG.7 | P2IES.7 |

[†] Signal from Comparator_A

[‡] Signal to Timer_A

[§] Signal from Timer_A

[¶] ADC12CLK signal is output of the 12-bit ADC module

[#] Signal to DMA, channel 0, 1 and 2

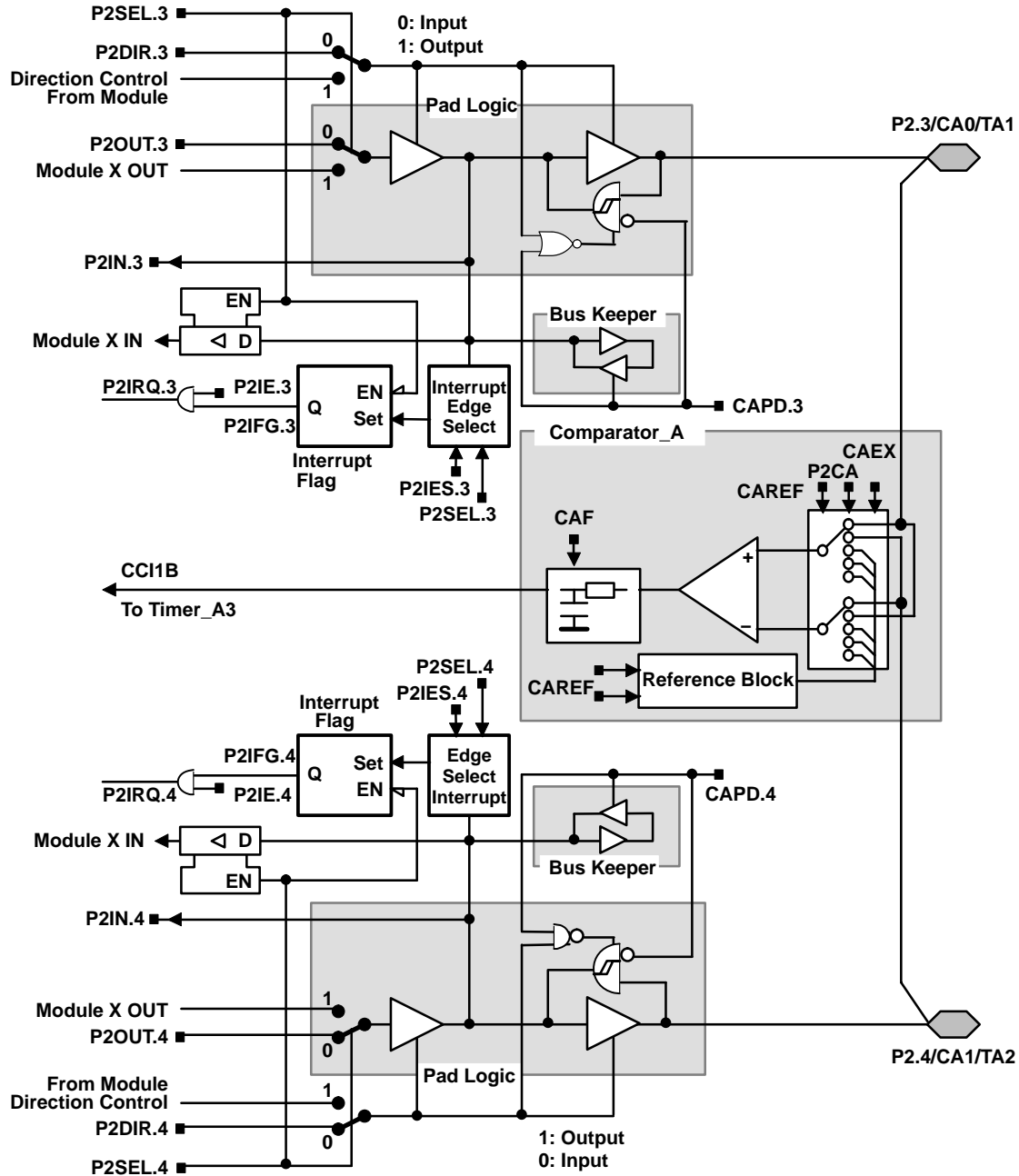
MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

APPLICATION INFORMATION

input/output schematics (continued)

port P2, P2.3 to P2.4, input/output with Schmitt trigger



| PnSel.x | PnDIR.x | DIRECTION CONTROL FROM MODULE | PnOUT.x | MODULE X OUT | PnIN.x | MODULE X IN | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|-------------------------------|---------|--------------|--------|-------------|--------|---------|---------|
| P2Sel.3 | P2DIR.3 | P2DIR.3 | P2OUT.3 | Out1 signal† | P2IN.3 | unused | P2IE.3 | P2IFG.3 | P2IES.3 |
| P2Sel.4 | P2DIR.4 | P2DIR.4 | P2OUT.4 | Out2 signal† | P2IN.4 | unused | P2IE.4 | P2IFG.4 | P2IES.4 |

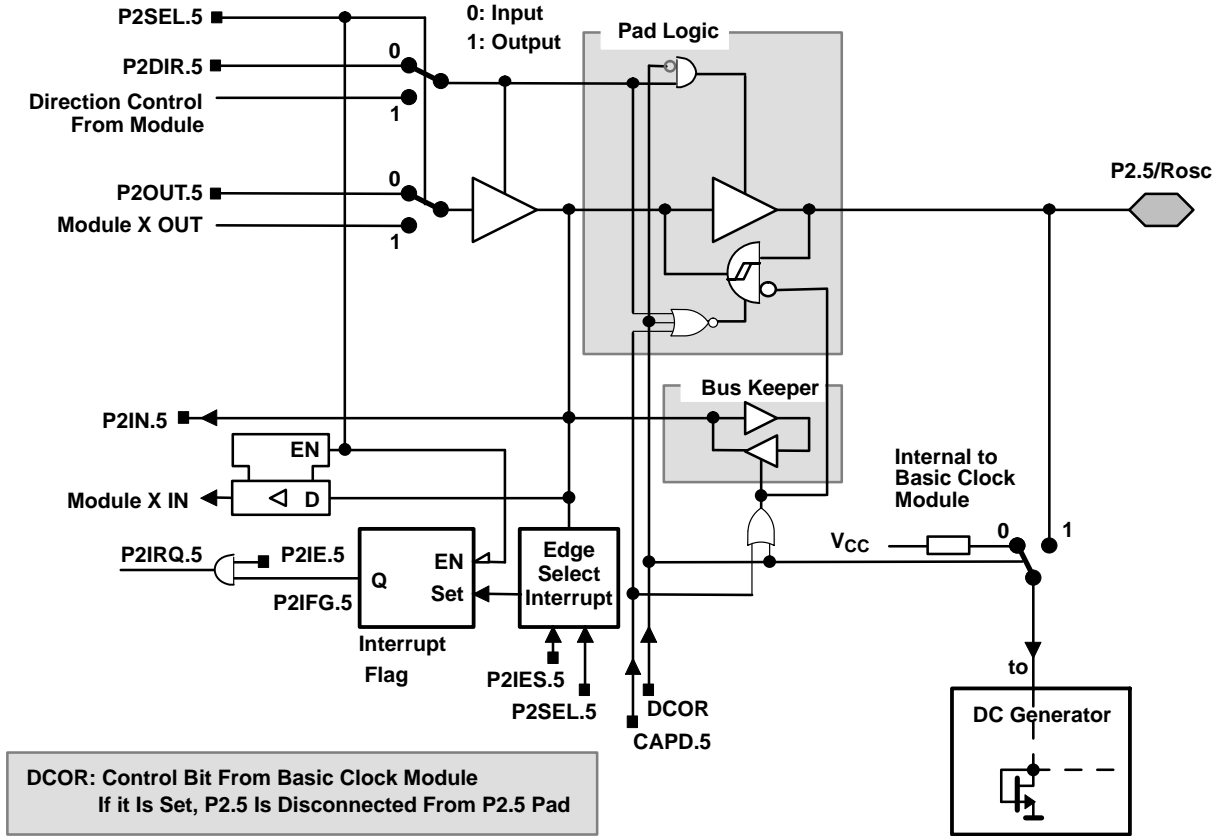
† Signal from Timer_A



APPLICATION INFORMATION

input/output schematics (continued)

port P2, P2.5, input/output with Schmitt trigger and R_{osc} function for the basic clock module



DCOR: Control Bit From Basic Clock Module
If it Is Set, P2.5 Is Disconnected From P2.5 Pad

| PnSel.x | PnDIR.x | DIRECTION CONTROL FROM MODULE | PnOUT.x | MODULE X OUT | PnIN.x | MODULE X IN | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|-------------------------------|---------|------------------|--------|-------------|--------|---------|---------|
| P2Sel.5 | P2DIR.5 | P2DIR.5 | P2OUT.5 | DV _{SS} | P2IN.5 | unused | P2IE.5 | P2IFG.5 | P2IES.5 |

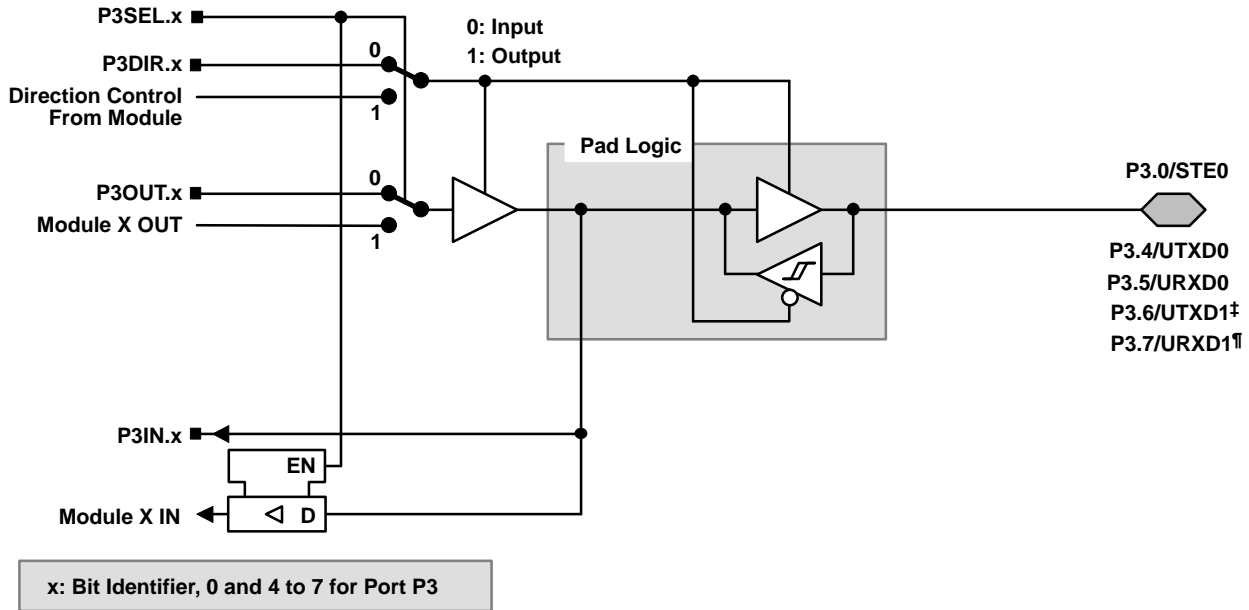
MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

APPLICATION INFORMATION

input/output schematics (continued)

port P3, P3.0 and P3.4 to P3.7, input/output with Schmitt trigger



| PnSel.x | PnDIR.x | DIRECTION CONTROL FROM MODULE | PnOUT.x | MODULE X OUT | PnIN.x | MODULE X IN |
|---------|---------|-------------------------------|---------|--------------------|--------|--------------------|
| P3Sel.0 | P3DIR.0 | DV _{SS} | P3OUT.0 | DV _{SS} | P3IN.0 | STE0 |
| P3Sel.4 | P3DIR.4 | DV _{CC} | P3OUT.4 | UTXD0 [†] | P3IN.4 | Unused |
| P3Sel.5 | P3DIR.5 | DV _{SS} | P3OUT.5 | DV _{SS} | P3IN.5 | URXD0 [§] |
| P3Sel.6 | P3DIR.6 | DV _{CC} | P3OUT.6 | UTXD1 [‡] | P3IN.6 | Unused |
| P3Sel.7 | P3DIR.7 | DV _{SS} | P3OUT.7 | DV _{SS} | P3IN.7 | URXD1 [¶] |

[†] Output from USART0 module

[‡] Output from USART1 module

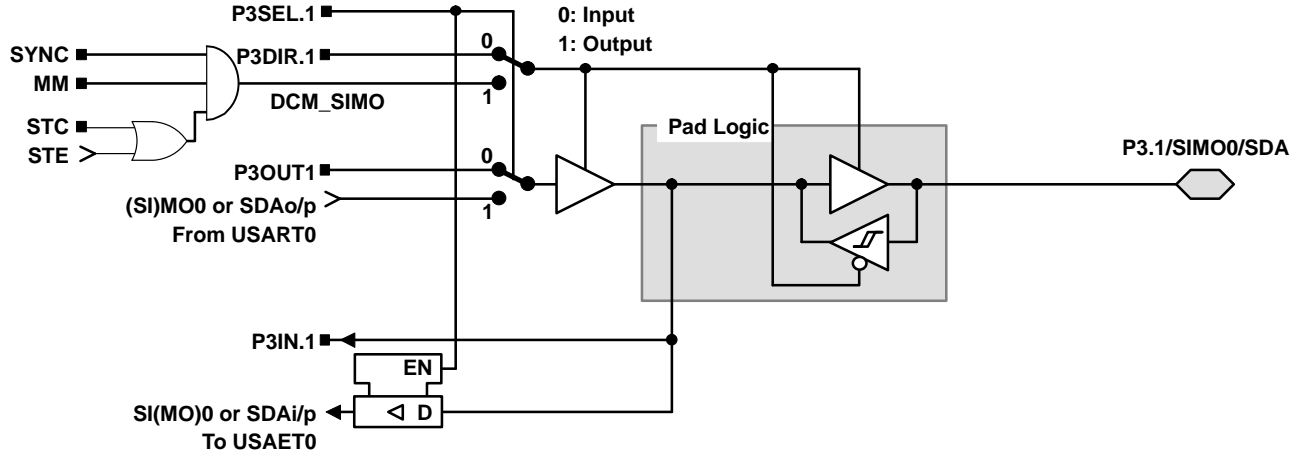
[§] Input to USART0 module

[¶] Input to USART1 module

APPLICATION INFORMATION

input/output schematics (continued)

port P3, P3.1, input/output with Schmitt trigger



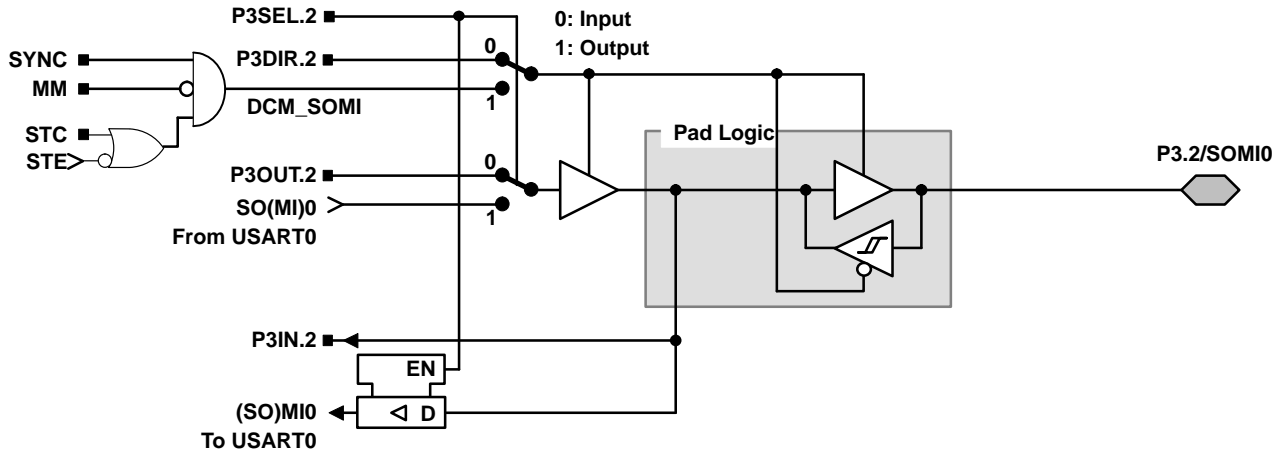
MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

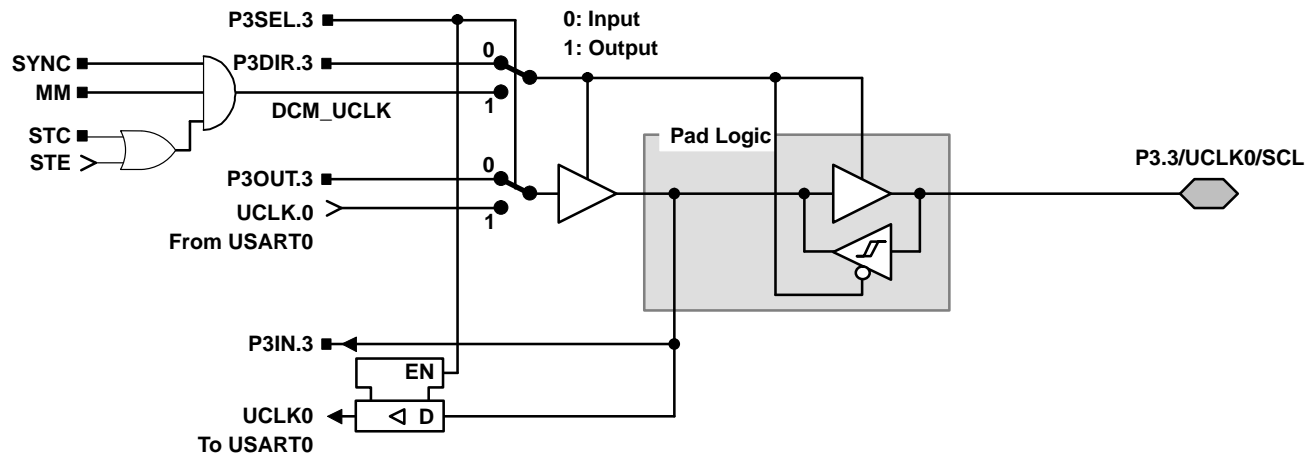
APPLICATION INFORMATION

input/output schematics (continued)

port P3, P3.2, input/output with Schmitt trigger



port P3, P3.3, input/output with Schmitt-trigger

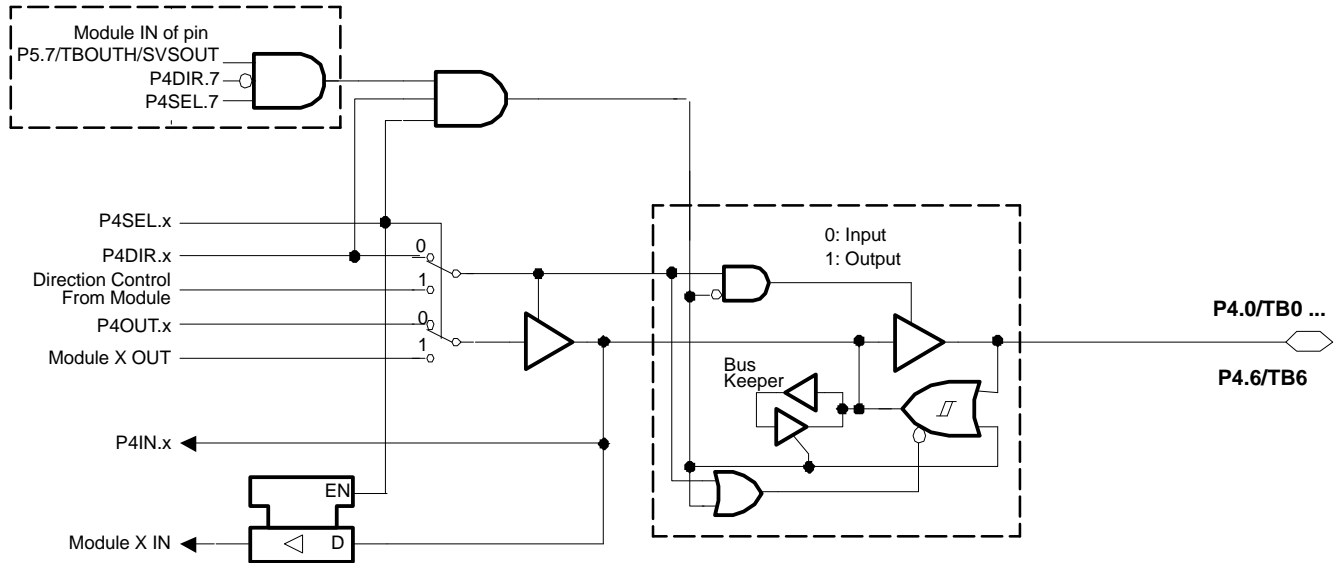


- NOTE: UART mode: The UART clock can only be an input. If UART mode and UART function are selected, the P3.3/UCLK0 is always an input.
- SPI, slave mode: The clock applied to UCLK0 is used to shift data in and out.
- SPI, master mode: The clock to shift data in and out is supplied to connected devices on pin P3.3/UCLK0 (in slave mode).
- I²C, slave mode: The clock applied to SCL is used to shift data in and out. The frequency of the clock source of the module must be ≥ 10 times the frequency of the SCL clock.
- I²C, master mode: To shift data in and out, the clock is supplied via the SCL terminal to all I²C slaves. The frequency of the clock source of the module must be ≥ 10 times the frequency of the SCL clock.

APPLICATION INFORMATION

input/output schematics (continued)

port P4, P4.0 to P4.6, input/output with Schmitt trigger



x: Bit Identifier, 0 to 6 for Port P4

| PnSel.x | PnDIR.x | DIRECTION CONTROL FROM MODULE | PnOUT.x | MODULE X OUT | PnIN.x | MODULE X IN |
|---------|---------|-------------------------------|---------|--------------------------|--------|----------------------------|
| P4Sel.0 | P4DIR.0 | P4DIR.0 | P4OUT.0 | Out0 signal [†] | P4IN.0 | CCI0A / CCI0B [‡] |
| P4Sel.1 | P4DIR.1 | P4DIR.1 | P4OUT.1 | Out1 signal [†] | P4IN.1 | CCI1A / CCI1B [‡] |
| P4Sel.2 | P4DIR.2 | P4DIR.2 | P4OUT.2 | Out2 signal [†] | P4IN.2 | CCI2A / CCI2B [‡] |
| P4Sel.3 | P4DIR.3 | P4DIR.3 | P4OUT.3 | Out3 signal [†] | P4IN.3 | CCI3A / CCI3B [‡] |
| P4Sel.4 | P4DIR.4 | P4DIR.4 | P4OUT.4 | Out4 signal [†] | P4IN.4 | CCI4A / CCI4B [‡] |
| P4Sel.5 | P4DIR.5 | P4DIR.5 | P4OUT.5 | Out5 signal [†] | P4IN.5 | CCI5A / CCI5B [‡] |
| P4Sel.6 | P4DIR.6 | P4DIR.6 | P4OUT.6 | Out6 signal [†] | P4IN.6 | CCI6A |

[†] Signal from Timer_B

[‡] Signal to Timer_B

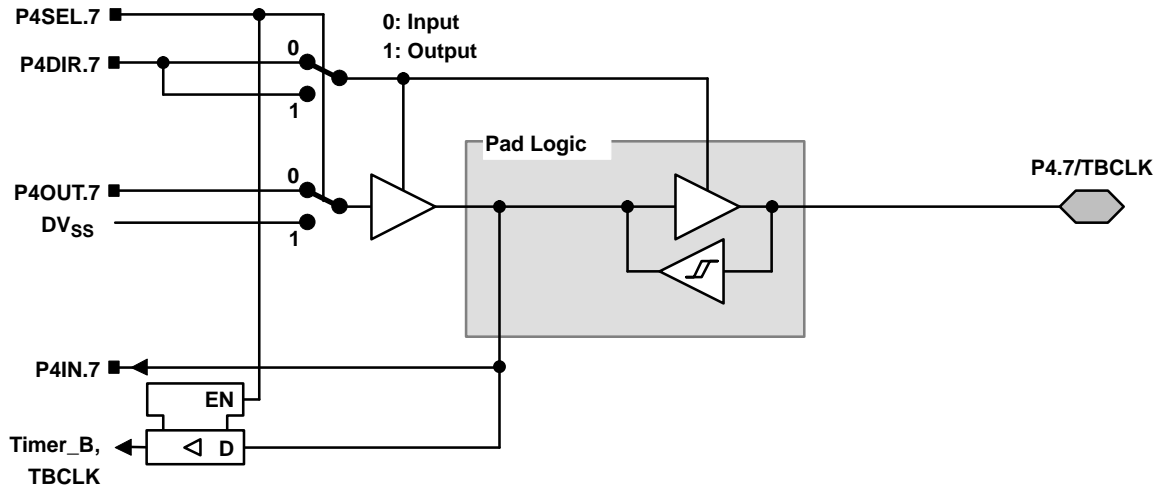
MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

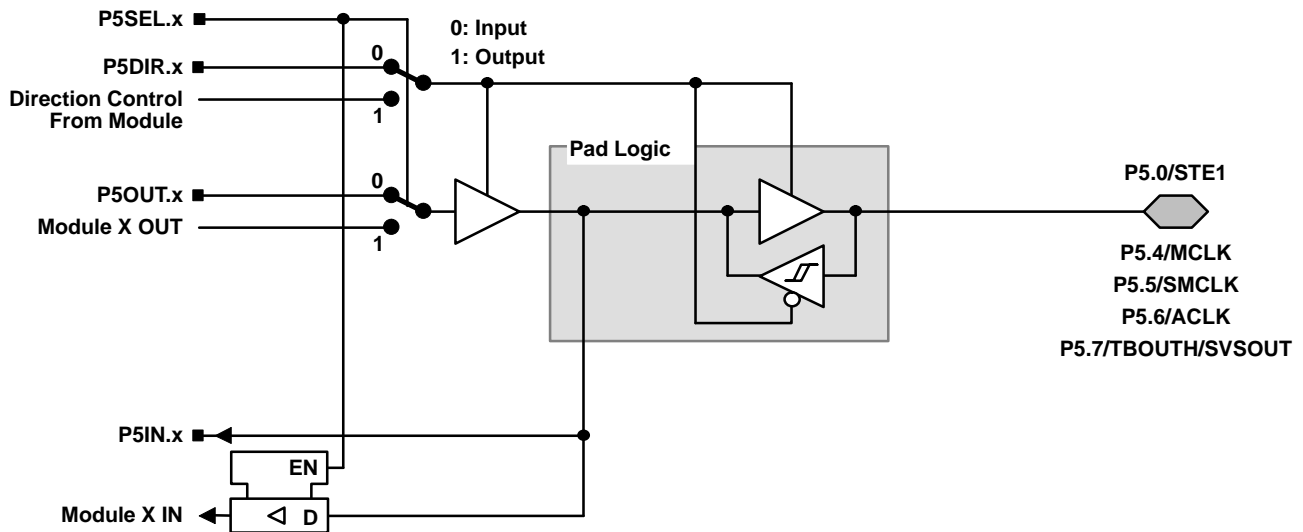
APPLICATION INFORMATION

input/output schematics (continued)

port P4, P4.7, input/output with Schmitt trigger



port P5, P5.0 and P5.4 to P5.7, input/output with Schmitt trigger



x: Bit Identifier, 0 and 4 to 7 for Port P5

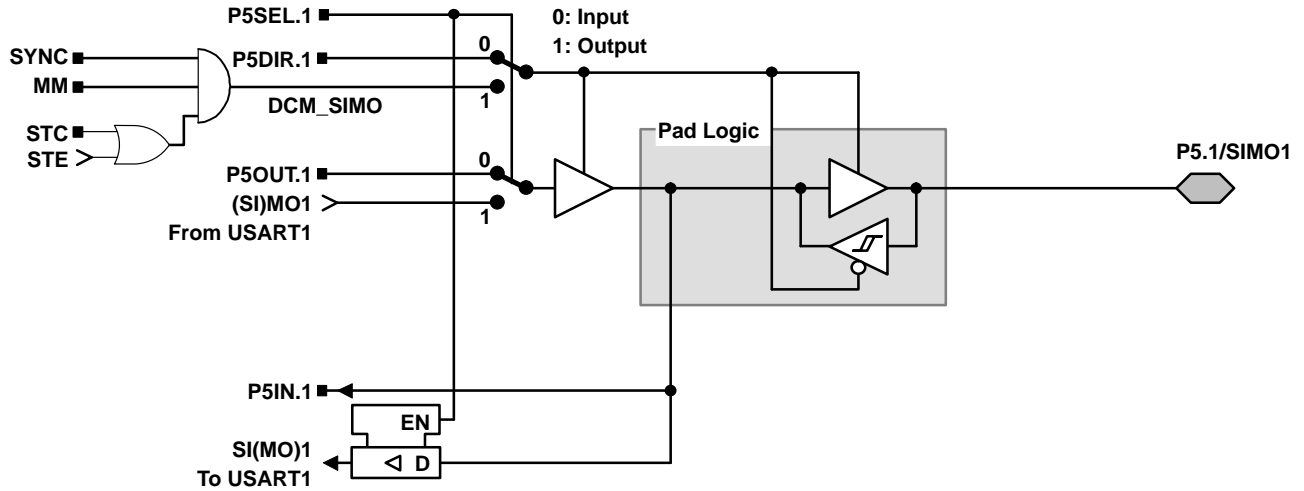
| PnSel.x | PnDIR.x | Dir. CONTROL FROM MODULE | PnOUT.x | MODULE X OUT | PnIN.x | MODULE X IN |
|---------|---------|--------------------------|---------|------------------|--------|-----------------------|
| P5Sel.0 | P5DIR.0 | DV _{SS} | P5OUT.0 | DV _{SS} | P5IN.0 | STE.1 |
| P5Sel.4 | P5DIR.4 | DV _{CC} | P5OUT.4 | MCLK | P5IN.4 | unused |
| P5Sel.5 | P5DIR.5 | DV _{CC} | P5OUT.5 | SMCLK | P5IN.5 | unused |
| P5Sel.6 | P5DIR.6 | DV _{CC} | P5OUT.6 | ACLK | P5IN.6 | unused |
| P5Sel.7 | P5DIR.7 | DV _{SS} | P5OUT.7 | SVSOUT | P5IN.7 | TBOOUTH _{iZ} |

NOTE: TBOOUTH_{iZ} signal is used by port module P4, pins P4.0 to P4.6. The function of TBOOUTH_{iZ} is mainly useful when used with Timer_B₇.

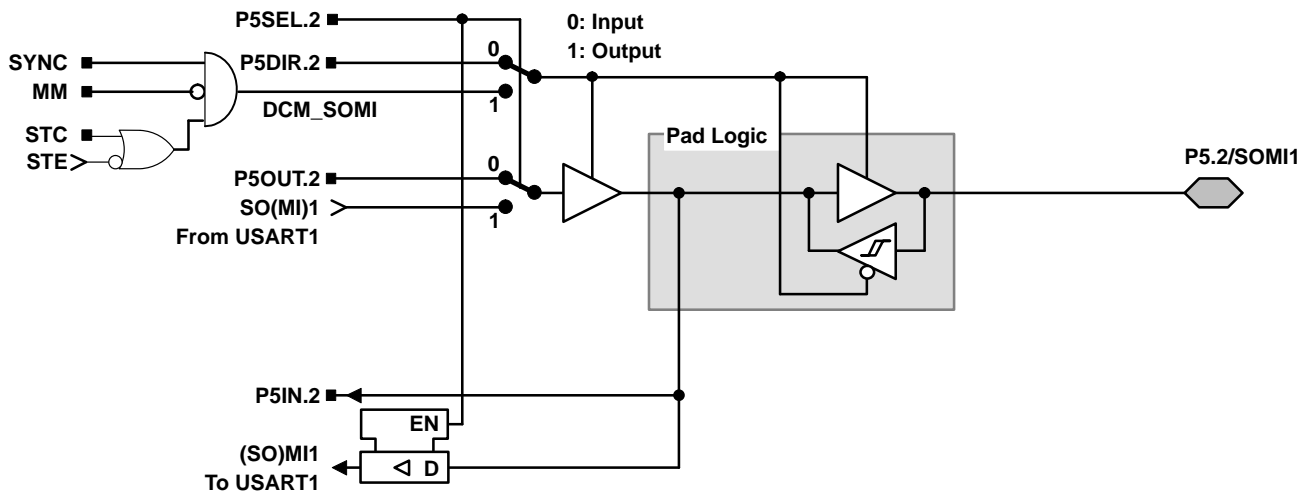
APPLICATION INFORMATION

input/output schematics (continued)

port P5, P5.1, input/output with Schmitt trigger



port P5, P5.2, input/output with Schmitt trigger



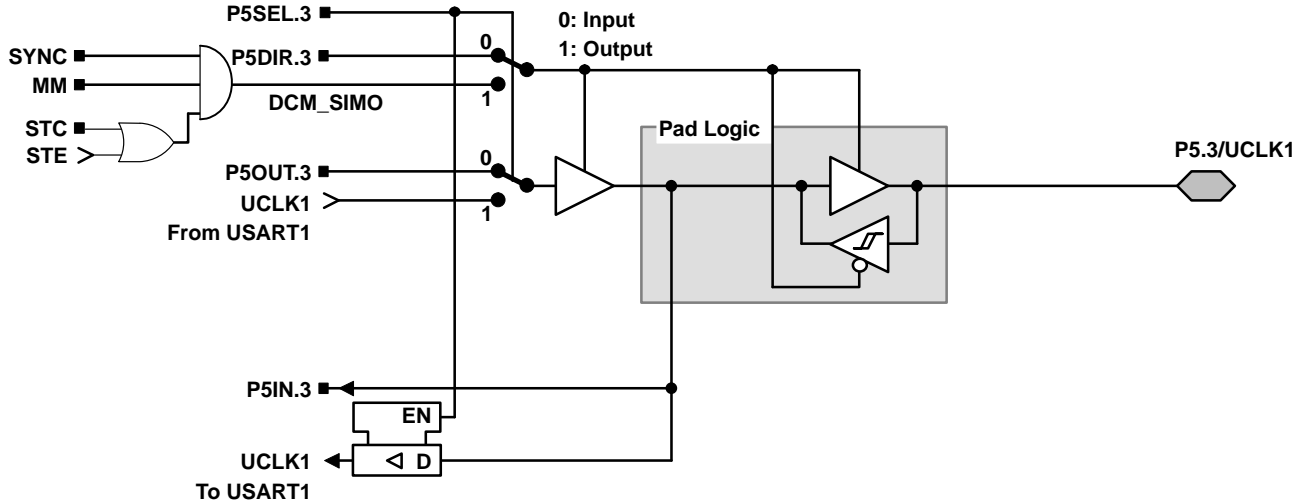
MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

APPLICATION INFORMATION

input/output schematics (continued)

port P5, P5.3, input/output with Schmitt trigger

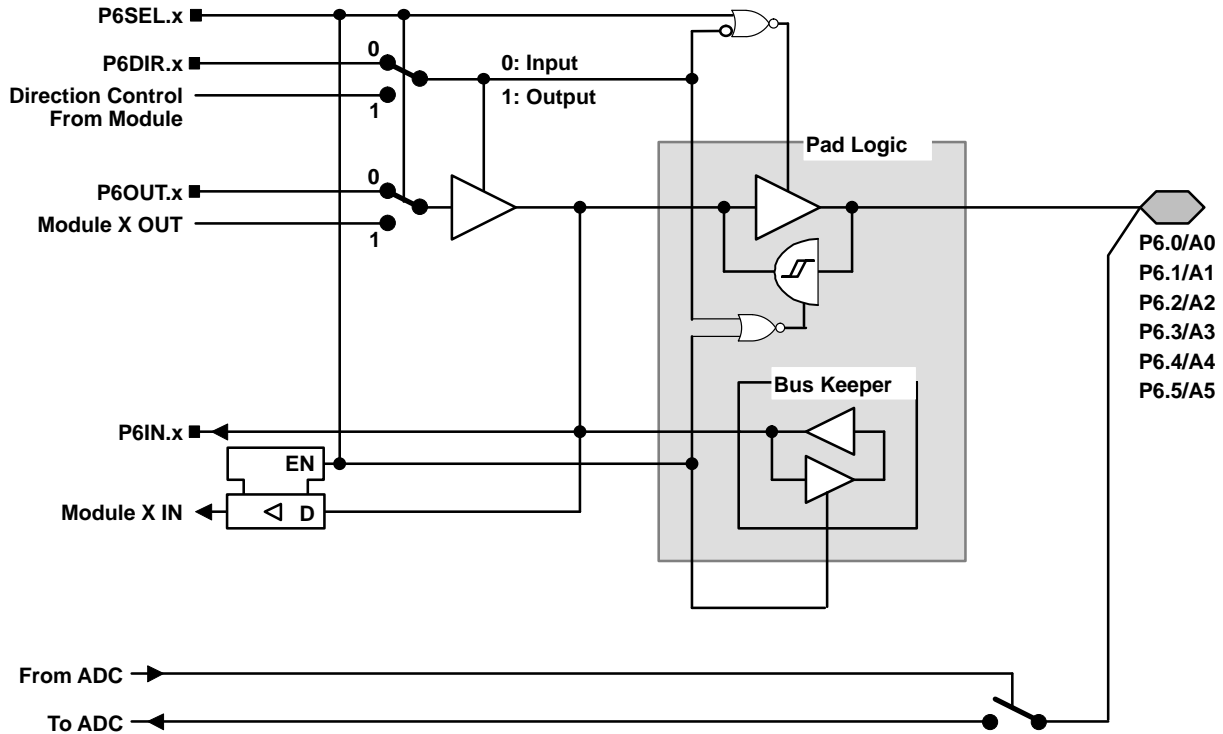


- NOTE: UART mode: The UART clock can only be an input. If UART mode and UART function are selected, the P5.3/UCLK1 direction is always input.
- SPI, slave mode: The clock applied to UCLK1 is used to shift data in and out.
- SPI, master mode: The clock to shift data in and out is supplied to connected devices on pin P5.3/UCLK1 (in slave mode).

APPLICATION INFORMATION

input/output schematics (continued)

port P6, P6.0 to P6.5, input/output with Schmitt trigger



x: Bit Identifier, 0 to 5 for Port P6

NOTE: Analog signals applied to digital gates can cause current flow from the positive to the negative terminal. The throughput current flows if the analog signal is in the range of transitions 0→1 or 1←0. The value of the throughput current depends on the driving capability of the gate. For MSP430, it is approximately 100 μA.

Use P6SEL.x=1 to prevent throughput current. P6SEL.x should be set, even if the signal at the pin is not being used by the ADC12.

| PnSel.x | PnDIR.x | DIR. CONTROL FROM MODULE | PnOUT.x | MODULE X OUT | PnIN.x | MODULE X IN |
|---------|---------|--------------------------|---------|------------------|--------|-------------|
| P6Sel.0 | P6DIR.0 | P6DIR.0 | P6OUT.0 | DV _{SS} | P6IN.0 | unused |
| P6Sel.1 | P6DIR.1 | P6DIR.1 | P6OUT.1 | DV _{SS} | P6IN.1 | unused |
| P6Sel.2 | P6DIR.2 | P6DIR.2 | P6OUT.2 | DV _{SS} | P6IN.2 | unused |
| P6Sel.3 | P6DIR.3 | P6DIR.3 | P6OUT.3 | DV _{SS} | P6IN.3 | unused |
| P6Sel.4 | P6DIR.4 | P6DIR.4 | P6OUT.4 | DV _{SS} | P6IN.4 | unused |
| P6Sel.5 | P6DIR.5 | P6DIR.5 | P6OUT.5 | DV _{SS} | P6IN.5 | unused |

NOTE: The signal at pins P6.x/Ax is used by the 12-bit ADC module.

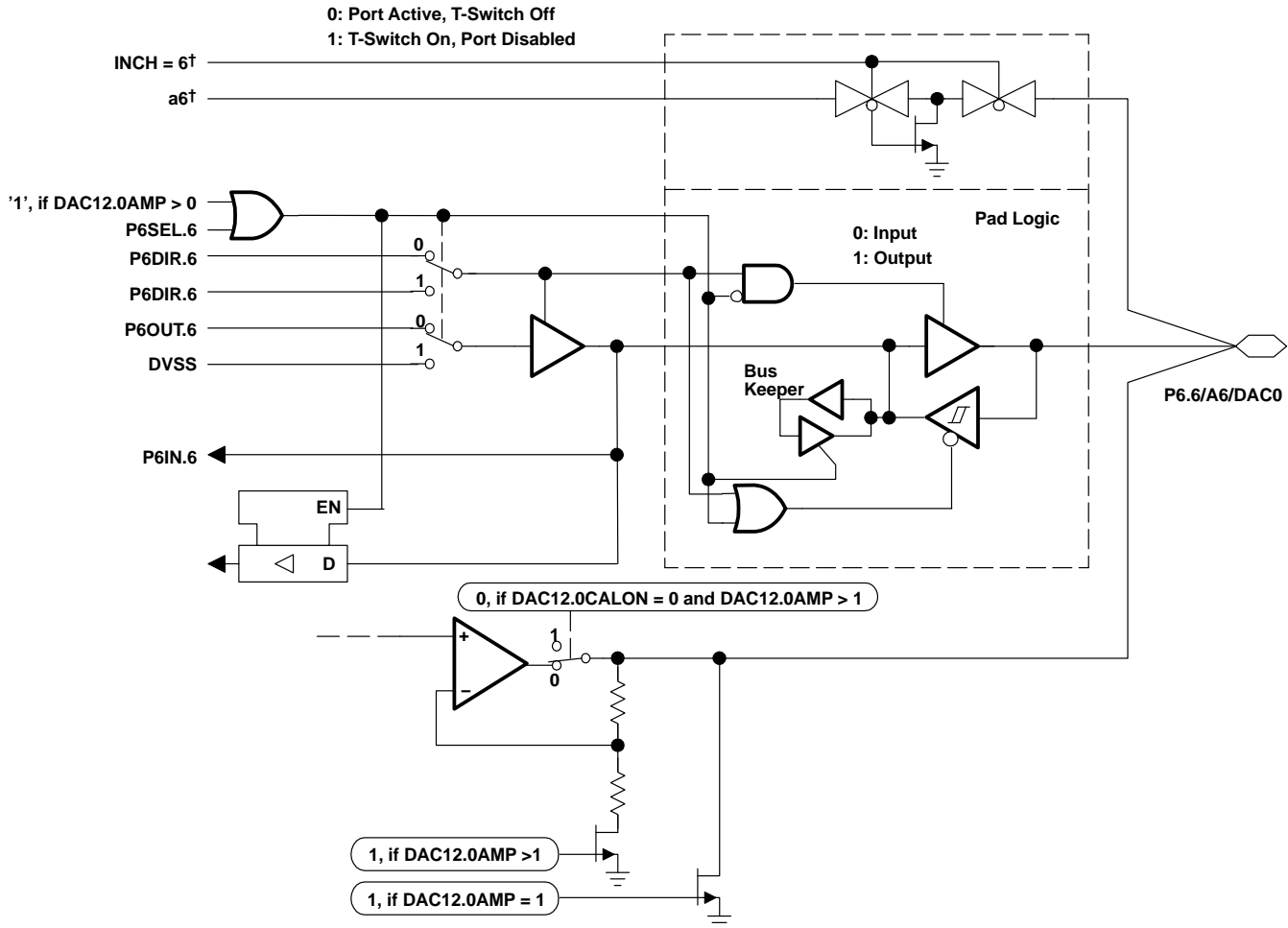
MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

APPLICATION INFORMATION

input/output schematics (continued)

port P6, P6.6, input/output with Schmitt trigger

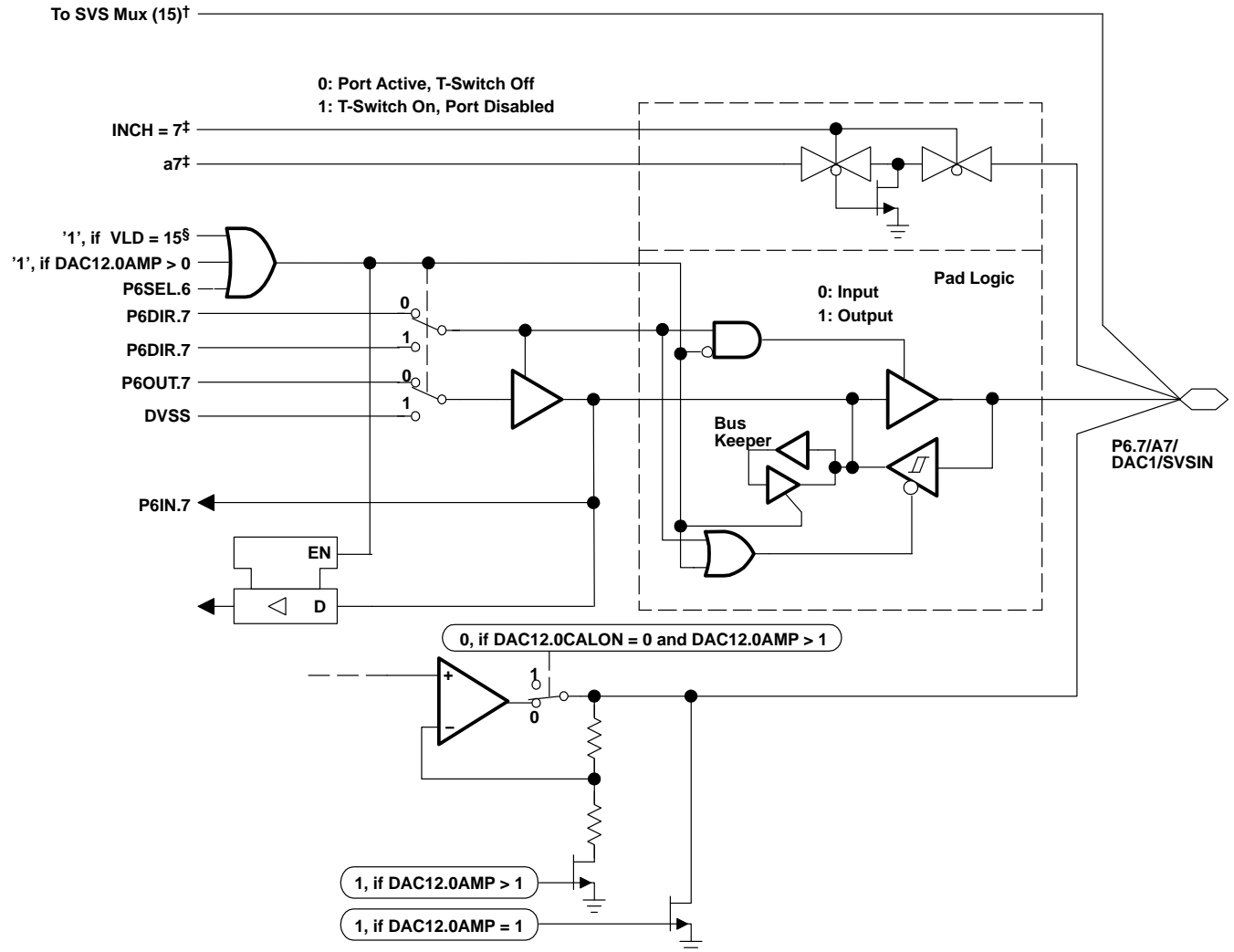


†Signal from or to ADC12

APPLICATION INFORMATION

input/output schematics (continued)

port P6, P6.7, input/output with Schmitt trigger



[†]Signal to SVS Block, Selected if VLD = 15

[‡]Signal From or To ADC12

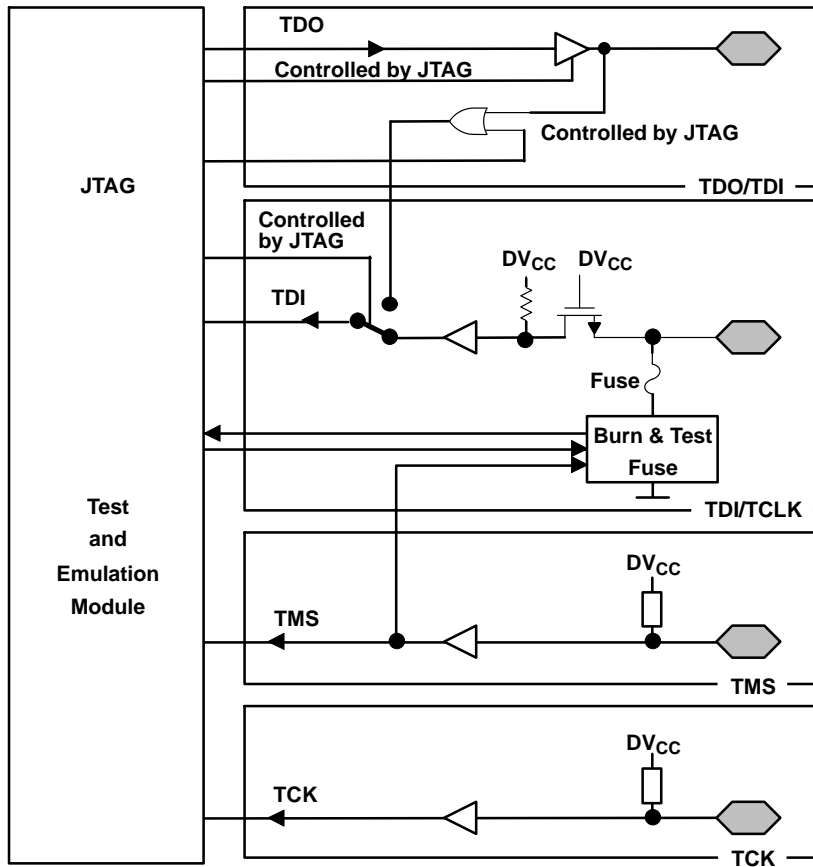
[§]VLD Control Bits are Located in SVS

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

APPLICATION INFORMATION

JTAG pins TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt trigger



During Programming Activity and During Blowing of the Fuse, Pin TDO/TDI Is Used to Apply the Test Input Data for JTAG Circuitry

APPLICATION INFORMATION

JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF} , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 27). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

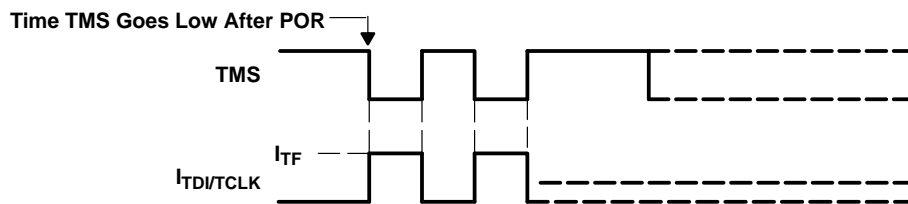


Figure 27. Fuse Check Mode Current, MSP430F15x/16x/161x

MSP430F15x, MSP430F16x, MSP430F161x MIXED SIGNAL MICROCONTROLLER

SLAS368G – OCTOBER 2002 – REVISED MARCH 2011

Data Sheet Revision History

| LITERATURE NUMBER | SUMMARY |
|-------------------|--|
| SLAS368F | In absolute maximum ratings table, changed T_{stg} min from -40°C to -55°C (page 25) Added Development Tools Support section (page 2) |
| SLAS368G | Changed limits on $t_{d(SV_{Son})}$ parameter (page 35) |



PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F155IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F155 | Samples |
| MSP430F155IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F155 | Samples |
| MSP430F155IRTDR | ACTIVE | VQFN | RTD | 64 | 2500 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | M430F155 | Samples |
| MSP430F155IRTD | ACTIVE | VQFN | RTD | 64 | 250 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | M430F155 | Samples |
| MSP430F156IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F156 | Samples |
| MSP430F156IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F156 | Samples |
| MSP430F156IRTDR | ACTIVE | VQFN | RTD | 64 | 2500 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | M430F156 | Samples |
| MSP430F156IRTD | ACTIVE | VQFN | RTD | 64 | 250 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | M430F156 | Samples |
| MSP430F157IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F157 | Samples |
| MSP430F157IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F157 | Samples |
| MSP430F157IRTD | ACTIVE | VQFN | RTD | 64 | 250 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | M430F157 | Samples |
| MSP430F1610IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F1610 | Samples |
| MSP430F1610IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F1610 | Samples |
| MSP430F1610IRTDR | ACTIVE | VQFN | RTD | 64 | 2500 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | M430F1610 | Samples |
| MSP430F1610IRTD | ACTIVE | VQFN | RTD | 64 | 250 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | M430F1610 | Samples |
| MSP430F1611IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F1611 | Samples |
| MSP430F1611IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F1611 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F1611IRTDR | ACTIVE | VQFN | RTD | 64 | 2500 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | M430F1611 | Samples |
| MSP430F1611IRTD | ACTIVE | VQFN | RTD | 64 | 250 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | M430F1611 | Samples |
| MSP430F1612IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F1612 | Samples |
| MSP430F1612IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F1612 | Samples |
| MSP430F1612IRTDR | ACTIVE | VQFN | RTD | 64 | 2500 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | M430F1612 | Samples |
| MSP430F1612IRTD | ACTIVE | VQFN | RTD | 64 | 250 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | M430F1612 | Samples |
| MSP430F167IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F167 | Samples |
| MSP430F167IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F167 | Samples |
| MSP430F167IRTD | ACTIVE | VQFN | RTD | 64 | 250 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | M430F167 | Samples |
| MSP430F168IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F168 | Samples |
| MSP430F168IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F168 | Samples |
| MSP430F168IRTD | ACTIVE | VQFN | RTD | 64 | 250 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | M430F168 | Samples |
| MSP430F169IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F169 | Samples |
| MSP430F169IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F169 | Samples |
| MSP430F169IRTDR | ACTIVE | VQFN | RTD | 64 | 2500 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | M430F169 | Samples |
| MSP430F169IRTD | ACTIVE | VQFN | RTD | 64 | 250 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | M430F169 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



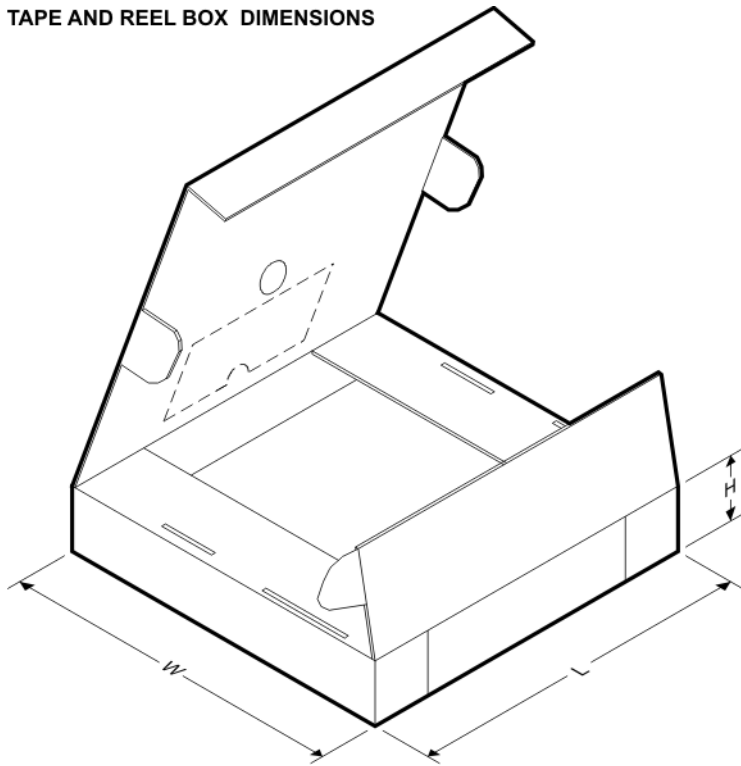
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F155IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F155IRTDR | VQFN | RTD | 64 | 2500 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F155IRTD | VQFN | RTD | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F156IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F156IRTDR | VQFN | RTD | 64 | 2500 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F156IRTD | VQFN | RTD | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F157IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F157IRTD | VQFN | RTD | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F1610IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F1610IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F1610IRTDR | VQFN | RTD | 64 | 2500 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F1610IRTD | VQFN | RTD | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F1611IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F1611IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F1611IRTDR | VQFN | RTD | 64 | 2500 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F1611IRTD | VQFN | RTD | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F1612IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F1612IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F1612IRTDR | VQFN | RTD | 64 | 2500 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F1612IRTD | VQFN | RTD | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F167IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F167IRTD | VQFN | RTD | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F168IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F168IRTD | VQFN | RTD | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F169IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F169IRTD | VQFN | RTD | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F155IPMR | LQFP | PM | 64 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F155IRTDR | VQFN | RTD | 64 | 2500 | 367.0 | 367.0 | 38.0 |
| MSP430F155IRTD | VQFN | RTD | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F156IPMR | LQFP | PM | 64 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F156IRTDR | VQFN | RTD | 64 | 2500 | 367.0 | 367.0 | 38.0 |
| MSP430F156IRTD | VQFN | RTD | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F157IPMR | LQFP | PM | 64 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F157IRTD | VQFN | RTD | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F1610IPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F1610IPMR | LQFP | PM | 64 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F1610IRTDR | VQFN | RTD | 64 | 2500 | 367.0 | 367.0 | 38.0 |
| MSP430F1610IRTDT | VQFN | RTD | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F1611IPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSP430F1611IPMR | LQFP | PM | 64 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F1611IRTDR | VQFN | RTD | 64 | 2500 | 367.0 | 367.0 | 38.0 |
| MSP430F1611IRTDT | VQFN | RTD | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F1612IPMR | LQFP | PM | 64 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F1612IPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSP430F1612IRTDR | VQFN | RTD | 64 | 2500 | 367.0 | 367.0 | 38.0 |
| MSP430F1612IRTDT | VQFN | RTD | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F167IPMR | LQFP | PM | 64 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F167IRTDT | VQFN | RTD | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F168IPMR | LQFP | PM | 64 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F168IRTDT | VQFN | RTD | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F169IPMR | LQFP | PM | 64 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F169IRTDT | VQFN | RTD | 64 | 250 | 210.0 | 185.0 | 35.0 |

GENERIC PACKAGE VIEW

RTD 64

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



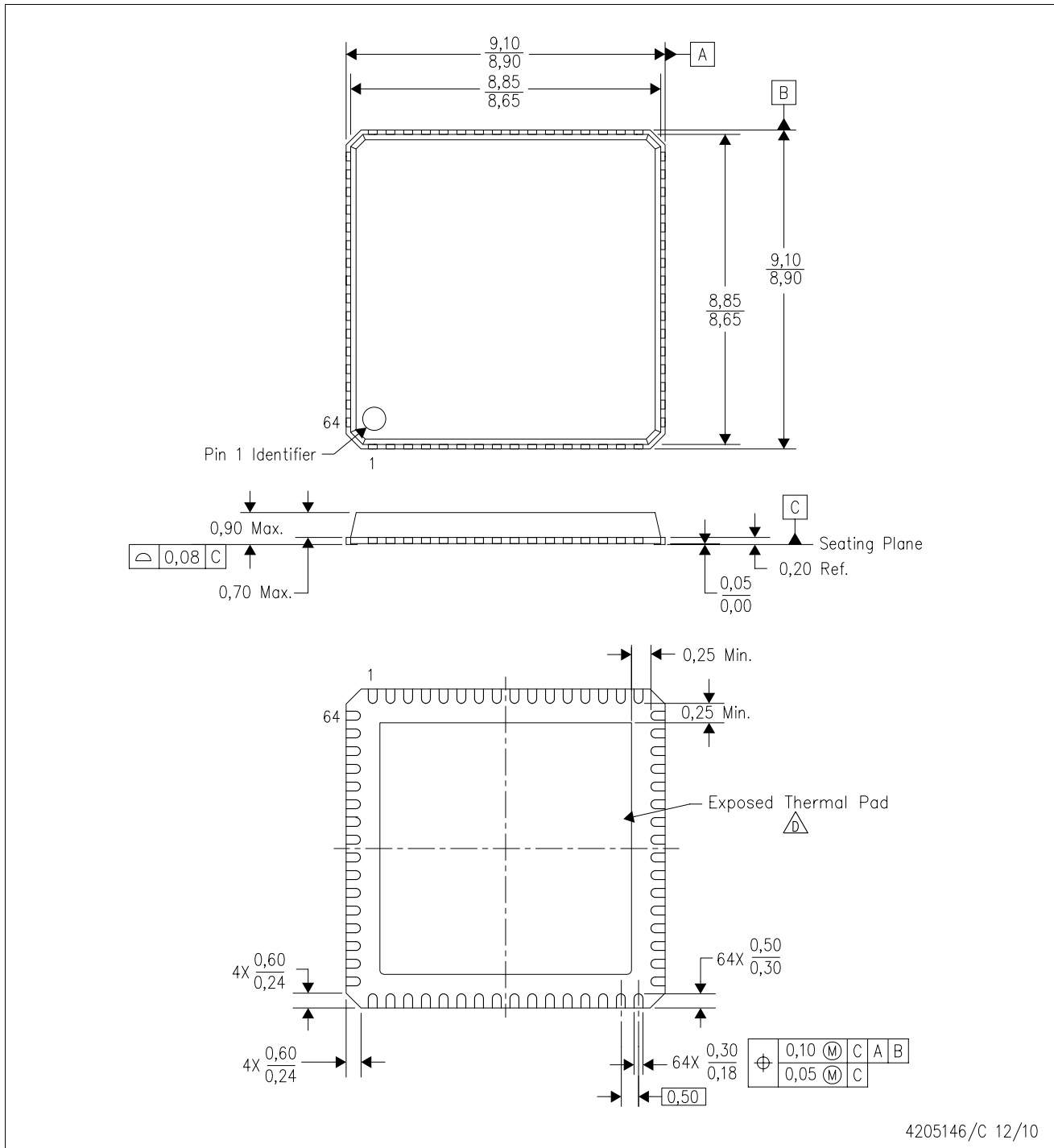
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.


4205146/D

MECHANICAL DATA

RTD (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

RTD (S-PVQFN-N64)

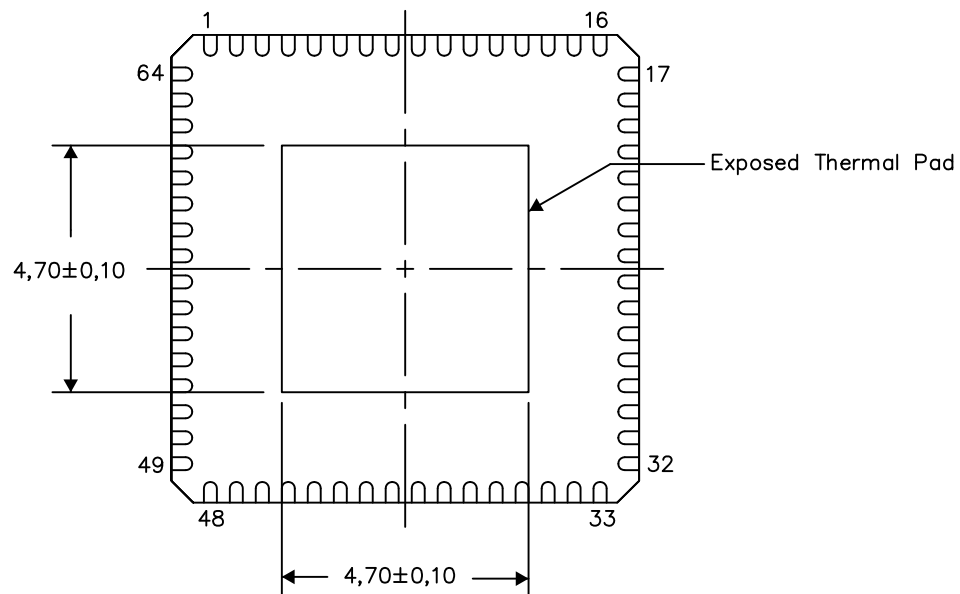
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

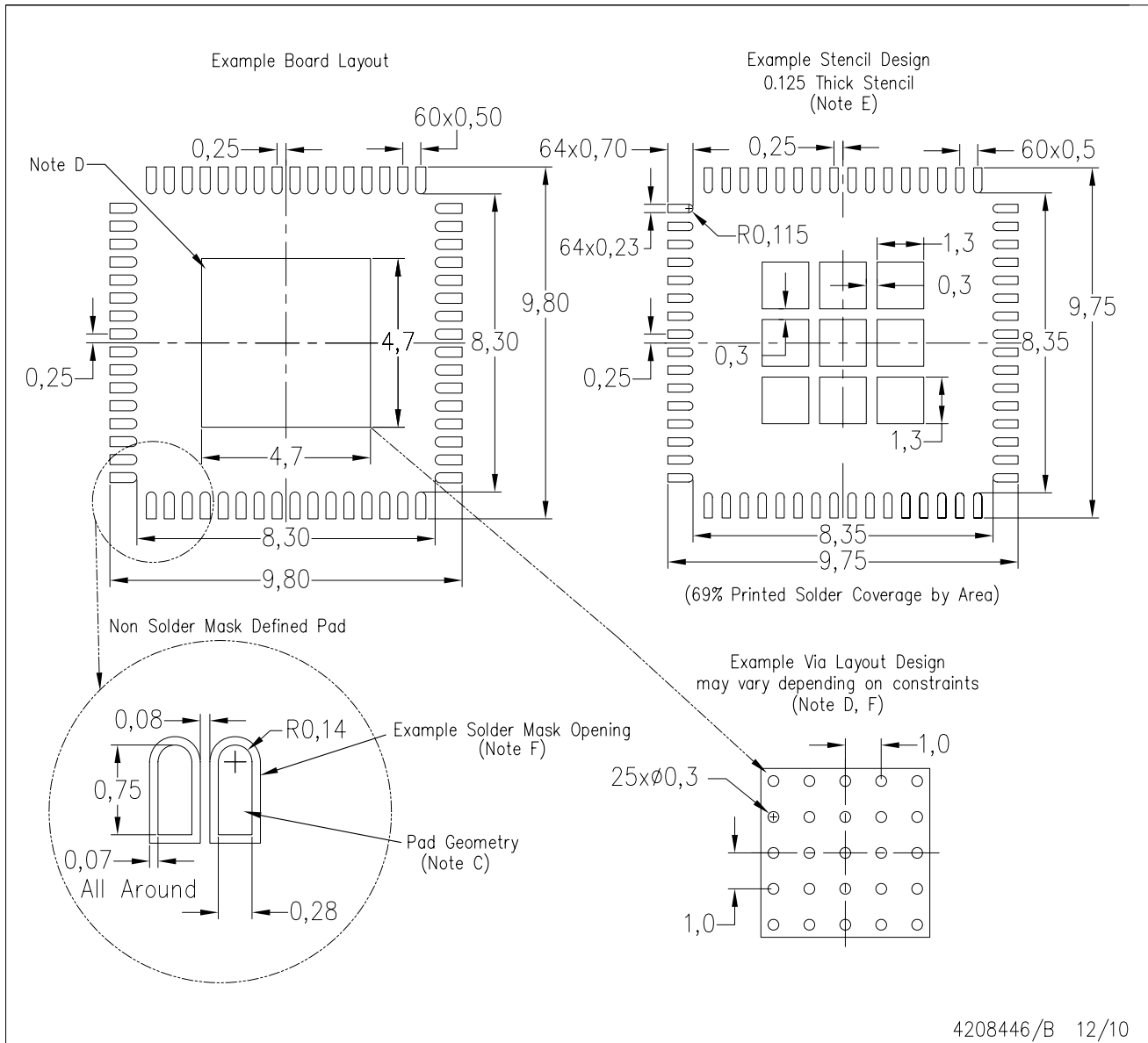
Exposed Thermal Pad Dimensions

4206338-3/F 09/14

NOTE: A. All linear dimensions are in millimeters

RTD (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Package, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customer should contact their board fabrication site for recommended solder mask tolerances and vias tenting recommendations for vias placed into the thermal pad.

PM0064A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



4215162/A 03/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated