



## Overview

### Features

- Optimized for headlight beam control applications
- Delivers up to 0.8 A continuous
- Low saturation voltage; typ. 1.2 V total @ 25 °C; 0.4 A
- Output protected against short circuit
- Overtemperature protection with hysteresis
- Over- and undervoltage lockout
- No crossover current
- Internal clamp diodes
- Enhanced power packages
- Range low-voltage detection with hysteresis
- Green Product (RoHS compliant)
- AEC Qualified



**PG-DSO-14**

Type	Ordering Code	Package
TLE 4206-2G	on request	PG-DSO-14

### Description

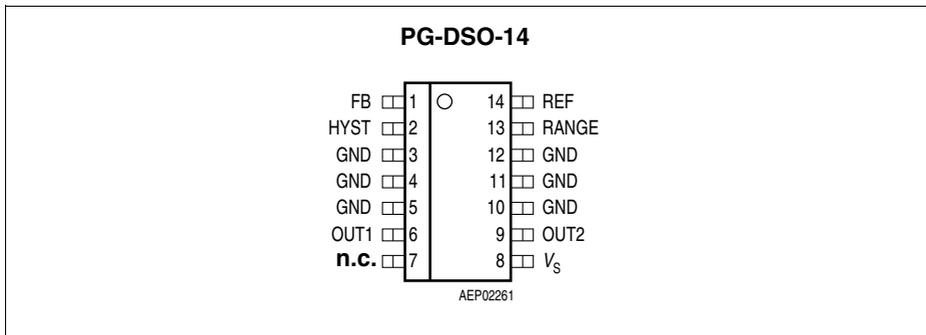
The TLE 4206-2G is a protected H-Bridge Driver designed specifically for automotive headlight beam control and industrial servo control applications. The part is built using Infineons bipolar high voltage power technology DOPL.

The standard enhanced power PG-DSO-14 package meets the application requirements and saves PCB-board space and costs.

The servo-loop-parameter pos.- and neg. Hysteresis, pos.- and neg. deadband and angle-amplification are programmable with external resistors. An internal window-comparator controls the input line. In the case of a fault condition, like short circuit to GND, short circuit to supply-voltage, and broken wire, the TLE 4206-2G stops the motor immediately (brake condition).

Furthermore the built in features like over- and undervoltage-lockout, short-circuit-protection and over-temperature-protection will open a wide range of automotive- and industrial applications.

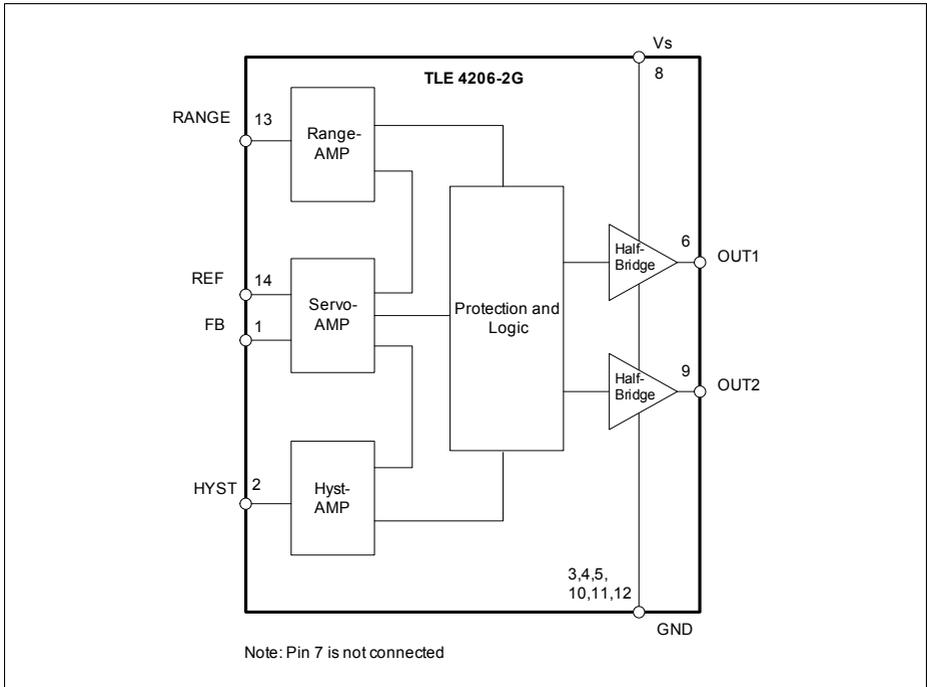
The TLE 4206-2G is a design-version of the TLE 4206. In the TLE 4206-2G, the current peak blanking Pin is disconnected. A hysteresis is introduced at the lower RANGE threshold. This allows reliable de-activation of the device by pulling the RANGE input to GND also under critical application conditions.



**Figure 1 Pin Configuration** (top view)

### Pin Definitions and Functions

Pin No. PG-DSO-14	Symbol	Function
1	FB	Feedback Input
2	HYST	Hysteresis I/O
<b>3, 4, 5, 10, 11, 12</b>	<b>GND</b>	<b>Ground</b>
<b>6</b>	<b>OUT1</b>	<b>Power Output 1</b>
7	n.c.	Not connected
<b>8</b>	$V_s$	<b>Power Supply Voltage</b>
<b>9</b>	<b>OUT2</b>	<b>Power Output 2</b>
13	RANGE	Range Input
14	REF	Reference Input



**Figure 2 Block Diagram**

**Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

**Voltages**

Supply voltage	$V_S$	- 0.3	45	V	-
Supply voltage	$V_S$	- 1	-	V	$t < 0.5 \text{ s}; I_S > - 2 \text{ A}$
Logic input voltages (FB, REF, RANGE, HYST, CPB)	$V_I$	- 0.3	20	V	-

**Currents**

Output current (OUT1, OUT2)	$I_{OUT}$	-	-	A	internally limited
Output current (Diode)	$I_{OUT}$	- 1	1	A	-
Input current (FB, REF, RANGE, HYST)	$I_{IN}$	- 2	2	mA	$t < 2 \text{ ms}; t/T < 0.1$
		- 6	6	mA	

**Temperatures**

Junction temperature	$T_j$	- 40	150	°C	-
Storage temperature	$T_{stg}$	- 50	150	°C	-

**Thermal Resistances**

Junction pin (PG-DSO-14)	$R_{thj-pin}$	-	25	K/W	measured to pin 5
Junction ambient (PG-DSO-14)	$R_{thjA}$	-	65	K/W	-

*Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.*

**Operating Range**

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	$V_S$	8	18	V	After $V_S$ rising above $V_{UV\ ON}$
Supply voltage increasing	$V_S$	- 0.3	$V_{UV\ ON}$	V	Outputs in tristate
Supply voltage decreasing	$V_S$	- 0.3	$V_{UV\ OFF}$	V	Outputs in tristate
Output current	$I_{OUT1-2}$	- 0.8	0.8	A	-
Input current (FB, REF)	$I_{IN}$	- 50	500	$\mu$ A	-
Junction temperature	$T_j$	- 40	150	$^{\circ}$ C	-

**Electrical Characteristics**

8 V <  $V_S$  < 18 V;  $I_{OUT1-2} = 0$  A;  $-40$  °C <  $T_j$  < 150 °C  
(unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Current Consumption**

Supply current	$I_S$	–	12	20	mA	–
Supply current	$I_S$	–	20	30	mA	$I_{OUT1} = 0.4$ A $I_{OUT2} = -0.4$ A
Supply current	$I_S$	–	30	50	mA	$I_{OUT1} = 0.8$ A $I_{OUT2} = -0.8$ A

**Over- and Under Voltage Lockout**

UV Switch ON voltage	$V_{UV\ ON}$	–	7.4	8	V	$V_S$ increasing
UV Switch OFF voltage	$V_{UV\ OFF}$	6.3	6.9	–	V	$V_S$ decreasing
UV ON/OFF Hysteresis	$V_{UVHY}$	–	0.5	–	V	$V_{UV\ ON} - V_{UV\ OFF}$
OV Switch OFF voltage	$V_{OV\ OFF}$	–	20.5	23	V	$V_S$ increasing
OV Switch ON voltage	$V_{OV\ ON}$	17.5	20	–	V	$V_S$ decreasing
OV ON/OFF Hysteresis	$V_{OVHY}$	–	0.5	–	V	$V_{OV\ OFF} - V_{OV\ ON}$

**Electrical Characteristics (cont'd)**

$8\text{ V} < V_S < 18\text{ V}$ ;  $I_{\text{OUT}1-2} = 0\text{ A}$ ;  $-40\text{ }^\circ\text{C} < T_j < 150\text{ }^\circ\text{C}$   
(unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Outputs OUT1-2**
**Saturation Voltages**

Source (upper) $I_{\text{OUT}} = -0.2\text{ A}$	$V_{\text{SAT U}}$	–	0.85	1.15	V	$T_j = 25\text{ }^\circ\text{C}$
Source (upper) $I_{\text{OUT}} = -0.4\text{ A}$	$V_{\text{SAT U}}$	–	0.90	1.20	V	$T_j = 25\text{ }^\circ\text{C}$
Sink (upper) $I_{\text{OUT}} = -0.8\text{ A}$	$V_{\text{SAT U}}$	–	1.10	1.50	V	$T_j = 25\text{ }^\circ\text{C}$
Sink (lower) $I_{\text{OUT}} = 0.2\text{ A}$	$V_{\text{SAT L}}$	–	0.15	0.23	V	$T_j = 25\text{ }^\circ\text{C}$
Sink (lower) $I_{\text{OUT}} = 0.4\text{ A}$	$V_{\text{SAT L}}$	–	0.25	0.40	V	$T_j = 25\text{ }^\circ\text{C}$
Sink (lower) $I_{\text{OUT}} = 0.8\text{ A}$	$V_{\text{SAT L}}$	–	0.45	0.75	V	$T_j = 25\text{ }^\circ\text{C}$

Total drop $I_{\text{OUT}} = 0.2\text{ A}$	$V_{\text{SAT}}$	–	1.0	1.4	V	$V_{\text{SAT}} = V_{\text{SAT U}} + V_{\text{SAT L}}$
Total drop $I_{\text{OUT}} = 0.4\text{ A}$	$V_{\text{SAT}}$	–	1.2	1.7	V	$V_{\text{SAT}} = V_{\text{SAT U}} + V_{\text{SAT L}}$
Total drop $I_{\text{OUT}} = 0.8\text{ A}$	$V_{\text{SAT}}$	–	1.6	2.5	V	$V_{\text{SAT}} = V_{\text{SAT U}} + V_{\text{SAT L}}$

**Clamp Diodes**

Forward voltage; upper	$V_{\text{FU}}$	–	1	1.5	V	$I_{\text{F}} = 0.4\text{ A}$
Upper leakage current	$I_{\text{L KU}}$	–	–	5	mA	$I_{\text{F}} = 0.4\text{ A}$
Forward voltage; lower	$V_{\text{FL}}$	–	0.9	1.4	V	$I_{\text{F}} = 0.4\text{ A}$

**Electrical Characteristics (cont'd)**

8 V <  $V_S$  < 18 V;  $I_{OUT1-2} = 0$  A;  $-40$  °C <  $T_j$  < 150 °C  
(unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Input-Interface**
**Input REF**

Quiescent voltage	$V_{REFq}$	–	200	–	mV	$I_{REF} = 0$ $\mu$ A
Input resistance	$R_{REF}$	–	6	–	k $\Omega$	0 V < $V_{REF}$ < 0.5 V

**Input FB**

Quiescent voltage	$V_{FBq}$	–	200	–	mV	$I_{FB} = 0$ $\mu$ A
Input resistance	$R_{FB}$	–	6	–	k $\Omega$	0 V < $V_{FB}$ < 0.5 V

**Input/Output HYST**

Current Amplification $A_{HYST} = I_{HYST} / (I_{REF} - I_{FB})$	$A_{HYST}$	0.8	0.95	1.1	–	$-20$ $\mu$ A < $I_{HYST}$ < $-10$ $\mu$ A; $10$ $\mu$ A < $I_{HYST}$ < $20$ $\mu$ A; $I_{REF} = 250$ $\mu$ A $V_{HYST} = V_S / 2$
Current Offset	$I_{HYSTIO}$	–2	0.35	3	$\mu$ A	$I_{REF} = I_{FB} = 250$ $\mu$ A $V_{HYST} = V_S / 2$
Threshold voltage High	$V_{HYH} / V_S$	–	52	–	%	–
Deadband voltage High	$V_{DBH} / V_S$	–	50.4	–	%	–
Deadband voltage Low	$V_{DBL} / V_S$	–	49.6	–	%	–
Threshold voltage Low	$V_{HYL} / V_S$	–	48	–	%	–
Hysteresis Window	$V_{HYW} / V_S$	3	4	5	%	$(V_{HYH} - V_{HYL}) / V_S$
Deadband Window	$V_{DBW} / V_S$	0.4	0.8	1.2	%	$(V_{DBH} - V_{DBL}) / V_S$

**Electrical Characteristics** (cont'd)

 $8\text{ V} < V_S < 18\text{ V}; I_{\text{OUT}1-2} = 0\text{ A}; -40\text{ }^\circ\text{C} < T_j < 150\text{ }^\circ\text{C}$   
(unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Input RANGE**

Input current	$I_{\text{RANGE}}$	- 1	-	1	$\mu\text{A}$	$0\text{ V} < V_{\text{RANGE}} < V_S$
Switch-OFF voltage High	$V_{\text{OFFH}}$	- 25	0	100	mV	refer to $V_S$
Switch-OFF voltage Low	$V_{\text{OFFL}}$	310	390	490	mV	refer to GND, $V_{\text{RANGE}}$ decreasing
Switch-ON voltage Low	$V_{\text{ONL}}$	400	500	550	mV	refer to GND, $V_{\text{RANGE}}$ increasing
Low-threshold hysteresis	$V_{\text{OFFLHYS}}$	50	110	-	mV	see Figure 6

**Thermal Shutdown**

Thermal shutdown junction temperature	$T_{\text{jSD}}$	150	175	200	$^\circ\text{C}$	-
Thermal switch-on junction temperature	$T_{\text{jSO}}$	120	-	170	$^\circ\text{C}$	-
Temperature hysteresis	$\Delta T$	-	30	-	K	-

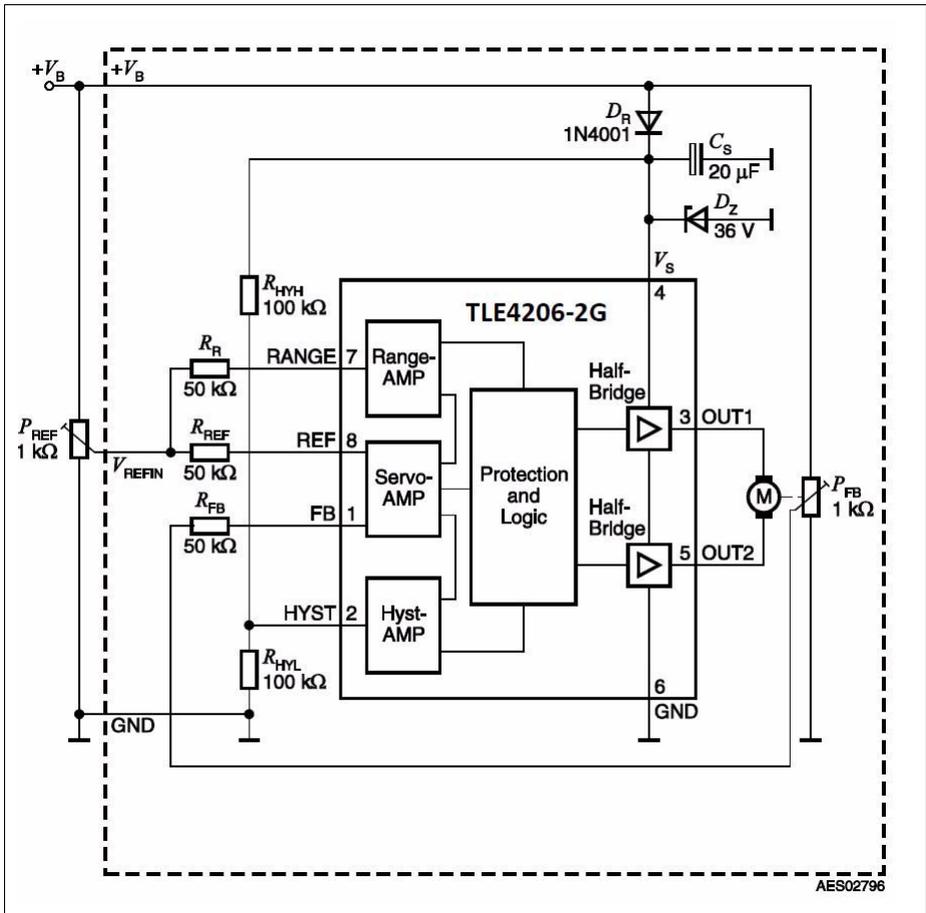
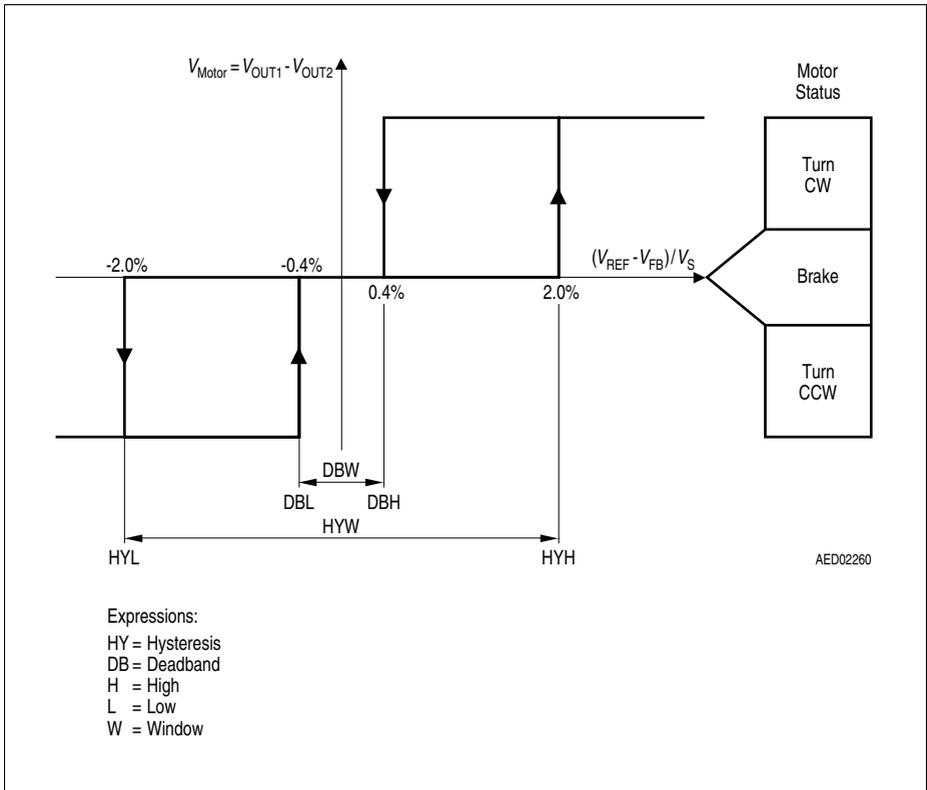


Figure 3 Application Circuit



**Figure 4 Hysteresis, Phaselag and Deadband-Definitions**

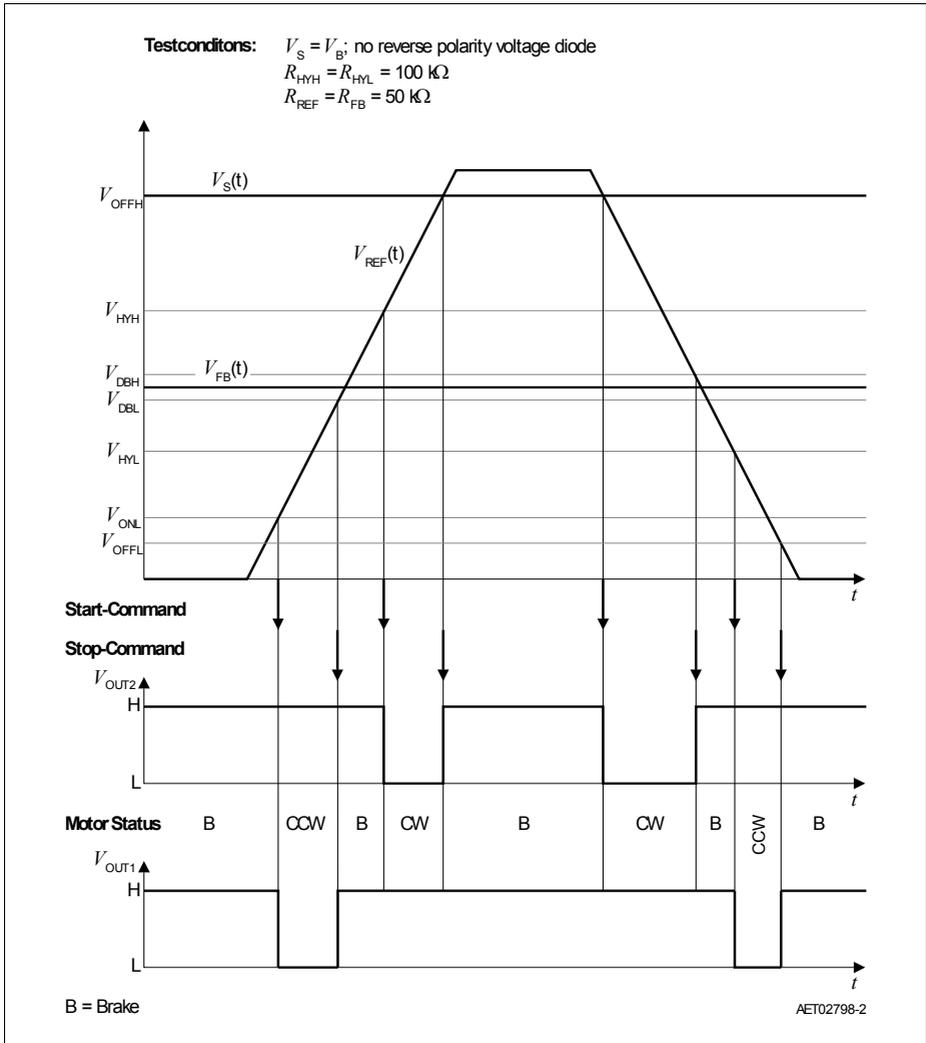
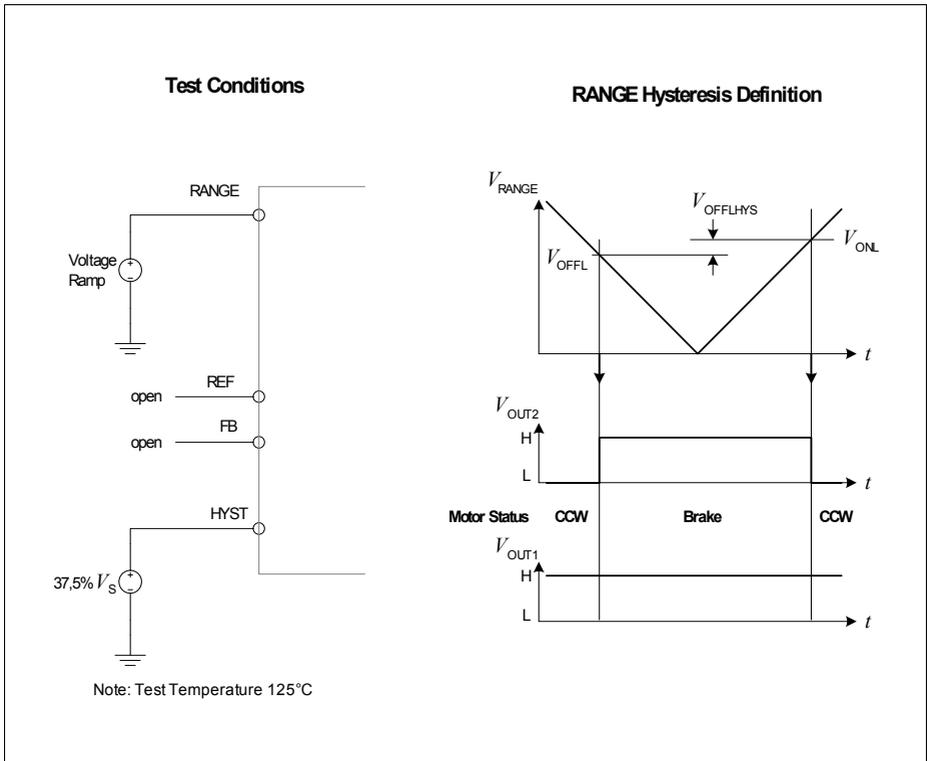


Figure 5 Timing and Phaselag



**Figure 6 RANGE Hysteresis and Test Conditions**



**Revision History**

<b>Version</b>	<b>Date</b>	<b>Changes</b>
Rev. 1.1	2007-08-10	RoHS-compliant version of the TLE 4206-2 <ul style="list-style-type: none"> <li>• All pages: Infineon logo updated</li> <li>• Page 1:               <ul style="list-style-type: none"> <li>“AEC qualified” and “RoHS” logo added, “Green Product (RoHS compliant)” and “AEC qualified” statement added to feature list, package names changed to RoHS compliant versions, package pictures updated, ordering codes removed</li> </ul> </li> <li>• Page 14:               <ul style="list-style-type: none"> <li>Package names changed to RoHS compliant versions, “Green Product” description added</li> </ul> </li> <li>• Revision History added</li> <li>• Legal Disclaimer added</li> </ul>
Rev. 1.2	2008-02-04	<ul style="list-style-type: none"> <li>• Editorial change: deleted "fully" (The term "fully protected" often leads to misunderstandings as it is unclear with respect to which parameters); page 1</li> <li>• Update Package picture; page1</li> <li>• Update Figure 1; page 2</li> </ul>
Rev. 1.3	2017-05-19	<ul style="list-style-type: none"> <li>• Package suffix deleted</li> </ul>

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