

## N-channel 650 V, 0.338 $\Omega$ typ., 10 A MDmesh™ V Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - preliminary data

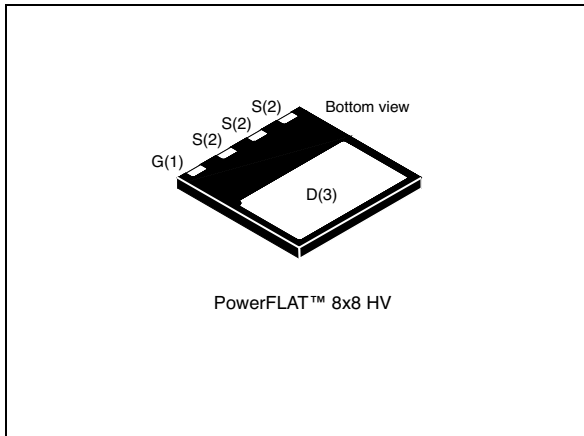
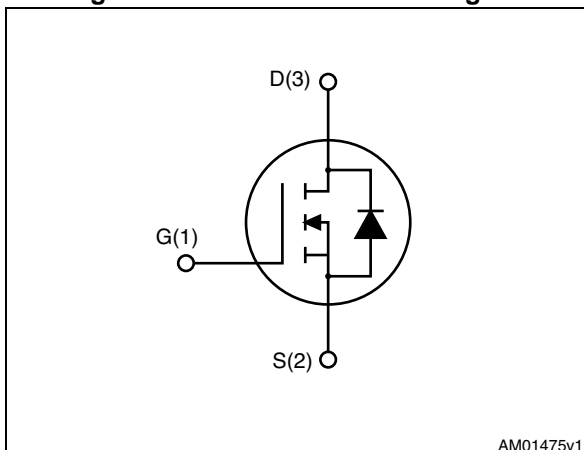


Figure 1. Internal schematic diagram



### Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	$I_D$
STL17N65M5	710 V	0.374 $\Omega$	10 A <sup>(1)</sup>

1. The value is rated according to  $R_{thj-case}$  and limited by package

- Worldwide best  $R_{DS(on)}$  \* area
- Higher  $V_{DSS}$  rating and high dv/dt capability
- Excellent switching performance

### Applications

- Switching applications

### Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL17N65M5	17N65M5	PowerFLAT™ 8x8 HV	Tape and reel

# contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	650	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	10	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	5.8	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	40	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	1.8	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	1.2	A
$P_{TOT}^{(3)}$	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	2.8	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	2.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	160	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to  $R_{thj-case}$ .
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of inch<sup>2</sup>, 2oz Cu.
4.  $I_{SD} \leq 10\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{Peak} < V_{(BR)DSS}$ ,  $V_{DD}=400\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.79	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient max	45	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of inch<sup>2</sup>, 2oz Cu.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	650			V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 650\text{ V}$ , $V_{GS} = 0$ $V_{DS} = 650\text{ V}$ , $V_{GS} = 0$ , $T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{GS} = \pm 25\text{ V}$ , $V_{DS} = 0$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 5.5\text{ A}$		0.338	0.374	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	816	-	pF
$C_{oss}$	Output capacitance		-	23	-	pF
$C_{riss}$	Reverse transfer capacitance		-	2.6	-	pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }520\text{ V}$	-	21	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related		-	70	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}$ , $I_D = 5.5\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15</a> )	-	22	-	nC
$Q_{gs}$	Gate-source charge		-	5.5	-	nC
$Q_{gd}$	Gate-drain charge		-	11	-	nC

- $C_{o(er)}^{(1)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- $C_{o(tr)}^{(2)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400\text{ V}$ , $I_D = 6\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16</a> and <a href="#">19</a> )	-	30	-	ns
$t_{r(v)}$	Voltage rise time		-	8	-	ns
$t_{f(i)}$	Current fall time		-	11	-	ns
$t_{c(off)}$	Crossing time		-	12.5	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		10	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		40	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see <a href="#">Figure 16</a> )	-	247		ns
$Q_{rr}$	Reverse recovery charge		-	2.4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	19.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 16</a> )	-	312		ns
$Q_{rr}$	Reverse recovery charge		-	3		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	19		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

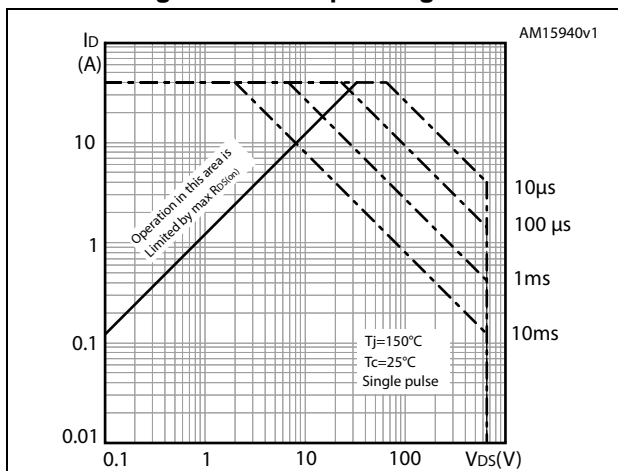


Figure 3. Thermal impedance

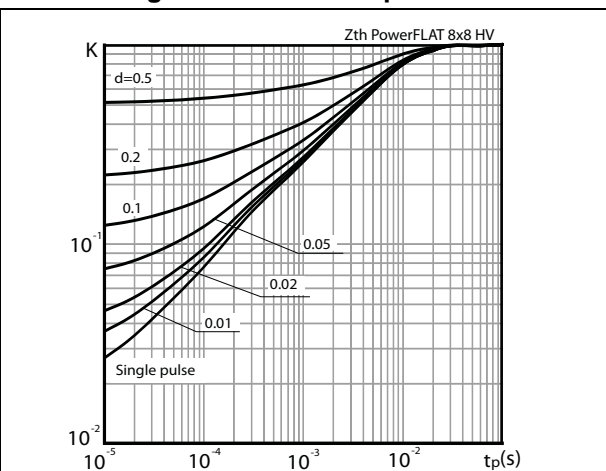


Figure 4. Output characteristics

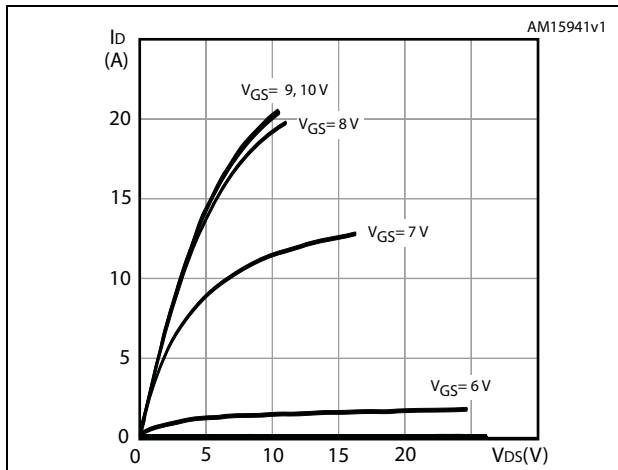


Figure 5. Transfer characteristics

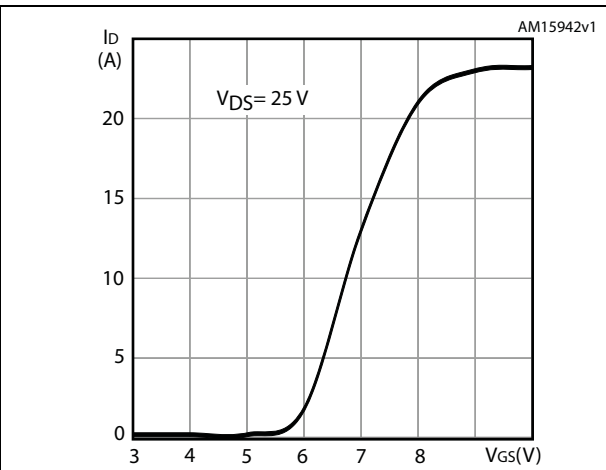


Figure 6. Gate charge vs gate-source voltage

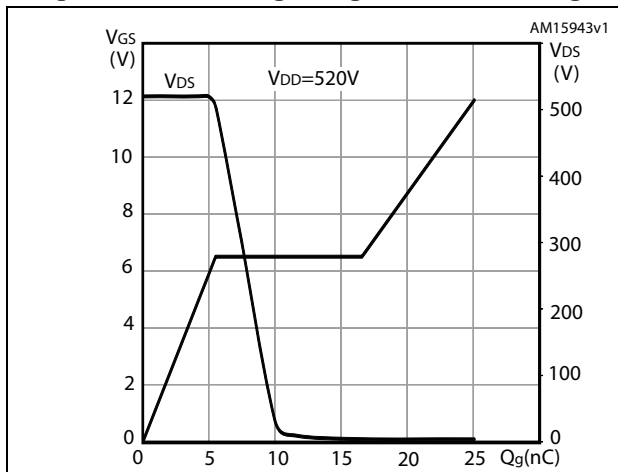


Figure 7. Static drain-source on-resistance

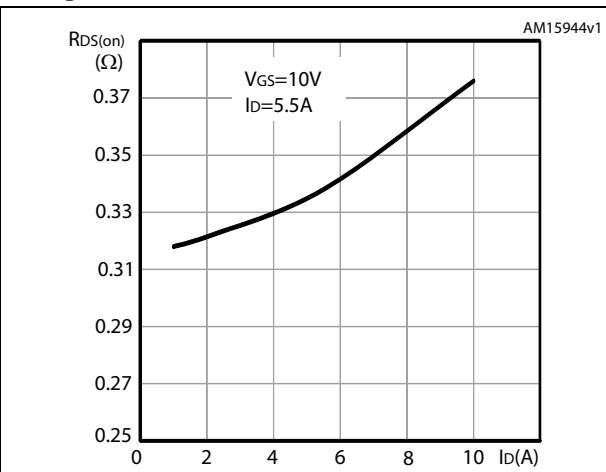


Figure 8. Capacitance variations

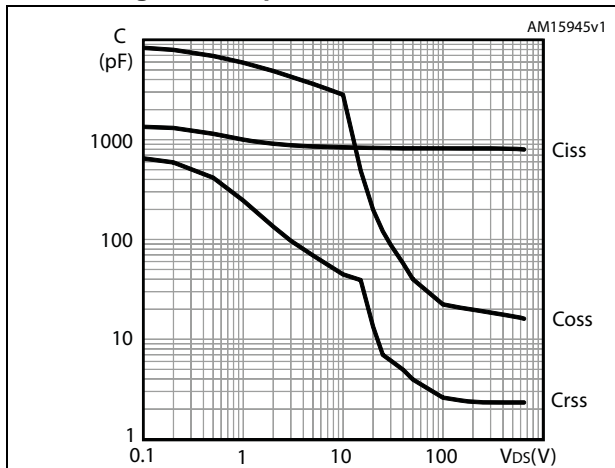


Figure 9. Normalized  $V_{DS}$  vs temperature

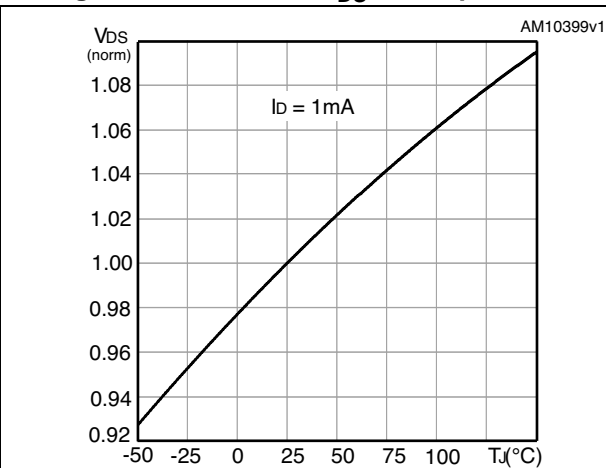


Figure 10. Normalized gate threshold voltage vs temperature

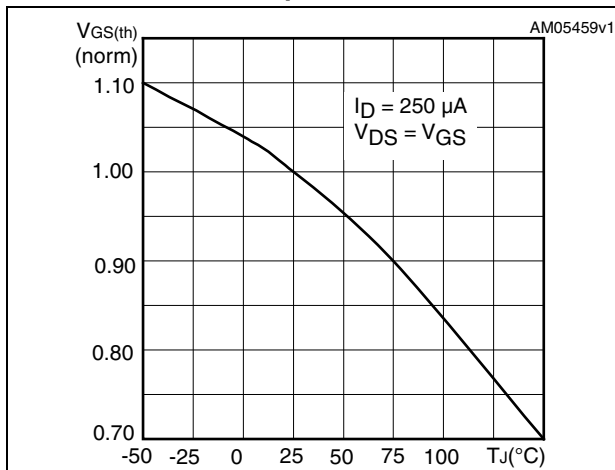


Figure 11. Normalized on-resistance vs temperature

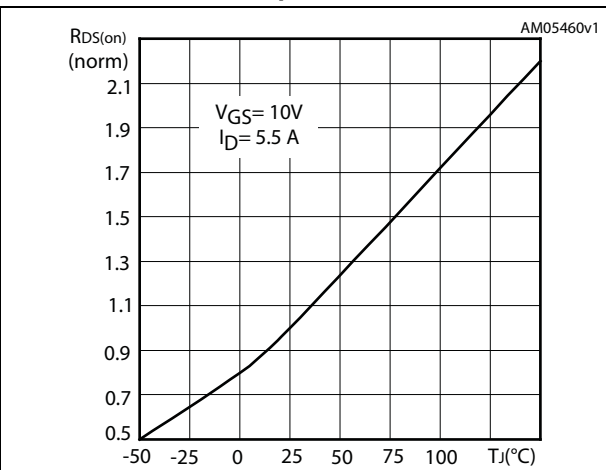


Figure 12. Source-drain diode forward characteristics

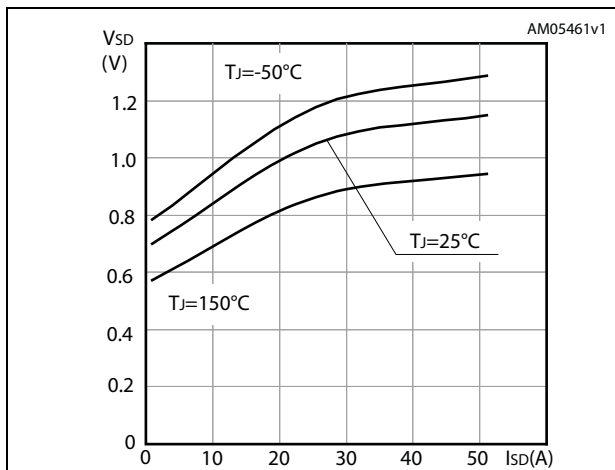
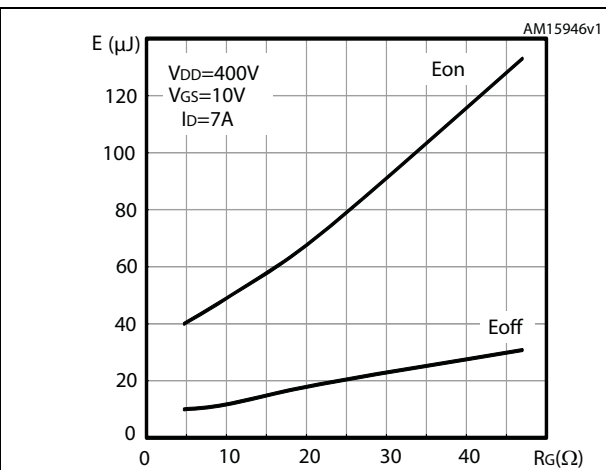


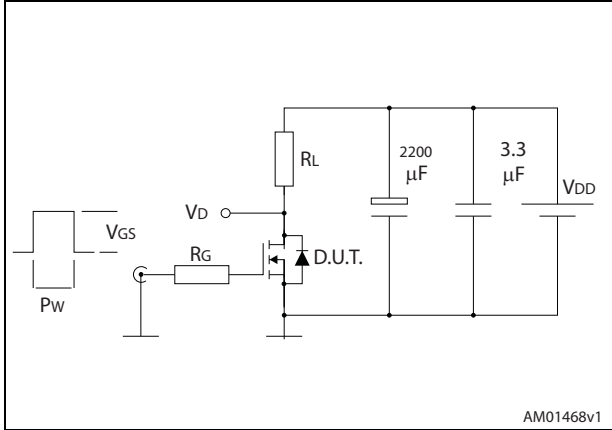
Figure 13. Switching losses vs gate resistance<sup>(1)</sup>



1. Eon including reverse recovery of a SiC diode

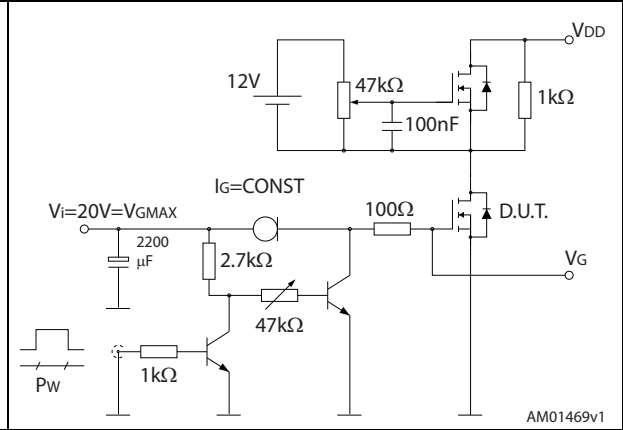
### 3 Test circuits

Figure 14. Switching times test circuit for resistive load



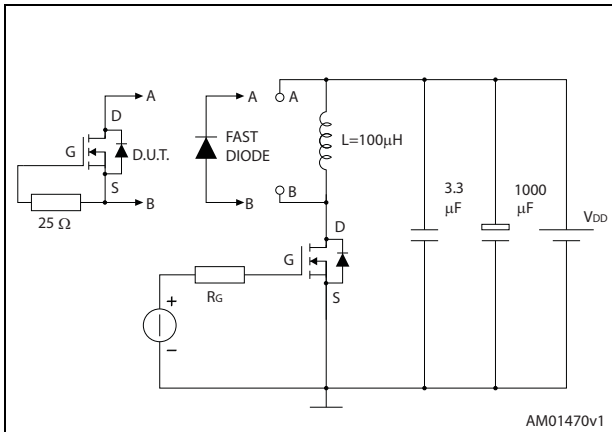
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Figure 15. Gate charge test circuit



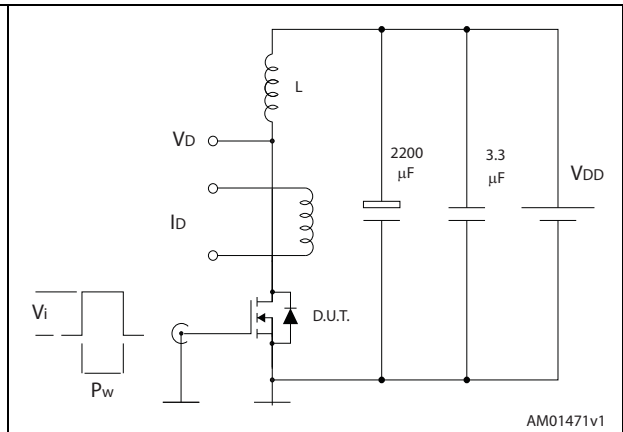
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Figure 16. Test circuit for inductive load switching and diode recovery times



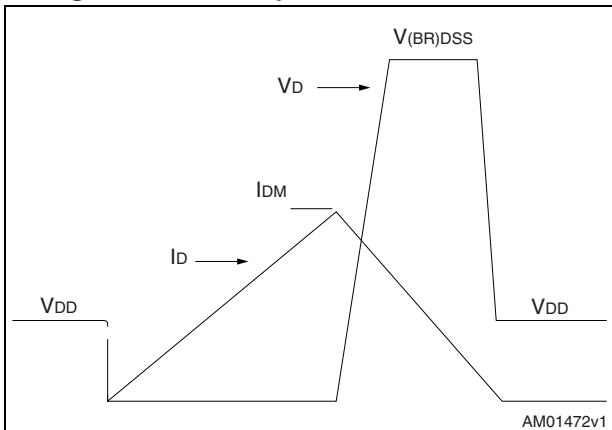
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Figure 17. Unclamped inductive load test circuit



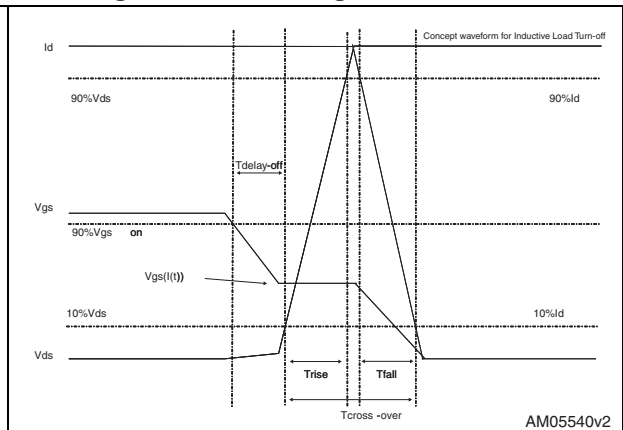
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Figure 18. Unclamped inductive waveform



AM01472v1

Figure 19. Switching time waveform



AM05540v2



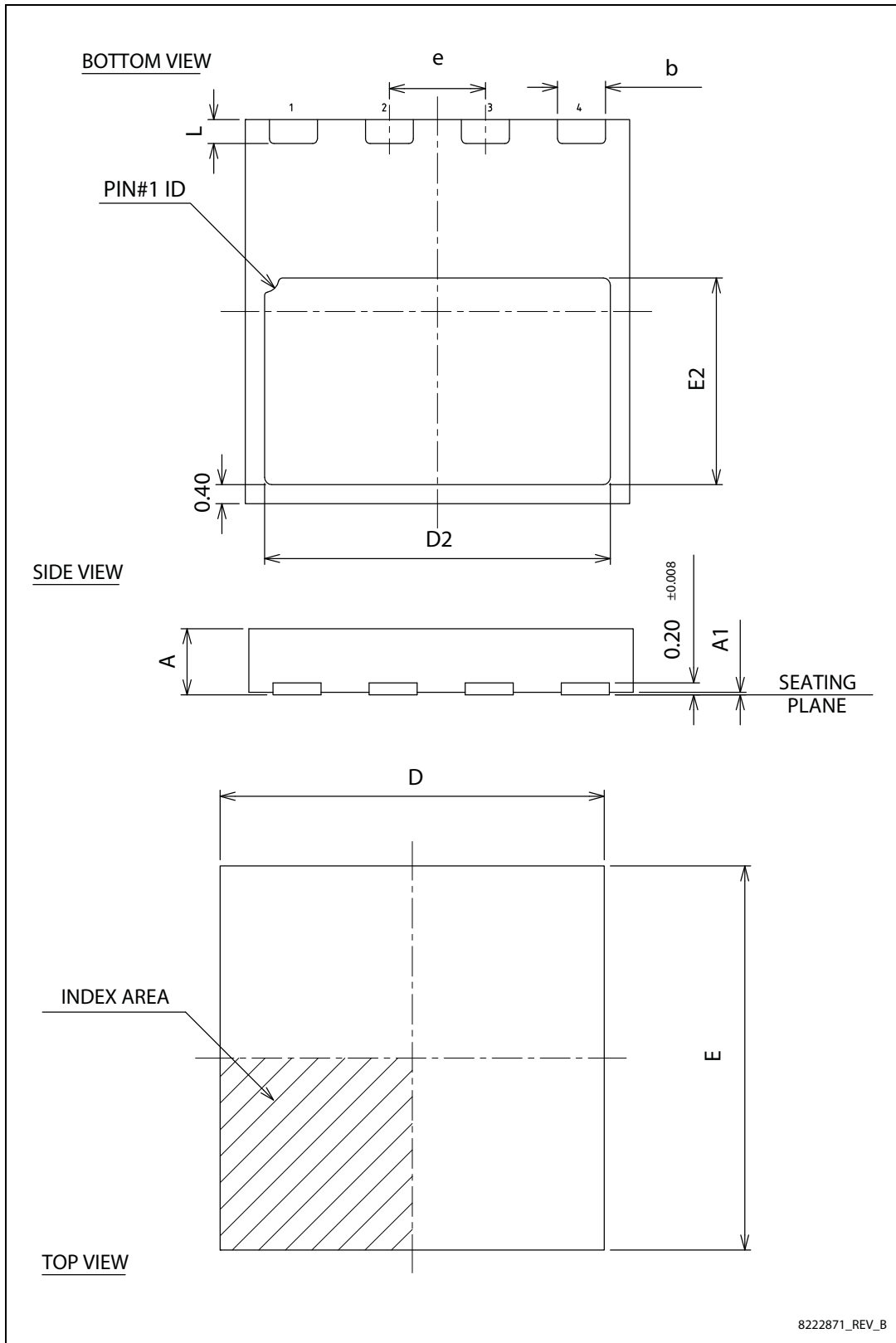
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Table 8. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

Figure 20. PowerFLAT™ 8x8 HV drawing mechanical data



8222871\_REV\_B

Figure 21. PowerFLAT™ 8x8 HV recommended footprint (dimension in millimeters)

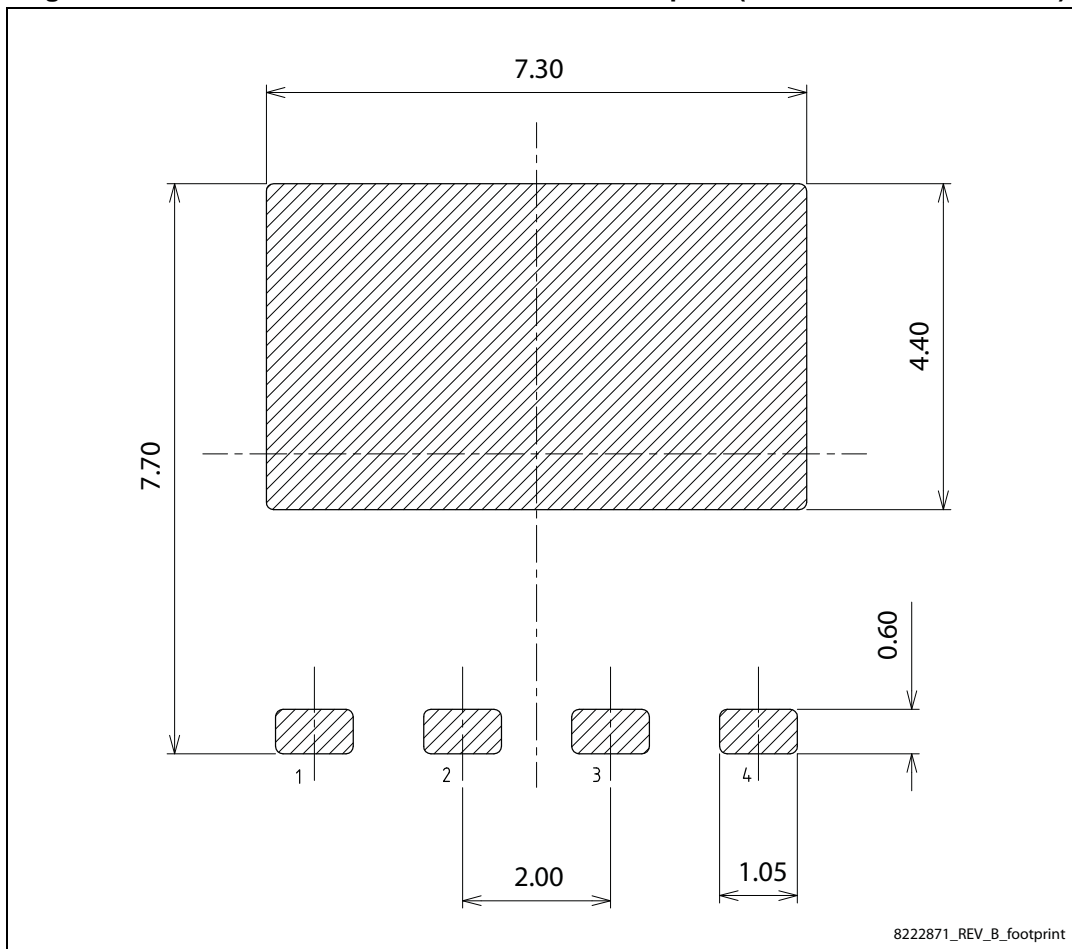
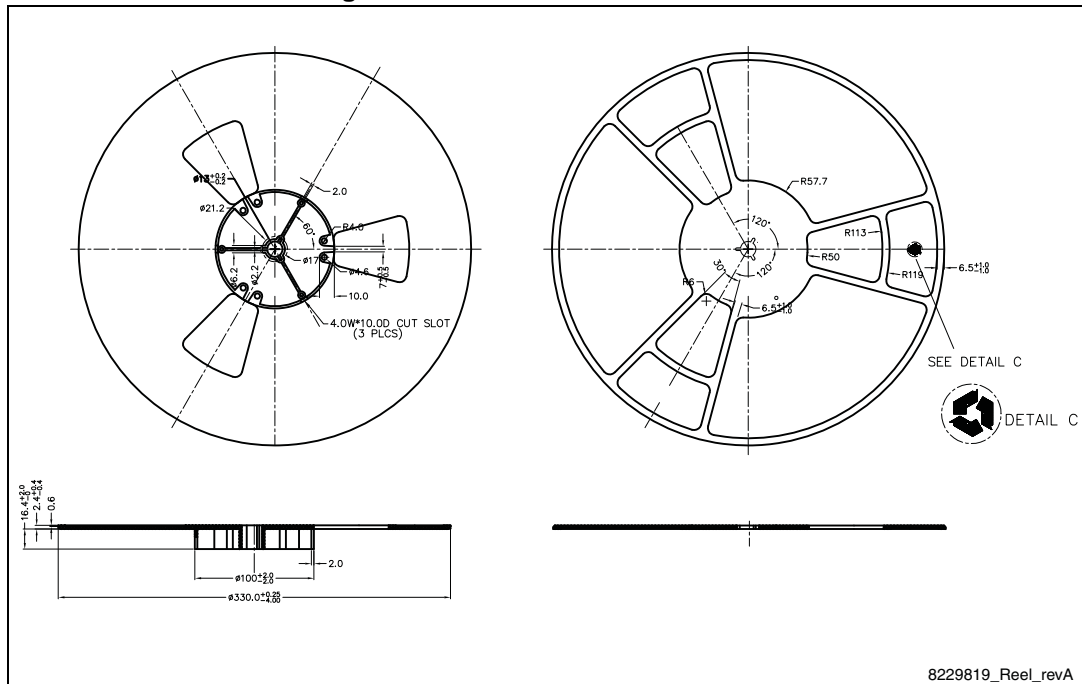




Figure 24. PowerFLAT™ 8x8 HV reel



## 6 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
05-Apr-2012	1	First release.
09-Jul-2013	2	<ul style="list-style-type: none"> <li>– Modified: <a href="#">note 1</a> and <a href="#">Figure 1</a> in first page</li> <li>– Modified: <math>I_D</math> value at <math>T_C=100\text{ °C}</math>, <math>T_{amb}=25\text{ °C}</math>, <math>T_{amb}=100\text{ °C}</math>, <math>P_{TOT}</math> and <math>E_{AS}</math> values in <a href="#">Table 2</a></li> <li>– Modified: <math>R_{thj-case}</math> value in <a href="#">Table 3</a>, the entire typical values in table <a href="#">Table 5</a>, <a href="#">6</a> and <a href="#">7</a></li> <li>– Inserted: <a href="#">Section 2.1: Electrical characteristics (curves)</a></li> <li>– Modified: <a href="#">Figure 15</a>, <a href="#">16</a> and <a href="#">17</a></li> <li>– Minor text changes</li> </ul>
17-Jul-2013	3	<ul style="list-style-type: none"> <li>– Minor text changes</li> <li>– Modified: <a href="#">Table 6</a></li> <li>– Updated: <a href="#">Section 4: Package mechanical data</a></li> </ul>

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