MCP2561/2FD

High-Speed CAN Flexible Data Rate Transceiver

Features:

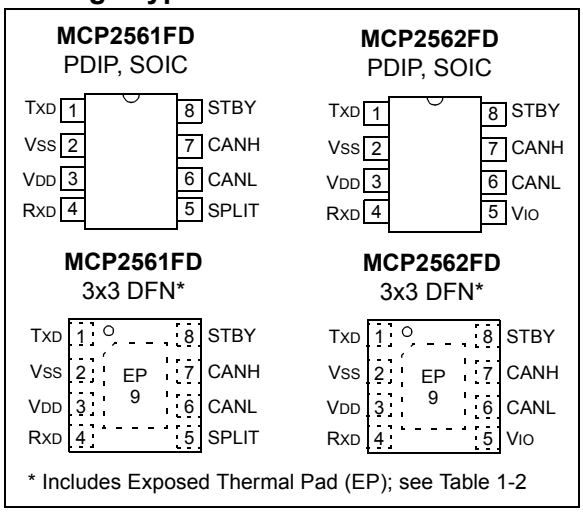
- Optimized for CAN FD (Flexible Data rate) at 2, 5 and 8 Mbps Operation
  - Maximum Propagation Delay: 120 ns
  - Loop Delay Symmetry: -10%/+10% (2 Mbps)
- Implements ISO-11898-2 and ISO-11898-5 Standard Physical Layer Requirements
- Very Low Standby Current (5 µA, typical)
- V_{IO} Supply Pin to Interface Directly to CAN Controllers and Microcontrollers with 1.8V to 5.5V I/O
- SPLIT Output Pin to Stabilize Common Mode in Biased Split Termination Schemes
- CAN Bus Pins are Disconnected when Device is Unpowered
  - An Unpowered Node or Brown-Out Event will Not Load the CAN Bus
- Detection of Ground Fault:
  - Permanent Dominant Detection on T_{XD}
  - Permanent Dominant Detection on Bus
- Power-on Reset and Voltage Brown-Out Protection on V_{DD} Pin
- Protection Against Damage Due to Short-Circuit Conditions (Positive or Negative Battery Voltage)
- Protection Against High-Voltage Transients in Automotive Environments
- Automatic Thermal Shutdown Protection
- Suitable for 12V and 24V Systems
- Meets or exceeds stringent automotive design requirements including “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications”, Version 1.3, May 2012
  - Radiated emissions @ 2 Mbps with Common Mode Choke (CMC)
  - DPI @ 2 Mbps with CMC
- High ESD Protection on CANH and CANL, meeting IEC61000-4-2 up to ±14 kV
- Available in PDIP-8L, SOIC-8L and 3x3 DFN-8L
- Temperature ranges:
  - Extended (E): -40°C to +125°C
  - High (H): -40°C to +150°C

Description:

The MCP2561/2FD is a second generation high-speed CAN transceiver from Microchip Technology Inc. It offers the same features as the MCP2561/2. Additionally, it guarantees Loop Delay Symmetry in order to support the higher data rates required for CAN FD. The maximum propagation delay was improved to support longer bus length.

The device meets the automotive requirements for CAN FD bit rates exceeding 2 Mbps, low quiescent current, electromagnetic compatibility (EMC) and electrostatic discharge (ESD).

Package Types



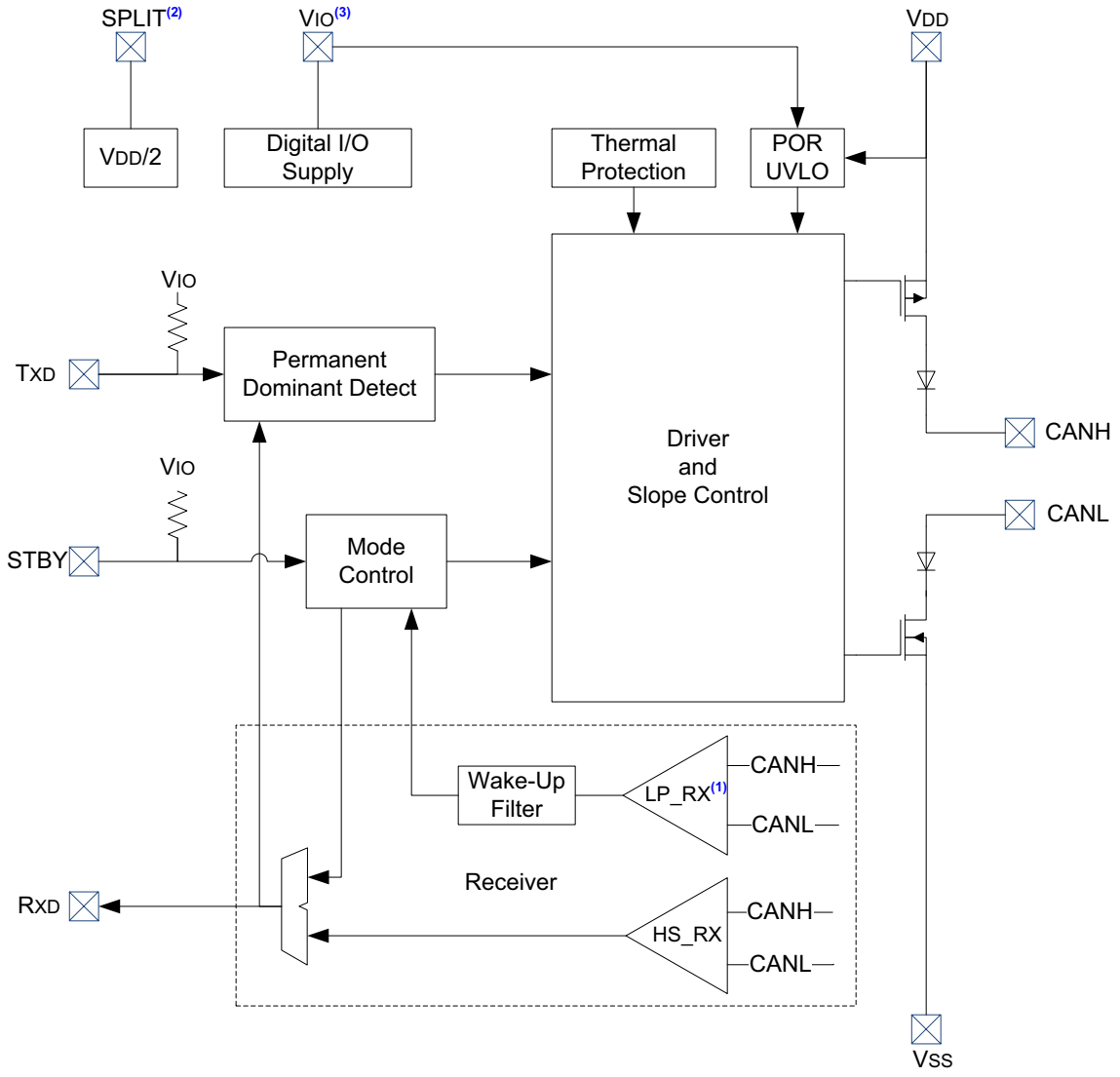
* Includes Exposed Thermal Pad (EP); see Table 1-2

MCP2561/2FD Family Members

Device	Feature	Description
MCP2561FD	SPLIT pin	Common mode stabilization
MCP2562FD	V_{IO} pin	Internal level shifter on digital I/O pins

Note: For ordering information, see the **“Product Identification System”** section on page 29.

Block Diagram



Note 1: There is only one receiver implemented. The receiver can operate in Low-Power or High-Speed mode.

2: Only MCP2561FD has the SPLIT pin.

3: Only MCP2562FD has the VIO pin. In MCP2561FD, the supply for the digital I/O is internally connected to VDD.

1.0 DEVICE OVERVIEW

The MCP2561/2FD is a high-speed CAN device, fault-tolerant device that serves as the interface between a CAN protocol controller and the physical bus. The MCP2561/2FD device provides differential transmit and receive capability for the CAN protocol controller, and is fully compatible with the ISO-11898-2 and ISO-11898-5 standards.

The Loop Delay Symmetry is guaranteed to support data rates that are up to 5 Mbps for CAN FD (Flexible Data rate). The maximum propagation delay was improved to support longer bus length.

Typically, each node in a CAN system must have a device to convert the digital signals generated by a CAN controller to signals suitable for transmission over the bus cabling (differential output). It also provides a buffer between the CAN controller and the high-voltage spikes that can be generated on the CAN bus by outside sources.

1.1 Mode Control Block

The MCP2561/2FD supports two modes of operation:

- Normal Mode
- Standby Mode

These modes are summarized in Table 1-1.

1.1.1 NORMAL MODE

Normal mode is selected by applying low-level voltage to the STBY pin. The driver block is operational and can drive the bus pins. The slopes of the output signals on CANH and CANL are optimized to produce minimal electromagnetic emissions (EME).

The high speed differential receiver is active.

1.1.2 STANDBY MODE

The device may be placed in Standby mode by applying high-level voltage to the STBY pin. In Standby mode, the transmitter and the high-speed part of the receiver are switched off to minimize power consumption. The low-power receiver and the wake-up filter blocks are enabled to monitor the bus for activity. The receive pin (R_{XD}) will show a delayed representation of the CAN bus, due to the wake-up filter.

The CAN controller gets interrupted by a negative edge on the R_{XD} pin (Dominant state on the CAN bus). The CAN controller must put the MCP2561/2FD back into Normal mode, using the STBY pin, in order to enable high speed data communication.

The CAN bus wake-up function requires both supply voltages, V_{DD} and V_{IO}, to be in valid range.

TABLE 1-1: MODES OF OPERATION

Mode	STBY Pin	R_{XD} Pin	
		LOW	HIGH
Normal	LOW	Bus is Dominant	Bus is Recessive
Standby	HIGH	Wake-up request is detected	No wake-up request detected

1.2 Transmitter Function

The CAN bus has two states:

- Dominant State
- Recessive State

A Dominant state occurs when the differential voltage between CANH and CANL is greater than $V_{DIFF(D)(I)}$. A Recessive state occurs when the differential voltage is less than $V_{DIFF(R)(I)}$. The Dominant and Recessive states correspond to the Low and High state of the T_{XD} input pin, respectively. However, a Dominant state initiated by another CAN node will override a Recessive state on the CAN bus.

1.3 Receiver Function

In Normal mode, the R_{XD} output pin reflects the differential bus voltage between CANH and CANL. The Low and High states of the R_{XD} output pin correspond to the Dominant and Recessive states of the CAN bus, respectively.

1.4 Internal Protection

CANH and CANL are protected against battery short-circuits and electrical transients that can occur on the CAN bus. This feature prevents destruction of the transmitter output stage during such a fault condition.

The device is further protected from excessive current loading by thermal shutdown circuitry that disables the output drivers when the junction temperature exceeds a nominal limit of +175°C. All other parts of the chip remain operational, and the chip temperature is lowered due to the decreased power dissipation in the transmitter outputs. This protection is essential to protect against bus line short-circuit-induced damage.

1.5 Permanent Dominant Detection

The MCP2561/2FD device prevents two conditions:

- Permanent Dominant condition on TXD
- Permanent Dominant condition on the bus

In Normal mode, if the MCP2561/2FD detects an extended Low state on the TXD input, it will disable the CANH and CANL output drivers in order to prevent the corruption of data on the CAN bus. The drivers will remain disabled until TXD goes High.

In Standby mode, if the MCP2561/2FD detects an extended Dominant condition on the bus, it will set the RXD pin to Recessive state. This allows the attached controller to go to Low-Power mode until the Dominant issue is corrected. RXD is latched High until a Recessive state is detected on the bus, and the wake-up function is enabled again.

Both conditions have a time-out of 1.25 ms (typical). This implies a maximum bit time of 69.44 µs (14.4 kHz), allowing up to 18 consecutive dominant bits on the bus.

1.6 Power-On Reset (POR) and Undervoltage Detection

The MCP2561/2FD has undervoltage detection on both supply pins: VDD and VIO. Typical undervoltage thresholds are 1.2V for VIO and 4V for VDD.

When the device is powered on, CANH and CANL remain in a high-impedance state until both VDD and VIO exceed their undervoltage levels. Once powered on, CANH and CANL will enter a high-impedance state if the voltage level at VDD drops below the undervoltage level, providing voltage brown-out protection during normal operation.

In Normal mode, the receiver output is forced to Recessive state during an undervoltage condition on VDD. In Standby mode, the low-power receiver is only enabled when both VDD and VIO supply voltages rise above their respective undervoltage thresholds. Once these threshold voltages are reached, the low-power receiver is no longer controlled by the POR comparator and remains operational down to about 2.5V on the VDD supply (MCP2561/2FD). The MCP2562FD transfers data to the RXD pin down to 1.8V on the VIO supply.

1.7 Pin Descriptions

Table 1-2 describes the pinout.

TABLE 1-2: MCP2561/2FD PIN DESCRIPTIONS

MCP2561FD 3x3 DFN	**MCP2561FD** PDIP, SOIC	**MCP2562FD** 3x3 DFN	**MCP2562FD** PDIP, SOIC	**Symbol**	**Pin Function**
1	1	1	1	TXD	Transmit Data Input
2	2	2	2	VSS	Ground
3	3	3	3	VDD	Supply Voltage
4	4	4	4	RXD	Receive Data Output
5	5	—	—	SPLIT	Common Mode Stabilization - **MCP2561FD** only
—	—	5	5	VIO	Digital I/O Supply Pin - **MCP2562FD** only
6	6	6	6	CANL	CAN Low-Level Voltage I/O
7	7	7	7	CANH	CAN High-Level Voltage I/O
8	8	8	8	STBY	Standby Mode Input
9	—	9	—	EP	Exposed Thermal Pad

1.7.1 TRANSMITTER DATA INPUT PIN (T_{XD})

The CAN transceiver drives the differential output pins CANH and CANL according to T_{XD}. It is usually connected to the transmitter data output of the CAN controller device. When T_{XD} is Low, CANH and CANL are in the Dominant state. When T_{XD} is High, CANH and CANL are in the Recessive state, provided that another CAN node is not driving the CAN bus with a Dominant state. T_{XD} is connected to an internal pull-up resistor (nominal 33 kΩ) to V_{DD} or V_{IO}, in the MCP2561FD or MCP2562FD, respectively.

1.7.2 GROUND SUPPLY PIN (V_{SS})

Ground supply pin.

1.7.3 SUPPLY VOLTAGE PIN (V_{DD})

Positive supply voltage pin. Supplies transmitter and receiver, including the wake-up receiver.

1.7.4 RECEIVER DATA OUTPUT PIN (R_{XD})

R_{XD} is a CMOS-compatible output that drives High or Low depending on the differential signals on the CANH and CANL pins, and is usually connected to the receiver data input of the CAN controller device. R_{XD} is High when the CAN bus is Recessive, and Low in the Dominant state. R_{XD} is supplied by V_{DD} or V_{IO}, in the MCP2561FD or MCP2562FD, respectively.

1.7.5 SPLIT PIN (MCP2561FD ONLY)

Reference Voltage Output (defined as $V_{DD}/2$). The pin is only active in Normal mode. In Standby mode, or when V_{DD} is off, SPLIT floats.

1.7.6 V_{IO} PIN (MCP2562FD ONLY)

Supply for digital I/O pins. In the MCP2561FD, the supply for the digital I/O (T_{XD}, R_{XD} and STBY) is internally connected to V_{DD}.

1.7.7 CAN LOW PIN (CANL)

The CANL output drives the Low side of the CAN differential bus. This pin is also tied internally to the receive input comparator. CANL disconnects from the bus when MCP2561/2FD is not powered.

1.7.8 CAN HIGH PIN (CANH)

The CANH output drives the high-side of the CAN differential bus. This pin is also tied internally to the receive input comparator. CANH disconnects from the bus when MCP2561/2FD is not powered.

1.7.9 STANDBY MODE INPUT PIN (STBY)

This pin selects between Normal or Standby mode. In Standby mode, the transmitter, high speed receiver and SPLIT are turned off, only the low power receiver and wake-up filter are active. STBY is connected to an internal MOS pull-up resistor to V_{DD} or V_{IO}, in the MCP2561FD or MCP2562FD, respectively. The value of the MOS pull-up resistor depends on the supply voltage. Typical values are 660 kΩ for 5V, 1.1 MΩ for 3.3V and 4.4 MΩ for 1.8V

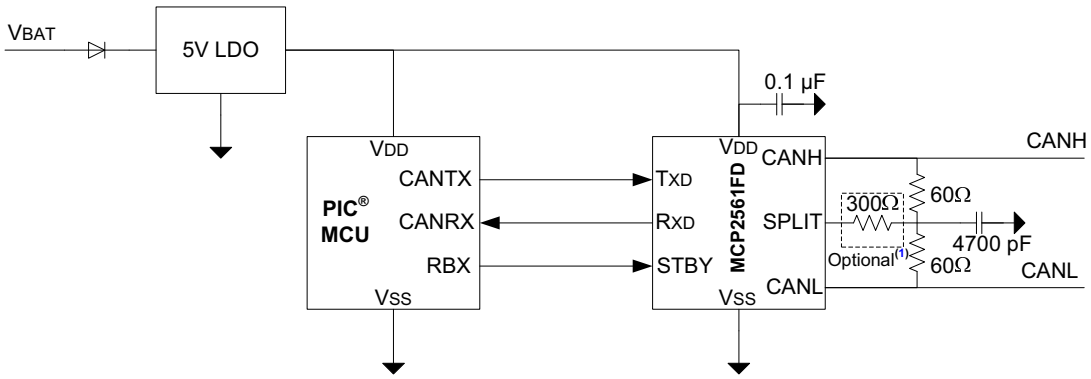
1.7.10 EXPOSED THERMAL PAD (EP)

It is recommended that this pad is connected to V_{SS} for the enhancement of electromagnetic immunity and thermal resistance.

1.8 Typical Applications

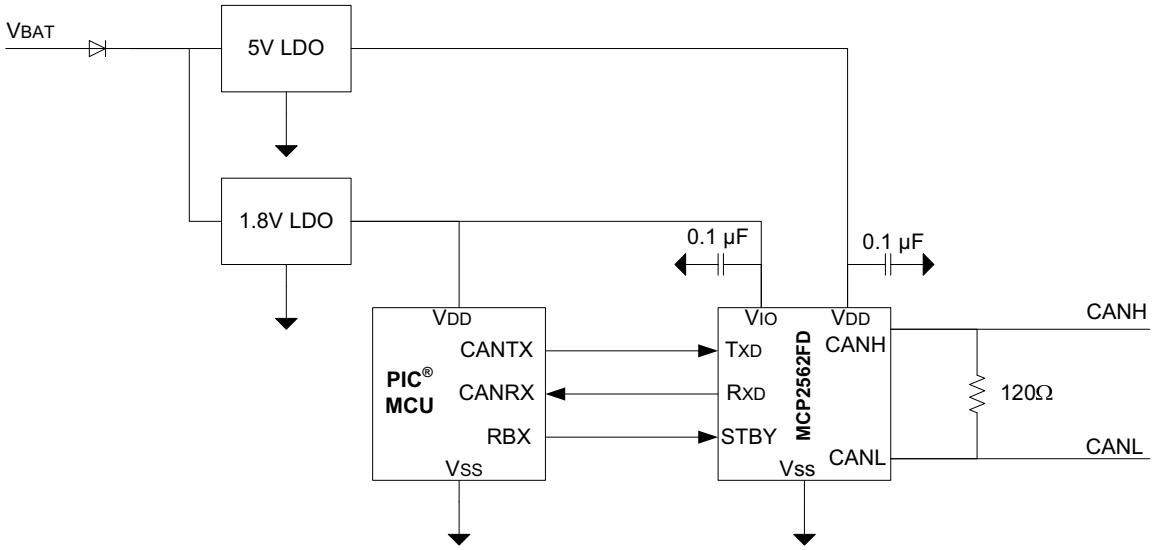
In order to meet the EMC/EMI requirements, a Common Mode Choke (CMC) might be required for data rates greater than 1 Mbps.

FIGURE 1-1: MCP2561FD WITH SPLIT PIN



Note 1: Optional resistor to allow communication during bus failure (CANL shorted to ground).

FIGURE 1-2: MCP2562FD WITH VIO PIN



2.0 ELECTRICAL CHARACTERISTICS

2.1 Terms and Definitions

A number of terms are defined in ISO-11898 that are used to describe the electrical characteristics of a CAN transceiver device. These terms and definitions are summarized in this section.

2.1.1 BUS VOLTAGE

V_{CANL} and V_{CANH} denote the voltages of the bus line wires CANL and CANH relative to ground of each individual CAN node.

2.1.2 COMMON MODE BUS VOLTAGE RANGE

Boundary voltage levels of V_{CANL} and V_{CANH} with respect to ground, for which proper operation will occur, if up to the maximum number of CAN nodes are connected to the bus.

2.1.3 DIFFERENTIAL INTERNAL CAPACITANCE, C_{DIFF} (OF A CAN NODE)

Capacitance seen between CANL and CANH during the Recessive state, when the CAN node is disconnected from the bus (see Figure 2-1).

2.1.4 DIFFERENTIAL INTERNAL RESISTANCE, R_{DIFF} (OF A CAN NODE)

Resistance seen between CANL and CANH during the Recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

2.1.5 DIFFERENTIAL VOLTAGE, V_{DIFF} (OF CAN BUS)

Differential voltage of the two-wire CAN bus, value $V_{DIFF} = V_{CANH} – V_{CANL}$.

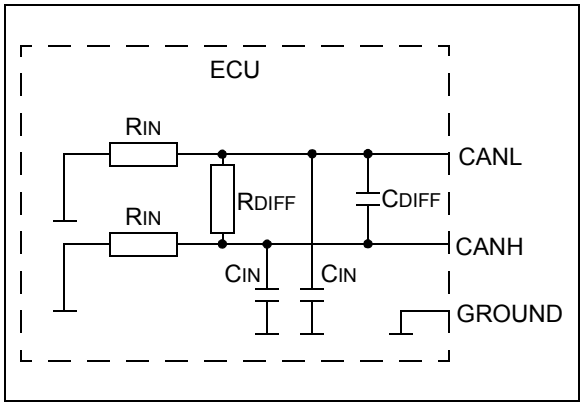
2.1.6 INTERNAL CAPACITANCE, C_{IN} (OF A CAN NODE)

Capacitance seen between CANL (or CANH) and ground during the Recessive state, when the CAN node is disconnected from the bus (see Figure 2-1).

2.1.7 INTERNAL RESISTANCE, R_{IN} (OF A CAN NODE)

Resistance seen between CANL (or CANH) and ground during the Recessive state, when the CAN node is disconnected from the bus (see Figure 2-1).

FIGURE 2-1: PHYSICAL LAYER DEFINITIONS



2.2 Absolute Maximum Ratings†

V_{DD} 7.0V

V_{IO} 7.0V

DC Voltage at T_{XD}, R_{XD}, STBY and V_{SS} ..... -0.3V to V_{IO} + 0.3V

DC Voltage at CANH, CANL and SPLIT ..... -58V to +58V

Transient Voltage on CANH, CANL (ISO-7637) (See Figure 2-5) ..... -150V to +100V

Storage temperature ..... -55°C to +150°C

Operating ambient temperature ..... -40°C to +150°C

Virtual Junction Temperature, T_{VJ} (IEC60747-1) ..... -40°C to +190°C

Soldering temperature of leads (10 seconds) ..... +300°C

ESD protection on CANH and CANL pins for **MCP2561FD** (IEC 61000-4-2) ..... ±14 kV

ESD protection on CANH and CANL pins for **MCP2562FD** (IEC 61000-4-2) ..... ±8 kV

ESD protection on CANH and CANL pins (IEC 801; Human Body Model) ..... ±8 kV

ESD protection on all other pins (IEC 801; Human Body Model) ..... ±4 kV

ESD protection on all pins (IEC 801; Machine Model) ..... ±300V

ESD protection on all pins (IEC 801; Charge Device Model) ..... ±750V

† NOTICE: Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2.3 DC Characteristics

Electrical Characteristics: Extended (E): T_{AMB} = -40°C to +125°C and High (H): T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.8V to 5.5V (Note 2), R_L = 60Ω, C_L = 100 pF; unless otherwise specified.

Characteristic	Sym	Min	Typ	Max	Units	Conditions
SUPPLY						
V_{DD} Pin						
Voltage Range	V_{DD}	4.5	—	5.5		
Supply Current	I_{DD}	—	5	10	mA	Recessive; V_{TXD} = V_{DD}
		—	45	70		Dominant; V_{TXD} = 0V
Standby Current	I_{DDS}	—	5	15	µA	**MCP2561FD**
		—	5	15		**MCP2562FD**; Includes I_{IO}
High Level of the POR Comparator	V_{PORH}	3.8	—	4.3	V	
Low Level of the POR Comparator	V_{PORL}	3.4	—	4.0	V	
Hysteresis of POR Comparator	V_{PORD}	0.3	—	0.8	V	
V_{IO} Pin						
Digital Supply Voltage Range	V_{IO}	1.8	—	5.5	V	
Supply Current on V_{IO}	I_{IO}	—	4	30	µA	Recessive; V_{TXD} = V_{IO}
		—	85	500		Dominant; V_{TXD} = 0V
Standby Current	I_{DDS}	—	0.3	1	µA	(Note 1)
Undervoltage detection on V_{IO}	$V_{UVD(IO)}$	—	1.2	—	V	(Note 1)
BUS LINE (CANH; CANL) TRANSMITTER						
CANH; CANL: Recessive Bus Output Voltage	$V_{O(R)}$	2.0	0.5V_{DD}	3.0	V	V_{TXD} = V_{DD}; No load
CANH; CANL: Bus Output Voltage in Standby	$V_{O(S)}$	-0.1	0.0	+0.1	V	STBY = V_{TXD} = V_{DD}; No load
Recessive Output Current	$I_{O(R)}$	-5	—	+5	mA	-24V < V_{CAN} < +24V
CANH: Dominant Output Voltage	$V_{O(D)}$	2.75	3.50	4.50	V	T_{XD} = 0; R_L = 50 to 65Ω
CANL: Dominant Output Voltage		0.50	1.50	2.25		R_L = 50 to 65Ω
Symmetry of Dominant Output Voltage (V_{DD} – V_{CANH} – V_{CANL})	$V_{O(D)(M)}$	-400	0	+400	mV	V_{TXD} = V_{SS} (Note 1)
Dominant: Differential Output Voltage	$V_{O(DIFF)}$	1.5	2.0	3.0	V	V_{TXD} = V_{SS}; R_L = 50 to 65Ω Figure 2-2, Figure 2-4
Recessive: Differential Output Voltage		-120	0	12	mV	V_{TXD} = V_{DD} Figure 2-2, Figure 2-4
		-500	0	50	mV	V_{TXD} = V_{DD}, no load. Figure 2-2, Figure 2-4

Note 1: Characterized; not 100% tested.

2: Only MCP2562FD has V_{IO} pin. For the MCP2561FD, V_{IO} is internally connected to V_{DD}.

3: -12V to 12V is ensured by characterization, tested from -2V to 7V.

2.3 DC Characteristics (Continued)

Electrical Characteristics: Extended (E): T_{AMB} = -40°C to +125°C and High (H): T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.8V to 5.5V (Note 2), R_L = 60Ω, C_L = 100 pF; unless otherwise specified.

Characteristic	Sym	Min	Typ	Max	Units	Conditions
CANH: Short Circuit Output Current	$I_{O(SC)}$	-120	85	—	mA	V_{TXD} = V_{SS}; V_{CANH} = 0V; CANL: floating
		-100	—	—	mA	same as above, but V_{DD}=5V, T_{AMB} = 25°C (Note 1)
CANL: Short Circuit Output Current		—	75	+120	mA	V_{TXD} = V_{SS}; V_{CANL} = 18V; CANH: floating
		—	—	+100	mA	same as above, but V_{DD}=5V, T_{AMB} = 25°C (Note 1)
BUS LINE (CANH; CANL) RECEIVER						
Recessive Differential Input Voltage	$V_{DIFF(R)(I)}$	-1.0	—	+0.5	V	Normal Mode; -12V < V(CANH, CANL) < +12V; See Figure 2-6 (Note 3)
		-1.0	—	+0.4		Standby Mode; -12V < V(CANH, CANL) < +12V; See Figure 2-6 (Note 3)
Dominant Differential Input Voltage	$V_{DIFF(D)(I)}$	0.9	—	V_{DD}	V	Normal Mode; -12V < V(CANH, CANL) < +12V; See Figure 2-6 (Note 3)
		1.0	—	V_{DD}		Standby Mode; -12V < V(CANH, CANL) < +12V; See Figure 2-6 (Note 3)
Differential Receiver Threshold	$V_{TH(DIFF)}$	0.5	0.7	0.9	V	Normal Mode; -12V < V(CANH, CANL) < +12V; See Figure 2-6 (Note 3)
		0.4	—	1.15		Standby Mode; -12V < V(CANH, CANL) < +12V; See Figure 2-6 (Note 3)
Differential Input Hysteresis	$V_{HYS(DIFF)}$	50	—	200	mV	Normal mode, see Figure 2-6, (Note 1)
Common Mode Input Resistance	R_{IN}	10	—	30	kΩ	(Note 1)
Common Mode Resistance Matching	$R_{IN(M)}$	-1	0	+1	%	V_{CANH} = V_{CANL}, (Note 1)
Differential Input Resistance	$R_{IN(DIFF)}$	10	—	100	kΩ	(Note 1)
Common Mode Input Capacitance	$C_{IN(CM)}$	—	—	20	pF	V_{TXD} = V_{DD}; (Note 1)
Differential Input Capacitance	$C_{IN(DIFF)}$	—	—	10		V_{TXD} = V_{DD}; (Note 1)
CANH, CANL: Input Leakage	I_{LI}	-5	—	+5	µA	V_{DD} = V_{TXD} = V_{STBY} = 0V. For **MCP2562FD**, V_{IO} = 0V. V_{CANH} = V_{CANL} = 5 V.

Note 1: Characterized; not 100% tested.

2: Only MCP2562FD has V_{IO} pin. For the MCP2561FD, V_{IO} is internally connected to V_{DD}.

3: -12V to 12V is ensured by characterization, tested from -2V to 7V.

2.3 DC Characteristics (Continued)

Electrical Characteristics: Extended (E): T_{AMB} = -40°C to +125°C and High (H): T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.8V to 5.5V (Note 2), R_L = 60Ω, C_L = 100 pF; unless otherwise specified.

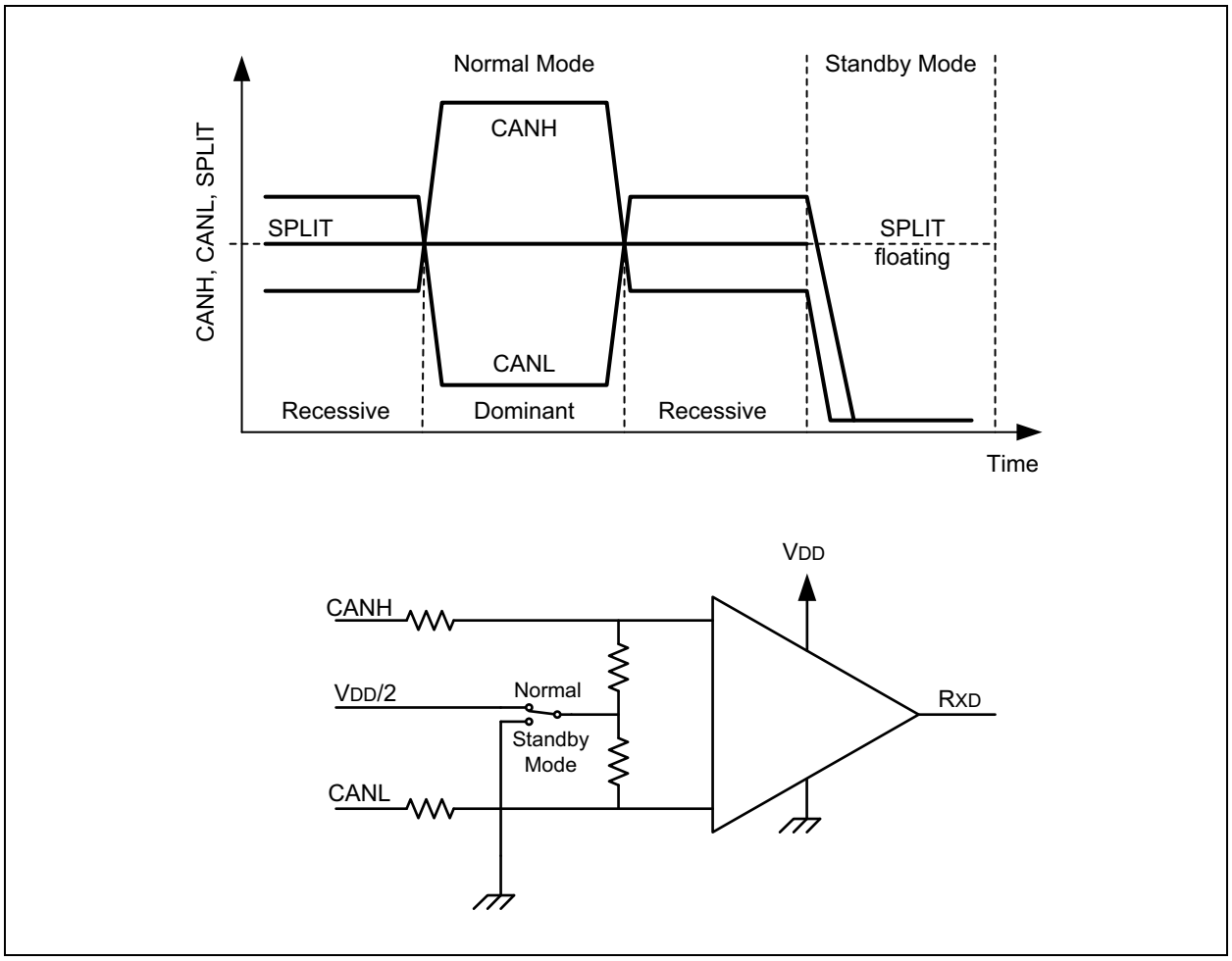
Characteristic	Sym	Min	Typ	Max	Units	Conditions
COMMON MODE STABILIZATION OUTPUT (SPLIT)						
Output Voltage	Vo	0.3V_{DD}	0.5V_{DD}	0.7V_{DD}	V	Normal mode; I_{SPLIT} = -500 µA to +500 µA
		0.45V_{DD}	0.5V_{DD}	0.55V_{DD}	V	Normal mode; $R_L \geq 1$ MΩ
Leakage Current	I_L	-5	—	+5	µA	Standby mode; V_{SPLIT} = -24V to + 24V (ISO 11898: -12V ~ +12V)
DIGITAL INPUT PINS (T_{XD}, STBY)						
High-Level Input Voltage	V_{IH}	0.7V_{IO}	—	V_{IO} + 0.3	V	
Low-Level Input Voltage	V_{IL}	-0.3	—	0.3V_{IO}	V	
High-Level Input Current	I_{IH}	-1	—	+1	µA	
T_{XD}: Low-Level Input Current	$I_{IL(TXD)}$	-270	-150	-30	µA	
STBY: Low-Level Input Current	$I_{IL(STBY)}$	-30	—	-1	µA	
RECEIVE DATA (R_{XD}) OUTPUT						
High-Level Output Voltage	V_{OH}	V_{DD} - 0.4	—	—	V	I_{OH} = -2 mA (**MCP2561FD**); typical -4 mA
		V_{IO} - 0.4	—	—		I_{OH} = -1 mA (**MCP2562FD**); typical -2 mA
Low-Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4 mA; typical 8 mA
THERMAL SHUTDOWN						
Shutdown Junction Temperature	$T_{J(SD)}$	165	175	185	°C	-12V < V(CANH, CANL) < +12V, (Note 1)
Shutdown Temperature Hysteresis	$T_{J(HYST)}$	20	—	30	°C	-12V < V(CANH, CANL) < +12V, (Note 1)

Note 1: Characterized; not 100% tested.

2: Only MCP2562FD has V_{IO} pin. For the MCP2561FD, V_{IO} is internally connected to V_{DD}.

3: -12V to 12V is ensured by characterization, tested from -2V to 7V.

FIGURE 2-2: PHYSICAL BIT REPRESENTATION AND SIMPLIFIED BIAS IMPLEMENTATION



2.4 AC Characteristics

Electrical Characteristics: Extended (E): T_{AMB} = -40°C to +125°C and High (H): T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.8V to 5.5V (Note 2), R_L = 60Ω, C_L = 100 pF; unless otherwise specified.

Param. No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions
1	t_{BIT}	Bit Time	0.2	—	69.44	µs	
2	f_{BIT}	Bit Frequency	14.4	—	5000	kHz	
3	$t_{TXD-BUSON}$	Delay T_{XD} Low to Bus Dominant	—	65	—	ns	(Note 1)
4	$t_{TXD-BUSOFF}$	Delay T_{XD} High to Bus Recessive	—	90	—	ns	(Note 1)
5	$t_{BUSON-RXD}$	Delay Bus Dominant to R_{XD}	—	60	—	ns	(Note 1)
6	$t_{BUSOFF-RXD}$	Delay Bus Recessive to R_{XD}	—	65	—	ns	(Note 1)
7	$t_{TXD - RXD}$	Propagation Delay T_{XD} to R_{XD}	—	90	120	ns	
			—	120	180	ns	R_L = 120Ω, C_L = 200 pF, (Note 1)
8a	$t_{BIT(RXD),2M}$	Recessive bit time on R_{XD} - 2 Mbps, Loop Delay Symmetry	450	485	550	ns	$t_{BIT(TXD)}$ = 500 ns, see Figure 2-10
			400	460	550	ns	$t_{BIT(TXD)}$ = 500 ns, see Figure 2-10, R_L = 120Ω, C_L = 200 pF, (Note 1)
8b	$t_{BIT(RXD),5M}$	Recessive bit time on R_{XD} - 5 Mbps, Loop Delay Symmetry	160	185	220	ns	$t_{BIT(TXD)}$ = 200 ns, see Figure 2-10
8c	$t_{BIT(RXD),8M}$	Recessive bit time on R_{XD} - 8 Mbps, Loop Delay Symmetry	85	105	140	ns	$t_{BIT(TXD)}$ = 120 ns, see Figure 2-10 (Note 1)
9	$t_{FLTR(WAKE)}$	Delay Bus Dominant to R_{XD} (Standby mode)	0.5	1	4	µs	Standby mode
10	t_{WAKE}	Delay Standby to Normal Mode	5	25	40	µs	Negative edge on STBY
11	t_{PDT}	Permanent Dominant Detect Time	—	1.25	—	ms	T_{XD} = 0V
12	t_{PDTR}	Permanent Dominant Timer Reset	—	100	—	ns	The shortest Recessive pulse on T_{XD} or CAN bus to reset Permanent Dominant Timer

Note 1: Characterized, not 100% tested.

FIGURE 2-3: TEST LOAD CONDITIONS

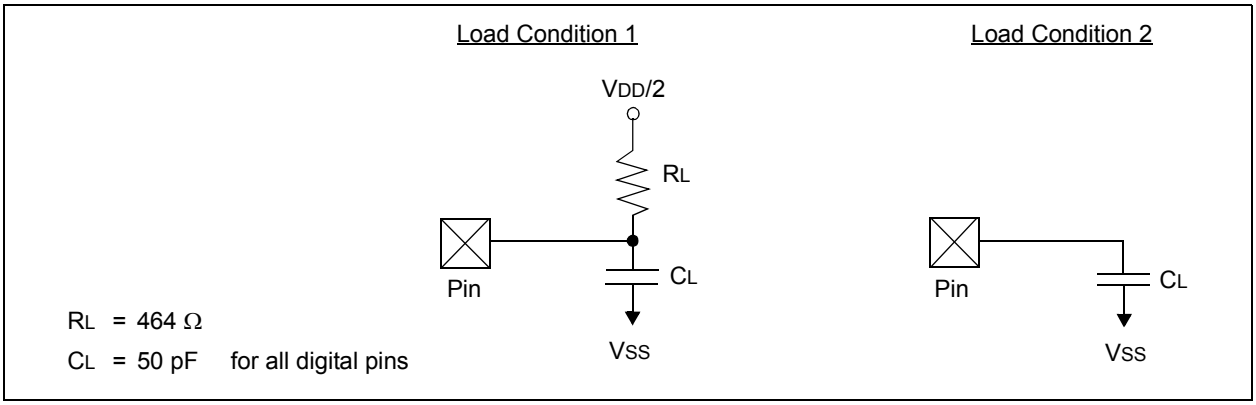
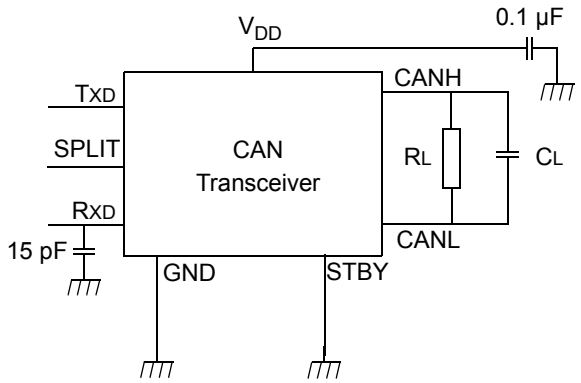
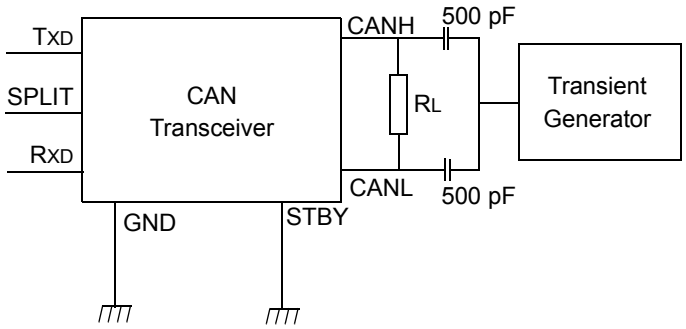


FIGURE 2-4: TEST CIRCUIT FOR ELECTRICAL CHARACTERISTICS



Note: On MCP2562FD, VIO is connected to VDD.

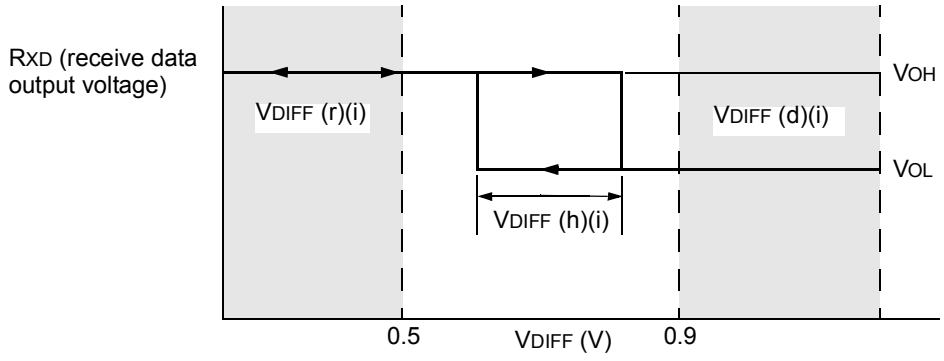
FIGURE 2-5: TEST CIRCUIT FOR AUTOMOTIVE TRANSIENTS



Note 1: On MCP2562FD, VIO is connected to VDD.

2: The wave forms of the applied transients shall be in accordance with ISO-7637, Part 1, test pulses 1, 2, 3a and 3b.

FIGURE 2-6: HYSTERESIS OF THE RECEIVER



2.5 Timing Diagrams and Specifications

FIGURE 2-7: TIMING DIAGRAM FOR AC CHARACTERISTICS

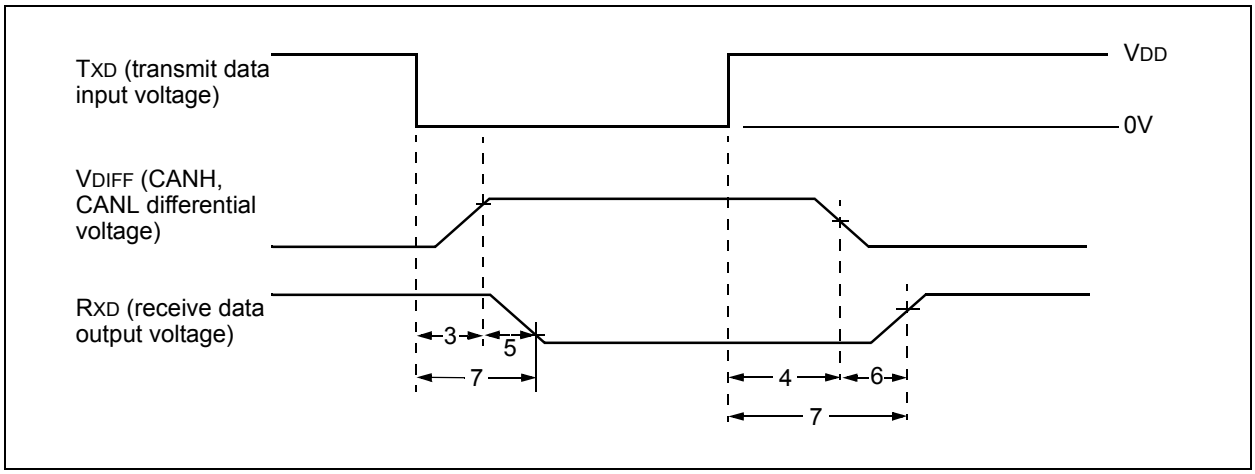


FIGURE 2-8: TIMING DIAGRAM FOR WAKEUP FROM STANDBY

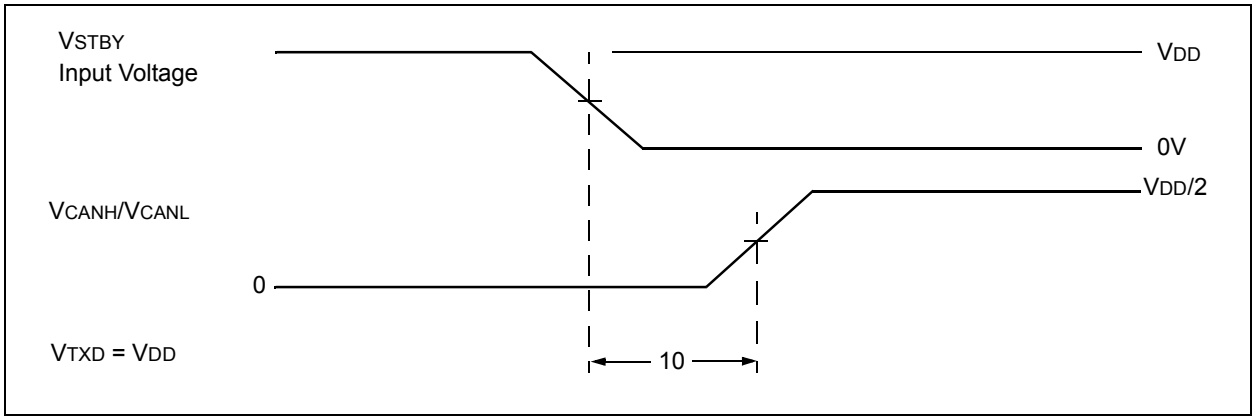


FIGURE 2-9: PERMANENT DOMINANT TIMER RESET DETECT

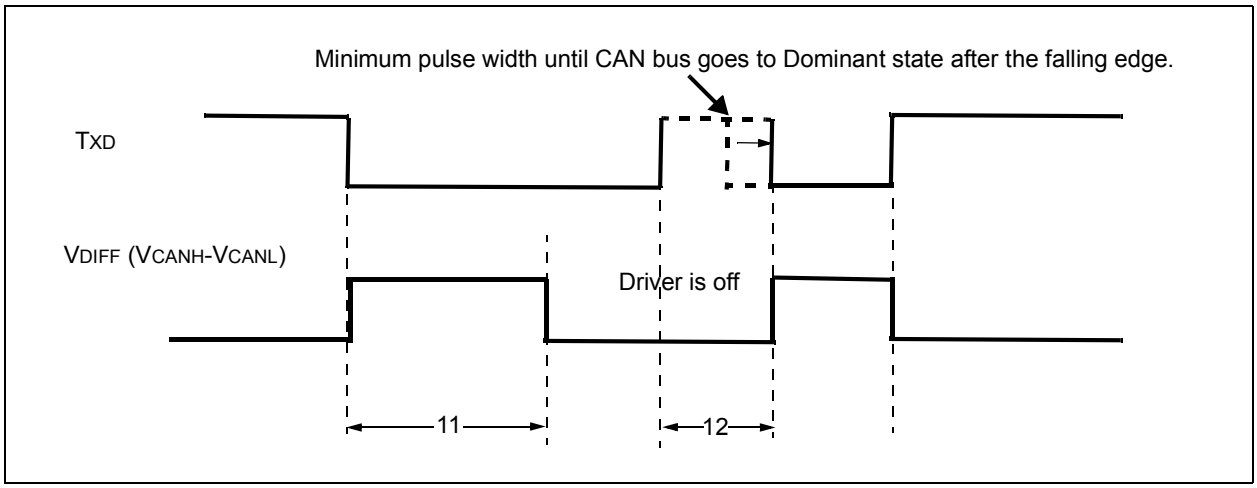
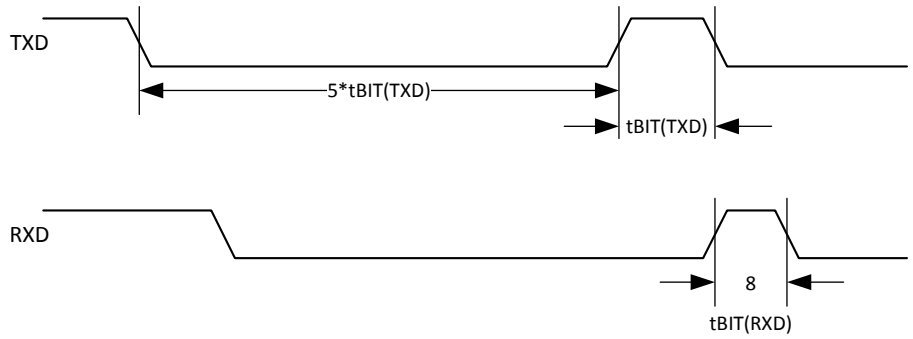


FIGURE 2-10: TIMING DIAGRAM FOR LOOP DELAY SYMMETRY



Note: The bit time of a recessive bit after five dominant bits is measured on the RXD pin. Due to asymmetry of the loop delay, and the CAN transceiver not being a push pull driver, the recessive bits tend to shorten.

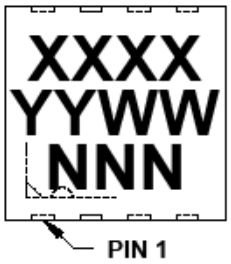
2.6 Thermal Specifications

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
		-40	—	+150		
Operating Temperature Range	T_A	-40	—	+150	°C	
Storage Temperature Range	T_A	-65	—	+155	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-DFN 3x3	θ_{JA}	—	56.7	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	89.3	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	

3.0 PACKAGING INFORMATION

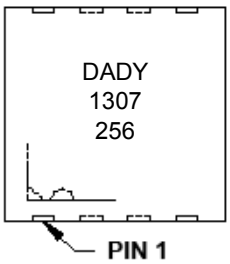
3.1 Package Marking Information

8-Lead DFN (3x3 mm)

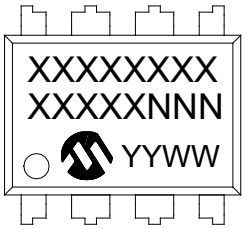


Part Number	Code
MCP2561FD-E/MF	DADY
MCP2561FDT-E/MF	DADY
MCP2561FD-H/MF	DADZ
MCP2561FDT-H/MF	DADZ
MCP2562FD-E/MF	DAEA
MCP2562FDT-E/MF	DAEA
MCP2562FD-H/MF	DAEB
MCP2562FDT-H/MF	DAEB

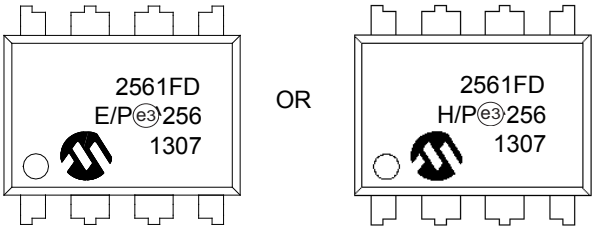
Example:



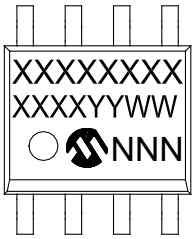
8-Lead PDIP (300 mil)



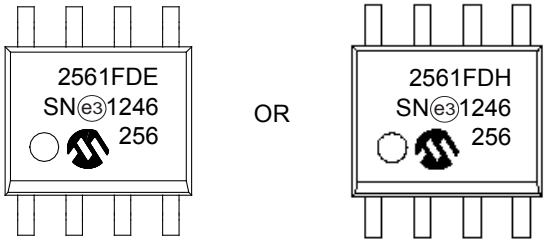
Example:



8-Lead SOIC (150 mil)



Example:

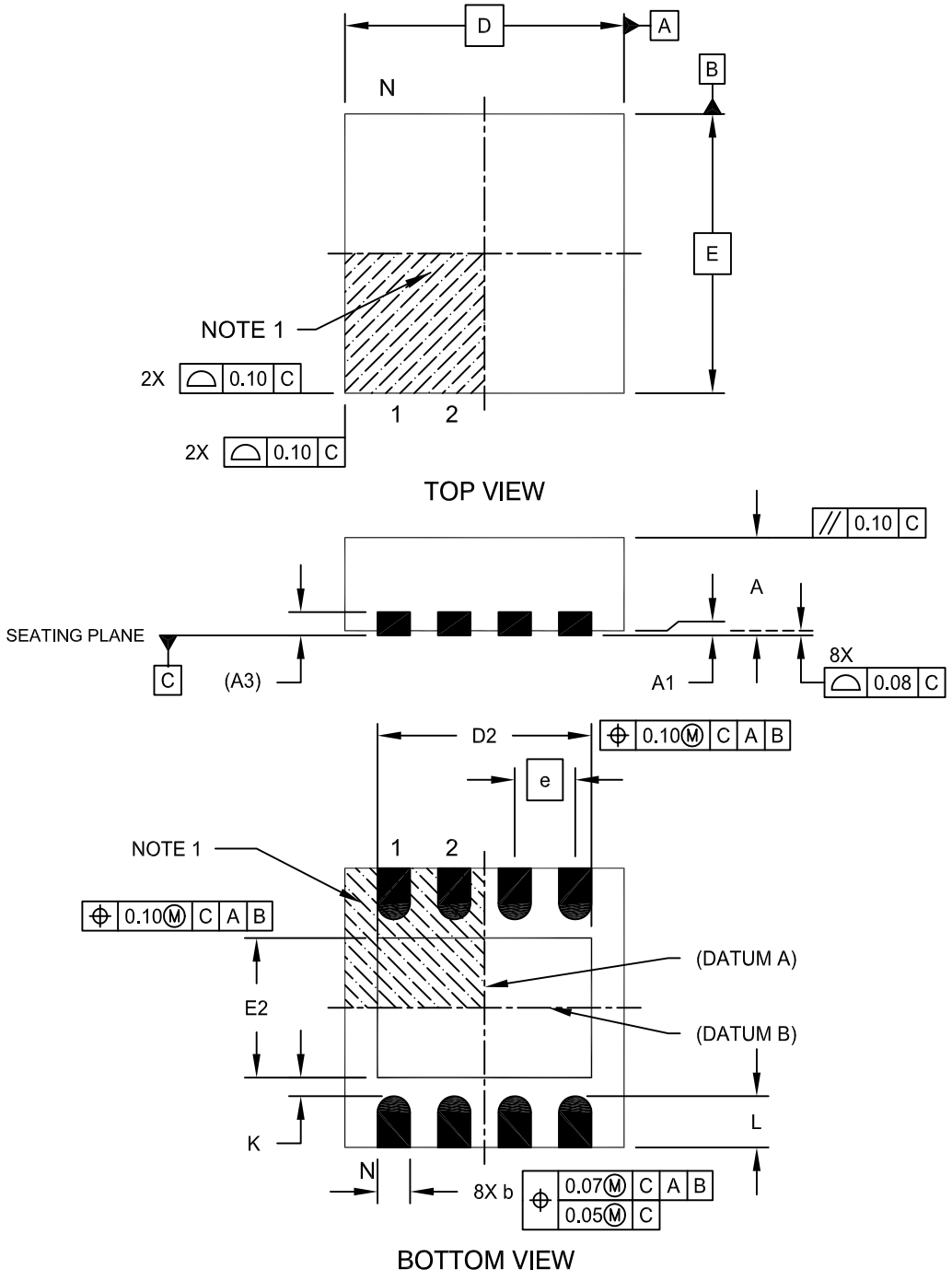


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

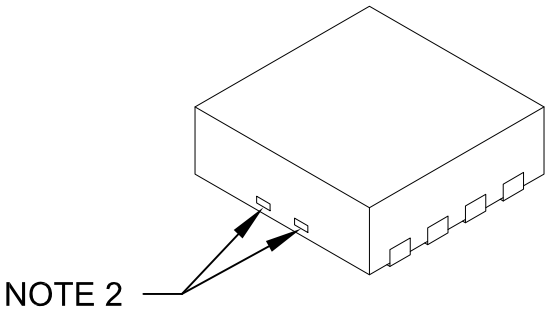
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-062C Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Width	E2	1.34	-	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.60	-	2.40
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.30	0.55
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

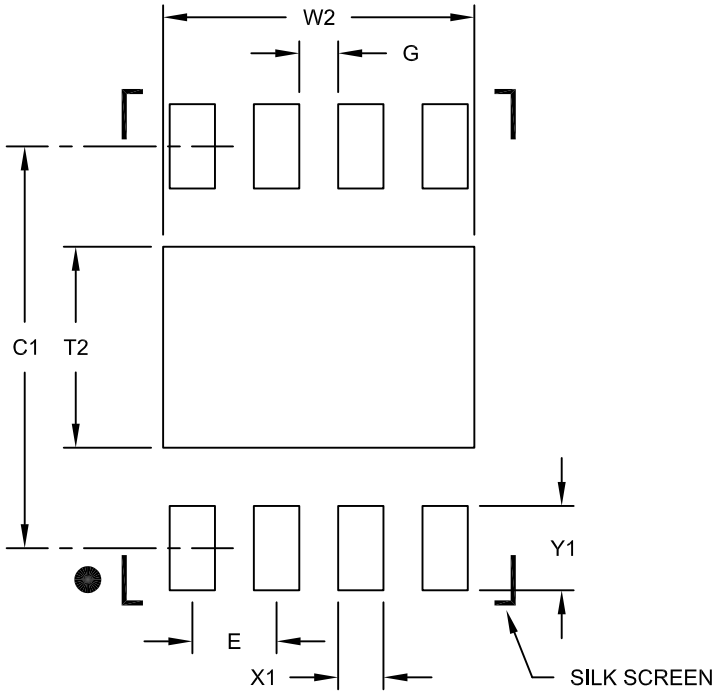
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-062C Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.65
Distance Between Pads	G	0.30		

Notes:

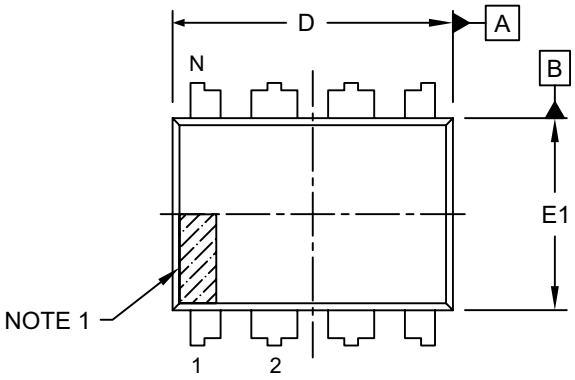
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

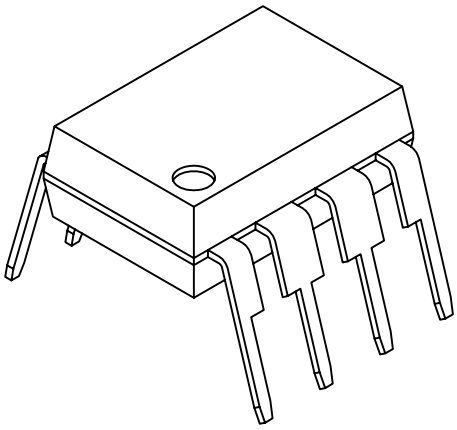
Microchip Technology Drawing No. C04-2062B

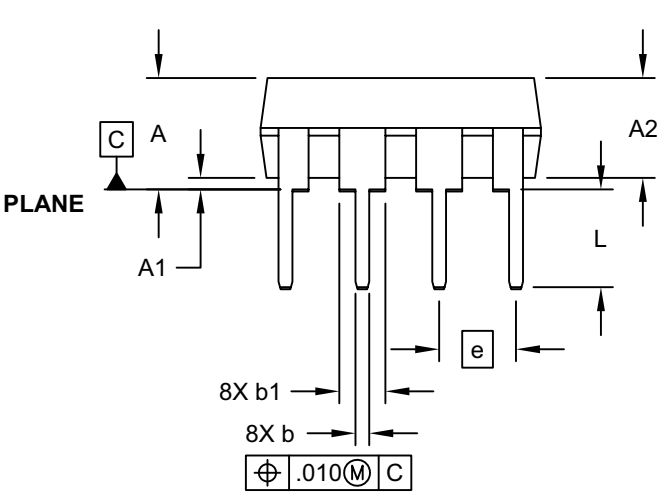
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

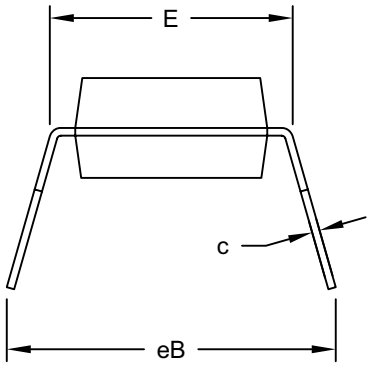


TOP VIEW





SIDE VIEW

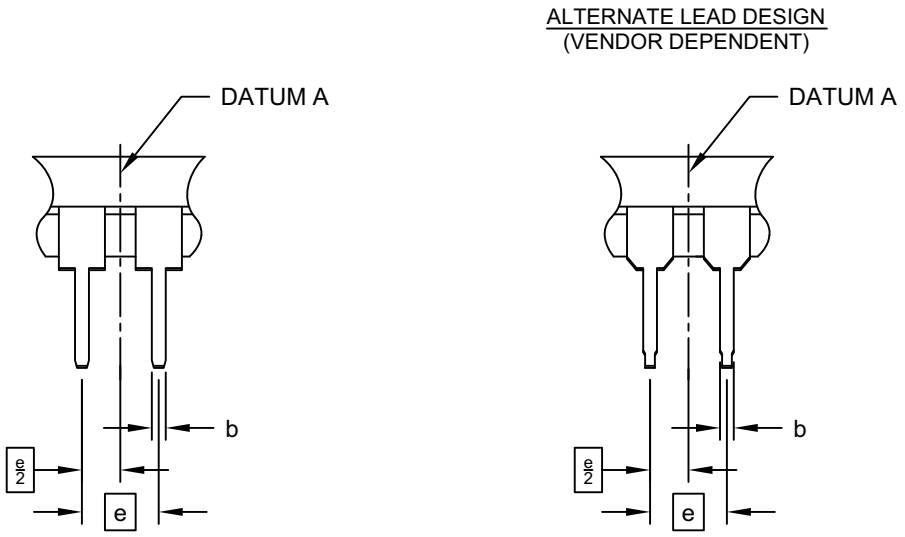


END VIEW

Microchip Technology Drawing No. C04-018D Sheet 1 of 2

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

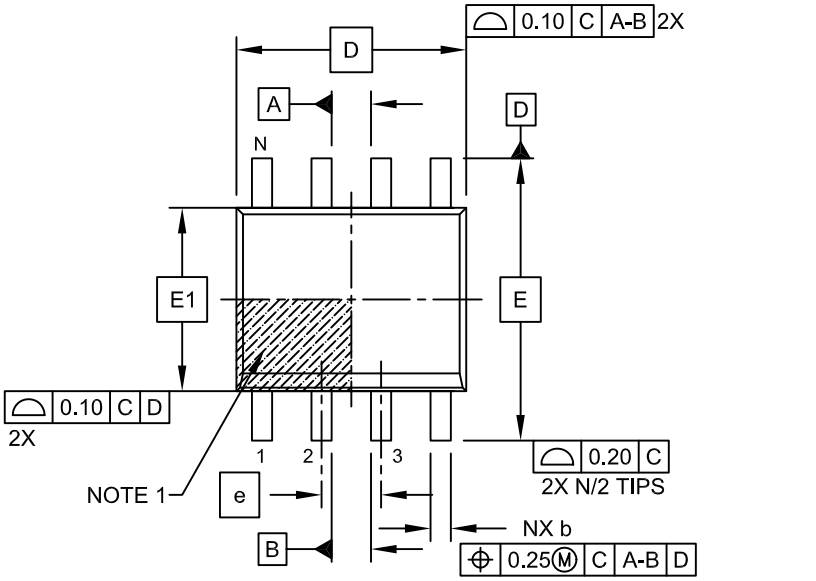
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

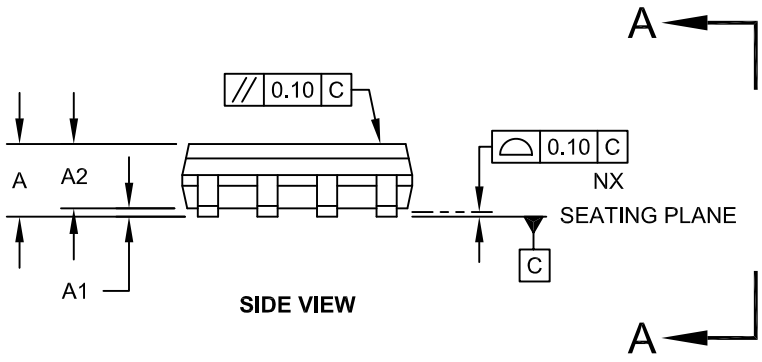
Microchip Technology Drawing No. C04-018D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

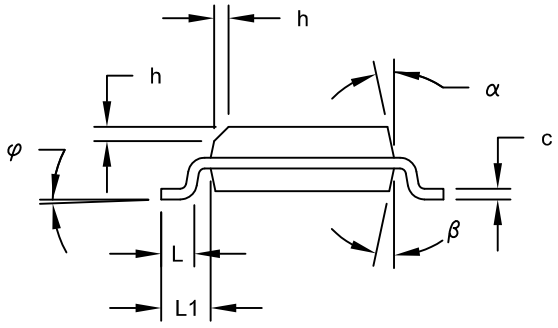
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

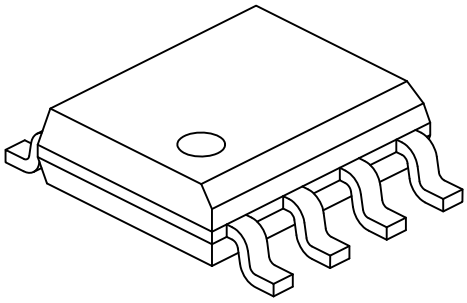


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

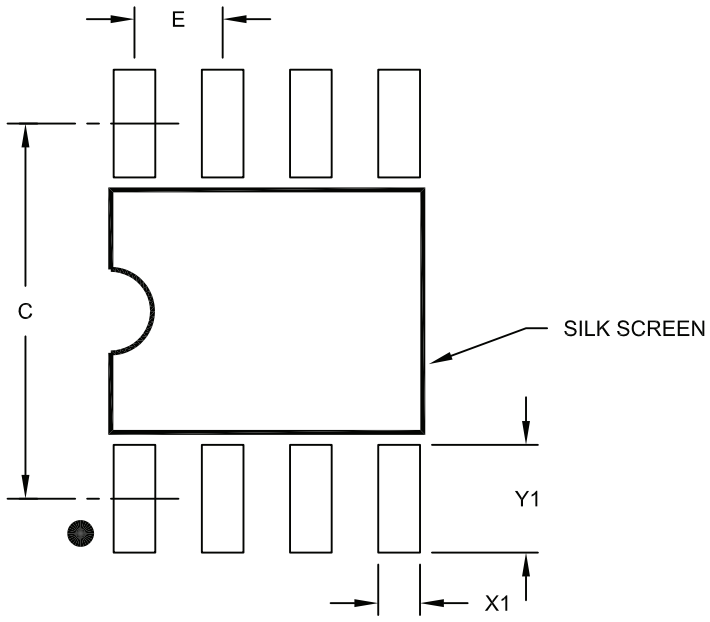
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (March 2014)

Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact the factory or one of the sales offices listed on the back page.

PART NO.	-X	/XX
Device	Temperature Range	Package

Device:
- MCP2561FD: High-Speed CAN Transceiver with SPLIT
- MCP2561FDT: High-Speed CAN Transceiver with SPLIT (Tape and Reel) (DFN and SOIC only)
- MCP2562FD: High-Speed CAN Transceiver with VIO
- MCP2562FDT: High-Speed CAN Transceiver with VIO (Tape and Reel) (DFN and SOIC only)

Temperature Range:
- E = -40°C to +125°C (Extended)
- H = -40°C to +150°C (High)

Package:
- MF = Plastic Dual Flat, No Lead Package - 3x3x0.9 mm Body, 8-lead
- P = Plastic Dual In-Line - 300 mil Body, 8-lead
- SN = Plastic Small Outline - Narrow, 3.90 mm Body, 8-lead

Examples:

a) MCP2561FD-E/MF: Extended Temperature, 8LD 3x3 DFN package.

b) MCP2561FDT-E/MF: Tape and Reel, Extended Temperature, 8LD 3x3 DFN package.

c) MCP2561FD-E/P: Extended Temperature, 8LD PDIP package.

d) MCP2561FD-E/SN: Extended Temperature, 8LD SOIC package.

e) MCP2561FDT-E/SN: Tape and Reel, Extended Temperature, 8LD SOIC package.

a) MCP2561FD-H/MF: High Temperature, 8LD 3x3 DFN package.

b) MCP2561FDT-H/MF: Tape and Reel, High Temperature, 8LD 3x3 DFN package.

c) MCP2561FD-H/P: High Temperature, 8LD PDIP package.

d) MCP2561FD-H/SN: High Temperature, 8LD SOIC package.

e) MCP2561FDT-H/SN: Tape and Reel, High Temperature, 8LD SOIC package.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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ISO/TS 16949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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