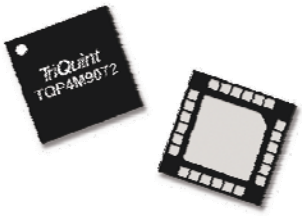
TQP4M9072

High Linearity 6-Bit, 31.5 dB Digital Step Attenuator

Applications

- Mobile Infrastructure
- LTE / WCDMA / CDMA / EDGE
- Test Equipments and Sensors
- IF and RF Applications
- General Purpose Wireless

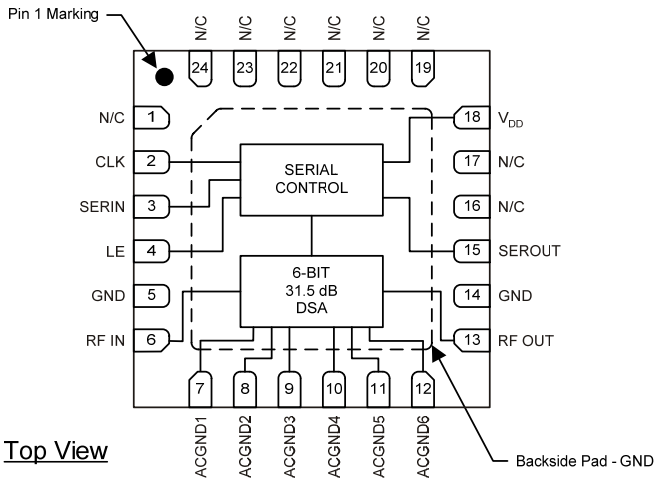


24-pin 4x4 mm leadless QFN package

Product Features

- DC – 4 GHz
- 0.5 dB LSB Steps to 31.5 dB
- +57 dBm Input IP3
- 1.7 dB Insertion Loss at 2.2 GHz
- Serial Control Interface
- No requirement for external bypass capacitors for operation above 700 MHz
- 50 Ω Impedance
- +5 V Supply Voltage. 3.3V TTL logic compatible

Functional Block Diagram



General Description

The TQP4M9072 is a high linearity, low insertion loss, 6 bit, 31.5 dB Digital Step Attenuator (DSA) operating over the DC – GHz frequency range. The digital step attenuator uses a single positive +5 V supply and has a serial periphery interface (SPI™) for changing attenuation states. This product maintains high attenuation accuracy over frequency and temperature. No external matching components are needed for the DSA. The product has an added feature of not requiring external AC ground capacitors for operation above 700 MHz.

The TQP4M9072 is available in a standard lead-free /green/RoHS-compliant 24-pin 4x4mm QFN package.

Also available from TriQuint is the TQP4M9071, a footprint and pin compatible DSA with a parallel control interface.

Pin Configuration

Pin No.	Label
1, 16-17, 19-24	N/C
2	CLK
3	SERIN
4	LE
6	RF IN
13	RF OUT
15	SEROUT
18	V_{DD}
7, 8, 9, 10, 11, 12	ACGND1 – ACGND6
5, 14	GND
Backside Pad	GND

Ordering Information

Part No.	Description
TQP4M9072	6 Bit, 31.5 dB DSA
TQP4M9072-PCB_ IF	40 – 500 MHz Evaluation Board
TQP4M9072-PCB_RF	0.7 – 4 GHz Evaluation Board

PCB includes USB control interface board, EVH.
Standard T/R size = 2500 pieces on a 13” reel.

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55 to 150 °C
Junction Temperature	150 °C
RF Input Power, 50 Ω,T = 85 °C	+28 dBm
Device Voltage (V_{DD})	+6.0 V
Digital Input Voltage	V_{DD} + 0.5 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{DD})	+3.3	+5	+5.25	V
Case Temperature	−40		+105	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions: V_{DD}=+5 V, Temp= +25 °C, 50 Ω system, Mode 1, No external bypass capacitors used on pins 7 – 12.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range	See Note 1 and 2.	DC		4000	MHz
Insertion Loss	1.0 GHz		1.3		dB
	2.0 GHz		1.6		dB
	2.2 GHz		1.7	2.2	dB
	3.5 GHz		2.1		dB
Return Loss	All States		17		dB
Accuracy Error	0.04 – 2.7 GHz, All States, Mode 2	± (0.3 + 3% of Atten. Setting) Max			dB
	0.7 – 2.7 GHz, All States, Mode 1 or Mode 2	± (0.3 + 3% of Atten. Setting) Max			dB
	2.7 – 3.5 GHz, All States, Mode 1 or Mode 2	± (0.4 + 4% of Atten. Setting) Max			dB
Attenuation Step	To be monotonic (Step Attenuation ≥ 0)	0	0.5		dB
Input IP3	Input Power = +15 dBm / tone, All States		+57		dBm
Input P0.1 dB	All States, DC – 4 GHz		+30		dBm
Time $_{rise\ /\ fall}$	10% / 90% RF		90		ns
Time $_{On}$, Time $_{Off}$	50% CTL to 10% / 90% RF		100		ns
Supply Voltage, V_{DD}			+5		V
Supply Current, I_{DD}			2.0		mA

Notes:
1. In Mode 1 no external bypass capacitors are used and operating frequency is 0.7 – 4GHz. See detailed device description.
2. In Mode 2 external bypass capacitors are used and operating frequency may be extended to 0.04 – 4GHz. See detailed device description.

Serial Control Interface

The TQP4M9072 has a CMOS SPI™ input compatible serial interface. This serial control interface converts the serial data input stream to parallel output word. The input is 3-wire (CLK, LE and SID) SPI™ input compatible. At power up, the serial control interface resets the DSA to the minimum gain state. The 6-bit SID (Serial Input Data) word is loaded into the register on rising edge of the CLK, MSB first. When LE is high, CLK is internally disabled.

Serial Control Timing Characteristics (Test conditions: V_{dd} = +5 V, Temp.=25°C)

Parameter	Condition	Min	Max	Units
Clock Frequency	50% Duty Cycle		10	MHz
LE Setup Time, t_{LESUP}	after last CLK rising edge	10		ns
LE Pulse Width, t_{LEPW}		30		ns
SERIN set-up time, t_{SDSUP}	before CLK rising edge	10		ns
SERIN hold-time, t_{SDHLD}	after CLK rising edge	10		ns
LE Pulse Spacing, t_{LE}	LE to LE pulse spacing	630		ns

Serial Control DC Logic Characteristics (Test conditions: V_{dd} = +5 V, Temp.=25°C)

Parameter	Condition	Min	Max	Units
Input Low State Voltage, V_{IL}		0	0.8	V
Input High State Voltage, V_{IH}		2.4	V_{dd}	V
Output High State Voltage, V_{OH}	On SOD pin	2.0	V_{dd}	V
Output Low State Voltage, V_{OL}	On SOD pin	0	0.8	V
Input Current, I_{IH} / I_{IL}	On SID, LE and CLK pins	−10	+10	µA

Serial Control DC Logic Characteristics (Test conditions: V_{dd} = +3.3 V, Temp.=25°C)

Input Low State Voltage, V_{IL}		0	0.8	V
Input High State Voltage, V_{IH}		2.8	V_{dd}	V
Input Current, I_{IH} / I_{IL}	On SID, LE and CLK pins	−10	+10	µA

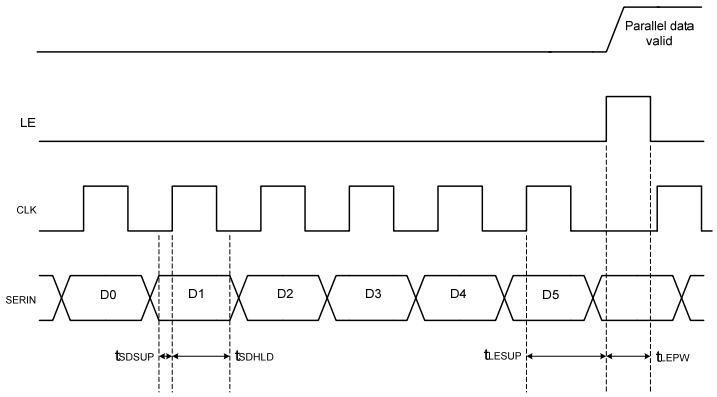
SERIN Control Logic Truth Table

6-Bit Control Word						Attenuation State
MSB					LSB	
D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	Reference : IL
1	1	1	1	1	0	0.5 dB
1	1	1	1	0	1	1 dB
1	1	1	0	1	1	2 dB
1	1	0	1	1	1	4 dB
1	0	1	1	1	1	8 dB
0	1	1	1	1	1	16 dB
0	0	0	0	0	0	31.5 dB

Any combination of the possible 64 states will provide an attenuation of approximately the sum of bits selected

Timing Diagram

CLK is internally disabled when LE is high

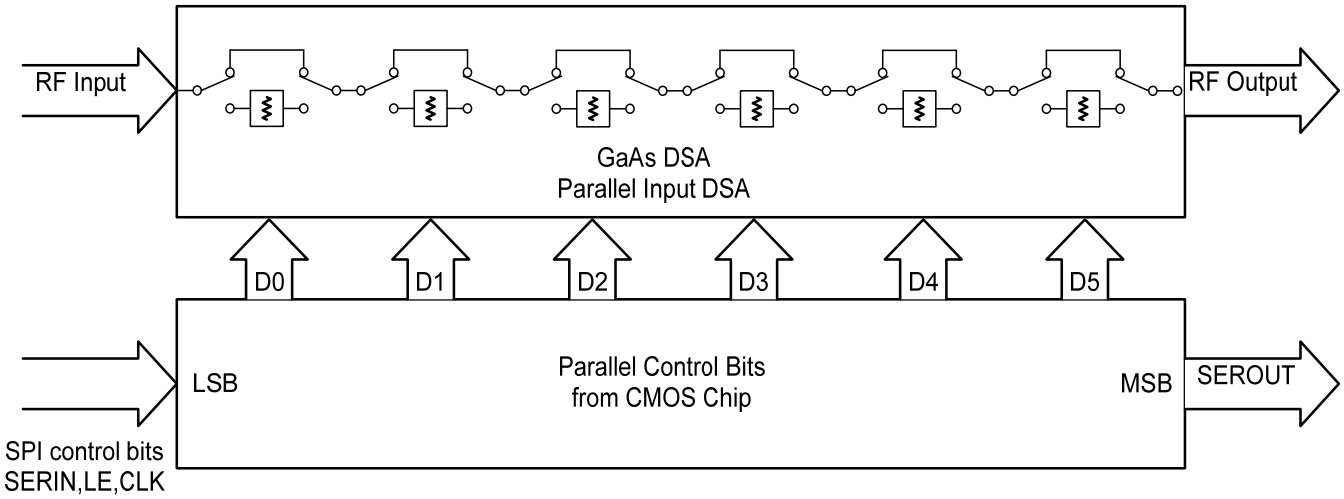


Detailed Device Description

The TQP4M9072 is a high linearity, low insertion loss, wideband, 6-bit, 31.5 dB digital step attenuator. The digital step attenuator uses a single 5 V supply and has a CMOS SPI™ controller. This product maintains high attenuation accuracy over frequency and temperature. The product does not require any external bypass capacitors on AC ground pins for operation above 700 MHz. The DSA performance remains unchanged for frequency range 0.7 – 4 GHz in either Mode 1 or Mode 2. The operating frequency may be extended to low frequency range (0.04 – 0.7 GHz) with external bypass capacitors on AC ground pins (ACGND1-ACGND6).

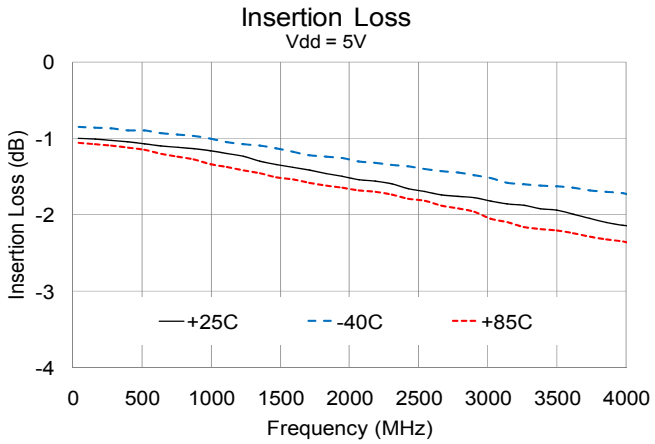
Further assistance may be requested from TriQuint Applications Engineering:
Email: **sjcapplications.engineering@triquint.com**

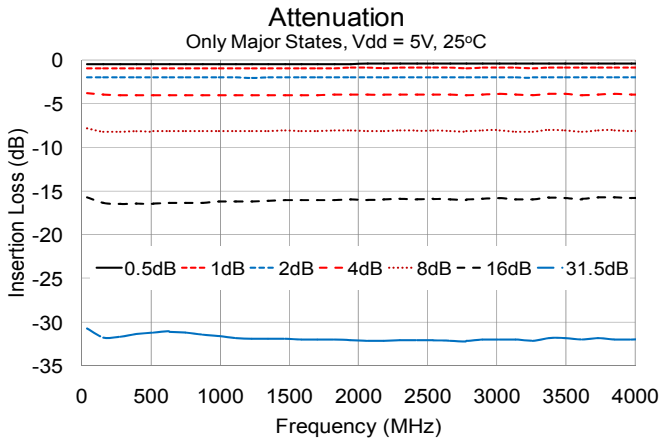
Functional Schematic Diagram

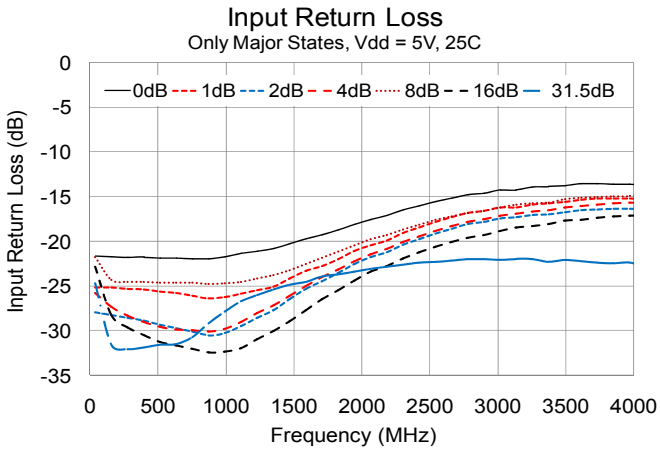


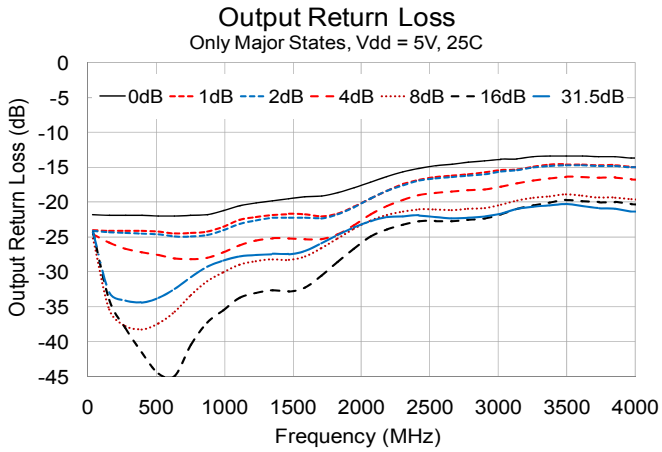
Typical Performance Plots

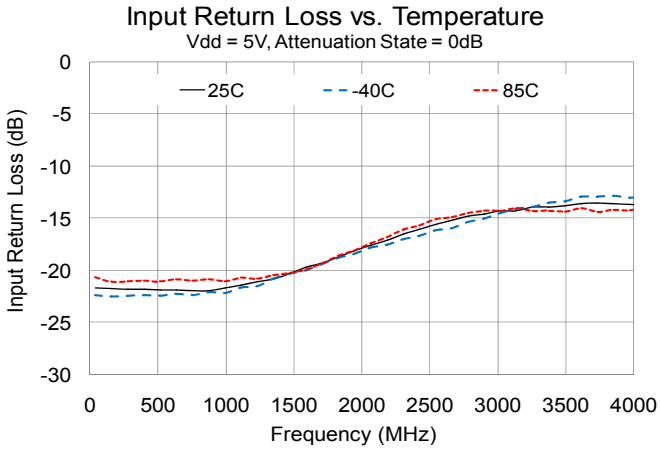
Performance plots data is measured using Bias Tee on RF ports in Mode 2 configuration. Mode 2 operation is required to obtain performance at frequencies lower than 0.7 GHz. For frequency range 0.7 – 4.0 GHz, data is identical in Mode 1 and Mode 2.

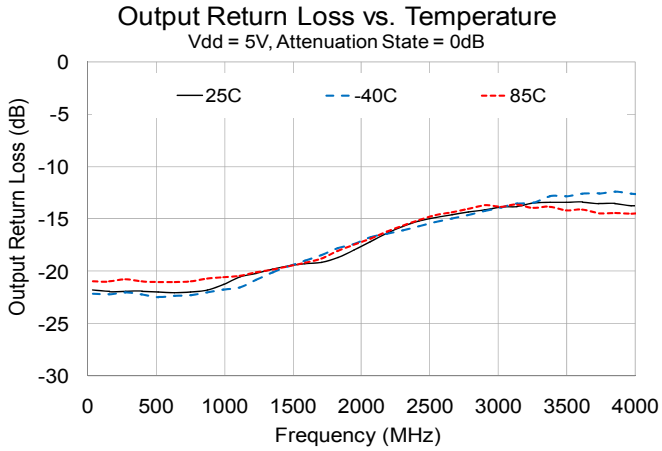




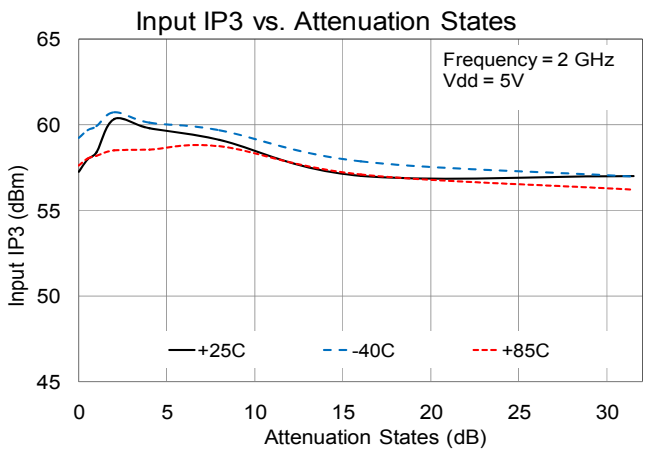


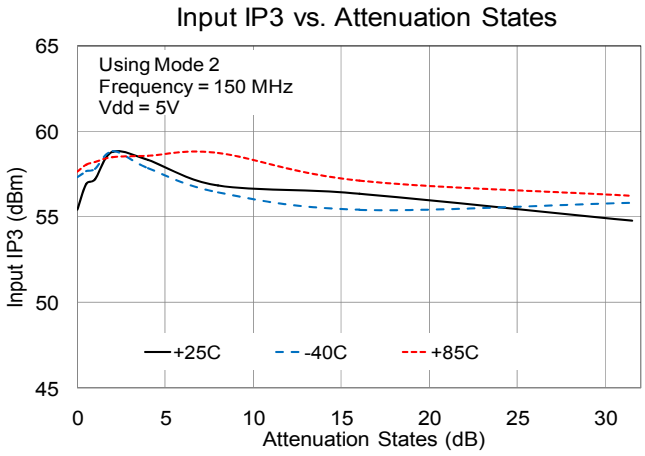


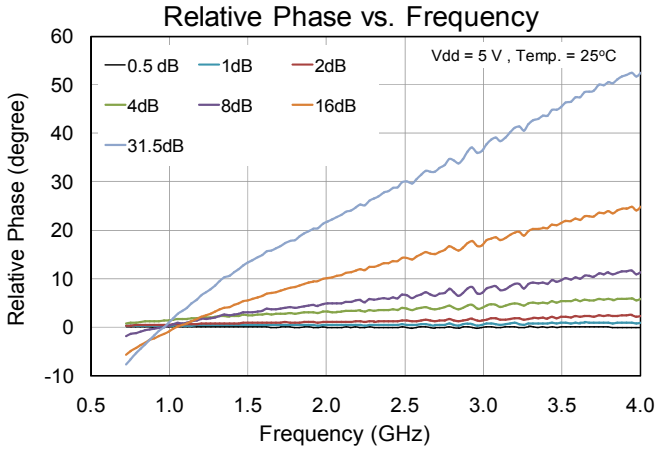


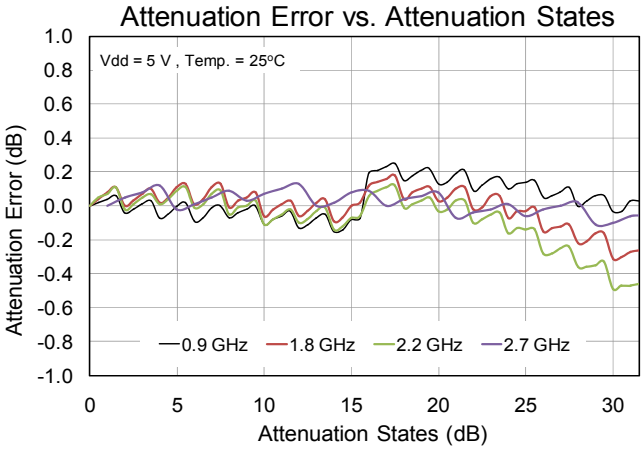


Typical Performance Plots



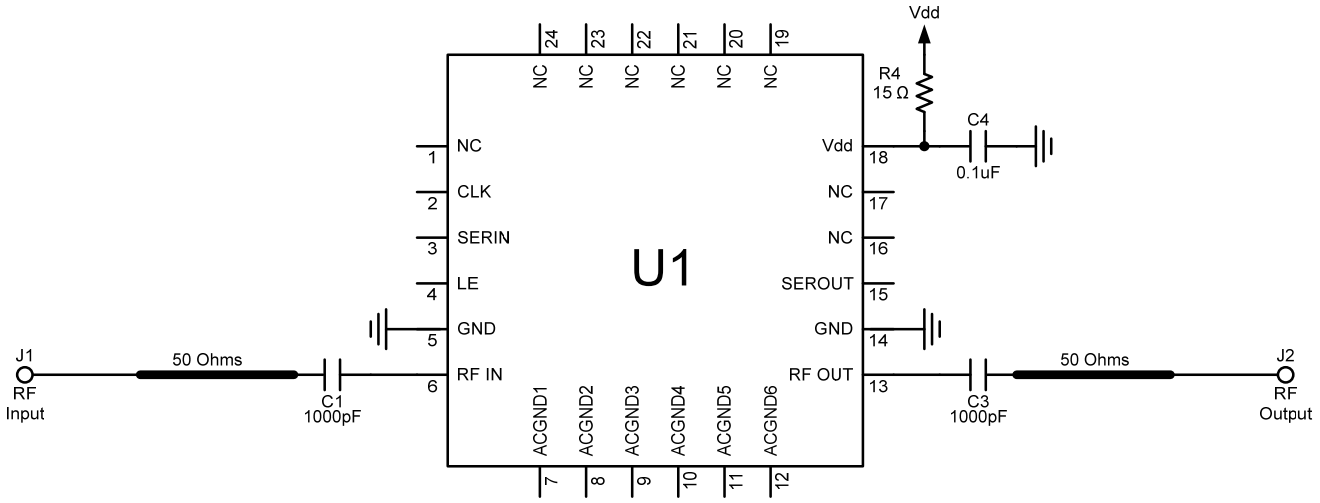






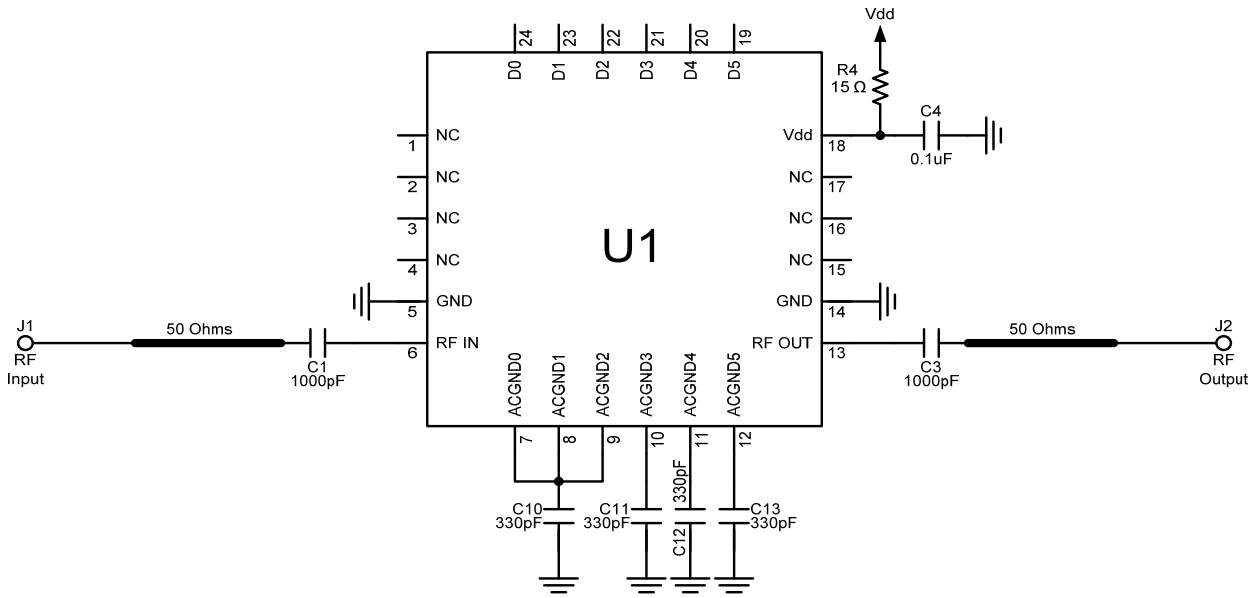
Mode 1: 0.7 – 4.0 GHz Operation (TQP4M9072-PCB_RF)

No external bypass capacitors required. There are 0.2 pF shunt capacitors (C5 and C7) next to RF connectors, on the application board, to resonate out the RF connector parasitic. These shunt capacitors are not required in the final application circuit.

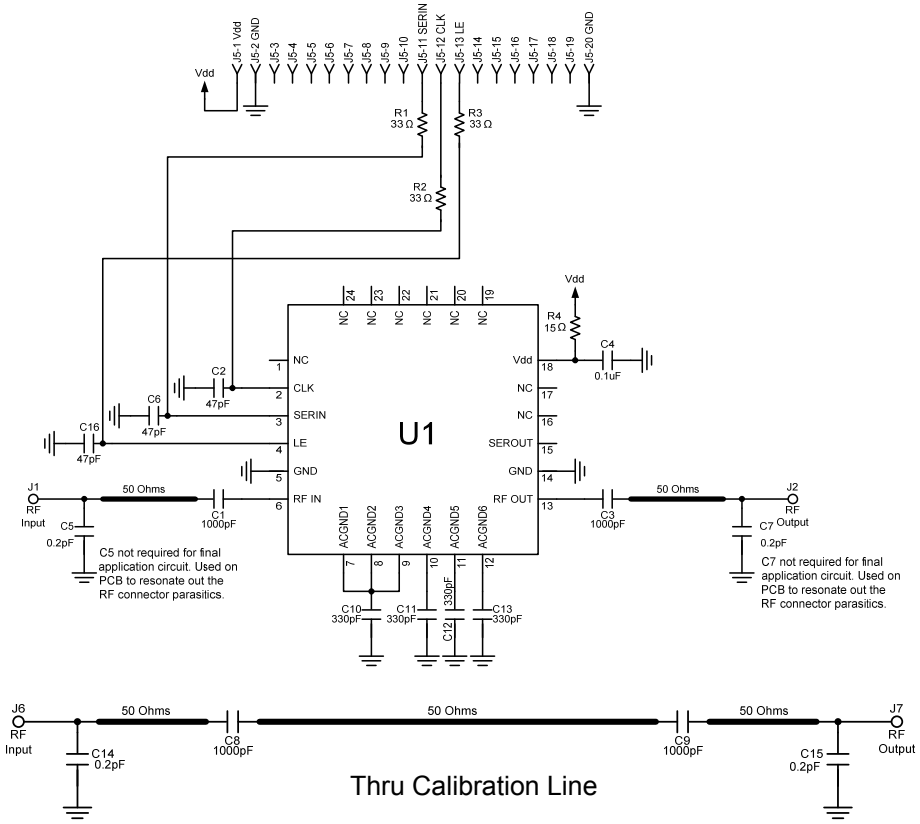


Mode 2: 0.04 – 4.0 GHz Operation (TQP4M9072-PCB_IF)

External bypass capacitors required on ACGND0 – ACGND5 pins. For improved operation below 0.1 GHz, blocking and bypass capacitors values can be increased to 10 nF. This circuit configuration can also be used for operation up to 4 GHz. The DSA performance remains unchanged for frequency range 0.7 – 4 GHz in either Mode 1 or Mode 2. There are 0.2 pF shunt capacitors (C5 and C7) next to RF connectors, on the application board, to resonate out the RF connector parasitic. These shunt capacitors are not required in the final application circuit.



TQP4M9072-PCB_RF/IF Schematic



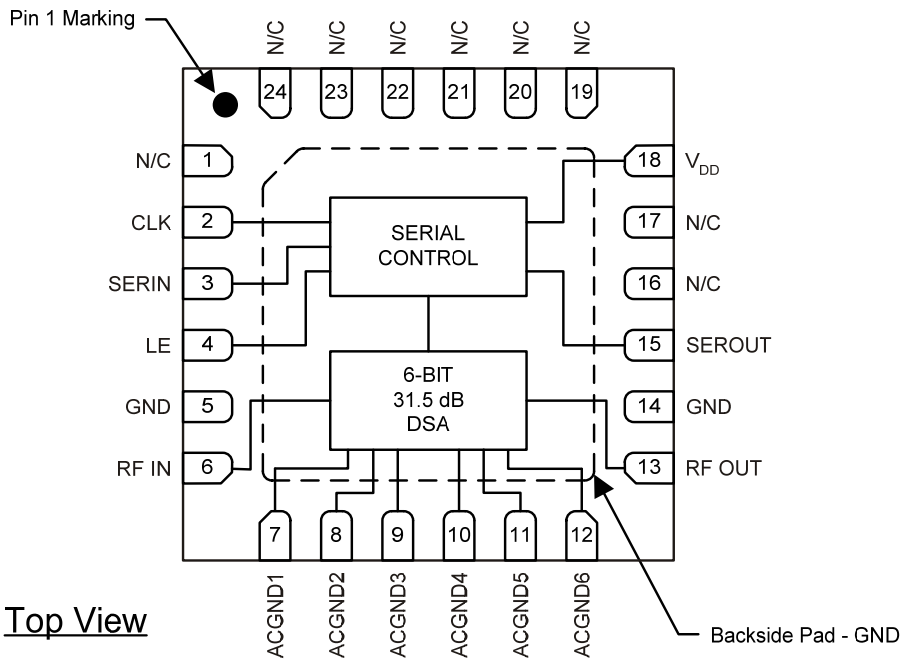
Bill of Material: TQP4M9071-PCB_RF

Reference Desg.	Value	Description	Manufacturer	Part Number
U1	n/a	High Linearity 6-Bit, 31.5dB, DSA	TriQuint	TQP4M9072
C2, C6, C16	47 pF	Cap, Chip, 0402, 50V, NPO, 5%	various	
C1,C3	1000 pF	Cap, Chip, 0402, 50V, X7R, 10%	various	
C4	0.1 uF	Cap, Chip, 0402, 50V, X7R, 10%	various	
R1, R2, R3	33 Ω	Res, Chip, 0402, 1/16W, 1%	various	
R4	15 Ω	Res, Chip, 0402, 1/16W, 5%	various	
C10, C11, C12, C13	DNP	Do Not Place	various	

Bill of Material: TQP4M9071-PCB_IF

Reference Desg.	Value	Description	Manufacturer	Part Number
U1	n/a	High Linearity 6-Bit, 31.5dB, DSA	TriQuint	TQP4M9072
C2, C6, C16	47 pF	Cap, Chip, 0402, 50V, NPO, 5%	various	
C1,C3	1000 pF	Cap, Chip, 0402, 50V, X7R, 10%	various	
C4	0.1 uF	Cap, Chip, 0402, 50V, X7R, 10%	various	
R1, R2, R3	33 Ω	Res, Chip, 0402, 1/16W, 1%	various	
R4	15 Ω	Res, Chip, 0402, 1/16W, 5%	various	
C10, C11, C12, C13	330 pF	Cap, Chip, 0402, 50V, X7R, 10%	various	

Pin Configuration and Description



Top View

Pin No.	Label	Description
2	CLK	Clock. This serial clock is used to clock in the serial data to the registers. The data is latched on the CLK rising edge. This input is a high impedance CMOS input.
3	SERIN	Serial Input Data. The 6-bit serial data is loaded MSB first. This input is a high impedance CMOS input.
4	LE	Latch Enable, When LE goes high, 6-bit data in the serial input register is transferred to the attenuator. When LE is high, CLK is disabled
6	RF IN	RF Input, DC voltage present, blocking capacitor required. Can be used for Input or Output.
7	ACGND1	AC ground for extended low frequency operation option
8	ACGND2	AC ground for extended low frequency operation option
9	ACGND3	AC ground for extended low frequency operation option
10	ACGND4	AC ground for extended low frequency operation option
11	ACGND5	AC ground for extended low frequency operation option
12	ACGND6	AC ground for extended low frequency operation option
13	RF OUT	RF Output, DC voltage present, blocking capacitor required. Can be used for Input or Output.
15	SEROUT	Serial Output Data
18	V_{DD}	Supply Voltage. Bypass capacitor required close to the pin. Dropping resistor highly recommended ensuring compatibility with different power supplies.
5, 14	GND	These pins must be connected to RF/DC ground
1, 16-17, 19-24	N/C	No electrical connection. Land pads should be provided for PCB mounting integrity.
Backside Pad	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

Applications Information

PC Board Layout

Top RF layer is .020" Rogers-4003, ϵ_r = 3.45, 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. Microstrip line details: width = .040", spacing = .020".

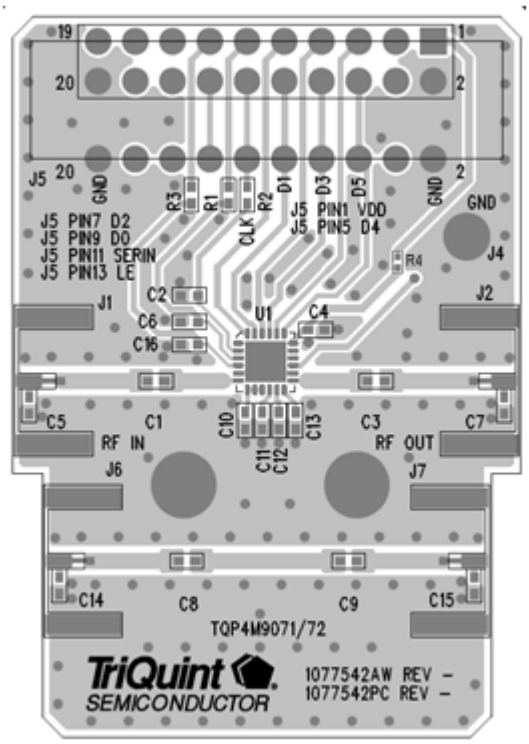
External DC blocking capacitors are required on RFin and RFout pins of the device. The supply voltage for the DSA is supplied externally through pin Vdd. Frequency bypassing for this pin is supplied by surface mount capacitor 0.1 uF (C4). This capacitor is placed close to the device pin in the board layout. To ensure application circuit is compatible with different standard power supplies, 15Ω (R4) dropping resistor is highly recommended on Vdd supply line.

R1, R2 and R3 are used as termination for digital noise or any noise reflection on Serial Input, CLK and LE pins.

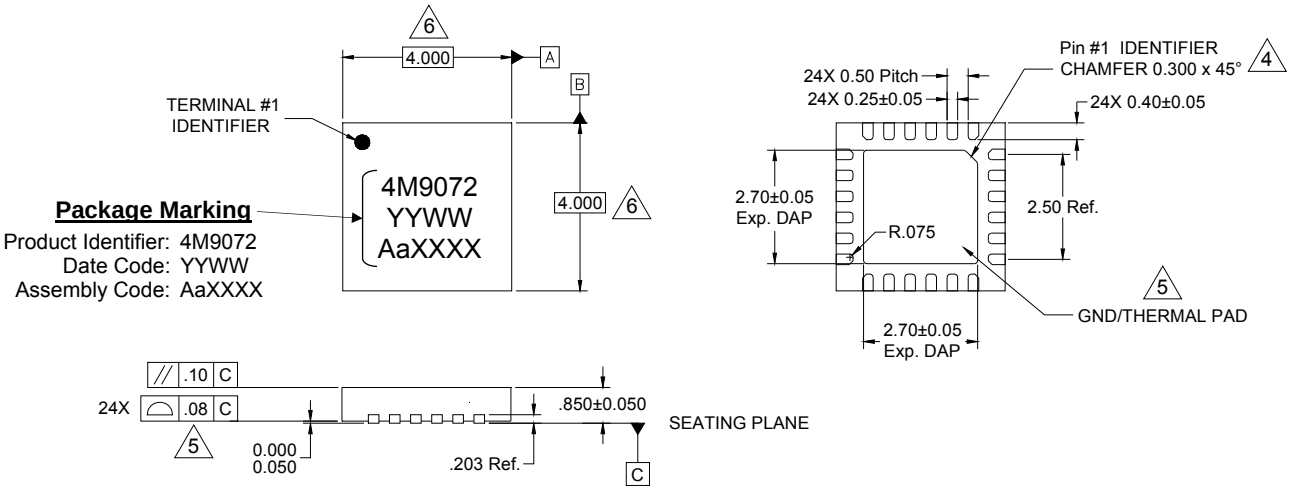
RF layout is critical for getting the best performance. RF trace impedance needs to be 50 ohm. For measuring the actual device performance on connectorized PC board, input losses due to RF traces need to be subtracted from the data measured through SMA connectors. The calibration microstrip line J6-J7 estimates the PCB insertion loss for removal from the evaluation board measured data. All data shown on the datasheet are de-embedded up to the device input/output pins.

The PC board is designed to test using USB control interface board, Evaluation Board Host (EVH). Each TQP4M9072 evaluation board is supplied with the EVH board, USB cable and EVH graphical user interface (EVH GUI) to change attenuation states. Manual for using EVH and Application note describing the EVH are also available. Refer to TriQuint's website for more information

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.



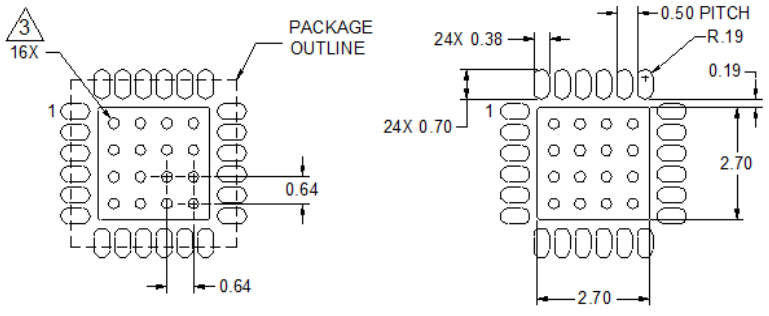
Package Marking and Dimensions



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
4. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins.
5. Package body length/width does not include plastic flash protrusion across mold parting line.

PCB Mounting Pattern



COMPONENT SIDE

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 1C
Value: ≥ 1000 V to < 2000 V
Test: Human Body Model (HBM)
Standard: ESDA/JEDEC Standard JS-001-2012

ESD Rating: Class C3
Value: ≥ 1000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101F

MSL Rating

MSL Rating: Level 1
Test: +260 °C convection reflow
Standard: JEDEC standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C maximum reflow temperature) and tin/lead (245 °C maximum reflow temperature) soldering processes.

Package lead plating: Annealed Matte Tin over Copper

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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Email: info-sales@triquint.com **Fax:** +1.503.615.8902

For technical questions and application information:

Email: sjcapplications.engineering@triquint.com

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