

SY54011R



Low Voltage 1.2V/1.8V CML 1:2 Fanout Buffer, 3.2Gbps, 3.2GHz

General Description

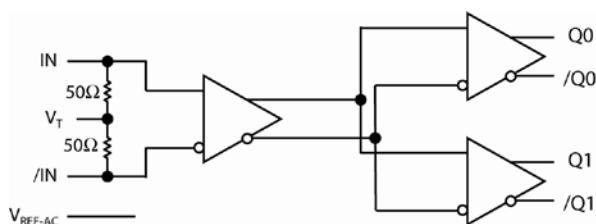
The SY54011R is a fully differential, low voltage 1.2V/1.8V CML 1:2 fanout buffer. It is optimized to provide two identical output copies with less than 15ps of skew and 50fs_{RMS} of typical additive phase jitter. The SY54011R can process clock signals as fast as 3.2GHz or data patterns up to 3.2Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS or CML differential signals, (AC- or DC-coupled from a 2.5V driver) as small as 100mV (200mV_{PP}) without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an integrated voltage reference ($V_{\text{REF-AC}}$) is provided to bias the VT pin. The outputs are CML, with extremely fast rise/fall times guaranteed to be less than 95ps.

The SY54011R operates from a 2.5V $\pm 5\%$ core supply and a 1.2V or 1.8V $\pm 5\%$ output supply and is guaranteed over the full industrial temperature range (-40°C to $+85^{\circ}\text{C}$). The SY54011R is part of Micrel's high-speed, Precision Edge[®] product line.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Block Diagram



Features

- 1.2V/1.8V CML 1:2 fanout buffer
- Guaranteed AC performance over temperature and voltage:
 - DC-to- > 3.2Gbps throughput
 - <300ps propagation delay (IN-to-Q)
 - <15ps within-device skew
 - <95ps rise/fall times
- Ultra-low jitter design
 - 50fs_{RMS} typical additive phase jitter
- High-speed CML outputs
- 2.5V $\pm 5\%$, 1.2V/1.8V $\pm 5\%$ power supply operation
- Industrial temperature range: -40°C to $+85^{\circ}\text{C}$
- Available in 16-pin (3mm x 3mm) MLF[®] package

Applications

- Data Distribution: OC-48, OC-48+FEC
- SONET clock and data distribution
- Fibre Channel clock and data distribution
- Gigabit Ethernet clock and data distribution

Markets

- Storage
- ATE
- Test and measurement
- Enterprise networking equipment
- High-end servers
- Access
- Metro area network equipment

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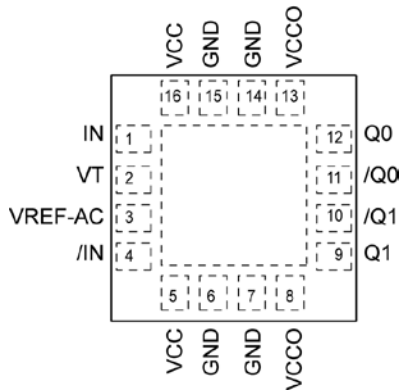
Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY54011RMG	MLF-16	Industrial	011R with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY54011RMGTR ⁽²⁾	MLF-16	Industrial	011R with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

- Contact factory for die availability. Dice are guaranteed at TA = 25°C, DC Electricals only.
- Tape and Reel.

Pin Configuration



16-Pin MLF[®] (MLF-16)

Pin Description

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair is the differential signal input to the device. Input accepts differential signals as small as 100mV (200mV _{PP}). Each input pin internally terminates with 50Ω to the VT pin.
2	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. See "Interface Applications" section.
3	VREF-AC	Reference Voltage: This output biases to V _{CC} -1.15V. It is used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the VT pin. Bypass with 0.1μF low ESR capacitor to VCC. Maximum sink/source current is ±0.5mA. See "Input Interface Applications" section.
5, 16	VCC	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors as close to the V _{CC} pins as possible. Supplies input and core circuitry.
8,13	VCCO	Output Supply: Bypass with 0.1μF//0.01μF low ESR capacitors as close to the V _{CCO} pins as possible. Supplies the output buffers.
6, 7, 14, 15	GND, Exposed pad	Ground: Exposed pad must be connected to a ground plane that is the same potential as the ground pins.
10, 9 11, 12	/Q1, Q1 /Q0, Q0	CML Differential Output Pairs: Differential buffered copies of the input signal. The output swing is typically 390mV. See "Interface Applications" section for termination information.

Absolute Maximum Ratings⁽³⁾

Supply Voltage (V_{CC}) -0.5V to +3.0V
 Supply Voltage (V_{CCO}) -0.5V to +2.7V
 V_{CC} - V_{CCO} <1.8V
 V_{CCO} - V_{CC} <0.5V
 Input Voltage (V_{IN}) -0.5V to V_{CC}
 CML Output Voltage (V_{OUT}) 0.6V to V_{CCO}+0.5V
 Current (V_T)
 Source or sink current on V_T pin ±100mA
 Input Current
 Source or sink current on (IN, /IN) ±50mA
 Current (V_{REF-AC})
 Source or sink current on V_{REF-AC}⁽⁶⁾ ±0.5mA
 Maximum operating Junction Temperature 125°C
 Lead Temperature (soldering, 20sec.) 260°C
 Storage Temperature (T_s) -65°C to +150°C

Operating Ratings⁽⁴⁾

Supply Voltage (V_{CC}) 2.375V to 2.625V
 (V_{CCO}) 1.14V to 1.9V
 Ambient Temperature (T_A) -40°C to +85°C
 Package Thermal Resistance⁽⁵⁾
 MLF[®]
 Still-air (θ_{JA}) 75°C/W
 Junction-to-board (Ψ_{JB}) 33°C/W

DC Electrical Characteristics⁽⁷⁾

T_A = -40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V _{CC}	Power Supply Voltage Range	V _{CC}	2.375	2.5	2.625	V
		V _{CCO}	1.14	1.2	1.26	V
		V _{CCO}	1.7	1.8	1.9	V
I _{CC}	Power Supply Current	Max. V _{CC}		15	22	mA
I _{CCO}	Power Supply Current	No Load. V _{CCO}		32	42	mA
R _{IN}	Input Resistance (IN-to-VT, /IN-to-VT)		45	50	55	Ω
R _{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V _{IH}	Input HIGH Voltage (IN, /IN)	IN, /IN	1.2		V _{CC}	V
V _{IL}	Input LOW Voltage (IN, /IN)	V _{IL} with V _{IH} of 1.2V	0.2		V _{IH} -0.1	V
V _{IH}	Input HIGH Voltage (IN, /IN)	IN, /IN	1.14		V _{CC}	V
V _{IL}	Input LOW Voltage (IN, /IN)	V _{IL} with V _{IH} of 1.14V, (1.2V-5%)	0.66		V _{IH} -0.1	V
V _{IN}	Input Voltage Swing (IN, /IN)	see Figure 4	0.1		1.0	V
V _{DIFF_IN}	Differential Input Voltage Swing (IN - /IN)	see Figure 5	0.2		2.0	V
V _{REF-AC}	Output Reference Voltage		V _{CC} -1.3	V _{CC} -1.15	V _{CC} -1.0	V
V _{T_IN}	Voltage from Input to VT				1.28	V

Notes:

- Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
- The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
- Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. θ_{JB} and Ψ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
- Due to the limited drive capability, use for input of the same package only.
- The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

CML Outputs DC Electrical Characteristics⁽⁷⁾

$V_{CC0} = 1.14V$ to $1.26V$ $R_L = 50\Omega$ to V_{CC0} ,

$V_{CC0} = 1.7V$ to $1.9V$, $R_L = 50\Omega$ to V_{CC0} or 100Ω across the outputs,

$V_{CC} = 2.375V$ to $2.625V$. $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	$R_L = 50\Omega$ to V_{CC0}	$V_{CC0}-0.020$	$V_{CC0}-0.010$	V_{CC0}	V
V_{OUT}	Output Voltage Swing	See Figure 4	300	390	475	mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 5	600	780	950	mV
R_{OUT}	Output Source Impedance		45	50	55	Ω

AC Electrical Characteristics

$V_{CC0} = 1.14V$ to $1.26V$ $R_L = 50\Omega$ to V_{CC0} ,

$V_{CC0} = 1.7V$ to $1.9V$, $R_L = 50\Omega$ to V_{CC0} or 100Ω across the outputs,

$V_{CC} = 2.375V$ to $2.625V$. $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	NRZ Data	3.2			Gbps
		$V_{OUT} > 200mV$ Clock	3.2			GHz
t_{PD}	Propagation Delay IN-to-Q	Figure 1	150	205	300	ps
t_{Skew}	Within Device Skew	Note 8		3	15	ps
	Part-to-Part Skew	Note 9			75	ps
t_{Jitter}	Additive Phase Jitter	Carrier = 622MHz. Integration Range: 12kHz – 20MHz		50		f_{SRMS}
t_R t_F	Output Rise/Fall Times (20% to 80%)	At full output swing.	30	60	95	ps
	Duty Cycle	Differential I/O	47		53	%

Notes:

- Within device skew is measured between two different outputs under identical input transitions.
- Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

Interface Applications

For Input Interface Applications see Figures 6-11 and for CML Output Termination see Figures 12-15.

CML Output Termination with VCCO 1.2V

For VCCO of 1.2V, Figure 12, terminate the output with 50Ω-to-1.2V, DC-coupled, not 100Ω differentially across the outputs.

If AC-coupling is used, Figure 15, terminate into 50Ω-to-1.2V before the coupling capacitor and then connect to a high value resistor to a reference voltage. Do not AC couple with internally terminated receiver. For example, 50Ω ANY-IN input. AC-coupling will offset the output voltage by 200mV and this offset voltage will be too low for proper driver operation.

Any unused output pair needs to be terminated when VCCO is 1.2V, do not leave floating.

CML Output Termination with VCCO 1.8V

For VCCO of 1.8V, Figure 12 and Figure 13, terminate with either 50Ω-to-VCCO or 100Ω differentially across the outputs. AC- or DC-coupling is fine.

Input AC Coupling

The SY54011R input can accept AC coupling from any driver. Tie VT to VREF-AC and bypass with a 0.1μF capacitor as shown in Figures 8 and 9.

Timing Diagrams

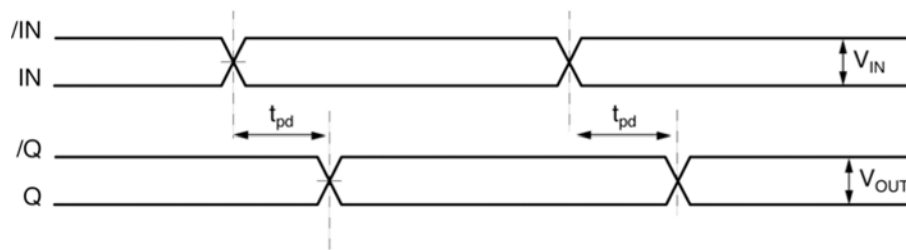
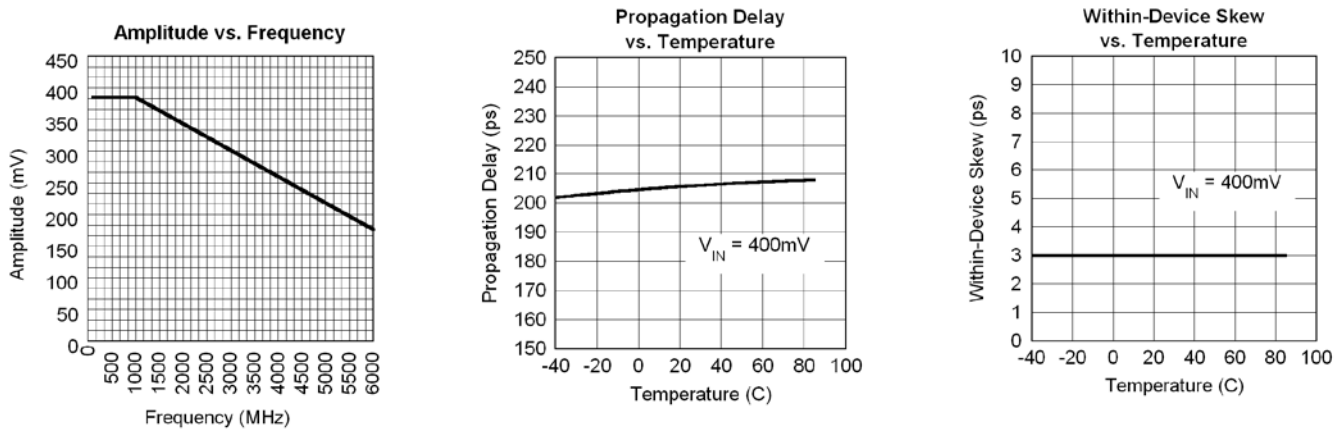


Figure 1. Propagation Delay

Typical Characteristics

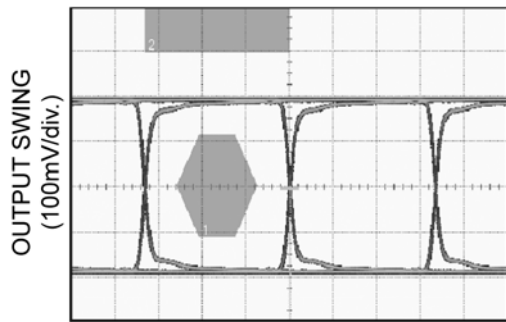
$V_{CC} = 2.5V$, $V_{CCO} = 1.2V$, $GND = 0V$, $V_{IN} = 100mV$; $R_L = 50\Omega$ to $1.2V$; $T_A = 25^\circ C$, unless otherwise stated.



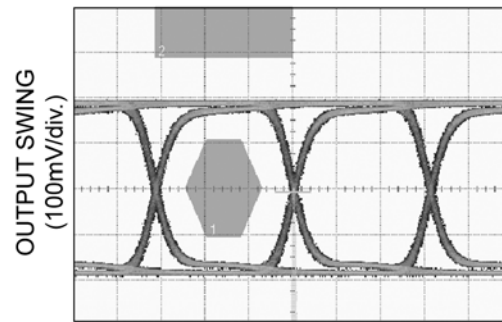
Functional Characteristics

$V_{CC} = 2.5V$, $V_{CCO} = 1.2V$, $GND = 0V$, $V_{IN} = 100mV$; $R_L = 50\Omega$ to $1.2V$, Data Pattern: $2^{23}-1$; $T_A = 25^\circ C$, unless otherwise stated.

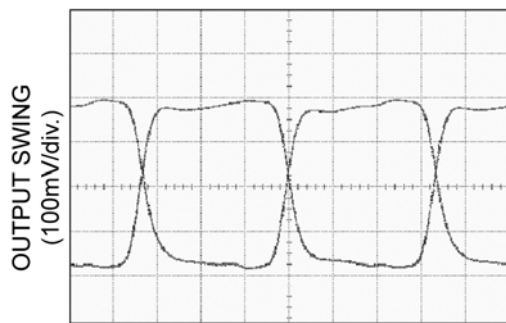
1.0Gbps Data



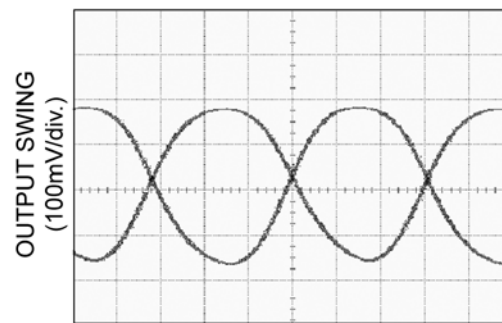
3.2Gbps Data



1.0GHz Clock

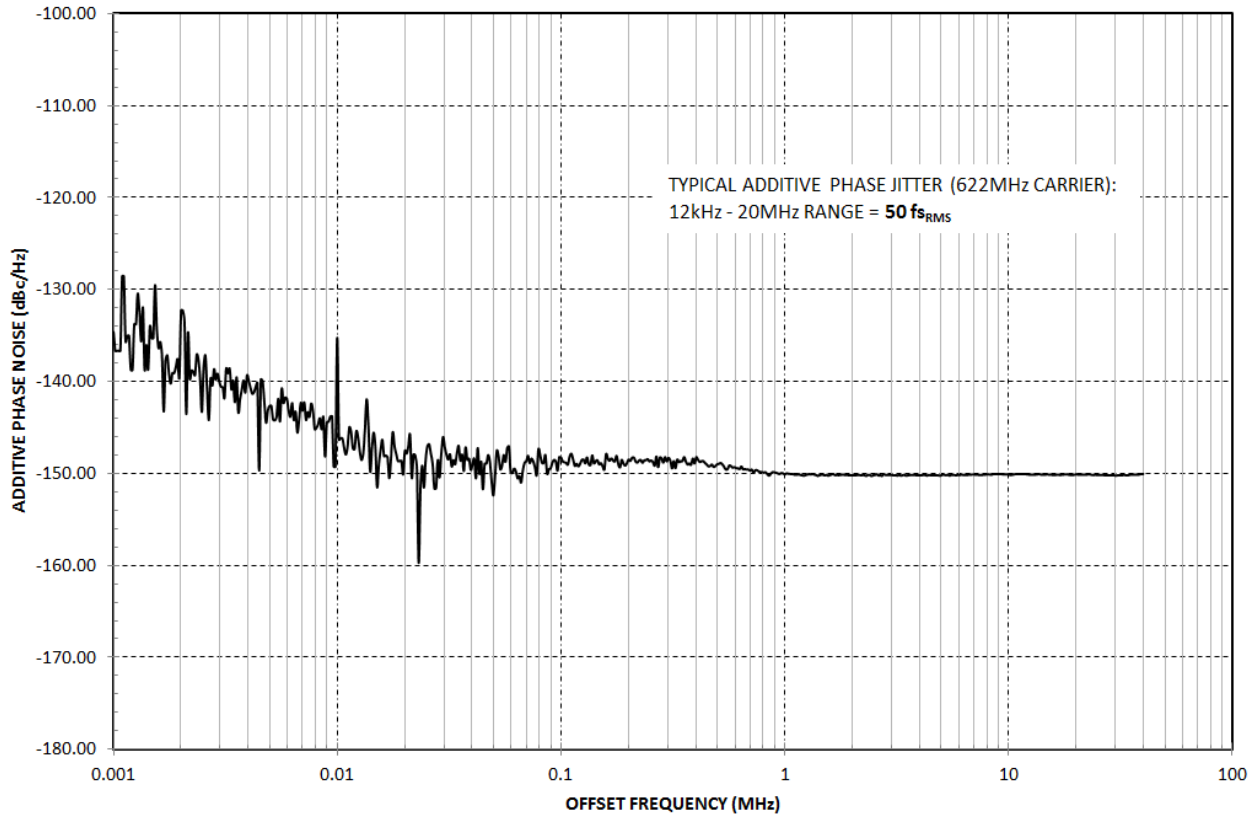


3.2GHz Clock



Additive Phase Noise Plot

$V_{CC} = +2.5V$, $GND = 0$, $T_A = 25^\circ C$



Input and Output Stage

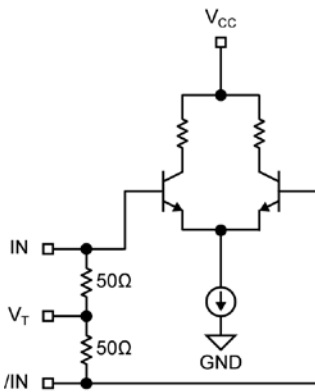


Figure 2. Simplified Differential Input Buffer

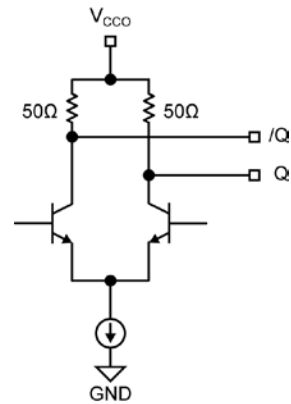


Figure 3. Simplified CML Output Buffer

Single-Ended and Differential Swings

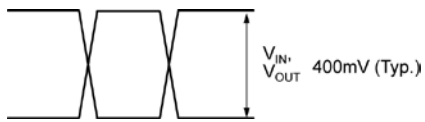


Figure 4. Single-Ended Swing

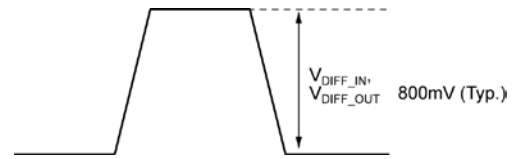


Figure 5. Differential Swing

Input Interface Applications

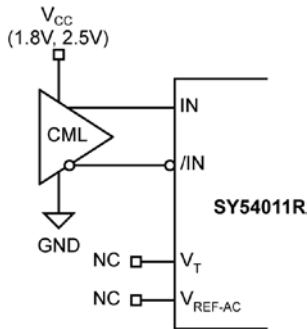


Figure 6. CML Interface (DC-Coupled, 1.8V, 2.5V)

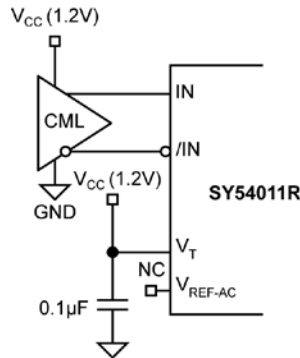


Figure 7. CML Interface (DC-Coupled, 1.2V)

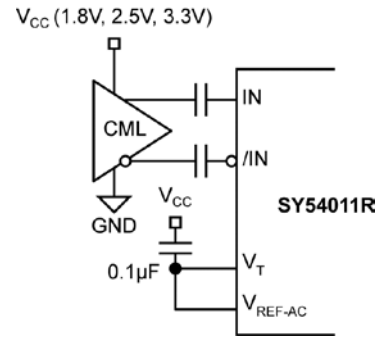


Figure 8. CML Interface (AC-Coupled)

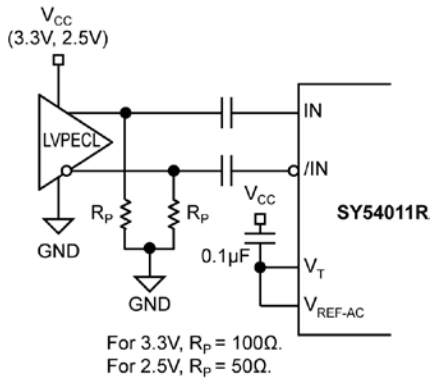


Figure 9. LVPECL Interface (AC-Coupled)

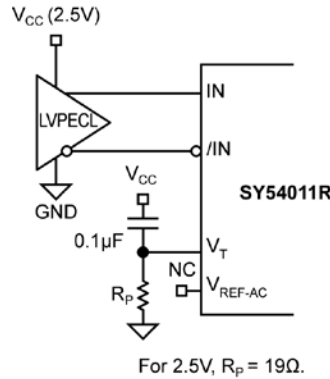


Figure 10. LVPECL Interface (DC-Coupled)

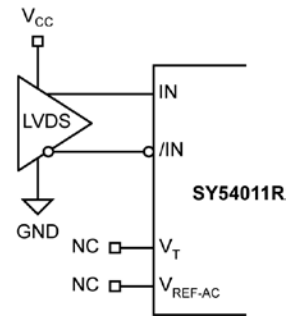
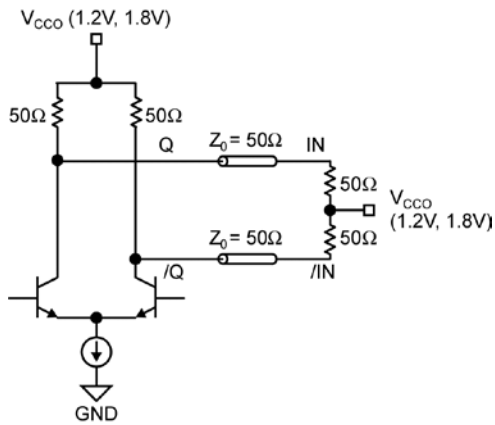
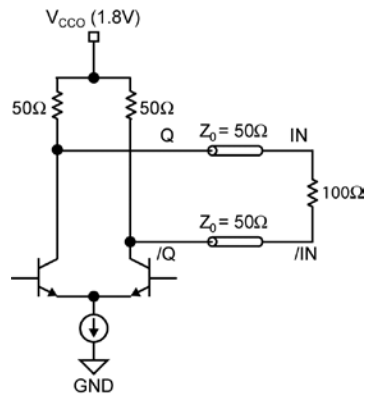


Figure 11. LVDS Interface

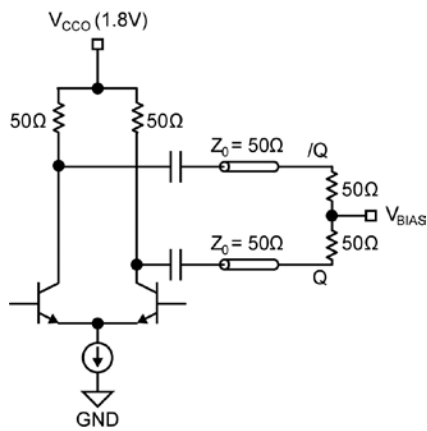
CML Output Termination



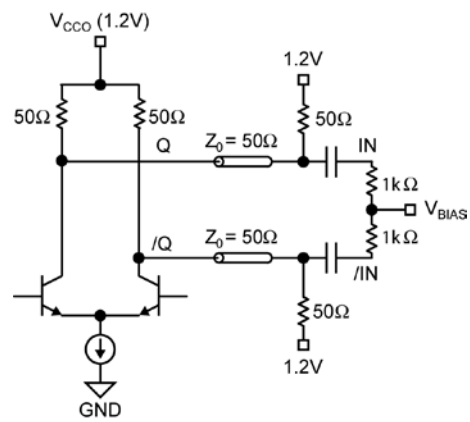
**Figure 12. 1.2V or 1.8V
CML DC-Coupled Termination**



**Figure 13. 1.8V
CML DC-Coupled Termination**

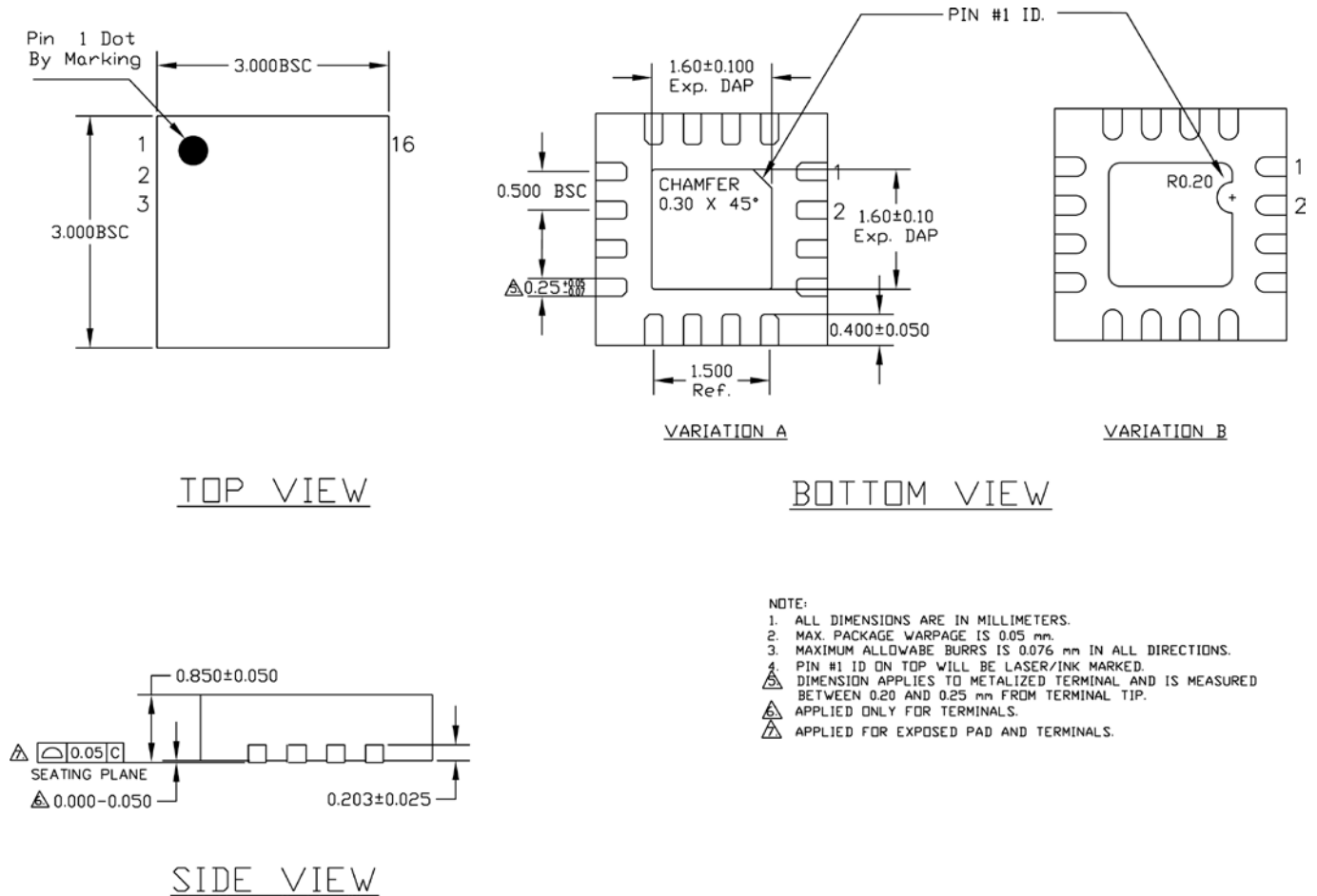


**Figure 14. CML AC-Coupled Termination
(V_{CCO} 1.8V only)**



**Figure 15. CML AC-Coupled Termination
(V_{CCO} 1.2V only)**

Package Information



16-Pin MLF[®] (3mm x3mm) (MLF-16)

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