

# 74LVC138A

3-to-8 line decoder/demultiplexer; inverting

Rev. 5 — 19 October 2011

Product data sheet

## 1. General description

The 74LVC138A is a 3-to-8 line decoder/demultiplexer. It accepts three binary weighted address inputs (A0, A1 and A2) and, when enabled, provides eight mutually exclusive outputs ( $\bar{Y}_0$  to  $\bar{Y}_7$ ) that are LOW when selected.

There are three enable inputs: two active LOW ( $\bar{E}_1$  and  $\bar{E}_2$ ) and one active HIGH (E3). Every output will be HIGH unless  $\bar{E}_1$  and  $\bar{E}_2$  are LOW and E3 is HIGH.

This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 74LVC138A devices and one inverter. The 74LVC138A can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

## 2. Features and benefits

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Mutually exclusive outputs
- Output drive capability 50  $\Omega$  transmission lines at 125 °C
- Complies with JEDEC standard:
  - ◆ JESD8-7A (1.65 V to 1.95 V)
  - ◆ JESD8-5A (2.3 V to 2.7 V)
  - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-B exceeds 200 V
  - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

**nexperia**

### 3. Ordering information

Table 1. Ordering information

Type number	Package	Temperature range	Name	Description	Version
74LVC138AD	SO16	−40 °C to +125 °C		plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC138ADB	SSOP16	−40 °C to +125 °C		plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LVC138APW	TSSOP16	−40 °C to +125 °C		plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC138ABQ	DHVQFN16	−40 °C to +125 °C		plastic dual in-line compatible thermal-enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

### 4. Functional diagram

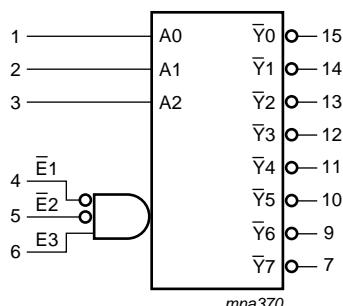


Fig 1. Logic symbol

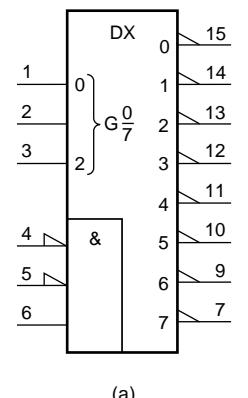
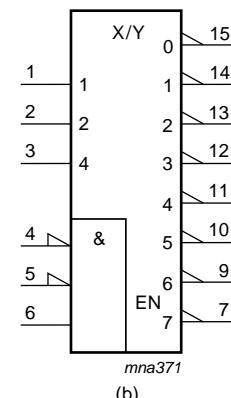


Fig 2. IEC logic symbol (a)



(b)

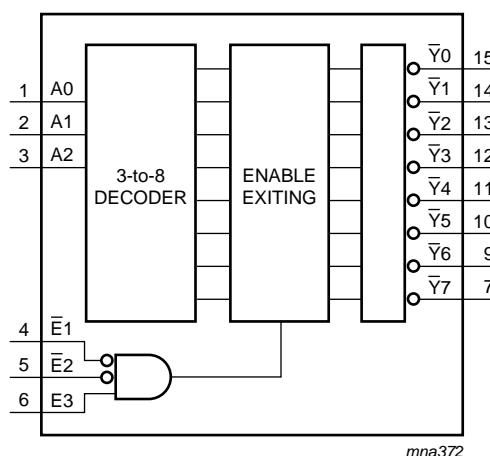


Fig 3. Functional diagram

## 5. Pinning information

### 5.1 Pinning

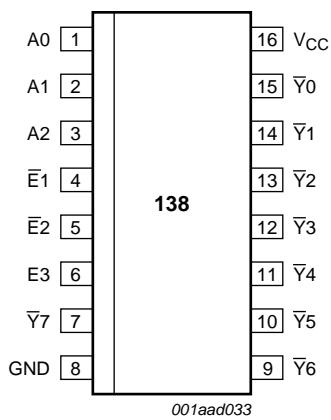
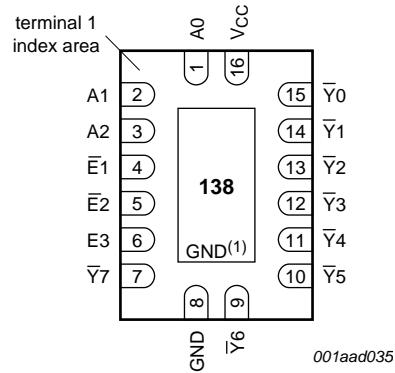


Fig 4. Pin configuration for SO16 and (T)SSOP16



Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration for DHVQFN16

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A0	1	address input
A1	2	address input
A2	3	address input
$\bar{E}1$	4	enable input (active LOW)
$\bar{E}2$	5	enable input (active LOW)
E3	6	enable input (active HIGH)
GND	8	ground (0 V)
$\bar{Y}[0:7]$	15, 14, 13, 12, 11, 10, 9, 7	output
V <sub>CC</sub>	16	supply voltage

## 6. Functional description

Table 3. Function table [1]

Input						Output							
$\bar{E}_1$	$\bar{E}_2$	$\bar{E}_3$	$A_0$	$A_1$	$A_2$	$\bar{Y}_0$	$\bar{Y}_1$	$\bar{Y}_2$	$\bar{Y}_3$	$\bar{Y}_4$	$\bar{Y}_5$	$\bar{Y}_6$	$\bar{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
						H	L	H	H	H	H	H	H
						L	H	L	H	H	H	H	H
						H	H	L	H	H	H	H	H
						L	L	H	H	H	L	H	H
						H	L	H	H	H	H	L	H
						L	H	H	H	H	H	H	L
						H	H	H	H	H	H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		[1] -0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$V_O$	output voltage	output HIGH or LOW state	[2] -0.5	$V_{CC} + 0.5$	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO16 packages: above 70 °C the value of  $P_D$  derates linearly with 8 mW/K.

For (T)SSOP16 packages: above 60 °C the value of  $P_D$  derates linearly with 5.5 mW/K.

For DHVQFN16 packages: above 60 °C the value of  $P_D$  derates linearly with 4.5 mW/K.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage	output HIGH or LOW state	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65 \text{ V to } 2.7 \text{ V}$	0	-	20	ns/V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	-	10	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.2 \text{ V}$	1.08	-	-	1.08	-	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	-	-	1.7	-	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2.0	-	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.2 \text{ V}$	-	-	0.12	-	0.12	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$						
		$I_O = -100 \mu\text{A}; V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	$V_{CC} - 0.2$	-	-	$V_{CC} - 0.3$	-	V
		$I_O = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.2	-	-	1.05	-	V
		$I_O = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.8	-	-	1.65	-	V
		$I_O = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	-	-	2.05	-	V
		$I_O = -18 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.4	-	-	2.25	-	V
		$I_O = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.2	-	-	2.0	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$						
		$I_O = 100 \mu\text{A}; V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	-	-	0.2	-	0.3	V
		$I_O = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.45	-	0.65	V
		$I_O = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.6	-	0.8	V
		$I_O = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.4	-	0.6	V
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	0.8	V
$I_I$	input leakage current	$V_{CC} = 3.6 \text{ V}; V_I = 5.5 \text{ V or GND}$	-	$\pm 0.1$	$\pm 5$	-	$\pm 20$	$\mu\text{A}$

**Table 6. Static characteristics ...continued**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.1	10	-	40	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	500	-	5000	μA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	4.0	-	-	-	pF

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	An to $\bar{Y}_n$ ; see <a href="#">Figure 6</a>	[2]					
		V <sub>CC</sub> = 1.2 V	-	14	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.5	5.2	11.5	0.5	12.7	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	3.0	6.5	1.5	7.3	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.2	6.8	1.5	8.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.7	5.8	1.0	7.5	ns
		E <sub>3</sub> to $\bar{Y}_n$ ; see <a href="#">Figure 6</a>	[2]					
		V <sub>CC</sub> = 1.2 V	-	14	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	5.5	11.4	1.0	12.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	3.2	6.5	1.5	7.1	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.3	6.8	1.5	8.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.9	5.8	1.0	7.5	ns
		$\bar{E}_n$ to $\bar{Y}_n$ ; see <a href="#">Figure 7</a>	[2]					
		V <sub>CC</sub> = 1.2 V	-	15	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	5.6	11.5	1.0	12.8	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.8	3.3	6.5	1.8	7.3	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.4	6.4	1.5	8.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.9	5.8	1.0	7.5	ns
t <sub>sk(o)</sub>	output skew time		[3]		-	1.0	-	1.5 ns

**Table 7. Dynamic characteristics ...continued**Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit	
			Min	Typ <sup>[1]</sup>	Max	Min	Max		
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub>	[4]					pF	
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	9.9	-				
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	15.8	-				
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	21.1	-				

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.[2] t<sub>PD</sub> is the same as t<sub>PLH</sub> and t<sub>PLH</sub>.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in  $\mu$ W).

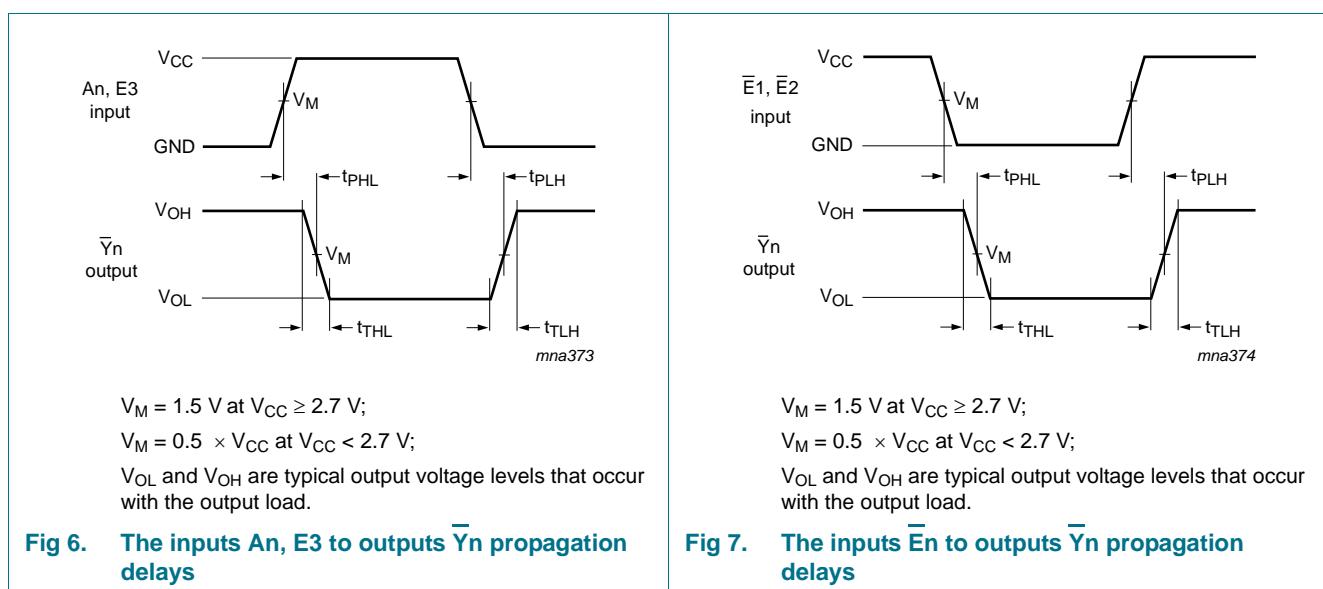
$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

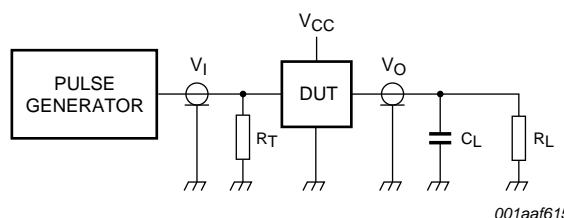
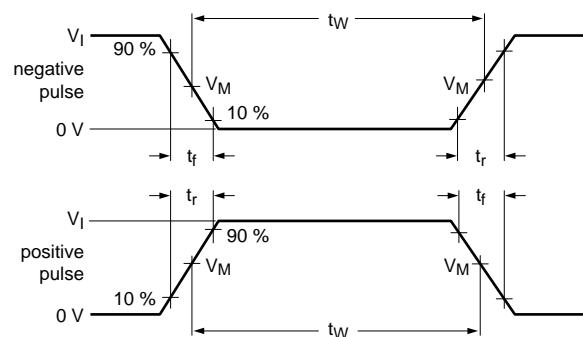
f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHzC<sub>L</sub> = output load capacitance in pFV<sub>CC</sub> = supply voltage in V

N = number of inputs switching

 $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

## 11. Waveforms





Test data is given in [Table 8](#). Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

**Fig 8. Test circuit for measuring switching times**

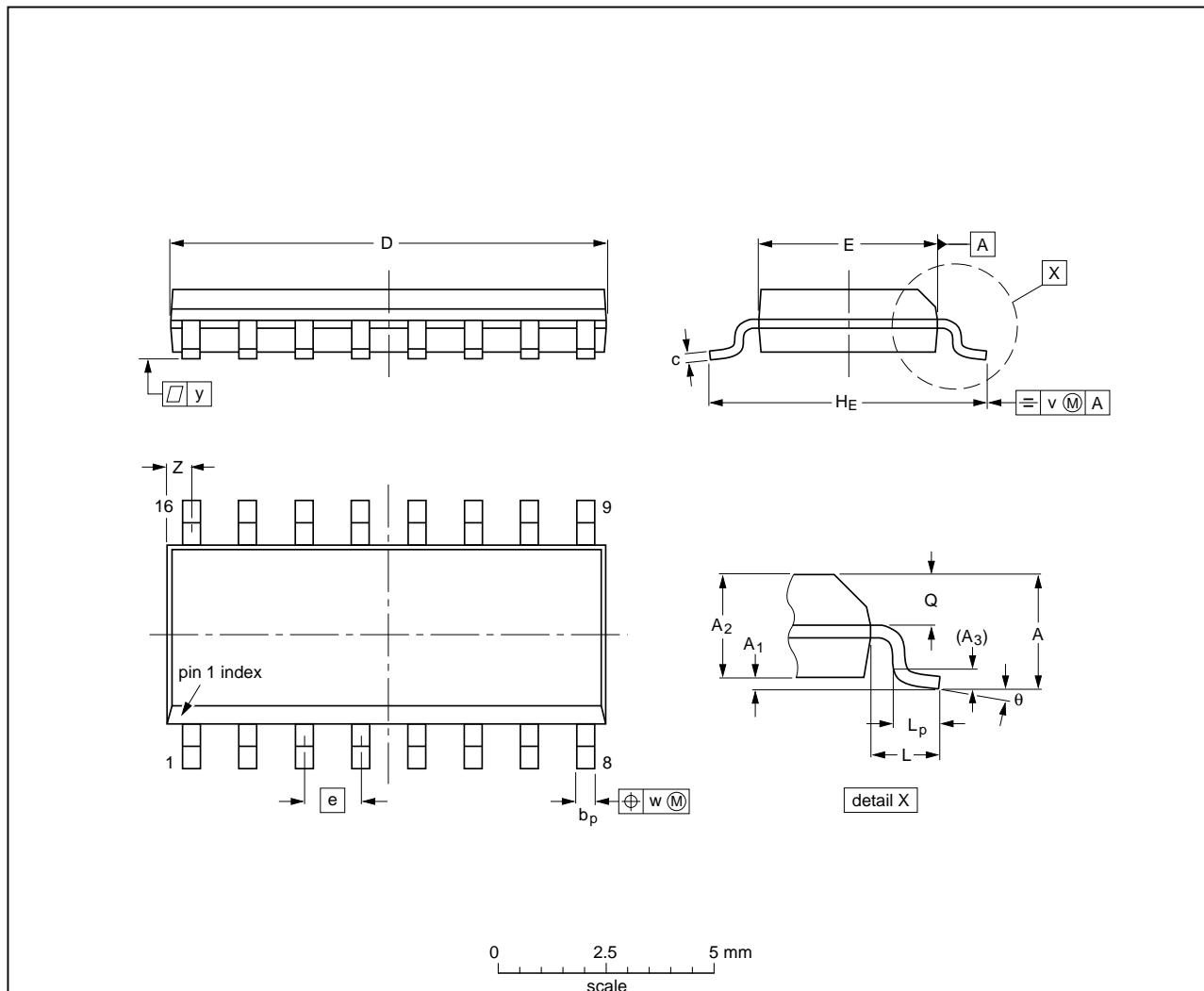
**Table 8. Test data**

Supply voltage	Input		Load	
	$V_I$	$t_r, t_f$	$C_L$	$R_L$
1.2 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 $\Omega$
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$

## 12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



### DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75 0.10	0.25 0.36	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	0°

### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig 9. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

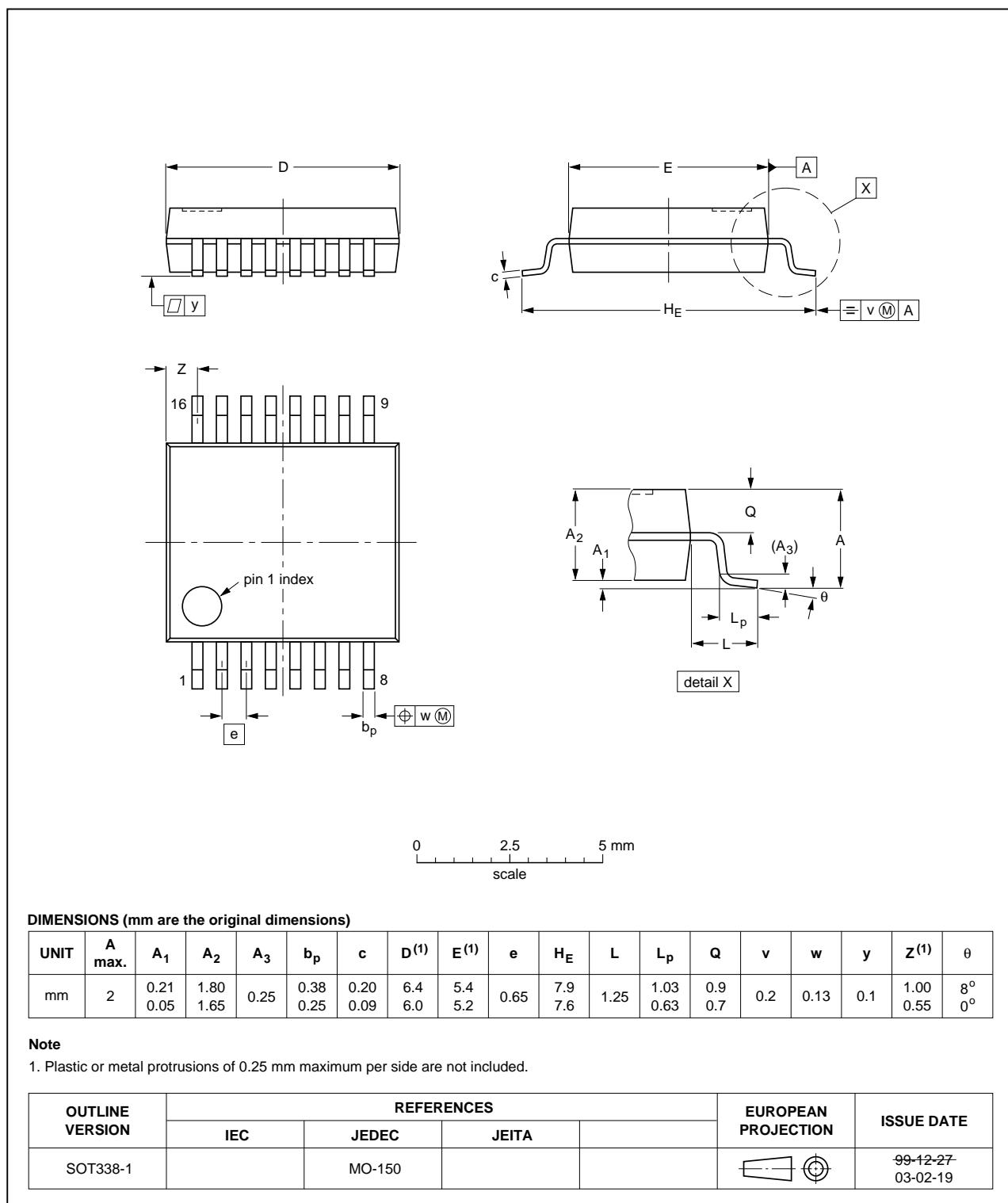
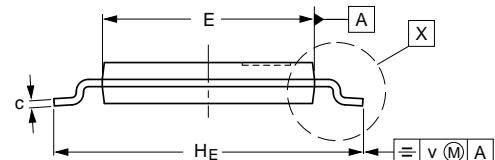
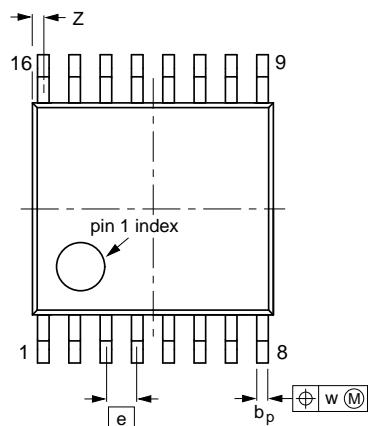
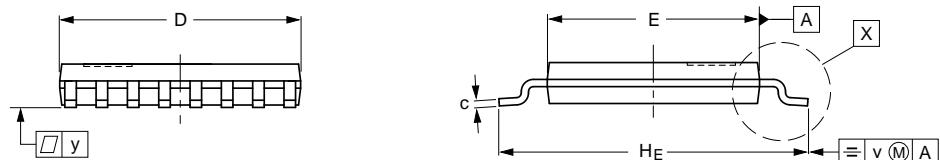


Fig 10. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



0      2.5      5 mm  
scale

## DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.1 0.05	0.15 0.08	0.95 0.80	0.25 0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65 0.65	6.6 6.2	1 1	0.75 0.50	0.4 0.3	0.2 0.2	0.13 0.13	0.1 0.1	0.40 0.06	8° 0°

## Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT403-1		MO-153			-99-12-27 03-02-18

Fig 11. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

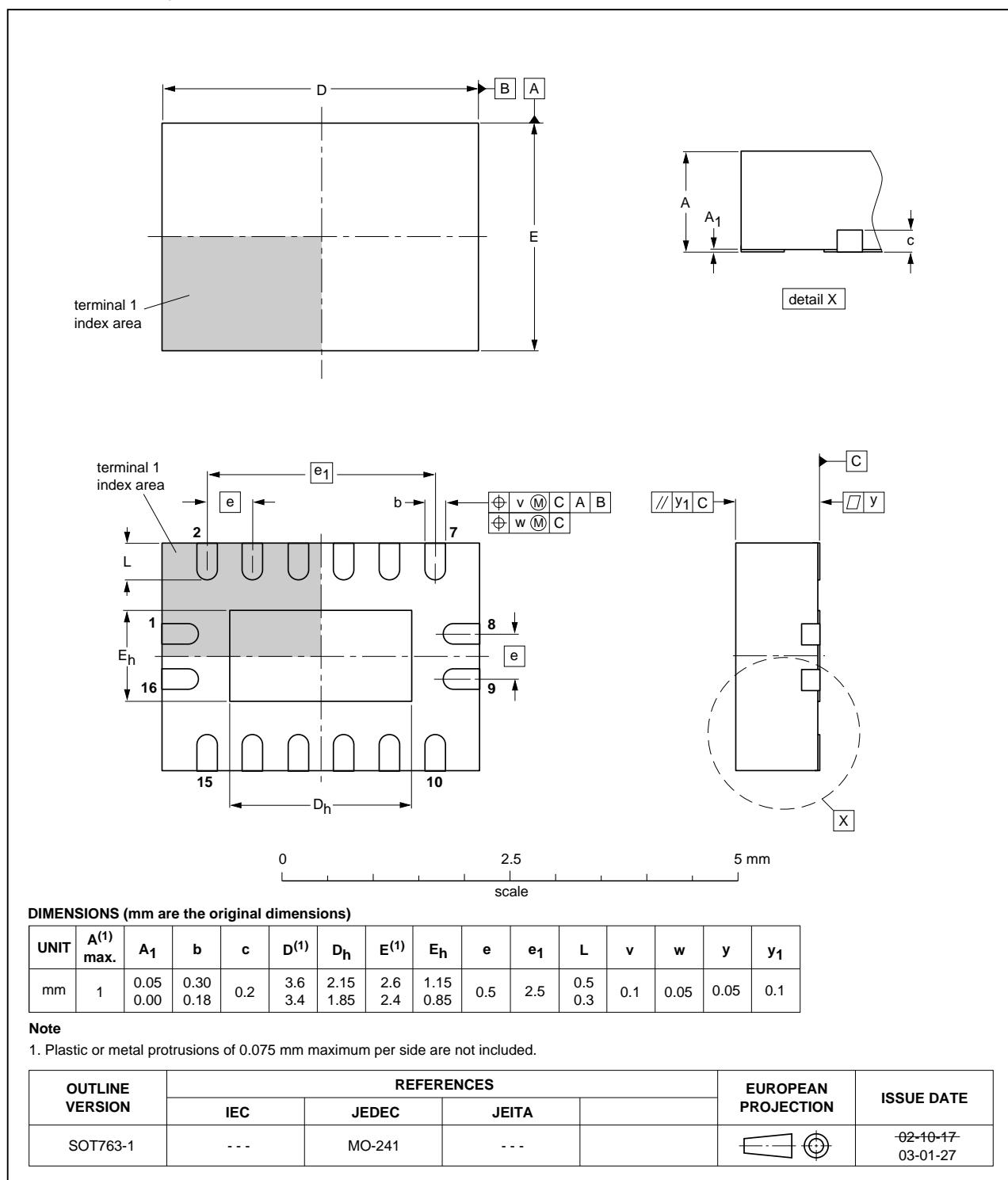


Fig 12. Package outline SOT763-1 (DHVQFN16)

## 13. Abbreviations

**Table 9. Abbreviations**

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

**Table 10. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC138A v.5	20111019	Product data sheet	-	74LVC138A v.4
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 4</a>, <a href="#">Table 5</a>, <a href="#">Table 6</a>, <a href="#">Table 7</a> and <a href="#">Table 8</a>: values added for lower voltage ranges.</li> </ul>			
74LVC138A v.4	20030506	Product specification	-	74LVC138A v.3
74LVC138A v.3	20020312	Product specification	-	74LVC138A v.2
74LVC138A v.2	19980428	Product specification	-	74LVC138A v.1
74LVC138A v.1	-	-	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 16. Contact information

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)

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